

Overview of Pillar-1: Technology

Detector Portfolio General Assembly meeting

19-21 November 2012; Karlsruhe

Heinz Graafsma (DESY) / Michael Fiederle (KIT)

Pillar-1

Reminder of Structure:

- > WP-1: 3D-ASICs
- > WP-2: 2D-Mixed signal ASICs
- > WP-3: High-Z and edgeless sensors
- > WP-4: Packaging
- > WP-5 Advanced Materials

Meetings:

- > Portfolio Kick-off Meeting in Karlsruhe: **21+22 Feb 2012**
- > Face-to-face meeting Pillar-1: **13+14 June 2012** in Hamburg
- > Face-to-face meeting WP-1 & WP-2 (ASICs) **10+11 Oct 2012** in Heidelberg (increased participation and interest of Universities)



3D-ASICs: technology at a glance (U.Trunk / DESY)



based on GF 130nm CMOS Low Power

1.5 V core, 3.3V IO

including ARM-provided SC library

1 poly, 5+1 metals per Tier

(Metal 6 is used as bond interface)

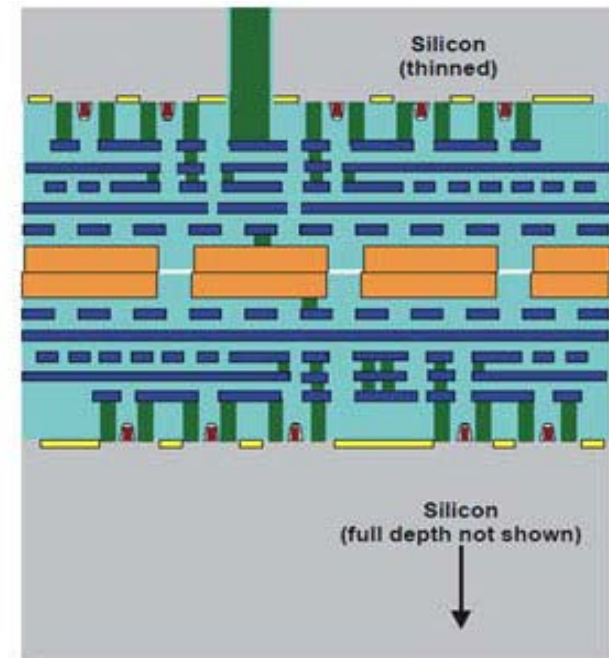
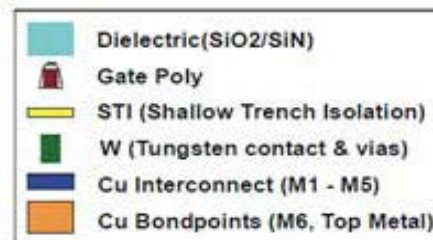


2 tiers, Face-to-Face coupling

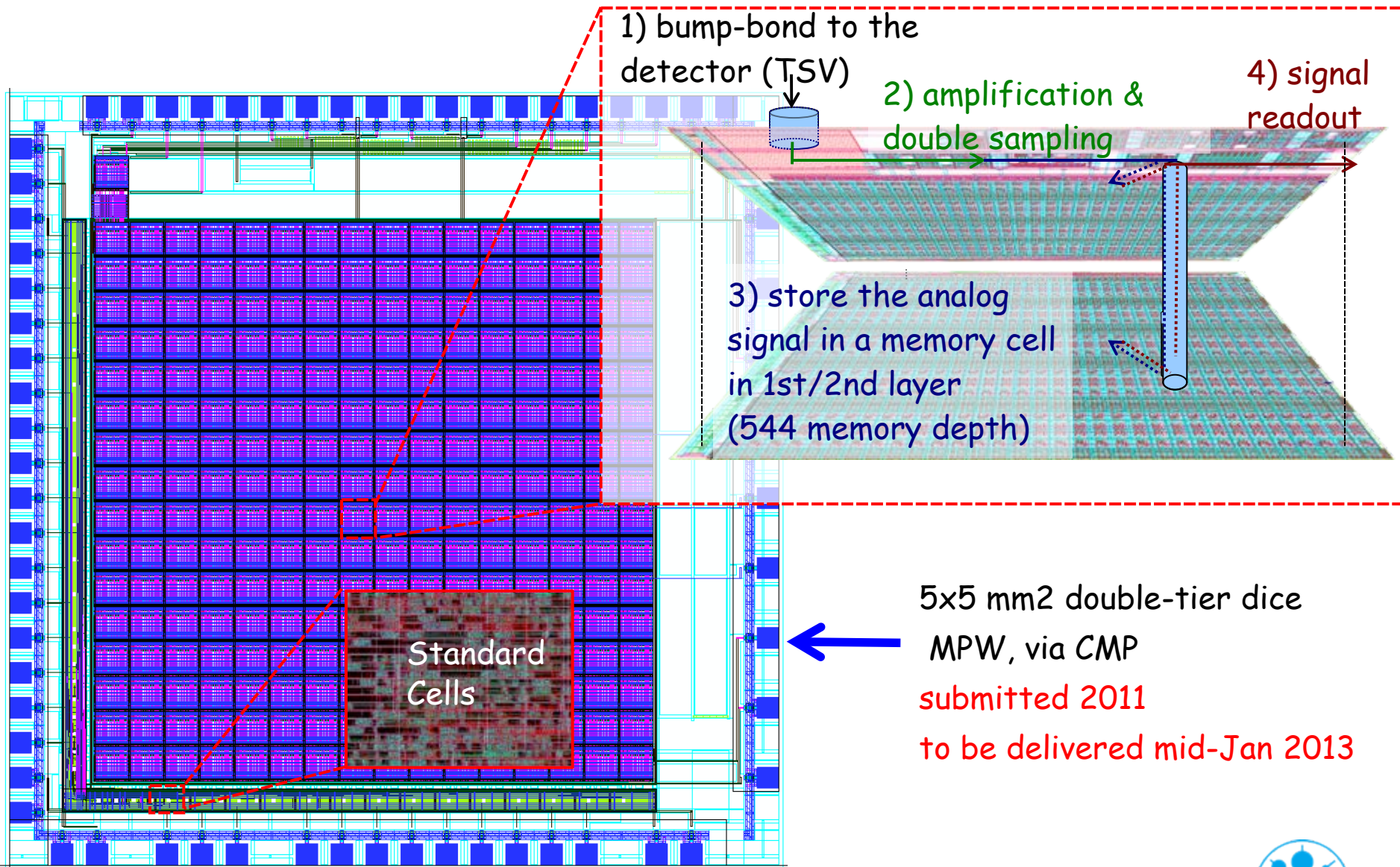
"Via-middle process" (TSVs etched before BEOL)

Cu-Cu bonding (both for mechanical and electrical contact)

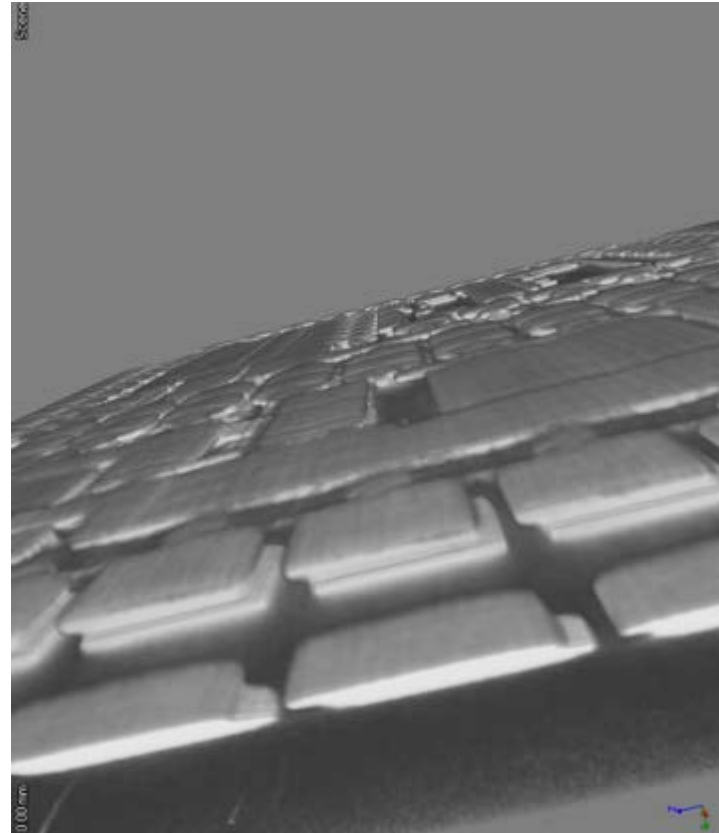
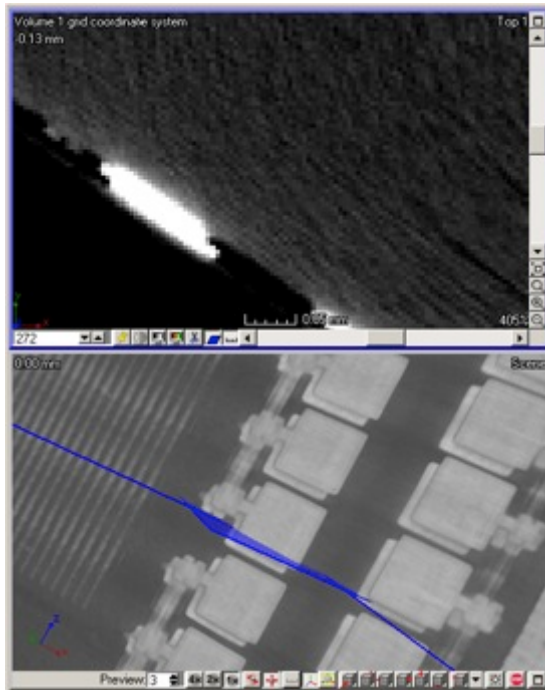
upper tier thinned down ~ 6um ; whole stack has ~ordinary wafer thickness



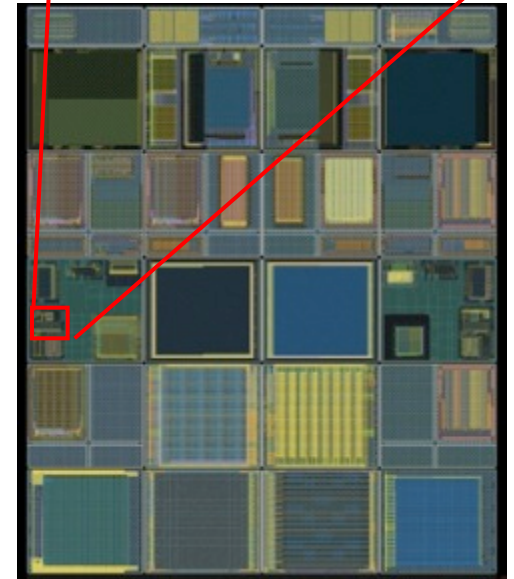
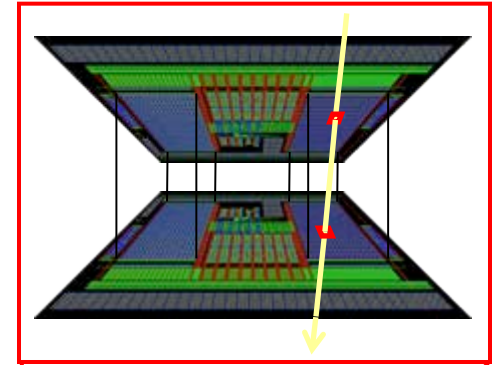
3D ASIC submission: an AGIPD evolution hypothesis



3D-ASICs X-ray tomography on an “inherited” project



M³APS
MPW, via CMP
submitted end 2009
delivered 2011 & 2012
(courtesy of INFN-Perugia)



2D-ASICs: Important decisions (C. Schmitt / GSI)

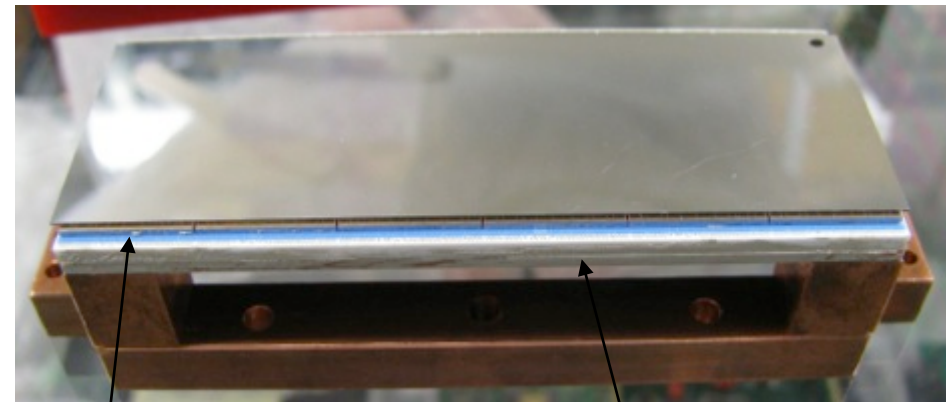
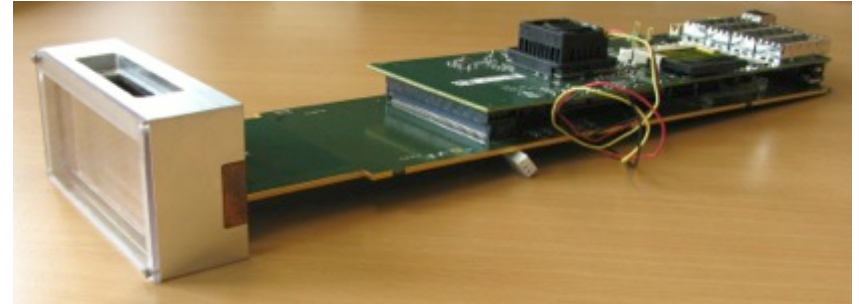
During the face-to-face meeting of the ASIC designer in Heidelberg; it was decided:

- > to investigate the possibility to use TSMC 65 nm (low power) as the common technology.
- > to create a repository/library of building blocks in order to share designs amongst Helmholtz centers (hosted by DESY).
- > to design a common analogue-digital readout chip, that will also be used as a vehicle for evolution towards 3D-integration (using Through Silicon Vias; TSV).
- > to consider to create a full-chip simulation tool (together with universities).
- > To hold the next face-to-face meeting in January 2013 to decide on the mixed-signal readout chip to be designed.



First version of the Helmholtz-Cube ready!

- > 6 by 2 chips (1536 by 512 pixels)
 - Large Si sensor from 6" wafer
 - 300 μ m Si sensor here
 - 2 x "Hexa" high-Z sensors
- > Ceramic circuit board (LTCC)
 - 14 layer board
 - Good match to germanium CTE
 - Cooling through thermal vias
- > 500-pin connector on board
 - Full parallel readout (8 LVDS data outputs per chip)
 - ~150 LVDS pairs total



6 x 2 Medipix3 chips

LTCC board

High-speed readout system

- > Previously developed prototype system (USB2 readout only)
- > High-speed readout with common DESY mezzanine card
 - Virtex-5 FPGA with PowerPC
 - 4 * 10 Gigabit Ethernet links
 - DDR2 RAM (8GB)
- > “Signal distribution” board connects to det. head
 - Space for vacuum barrier with germanium detector
- > Currently working on high-speed readout firmware



10GBE links

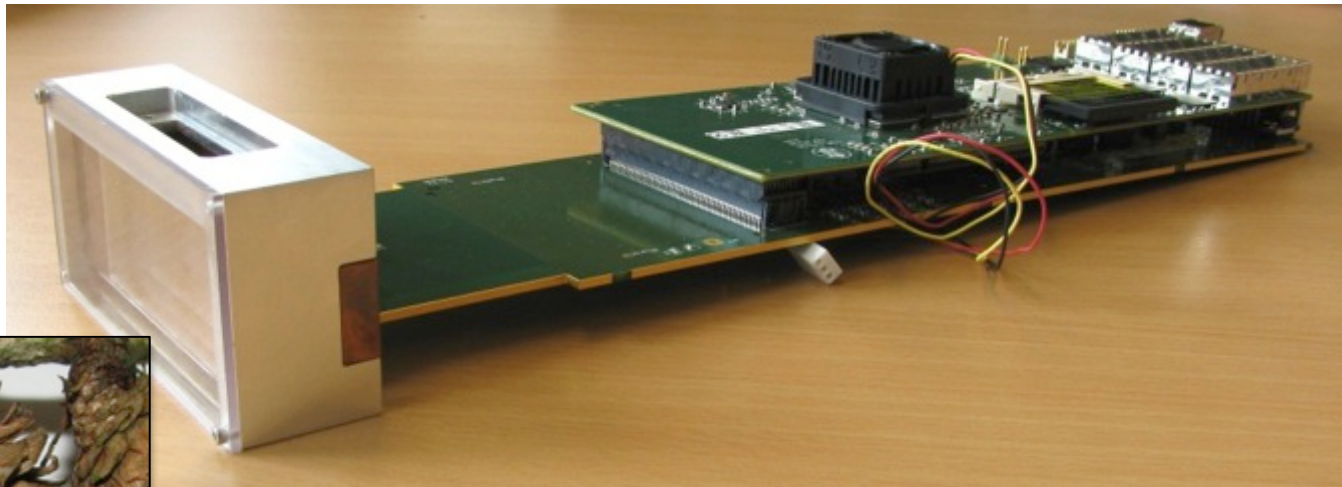
Connector to det. head



Power / trigger in

Test results with Si module

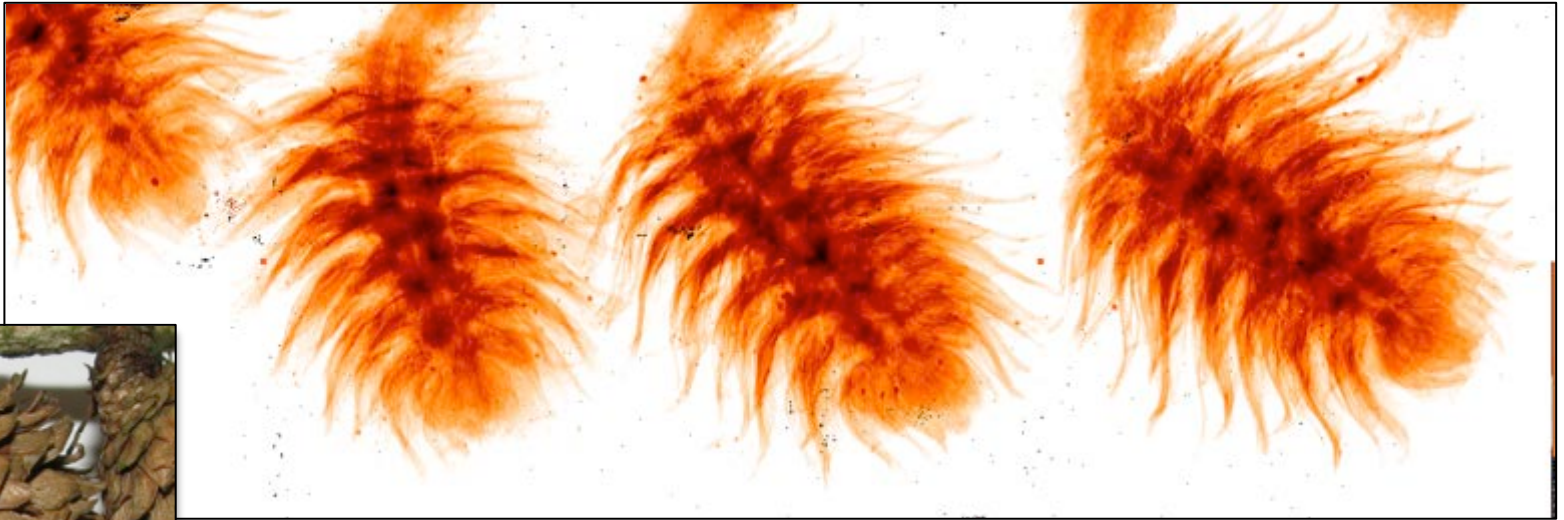
- First full Si module assembled (300 μ m thick sensor from Canberra)
 - Solder bonding at IZM
 - All 12 chips successfully bonded and functional
 - Small no. of bad pixels on chips and bad bumps on test module



Flat-field corrected image, Mo X-ray tube, 40kV

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One system delivered to KIT for hybridization with CdTe

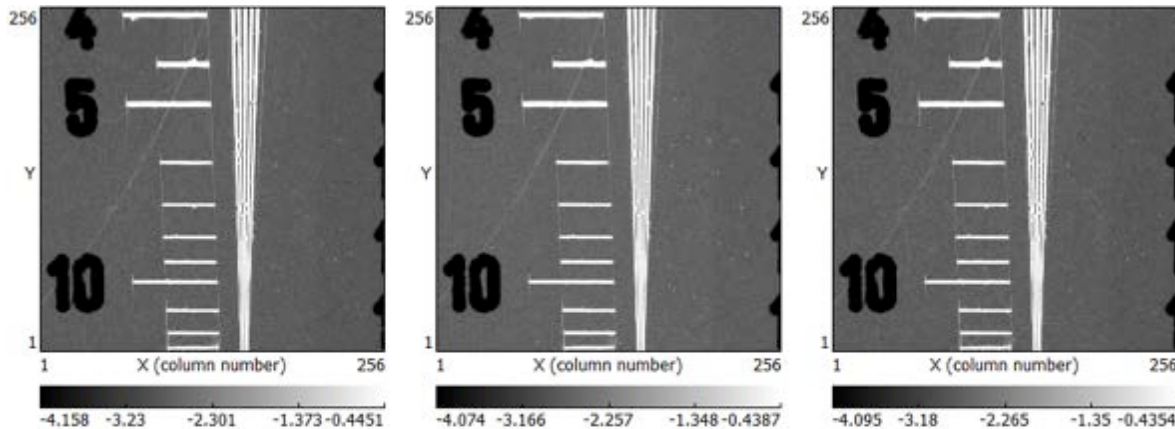
High-Z development (M. Fiederle / KIT-FMF)

- > Processing of High-Z semiconductors: CdTe and GaAs
- > Development of monolithic sensors with 165 / 110 / 55 μm pixels
- > Active area 28 x 43 mm^2 => maximum size of available material
- > Tasks:
 - Wafer level: metallization, passivation, UBM, bump deposition, dicing
 - Sensor level: flip-chip bonding, assembling, wire bonding
- > Photon Counting Chip: Medipix3 – Version 3RX (latest):
 - Full functionality: Single Pixel Mode SPM, Charge Summing Mode CPM, Color Mode with Super Pixels 110 μm => 8 (eight) energy thresholds
- > First assemblies: CdTe 3RX 55 μm and CdTe 3RX 110 μm



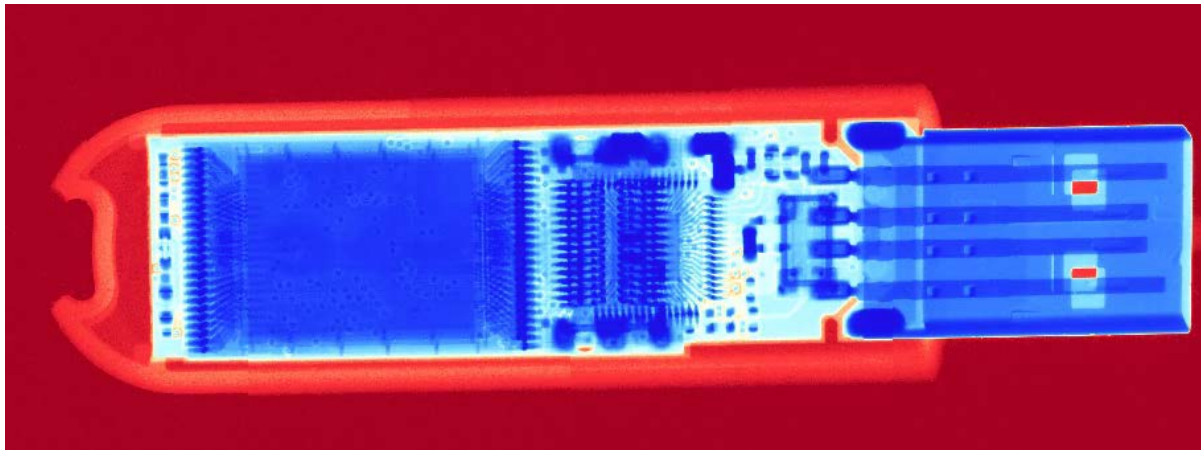
High-Z development (M. Fiederle / KIT-FMF)

- > X-ray images with CdTe 55 μm 3RX: **lowest energy < 3keV**



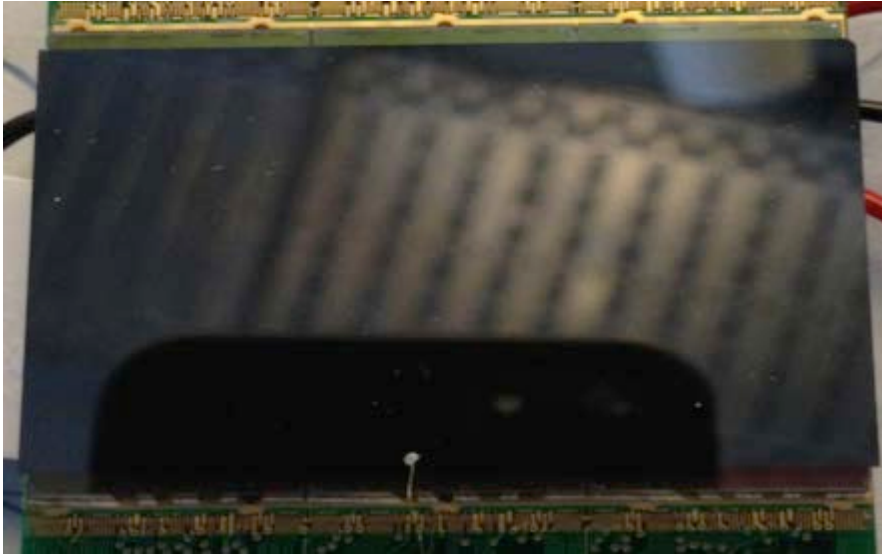
CSM low SPM CSM high
MPX3RX 55 μm SHGM CdTe 1mm -360V X-ray 30 kVp

- > X-ray images with CdTe 110 μm 3RX:



High-Z development (M. Fiederle / KIT-FMF)

> CdTe Hexa 28x43 mm² with Medipix 3RX

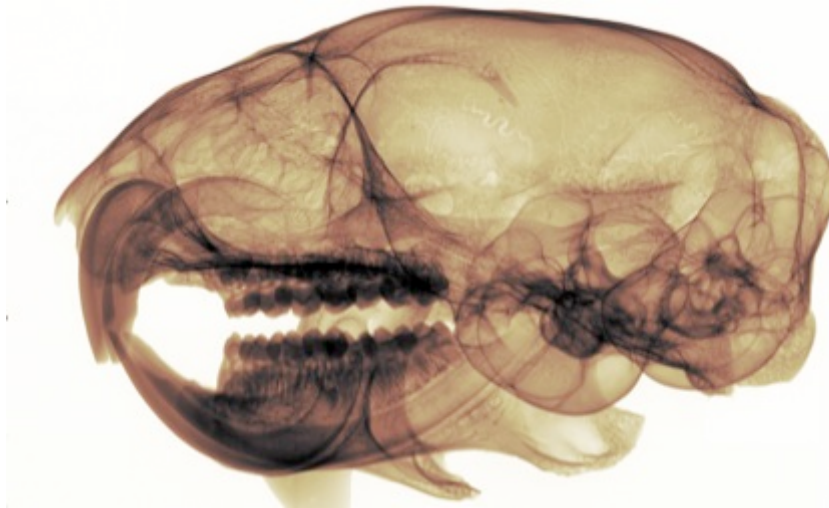


> Assembling on HGF-Cube boards:

- One hexa in the first step
- Adjustment of back-side contact (gold wire glued to CdTe)
- Tests in the next two weeks
- First Cube with one Hexa in December 2012

High-Z development (M. Fiederle / KIT-FMF)

- > GaAs Medipix2/3 assemblies: good performance for energies < 40 keV
- > GaAs assemblies processed by FMF (first Hexa 1Q 2013)



TPX 55 μ m
GaAs 500 μ m
Bias: -230V
8x5 tiles, width 34mm

- > 3D sensors structures:
 - Medipix3 layout in collaboration with CNM Barcelona
 - Silicon assemblies with 55 and 110 μ m pixels in 2Q 2013
 - Experiments with GaAs and CdTe in 2014

Packaging (Th. Blank /IPE/KIT)



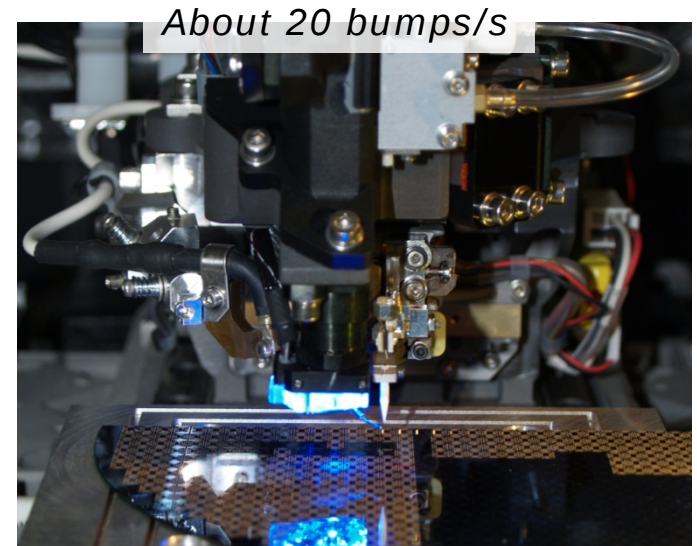
The wire is snapped off after the ball is initially connected to the die

No UBM is required
No chemical process

Wire Diameter	Capillary	Bump diameter
30um	Standard	67um
15um	414FE-S108-R35 414FF-V208-R33	37 um
12.5um (Tanaka)	PI-15038-181F- ZP34T	25um



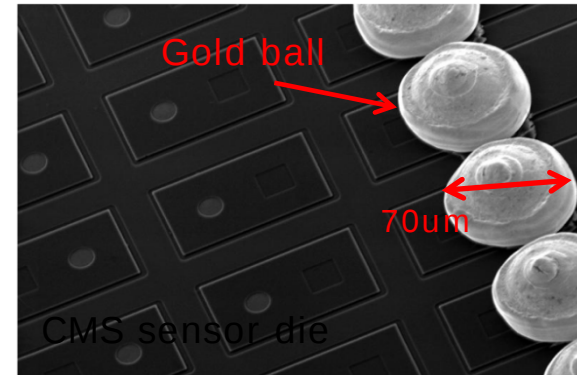
Bump diameter comparable with the traditional bump-bonding processes



Packaging (Th. Blank /IPE/KIT)

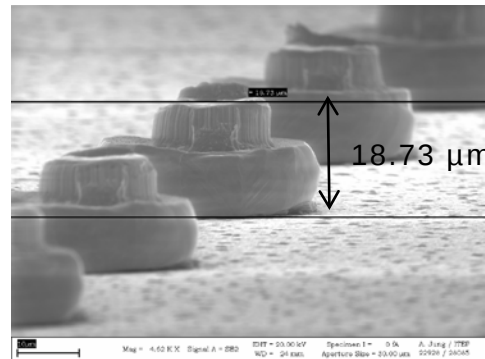
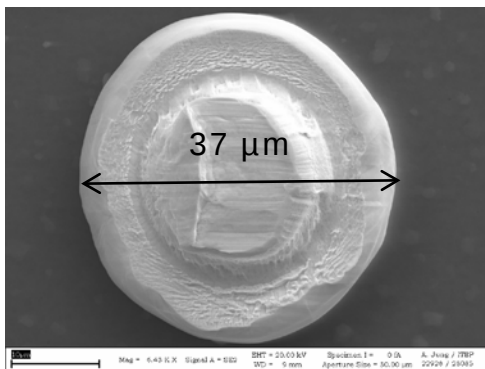
First results...

- Sensor wafer: FZ200N-W4 (*new*)
- Gold wire diameter 30 μm & standard capillary



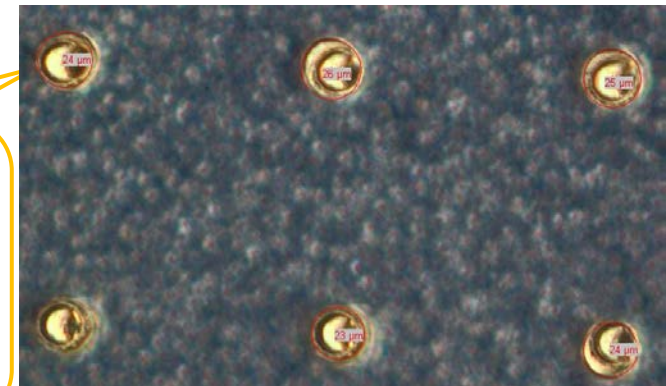
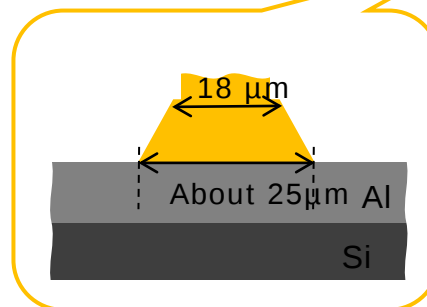
First small gold bumps ...

- 15 μm diameter gold wire
- Shear test (mean) = 8.54 ± 1.12 gr/bump



Preliminary results (12.5 μm wire)

- Bump diameter 25 μm
- Shear test $\rightarrow$ on-going

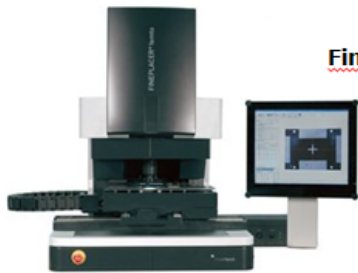


Packaging (Th. Blank /IPE/KIT)

> Infrastructure

Installation of ISO 6 (Class 1000) Clean Room Area for FC-Processes at the end of December

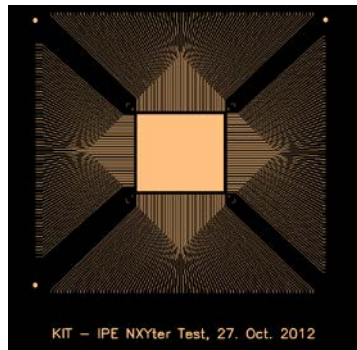
Flip-chip Bonding process in IPE



Finetech's automated fineplacer FEMTO

- ✓ accuracy < 1 μm
- ✓ Wide-range of the bonding parameters:
- ✓ Several metals bumps (SnPb, In, SAC, gold, ..)
- ✓ Heating chamber with formic-acid atmosphere for bumps reflow

FC-bonding machine ordered, will be installed at the end of this year



Evaluation of Screen & Stencil Printing Processes

50 μm Lines/ 50 μm Space on Al₂O₃



Wafer dicing process @ KIT-IPE



Wafer dicing machine DAD 320

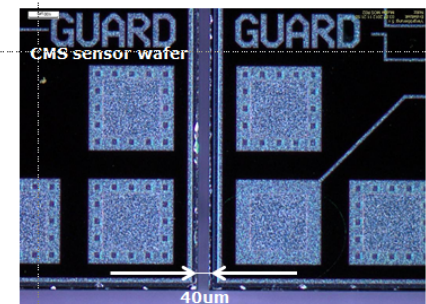
Maximum wafer size: 6 inch (15.2 cm)

Maximum Spindle Speed: 40.000 RPM

Wide available Disco Diamond Blades: silicon, GaAs, GaP, LiTaO₃, glass, quartz, crystal, ceramics, etc.

Under investigation an blade upgrade:

- > cut in the range of 30 μm
- > reduction of the scratch area

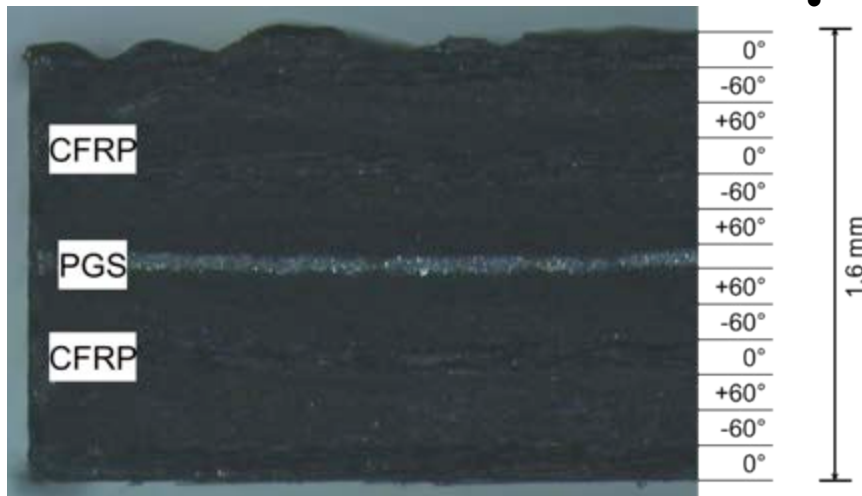


Advanced Materials (A. Mussgiller / DESY)

Special requirement from particle physics: light weight detectors

- Minimize multiple scattering for increased precision
- Good thermal conductivity
- Good dimensional stability

Example: high-tech foil for mechanical stability combined with excellent thermal conductivity.



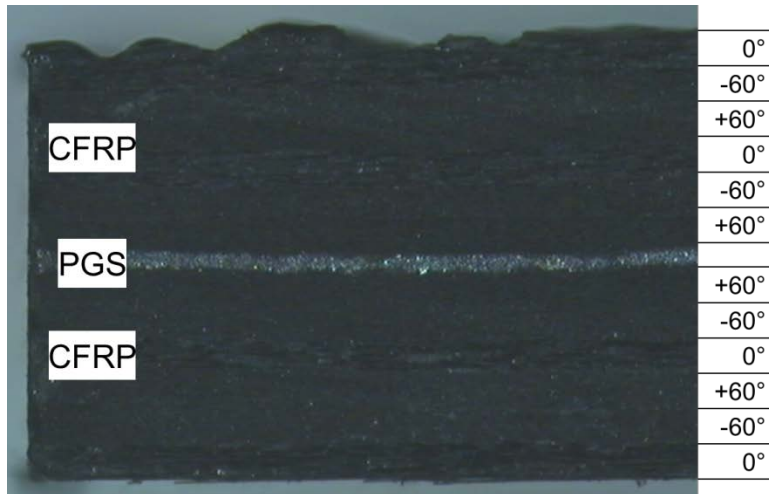
- graphite foil laminated into carbon fibre (CFRP) structure
 - pyrolytic graphite sheet (PGS) has very high thermal conductivity ($\sim 700 \text{ W/m/K}$)
 - adhesive bonding PGS sheets to structural elements is challenging
 - shear stress could result in delamination either at glue to foil interface or inside foil

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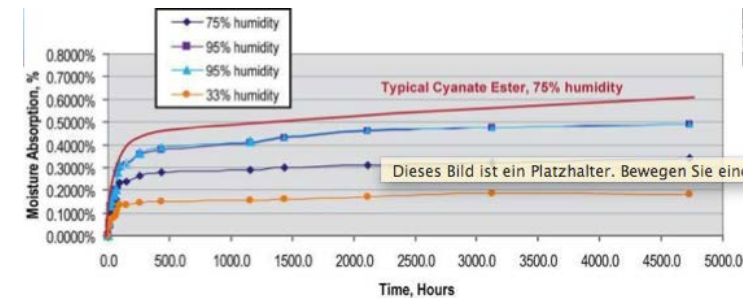
- graphite foil laminated into carbon fibre (CFRP) structure
- pyrolytic graphite sheet (PGS) has very high in-plane thermal conductivity ($\sim 700 \text{ W/m/K}$)
- adhesive bonding PGS sheets to structural elements is challenging
- shear stress could result in delamination either at glue to foil interface or inside foil
- thermal and mechanical characteristics of samples will be tested
- effect of irradiation will be investigated

> Market survey produced a few promising material solutions for HEP

- foams, carbon fibres and resin systems, and glues

> e.g. novel resin system by TenCate

- on the market since 2008 - the standard in satellite structures
- low moisture uptake
- radiation tolerance will be tested
- details will be discussed during this meeting



> PhD position at DESY has been advertised

- next interviews scheduled for early December
- hope to fill position by February

What is next?

- > Hybridization of CdTe to current HGF-Cube.
- > Distribute more HGF-cubes to centers for testing.
- > Come to decisions on ASIC:
 - Common technology; joint readout ASIC; simulation package
- > Discuss whether to merge WP-1/3D-asic and mixed WP-2/mixed signal ASIC (discuss in Pillar meeting; decide in EB-meeting).
- > See how WP-4/packaging can contribute to next version of HGF-cube. Increase interaction between WP-4 and WP-1,2,3.
- > Discuss with Pillar-2 if/how to integrate high-speed I/O into HGF-cube.

