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Matlab/Simulink and HDL-coder

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With the many existing ASIC/FPGA development tools, techniques, and languages available today, the selection of the right methodology or set of solutions can be daunting. Moving away from the communication obstacle towards algorithm development and design implementation will help to satisfy the ever-increasing demands for the processing performance, while reducing hardware cost and power consumption, particularly decreasing the development cycle time and achieving robustness for future improvement. In this work, we introduce an algorithm development environment MATLAB/Simulink from MathWorks, where Simulink is a graphical environment for simulation and Model-Based data processing systems. With the intention of bridging the gap between algorithm development and hardware implementation, MathWorks produces an additional product called HDL Coder, which generates portable, synthesizable Verilog and VHDL code from MATLAB functions, Simulink models, and State flow charts. HDL Coder provides a visible and efficient method for the system setup and optimization by controlling HDL architecture and implementation, highlighting critical paths, and generation of hardware resource utilization estimates. Together with HDL Coder, another tool HDL Verifier from MathWorks makes the possibility of so-called Co-simulation, which realizes the communication between Simulink and HDL simulator like the ModelSim. Designers could set up any test stimulus in Simulink model and feed them into ModelSim environment, consequently, verify the system functions and the equivalence of the hardware implementation to the algorithm model.

Summary

Accelerate ASIC/FPGA development with MATLAB/Simulink and HDL-Coder.

Author: Mr XIONG, Renhai (Forschungszentrum Jülich)

Presenter: Mr XIONG, Renhai (Forschungszentrum Jülich)

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