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Data Concentrator for the Belle II DEPFET Pixel Detector

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The innermost two layers of the Belle II detector located at the KEK facility in Tsukuba, Japan, will be covered by high granularity DEPFET pixel (PXD) sensors. This leads to a high data rate of around 60 Gbps, which has to be significantly reduced by the Data Acquisition System. For the data reduction the hit information of the surrounding silicon strip detector (SVD) is used to define so-called Regions of Interest (ROI) and only the information of the pixels located inside these ROIs are saved. The ROIs for the pixel detector are computed by reconstructing track segments from SVD data and back
extrapolation to the PXD. A data reduction of up to a factor of 10 can be achieved this way. All the necessary processing stages, the receiving and multiplexing of the data on many optical links from the SVD, the track reconstruction and the definition of the ROIs, will be performed by the Data Concentrator. The planned hardware design is based on a distributed set of Advanced Mezzanine Cards (AMC) each equipped with a Field Programmable Gate Array (FPGA) chip and 4 optical transceivers.

In this talk, the hardware and firmware development of the algorithms to multiplex the incoming data streams on Xilinx Rocket IOs and the necessary pre-processing steps in each FPGA are discussed. In addition, a prototype implementation of the FPGA-based tracking algorithm will be presented with some preliminary simulation results.

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