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Parallelisation potential of image segmentation in hierarchical island structures on hardware-accelerated platforms in real-time applications

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The presented work addresses two types of compact HPC platforms found to be most successful nowadays: FPGA-based expansion cards and graphics processing unit coprocessing boards. The FPGA and GPU architectures are shortly discussed to identify the major aspects of the application design for these platforms.
The application in focus is a fast automated image segmentation method (GSC, Grey Value Structure Code). This complex method is feasible for different application areas and provides high-quality segmentation results. An analysis of the parallelisation potential of the applied method is carried out. Relying on many statistical measurements and results of versatile system models the GSC algorithm is specially reelaborated for the implementation on the two massive parallel computation platforms to achieve a high performance needed for real-time application set-ups. A special attention has been paid to the question of an effective computation organisation for the target platforms. The two implementations are compared to highlight their relative merits and downsides for this complex and computation intensive application.
The results of the work show that even having a considerably longer development cycle the FPGA-based solution on the Xilinx Virtex II Pro architecture can compete with the implementation on the specialised nVidia Tesla C1060 card. Compared to a single CPU (Opteron 2.6 GHz) the FPGA accelerates the application by a factor of about 23, while the GPU outperforms with factors of 13 to 20 dependent on the image resolution.

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