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High Level Synthesis with Xilinx HLS

Tuesday, December 4, 2012 9:00 AM (1h 30m)

Agenda

Functional Abstraction Level
High Level Synthesis HLS
Control & Datapath Extraction
Scheduling & Binding
Arbitrary Precision Data Types
Top Level I/O Ports
Loops
Arrays
Interfaces
First Example
Latency & Throughput
Optimizations

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Session Classification: Invited Talk