Contribution ID: **3** Type: **not specified**

An FPGA Platform for Ultra-fast Data Acquisition

Tuesday, December 4, 2012 1:40 PM (25 minutes)

The next generation of physical experiments demands high-throughput data readout systems combined with embedded data processing. We will present the current status of a multi-purpose high-performance data-acquisition system that has been developed at KIT. The design is based on three customizable IP cores used to build a multi-purpose and high bandwidth DAQ system: The first IP-core is a PCIe interface including a Bus Master DMA (BDM) architecture with a bandwidth of up to 32Gb/s. The second IP-core is a multi-port DDR3 memory interface that works with up to 51Gb/s. The last IP-core is a fast SerDes input stage with automatic parallel data pattern alignment logic. A 64-bit Linux driver seamlessly integrates the DAQ platform into any CPU/GPU server infrastructure. The multi-purpose readout architecture and its application to selected physical experiments are presented and the performance will be discussed. The remaining bottleneck for current DAQ systems at this high data rates is the storage of the data. We propose solutions to overcome this limitation with emerging electronics components and ultra-fast serial links. We will discuss both FPGA peer-to-peer connections, based on PCIe Gen3 and fast local data storage with NAND Flash solid state storage, and an FPGA-to-network architecture. The second approach embeds the DAQ platform directly in high-performance networks, well established for super computing (e.g. Infiniband).

Summary

New projects, currently under development for the synchrotron ANKA at KIT, require fast data acquisition systems with embedded FPGA data processing. The requirements of these experiments include high data throughput of up to 50Gb/s [1].
A modular FPGA readout architecture has been developed for this purpose. The full platform consist of hardware FPGA-IP logic blocks and software 64bit Linux drivers for high-throughput readout [2]. Three IP-cores have been developed to support a general multi-purpose and fast DAQ system. The system comprises parallel SerDes input stages, each able to manage a differential LVDS high-speed serial data rate up to 500Mb/s per lane, a multi-port DDR3 memory interface, used for temporary data storage and on-line data elaboration and a PCIe –Bus Master DMA logic, used to transfer the data from the FPGA-board directly to the main computer memory and vice versa. The term Bus Master indicates the ability of a PCIe port to initiate PCIe transactions, typically memory read and write transactions. This implementation has many advantages over standard Programmed Input/Output (PIO) data transfers. In addition, the DMA engine releases the CPU from directly transferring the data and results in better overall system performance through lower CPU utilization. The PCIe IP-core is able to reach a bandwidth up to 32Gb/s. The architecture includes an addressable 32-bit bank register implemented in the dedicated Base Address Register (BAR) space. Bank registers are used to access status and configuration of the DMA engine and user applications.
The storage system is the last bottleneck for our current DAQ systems at this high data rate. We propose solutions to overcome this limitation with emerging electronic components and ultra-fast serial links. We will discuss two solutions, an FPGA peer-to-peer connection and an FPGA-to-network architecture. The first approach employs the new generation of the PCIe protocol to transfer data between the main readout board and the PC host board equipped with an array of NAND Flash solid state storage. In the second approach the main readout board includes an InfiniBand interface to transfer data to a high-performance network. Both strategies improve the scalability of the presented DAQ platform for the highest data rates.

[1] M. Caselle, S. Chilingaryan, A. Kopmann, U. Stevanovic, M. Vogelgesang: Ultra-Fast Streaming Camera Platform for Scientific Applications. Submitted to Proc. IEEE real-time conference, June 11-15, 2012, Berkeley.

[2] S. Chilingaryan, M. Caselle, A. Kopmann, U. Stevanovic, M. Vogelgesang: ALPS –Advanced Linux PCI Services for Rapid Development of DAQ Systems for Linux. Submitted to Proc. IEEE real-time conference, June 11-15, 2012, Berkeley.

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Session Classification: Talks TUE2