FPGA Based Data Digitisation with Commercial Elements

Cahit Uğur,
Wolfgang Koenig, Jan Michel, Marek Palka, Michael Traxler

GSI Helmholtz Centre for Heavy Ion Research, Darmstadt – Germany
Goethe-University, Frankfurt – Germany
Jagiellonian University, Krakow – Poland

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Outline

- Motivation
- Time digitisation in FPGAs
- Signal discrimination using FPGAs
- Amplitude digitisation with FPGAs
- Charge digitisation with FPGAs
- Summary

Motivation & Idea

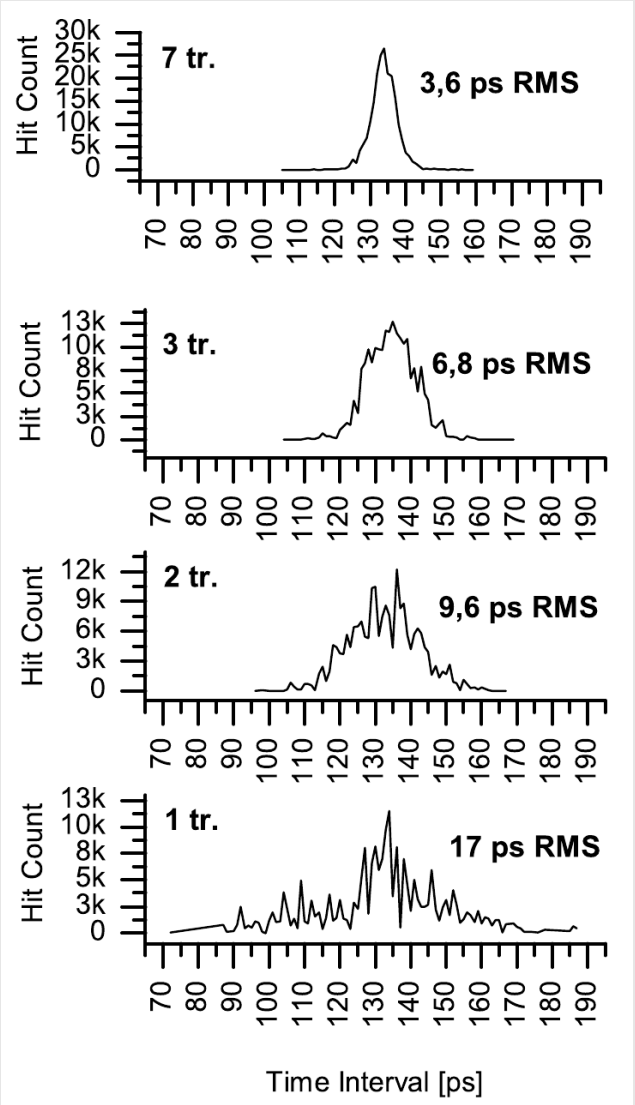
- **Use commercial off the shelf FPGAs as FEE**
  - Easily available, industrial quality design, package and documentation
  - Upgrade included (new silicon on the roadmap of the vendor)
  - Vendor independent

- **How to achieve that goal?**
  - We “misuse” digital FPGAs in the asynchronous and analogue domain for:
  - Precise Time to Digital Conversion (TDC)
  - Deploying **CO**mplex, com**ME**rcial FPGAs as discriminators, DACs, ADC and QDC only adding a minimal number of external components

- The design: **K**eep **I**t **S**mall & **S**imple: **Come & Kiss**

Precise TDCs in FPGAs

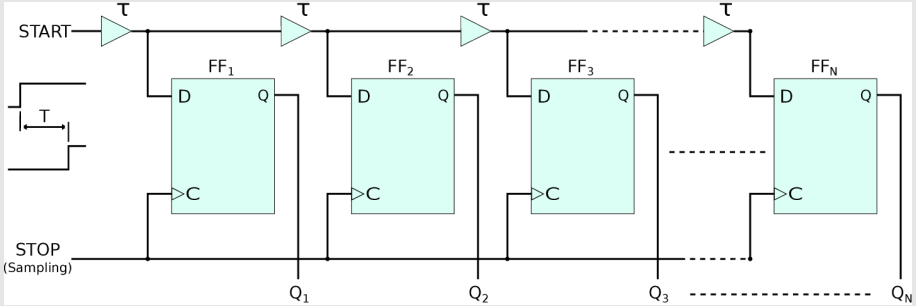
- TDC time precision down to 3.6 ps [RMS] (between two channels) using the wave union method [Jinyuan Wu] are possible
  - No cut on tails!
- Tradeoff for number of channels, time precision and dead time can be adjusted to the needs of the application
  - 64 channels in a FPGA
  - ~10 ps RMS time precision [RMS]
- TDCs in FPGAs work much better than expected (e.g. LVDS receivers): Let's use them for more applications!



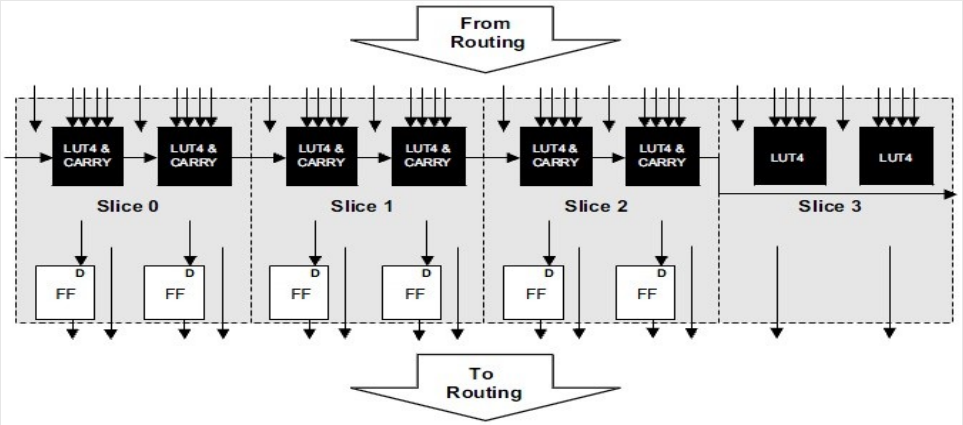
Published IEEE 2011, E.Bayer et al.

Time Digitisation in FPGA
using TDCs implemented in FPGAs

- Tapped delay line is used for fine time measurements – suits well with the FPGA architecture
- Delay elements are realised by LUTs
- Fast carry chain structure forms the delay line
- Registers are used to sample the delay line



Tapped Delay Line Method



PFU Diagramm

Time Digitisation in FPGA
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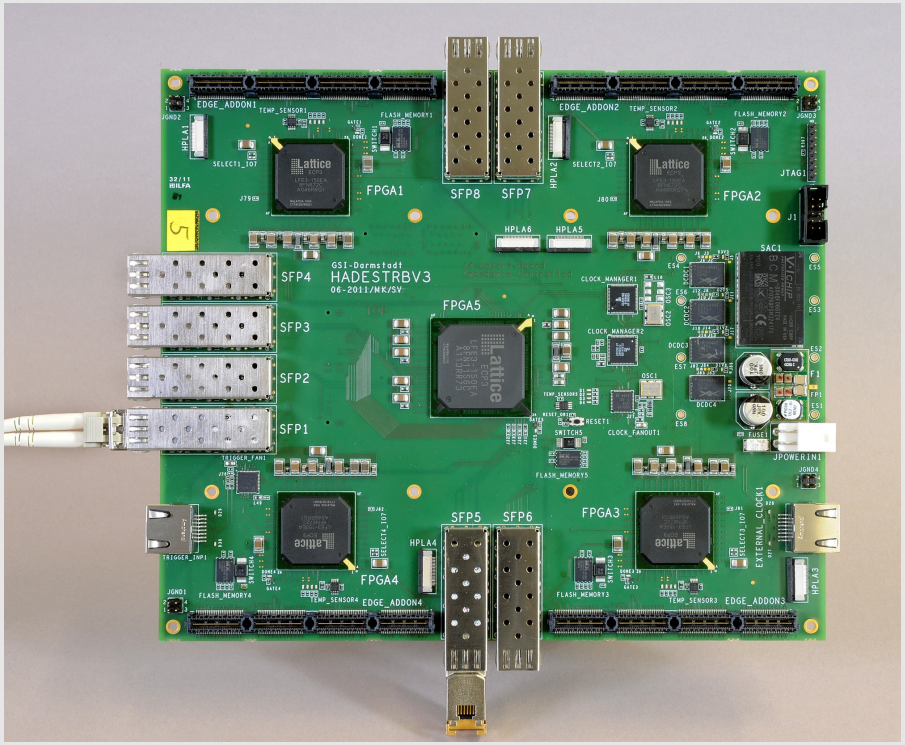


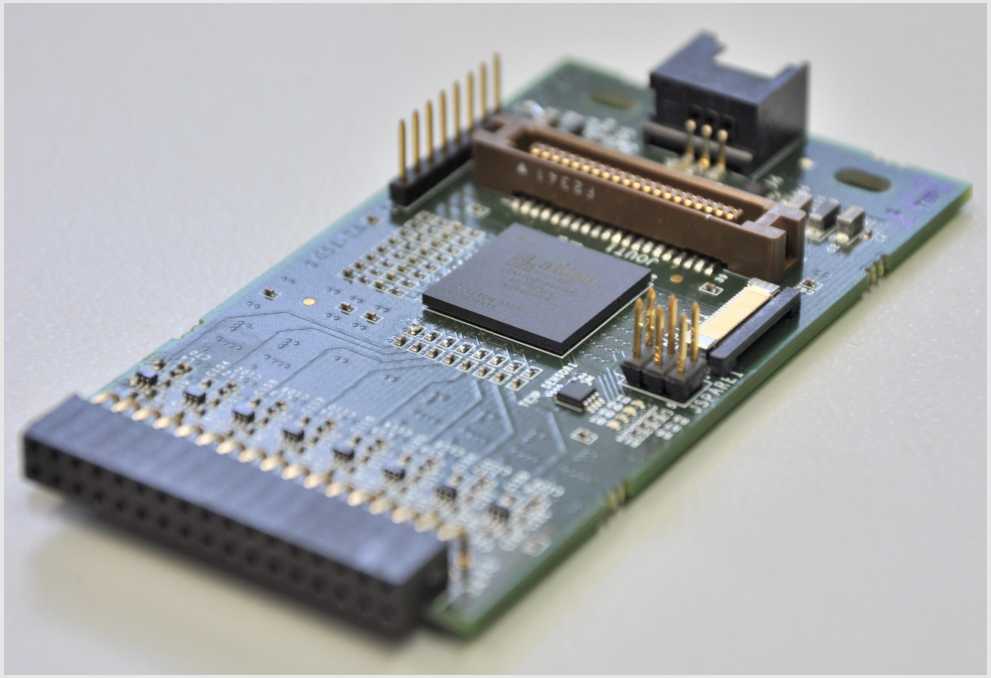
TRB3: the TRB3 collaboration
Photo by Gaby Otto, GSI Darmstadt, 28.09.2011.

- TRB3 with 4 FPGA-TDCs with a total of 256+4 channels
- ~20 ps time precision
- <1 ns min. pulse width limitation, no limitation in max. pulse width
- 50 MHz max. hit rate
- 300 kHz max. data readout trigger rate
- Works also in trigger less mode with time stamps
- TrbNetwork for internal/external communication
- Direct GbE connection for data and slow control; no CPU on board, all implemented in FPGA
- Usable for large system as well as stand alone system: just 48V and GbE are needed to take data
- Can be used as a pure digital board, for example as a data/trigger hub
- Applications: The time information encoded in the discriminated detector signal can be measured with FPGA-TDCs: Leading edge and pulse width

Signal Discrimination using FPGA

Input LVDS buffers as discriminators

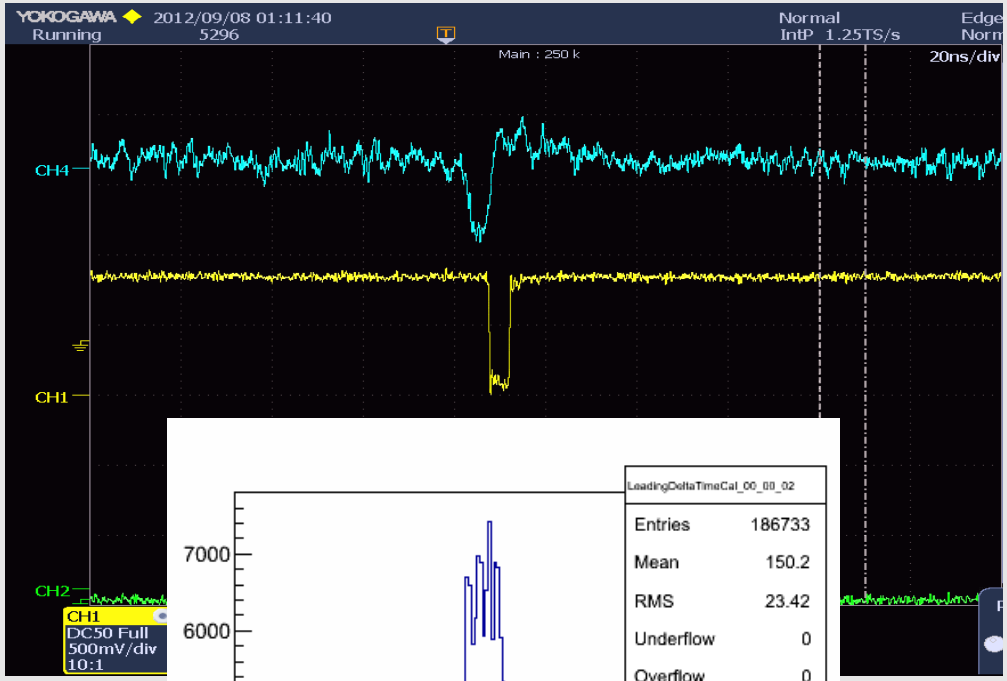
- The signals from the detector are pre-amplified with commercial amplifiers (MMICs)
- Input LVDS buffers in FPGAs are used as discriminators – Lattice MachXO2 is used
- The leading edge time and Time over Threshold is encoded in the digital pulse generated at the output LVDS buffers
- The thresholds are set by using the FPGA as DAC via PWM and low pass filter
- All the FEE is directly at the detector and only digital signals is are sent out for measurement
- For precise time measurements of the digital pulse, the TDC implemented in FPGA is used (TRB3)

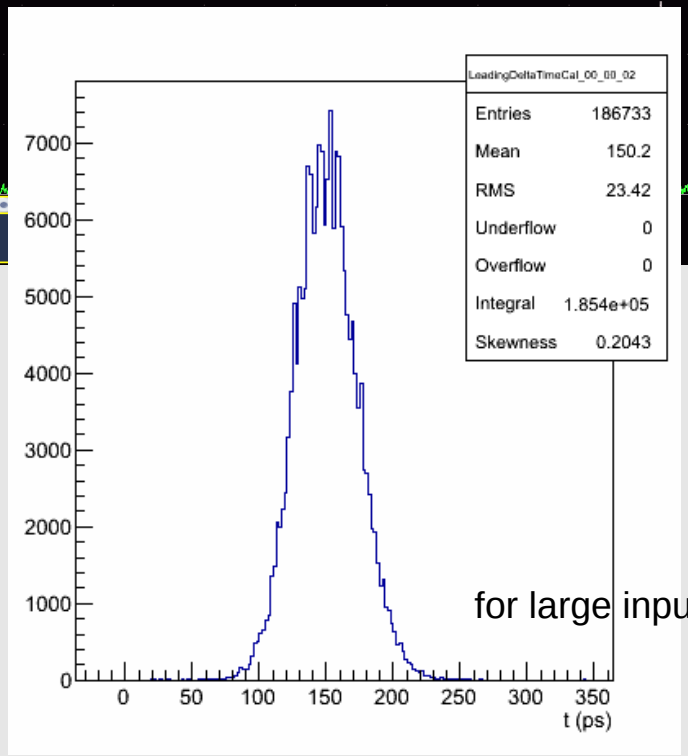


Signal Discrimination using FPGA

Input LVDS buffers as discriminators

- Tested with 500 µV, 6 ns width, analogue signal as input to PCB
- Amplified by factor 40, discriminated at the FPGA-LVDS receiver and sent out to TRB3 as a LVDS signal
- Threshold is set on the reference LVDS input via a PWM + low-pass with a resolution of <100µV
- FEE cost (without PCB+connectors) per channel only 0,56€ (16 channel version)
- Tested recently at the PANDA DIRC beam time at Jülich with 2400 channels PMT/MCP-PMT: single photons are seen!

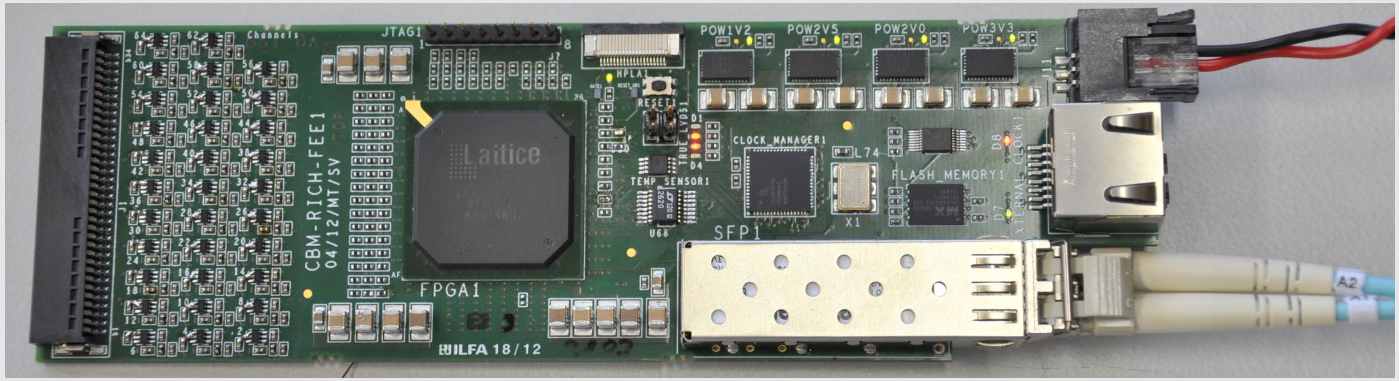




for large input signals

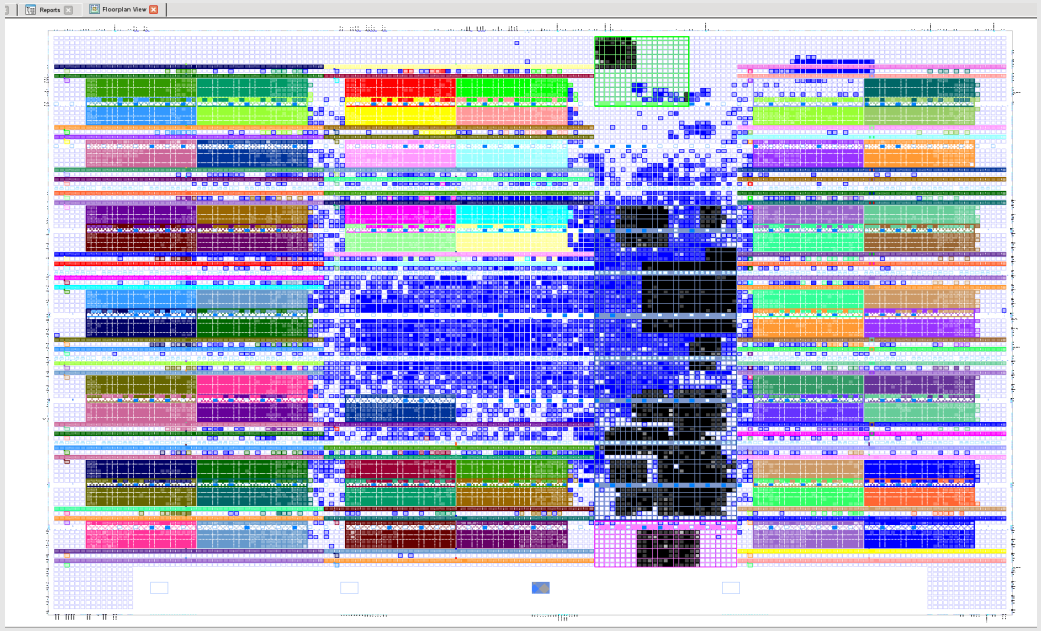
Time Digitisation in FPGA

FEE & 65 channel TDC on a board plugged to the detector



- 64 signals from detector
- Amplification
- Thresholds
- Input signal discrimination
- Time measurement
- Data readout

- Trigger signal is digitised for reference time (65th channel)
- Data readout through 2GBit/s optical link
- 5x16 cm to be plugged on the back of an MCP-PMT
- Very high density for FEE & 65 channel TDC + DAQ + Power
- Tested during the CBM October 2012 test beam
- The Sync message is processed at the internal TRB3-CTS and distributed to 4 FEEs
- Half detector readout with CBMRICH-FEE, other half with nXYTER



Time Digitisation in FPGA

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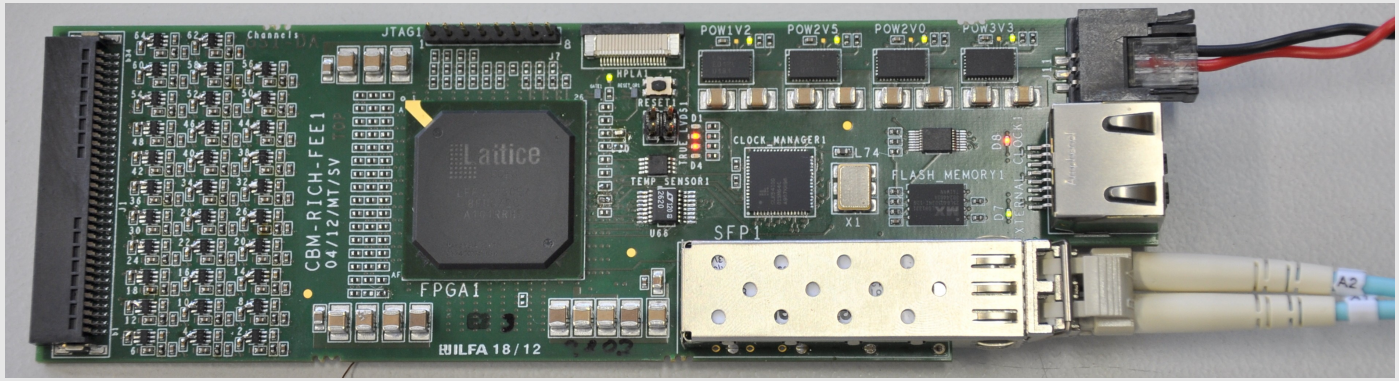

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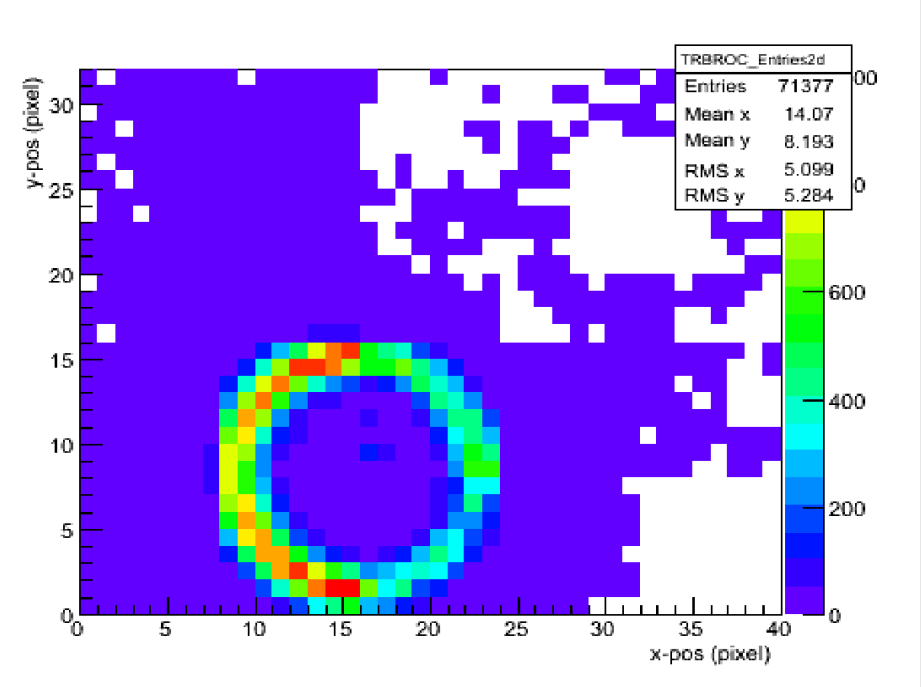
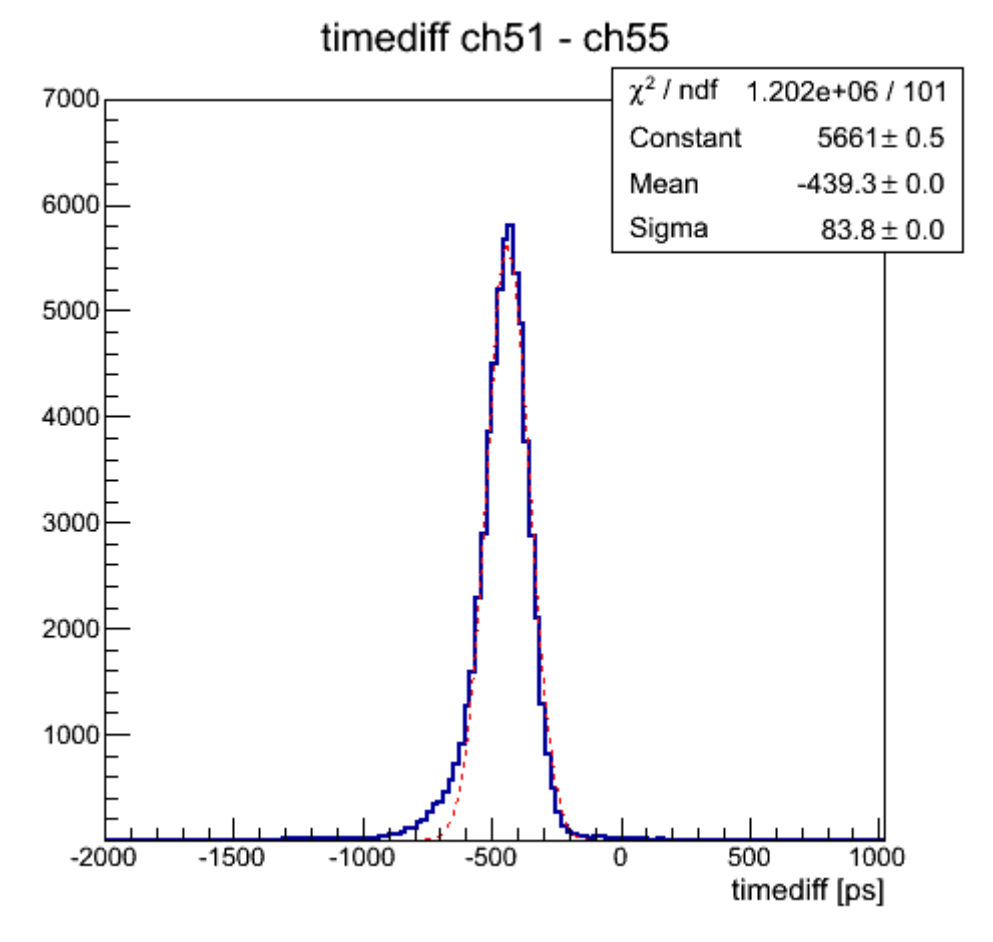


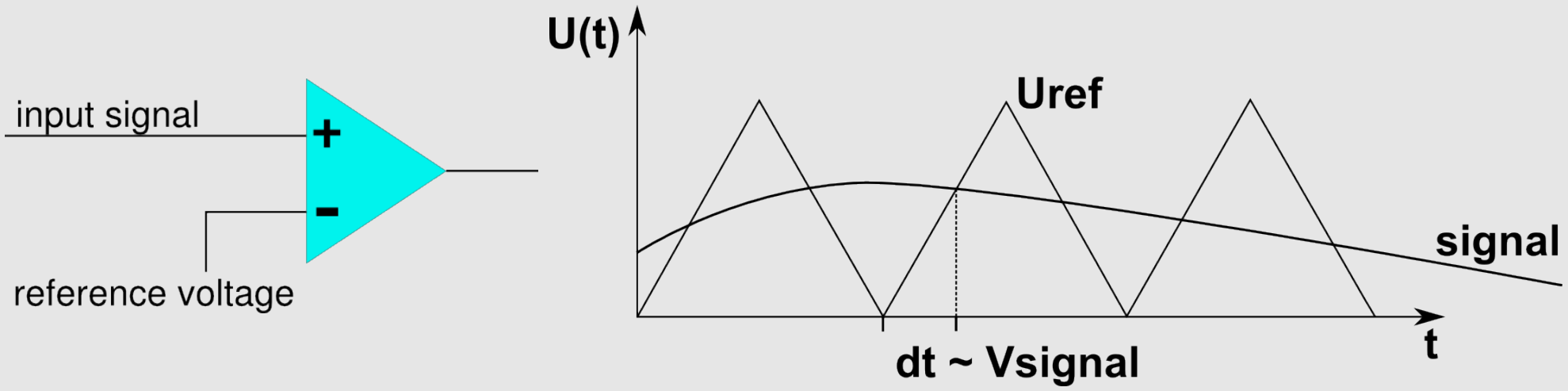
Time Digitisation in FPGA

FEE & TDC on the same board



- Time difference between pulser output signals is measured
  - 84 ps time precision
- Layout errors cause small oscillation on output of amplifiers which destroy the good time precision

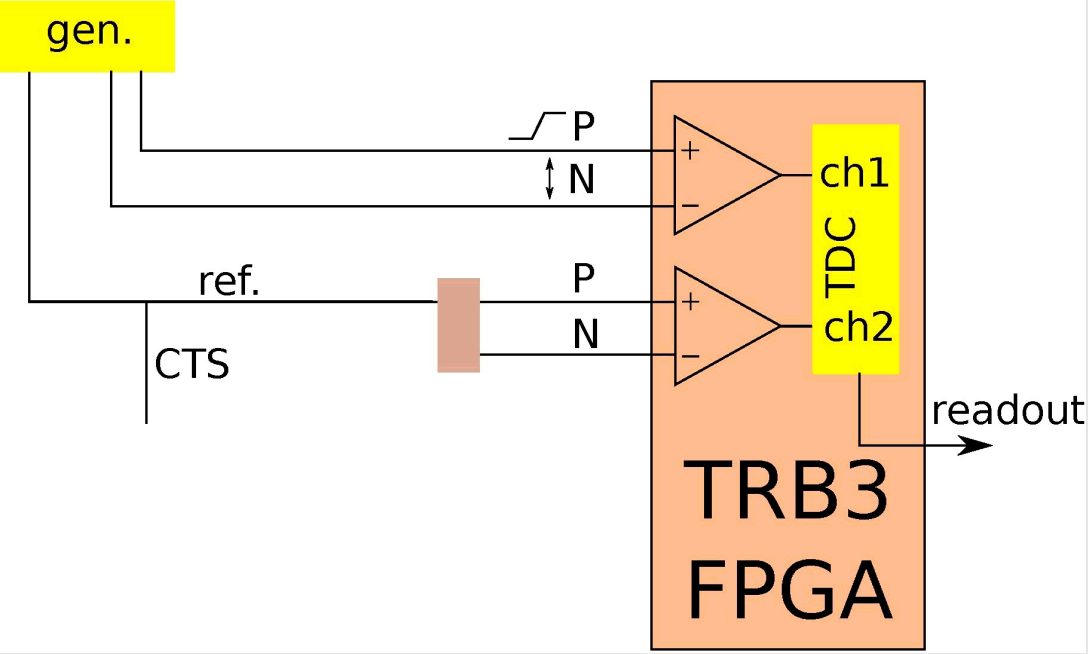
Amplitude Digitisation in FPGA
concept

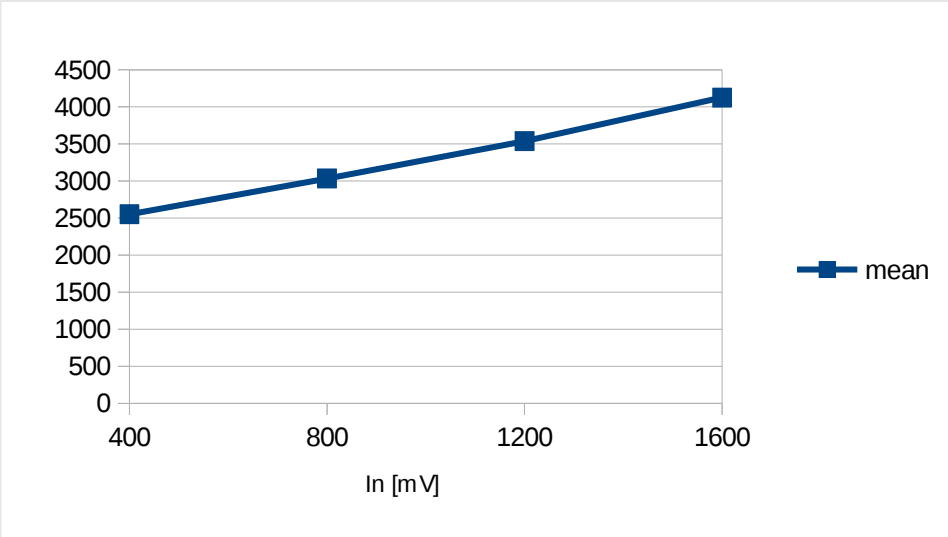


- Generate ramp on reference pin, measure time until ref. crosses signal
- 10bit ADC, 50MSPS needs 20ps time precision
- Advantage: many channels in one FPGA (one ramp generator), no data transfer to the FPGA, low power
- Question: What performance can be really reached?

Amplitude Digitisation in FPGA

Switching Characteristics



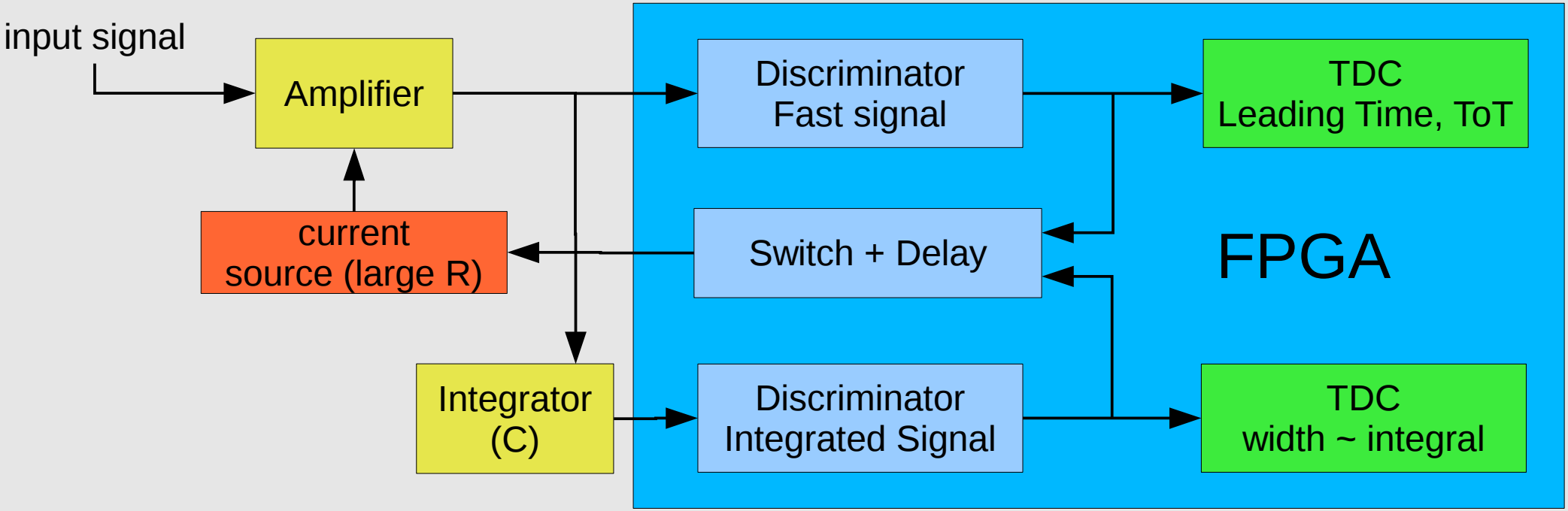


- measurements with externally generated signals show that
  - the ADC concepts works
  - the measured TDC time precision for 26ns ramps is compatible with a ADC with 10 bits precision and 20 MSPS
- An integrated solution with on board ramp generator has to be implemented and evaluated

Ch2 level [mV]	Mean[ps]	Jitter (RMS)[ps]
400	2551	50
800	3034	24
1200	3538	18
1600	4125	15

Charge Measurement with FPGAs QDC-concept

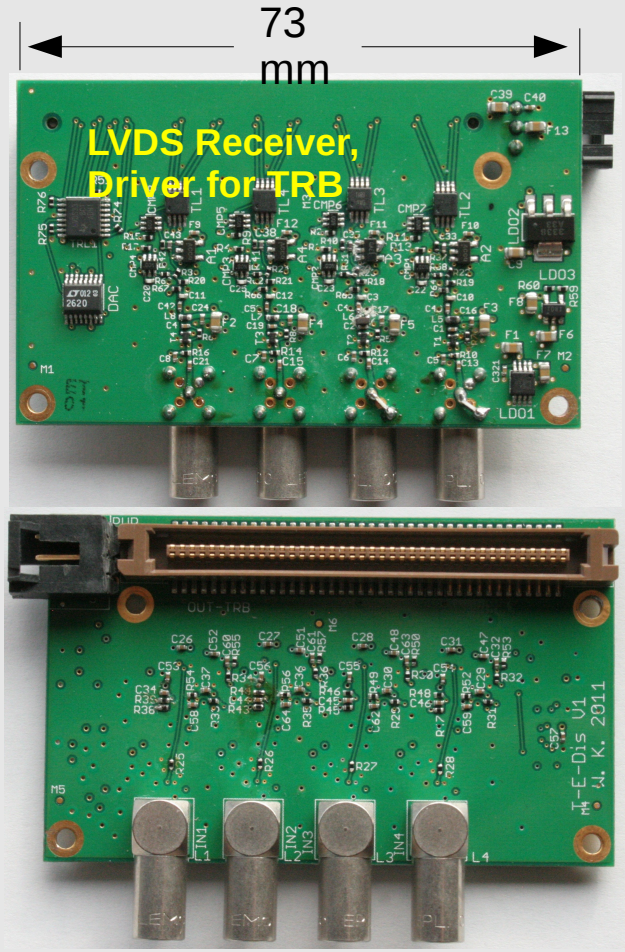
- Idea: Modified Wilkinson ADC
  - Integrate input signal with a capacitor
  - Discharge via current source → fast crossing of zero
  - Measure time to reach zero ~ Q



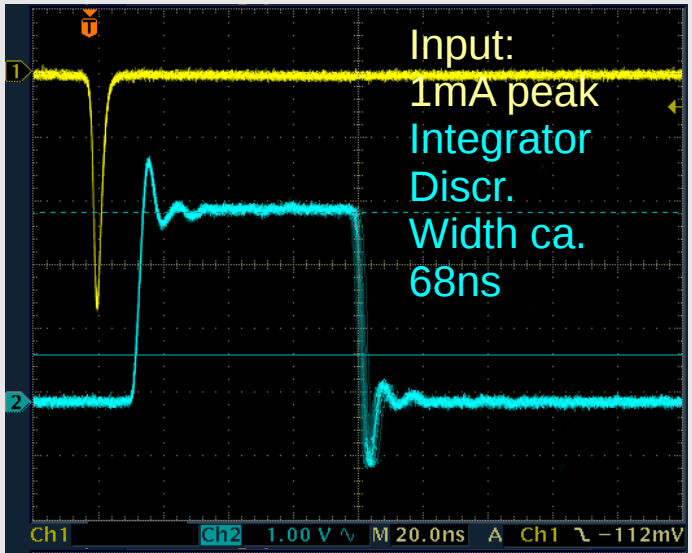
QDC Prototype

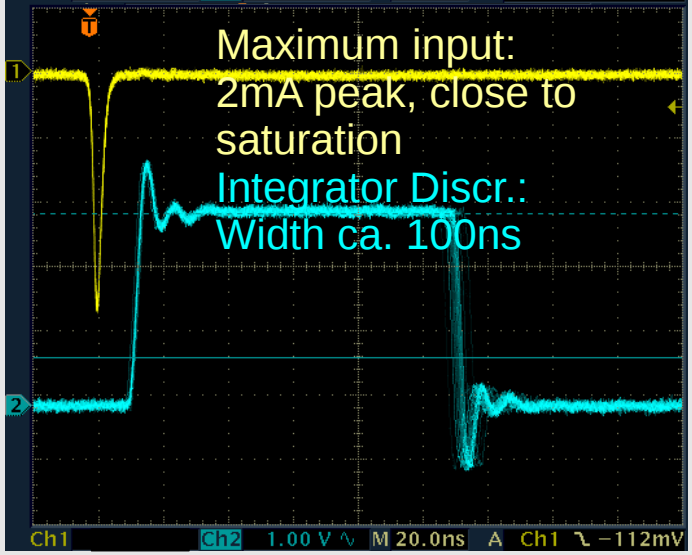
- First results with offline correction: 0.2% charge precision, dynamic range: 50
- Alternative circuit (less components) has recently been built (Krakow) and tested. Comparison is still to be done.
- Applications: Calorimeters, e.g. HADES-ECal, CBM-PSD?

Prototype Board (4 channels) for TRB 2



Size determined by connectors and TRB 2 infrastructure





Conclusion & Outlook (I)

- A multi-purpose FPGA based TDC module with 256+4 channels and a time precision <20ps RMS, <1ns min. pulse-width detection has been developed
- With the integrated trigger system and GbE all you need is power and Ethernet cable to run a DAQ
- FPGA based discriminator boards as well as highly integrated full-system solutions to be plugged on the detector have been built: results from the lab and from test beam times are very promising and bugs have been identified and removed.
- Advantages: “simple” concept, components from the shelf (fast realisation), very flexible, TDC and DAQ is finished and read to use
- Disadvantage: larger than a tailored ASIC solution, but still quite small
- Double edge detection in single TDC channel is implemented but currently still be worked on (degradation of precision)
- ADC design using precise TDCs is being implemented
- TDC-based QDC prototype has been successfully tested, system for HADES Calorimeter application is currently in design phase

Conclusion & Outlook (II)

- The main advantage of the proposed solution is **not** in the available hardware (TRB3, Padiwa, etc.), but the
  - existing group of highly motivated people keeping the project alive (8 persons deeply involved)
  - existing know-how and code base of a system which has been developed over the last 4 years and (painfully) debugged during test and production beam times
  - large “user” community (in fact co-developers as they find the bugs in the system during heavy use)
    - HADES, PANDA-Straw-Tracker, PANDA-DIRC (Barrel, Disc), CBM-MVD, CBM-RICH, Neutron Detector (A1-Collaboration), BN@N (Dubna) + many smaller users
    - Hopefully: CBM-PSD and CBM-TOF

Thank you for your attention!

References

[1] J. Kalisz, Review of methods for time interval measurements with picosecond resolution, Metrologia, 2004.
[2] LatticeECP2/M Family Handbook, HB1003, Version 04.3, March 2009.
[3] J. Song et al., A high-resolution time-to-digital converter implemented in field-programmable-gate-arrays,IEEE TRANSACTIONS ON NUCLEAR SCIENCE, 2006.

Backup Slides

TDC in FPGA
Tapped Delay Line Method

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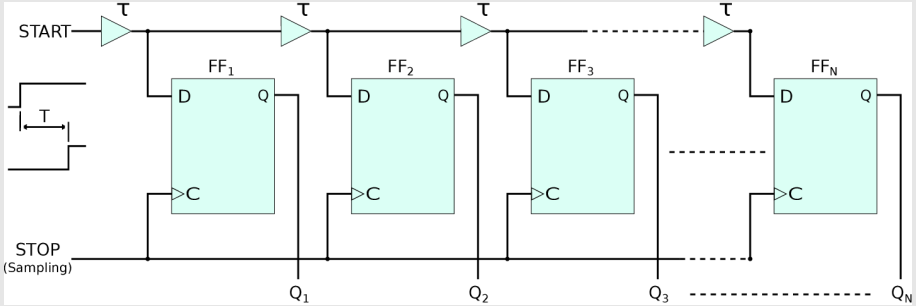
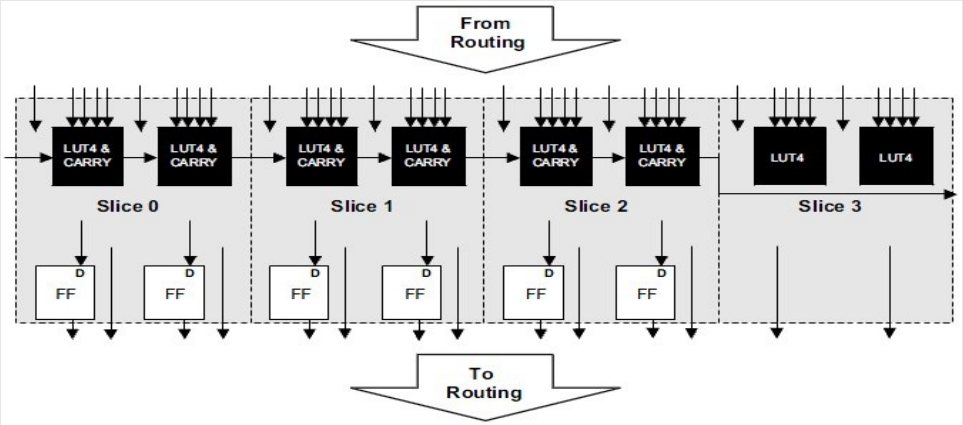


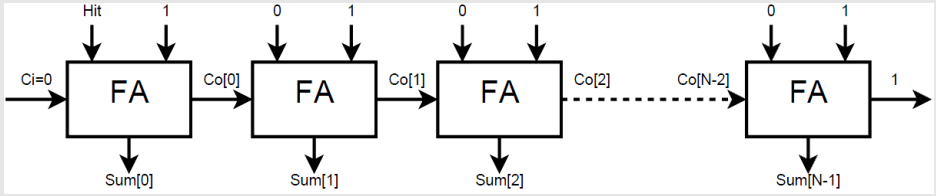
Tapped Delay Line Method [1]



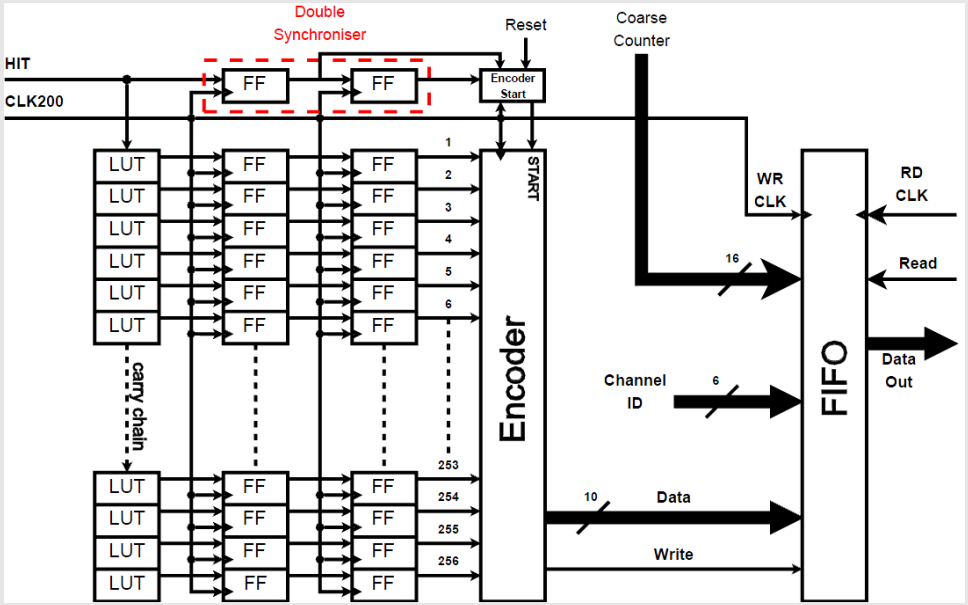
PFU Diagramm [2]

TDC in FPGA

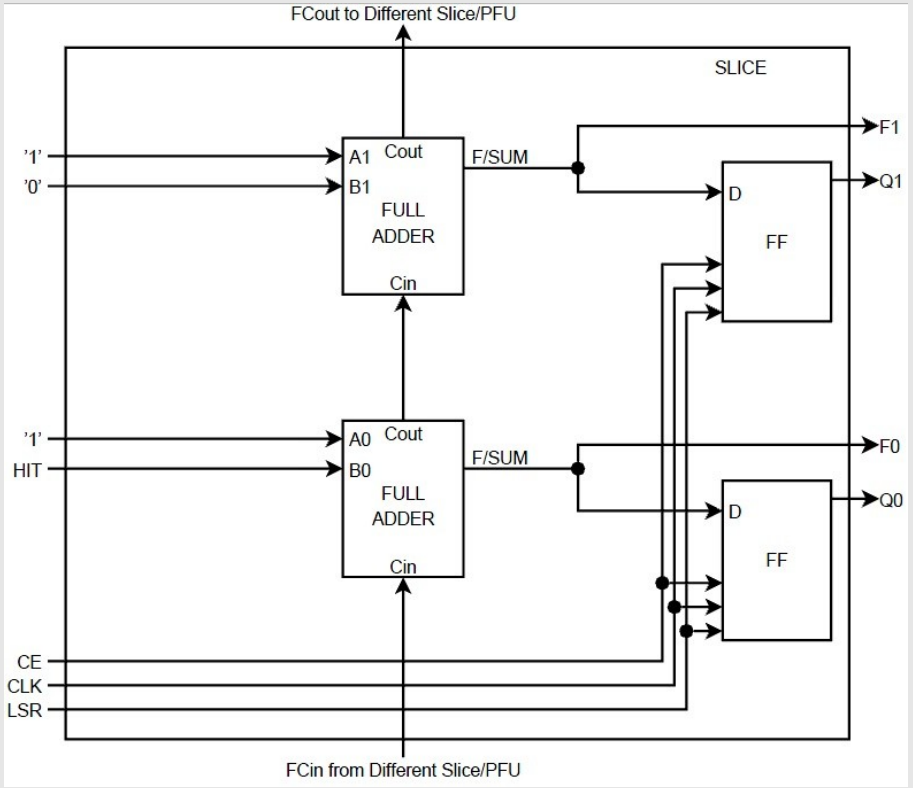
Architecture of the TDC



Delay line is realised with Full Adders [3]



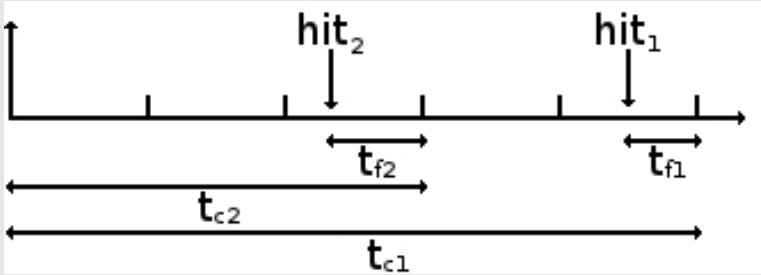
TDC Architecture



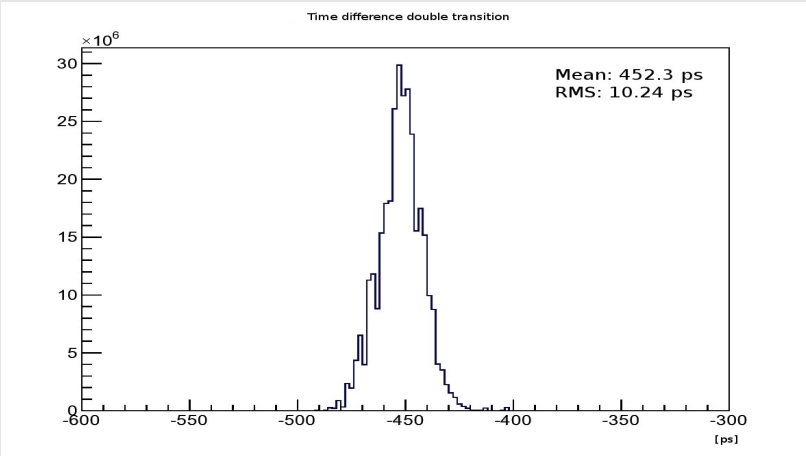
Slice diagram with LUTs programmed as Full Adders

Laboratory Test Results

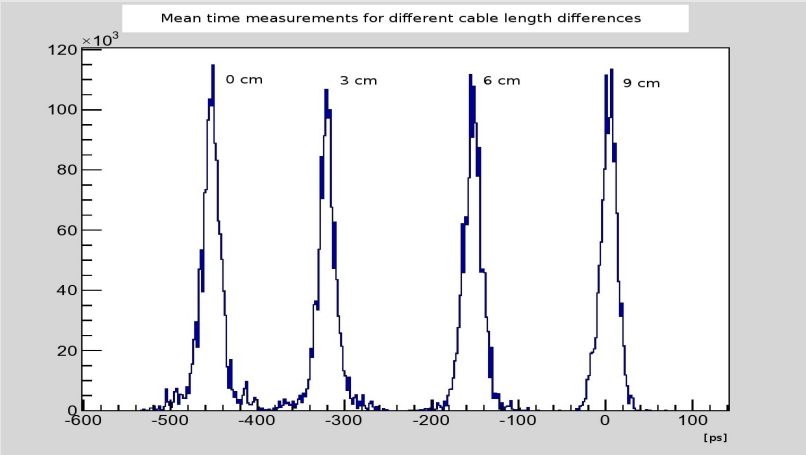
- Time difference measured between 2 channels
- $\Delta t = (t_{coarse1} - t_{coarse2}) - (t_{fine1} - t_{fine2})$
- RMS measured: 10.34 ps against the same clock
- Precision: 10.34 ps / √2 = 7.3 ps RMS



Time difference between two measurements

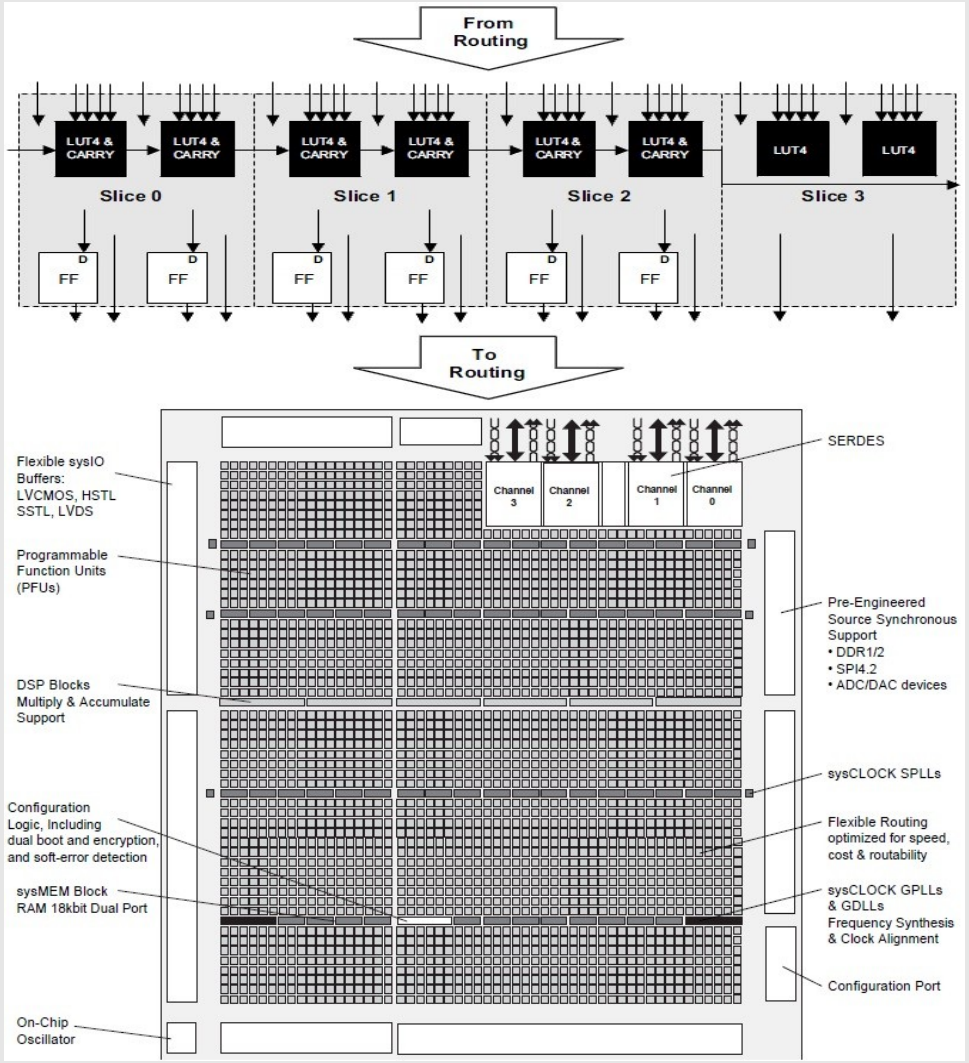


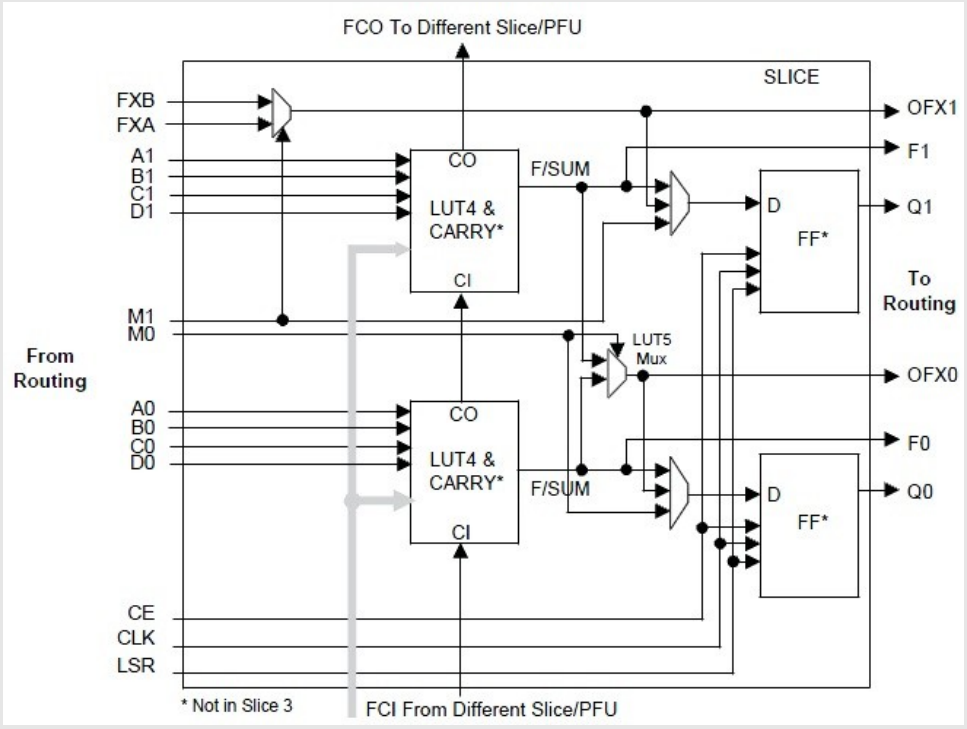
Time precision test



Mean measurement test

Architecture of Time-to-Digital Converter

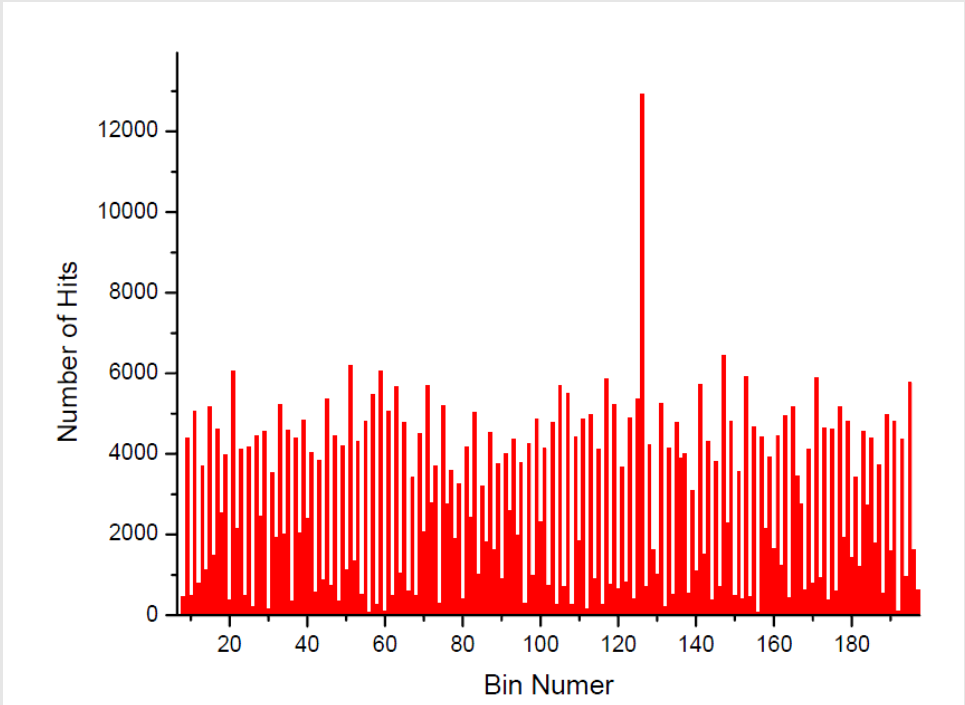


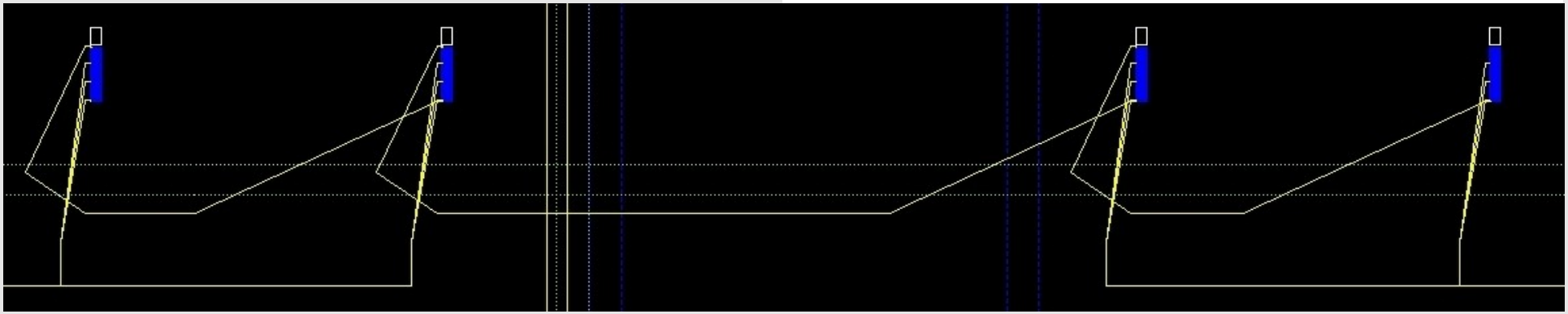


Lattice ECP2M FPGA Slice Diagram, PFU Diagram and Floorplan

Architectural Effects of FPGA

- Effect of primary clock line in the FPGA
- Effect of longer inter-slice routings
- Effect of PFU architecture





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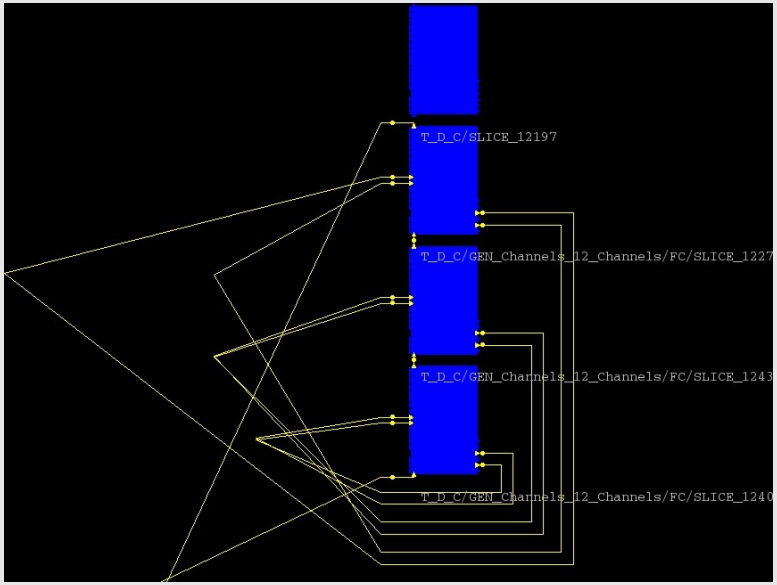

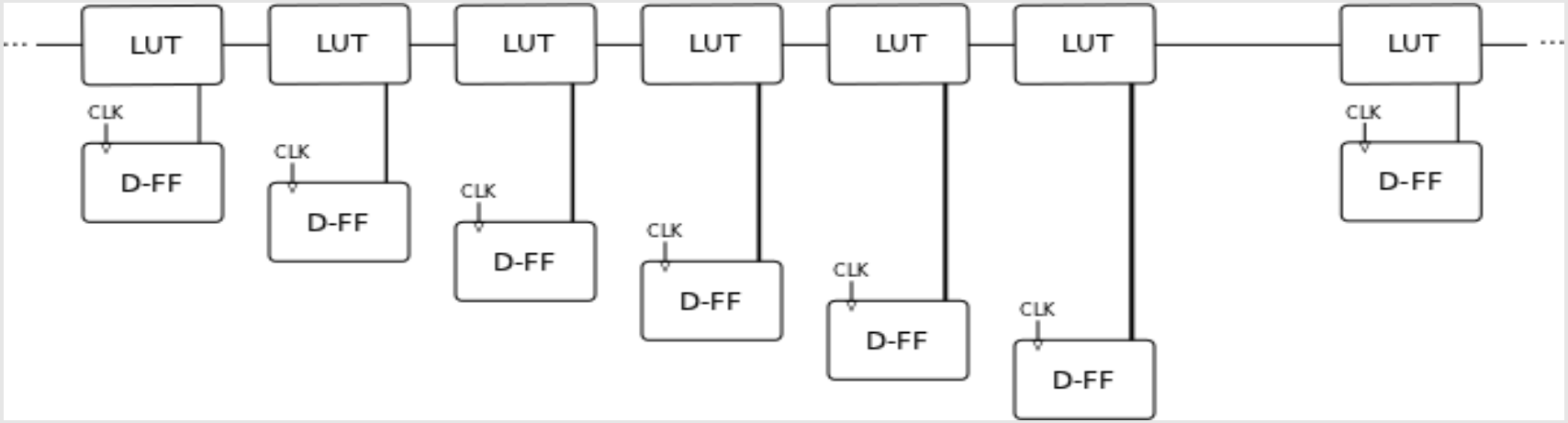

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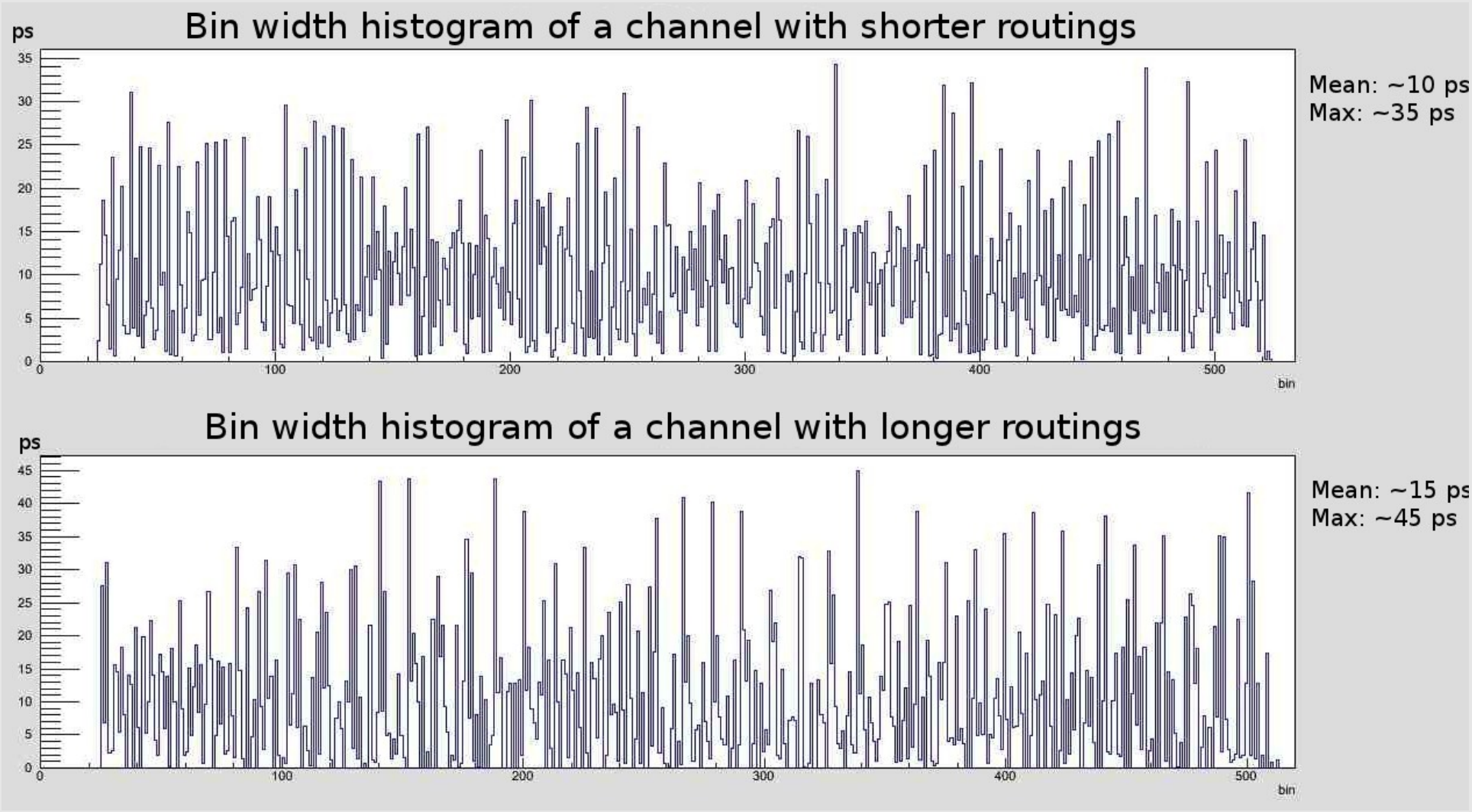

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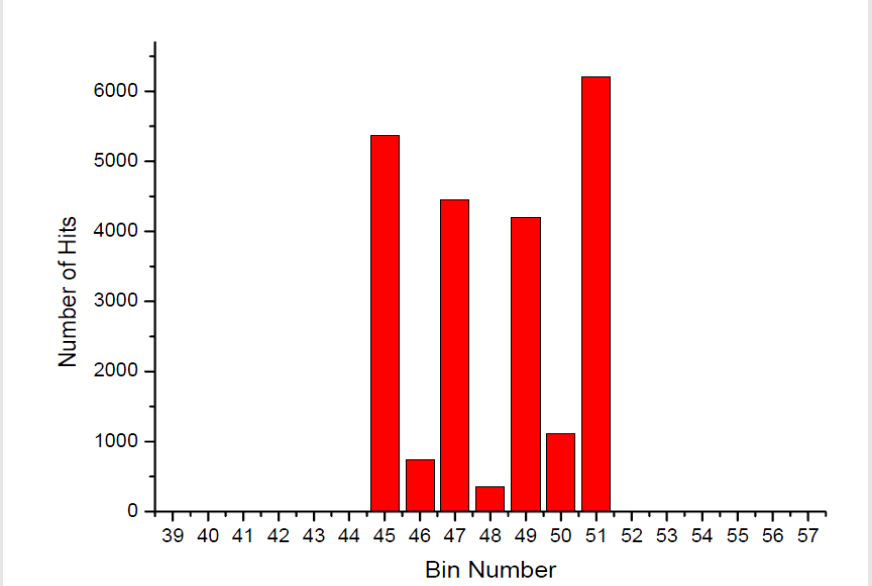
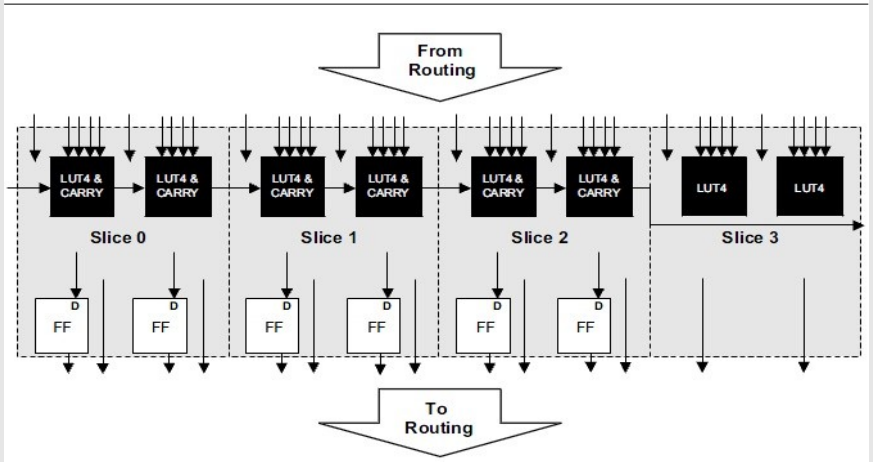
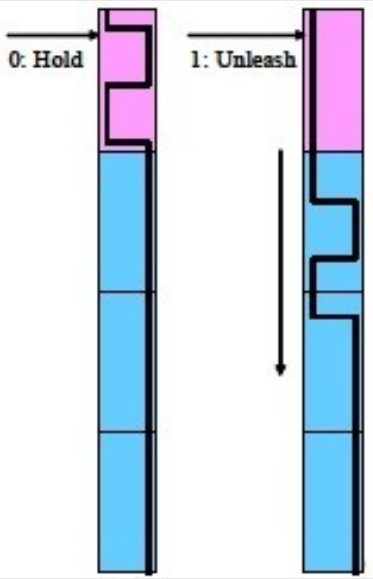
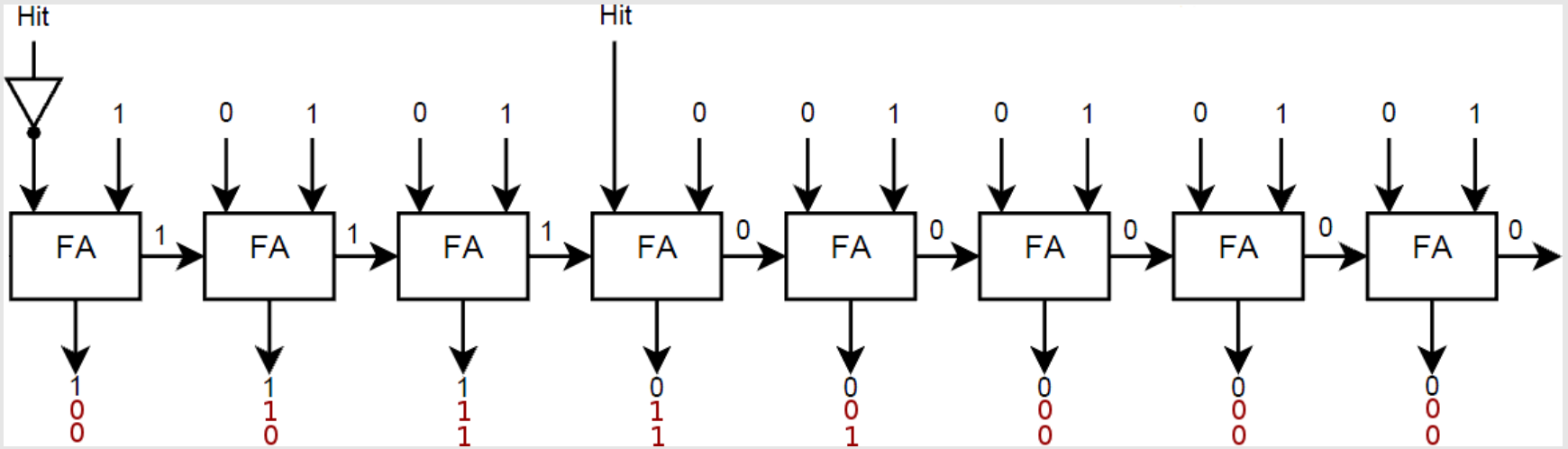




Wave Union Launcher

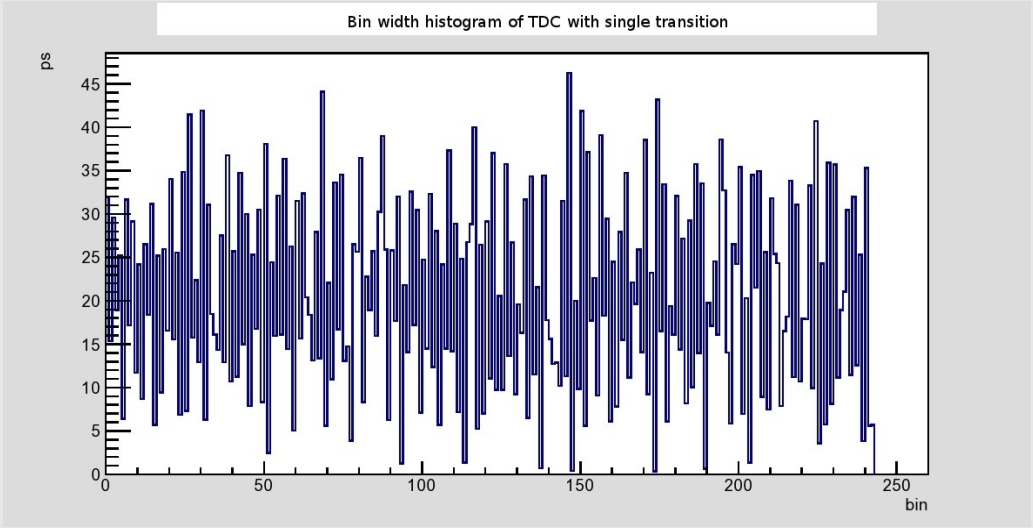
- More than one delay line is necessary in order to reduce the effect of wide bins
- Wave union launcher is implemented
- Bin widths & non-linearities are reduced



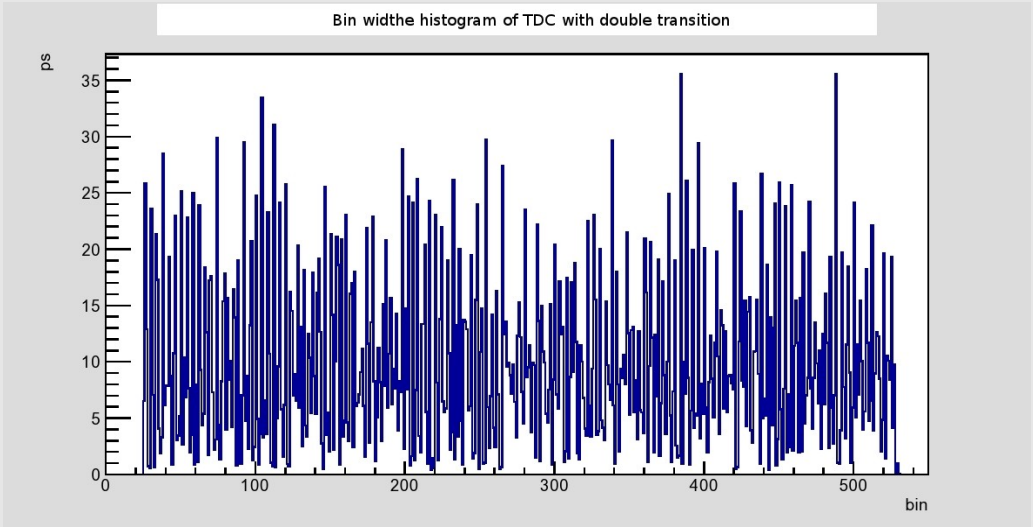


Wave Union Launcher

- More virtual bins
- Narrower bins
- Homogeneous bin distribution



Bins: ~240
Mean: ~20 ps
Max: ~45 ps



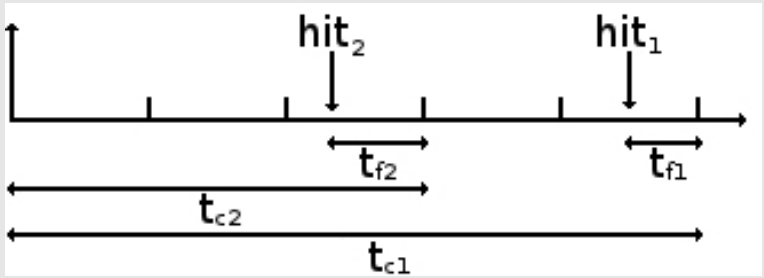
Bins: ~520
Mean: ~10 ps
Max: ~35 ps

Statistical Error & Precision

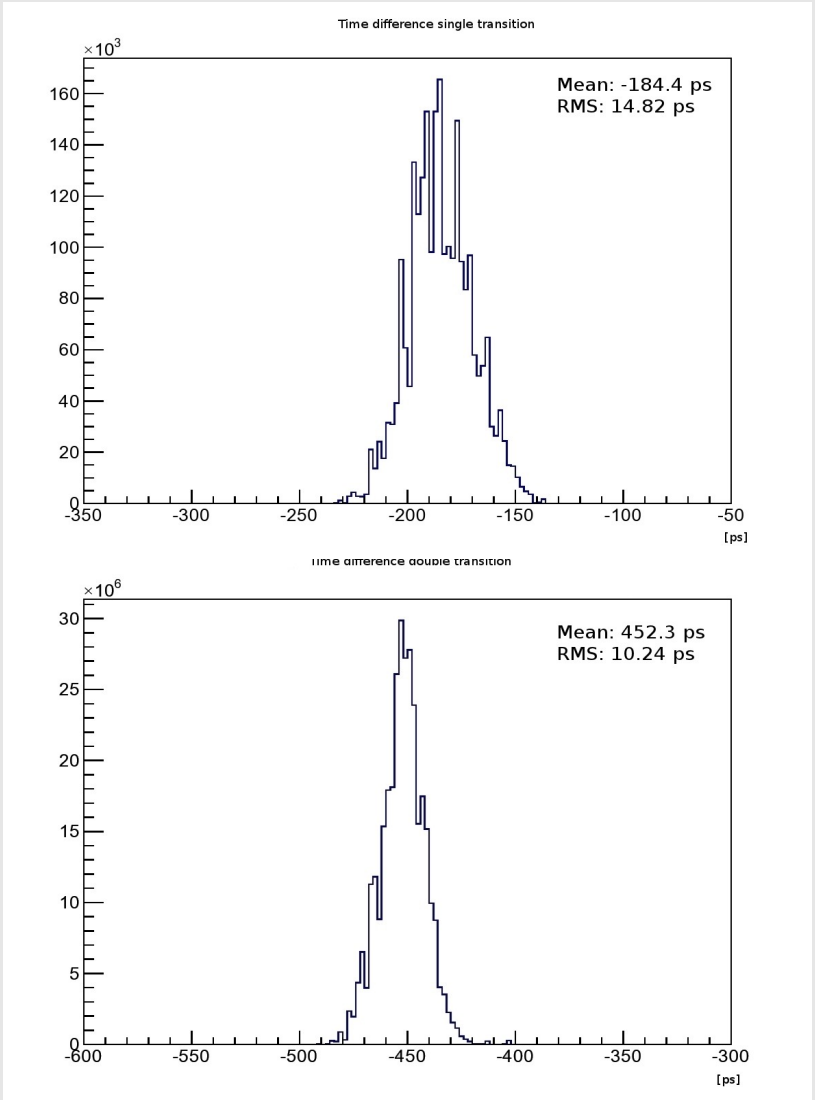
- Time difference measured between 2 channels
- $\Delta t = (t_{coarse1} - t_{coarse2}) - (t_{fine1} - t_{fine2})$
- RMS measured: 10.34 ps

  against same clock
- Precision: 10.34 ps / √2 = 7.3 ps
- Effect of 2 transitions:

  14.82 ps / 10.34 ps = 1.43 factor

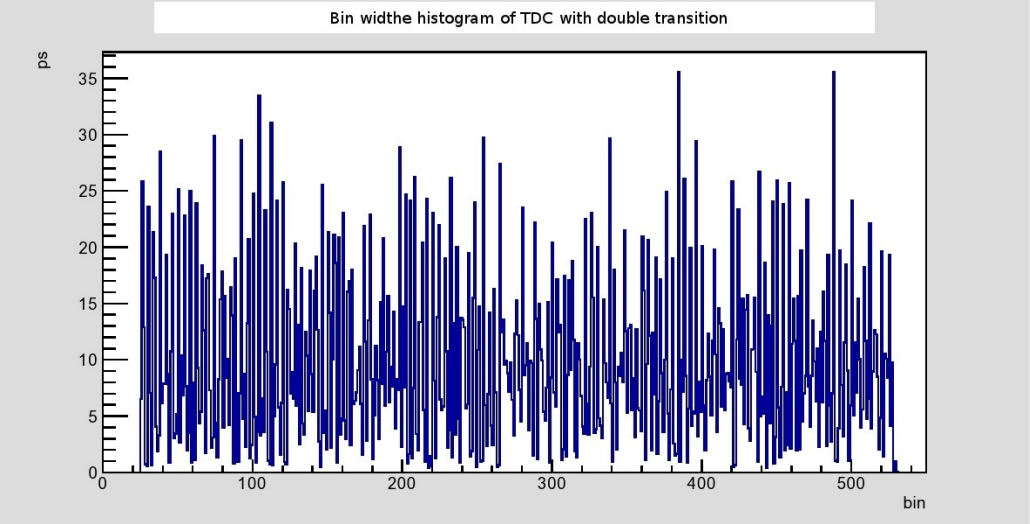


Time difference between two measurements

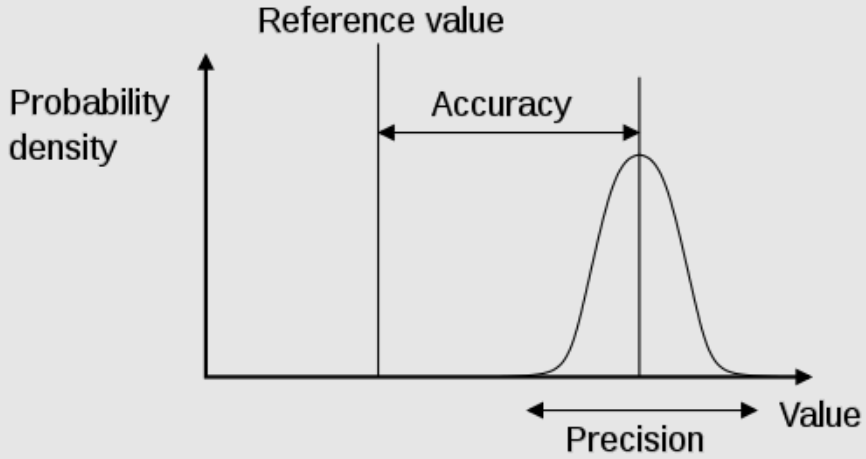


Resolution vs. Precision

- Resolution: The smallest unit of measure or the smallest change that can be displayed or recorded by an instrument (sometimes referred to as granularity*



- Precision: How reproducible or close identical measurements will be reported as a percentage of full scale*



http://en.wikipedia.org/wiki/Accuracy_and_precision

* http://www.foodtechcorp.com/accuracy-resolution-and-precision-explained.html