JÜLICH
FORSCHUNGSZENTRUM

The Jülich Digital Readout System for PANDA Developments

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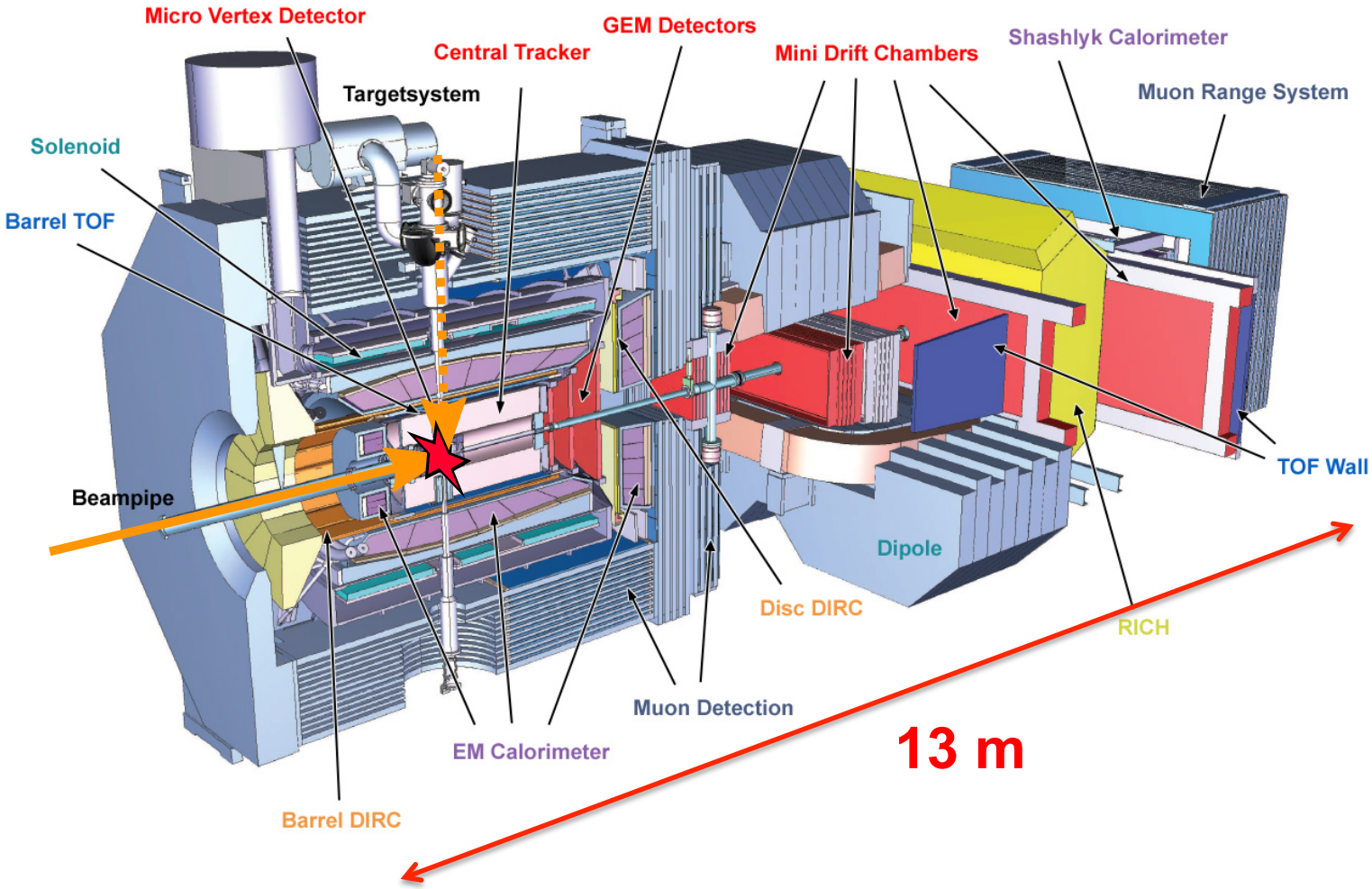
Outline

- The PANDA experiment
- The Micro Vertex Detector
- The Jülich Digital Readout System :
  - Software
  - Hardware
  - Firmware
- UDP implementation
- GBT implementation
- Summary

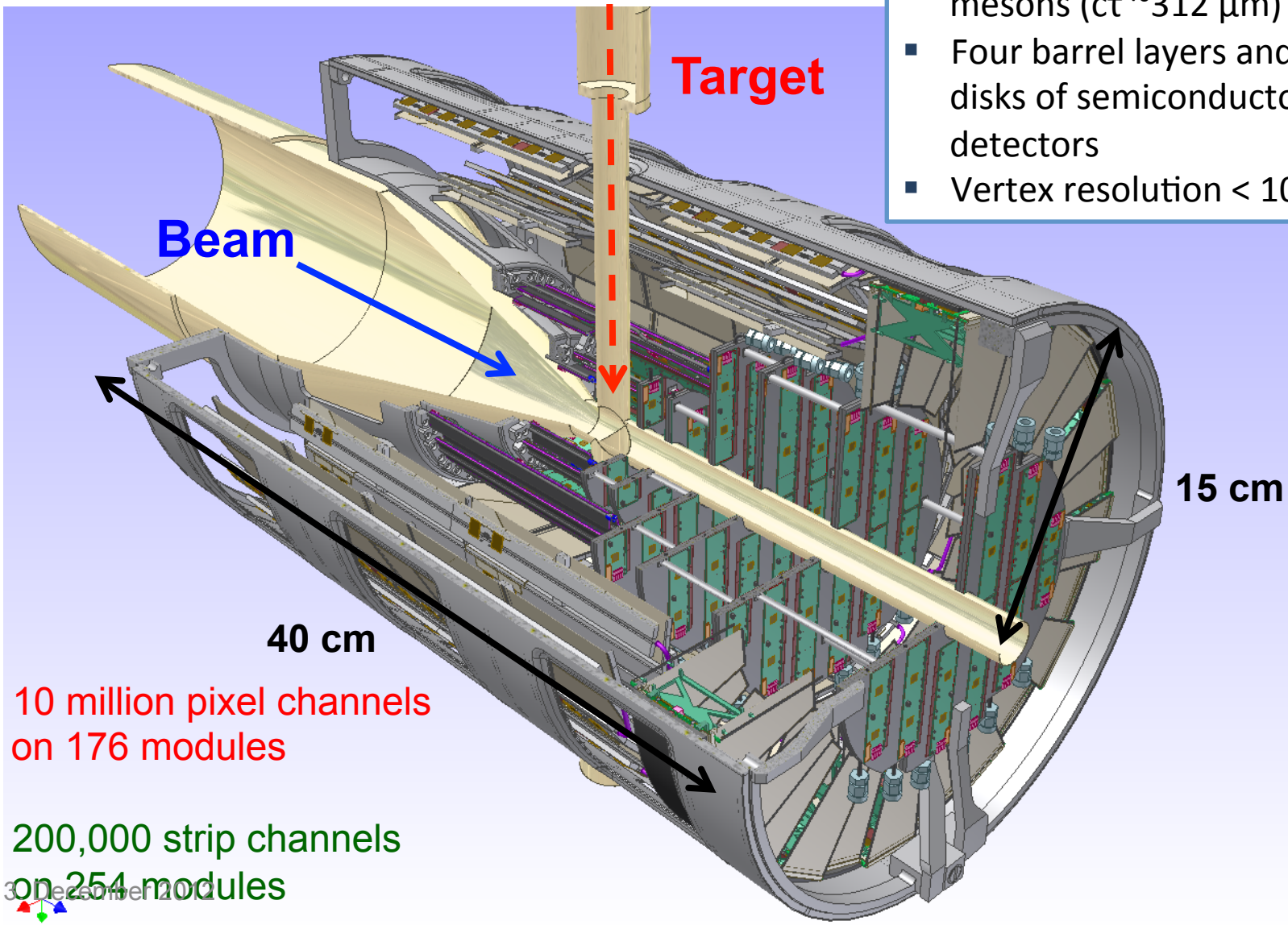
The $\bar{P}$ANDA experiment



- Study of the strong force
- Open and hidden charm spectroscopy
- Fixed target experiment
- Beam momentum 1.5 – 15 GeV/c
- $\bar{p}p$ / $\bar{p}A$ reaction
- Phase space cooled beam

Micro Vertex Detector (MVD)

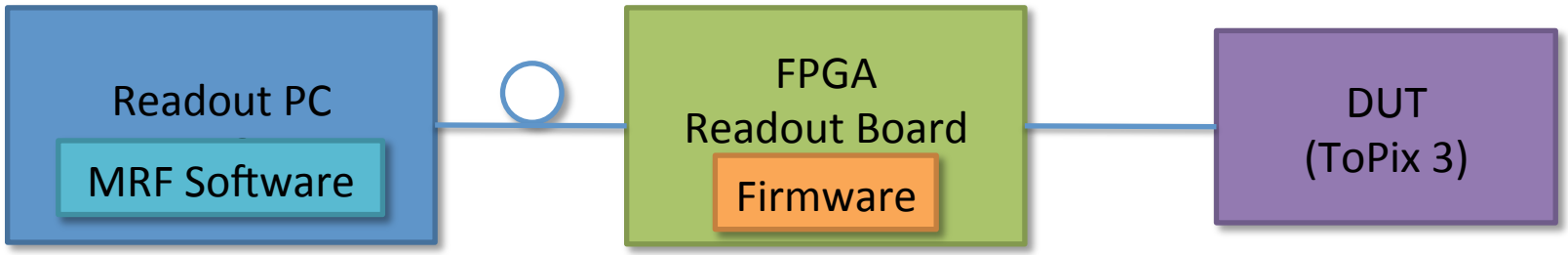
- Main task: vertexing of D-mesons (cτ ~312 µm)
- Four barrel layers and six disks of semiconductor detectors
- Vertex resolution < 100 µm



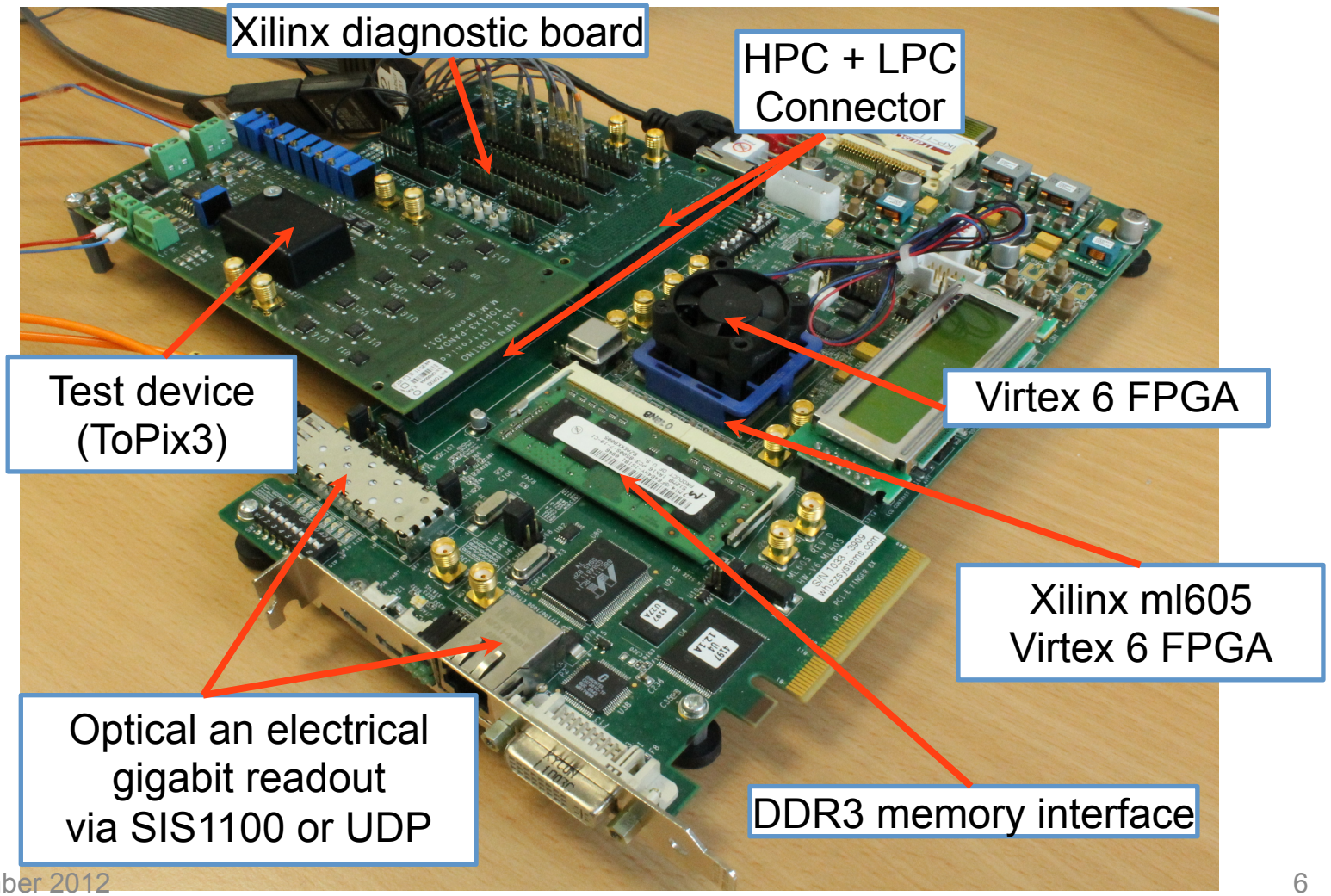
- 10 million pixel channels on 176 modules
- 200,000 strip channels on 254 modules

Jülich Digital Readout System

- Readout system necessary for front end ASIC development
- One system to characterize different ASICs – modular approach desirable
- Capable of single ASICs and whole detector parts
- Requirements: Fast for high data rates, flexible for different kinds of ASICs and easy adoptable to reduce development time

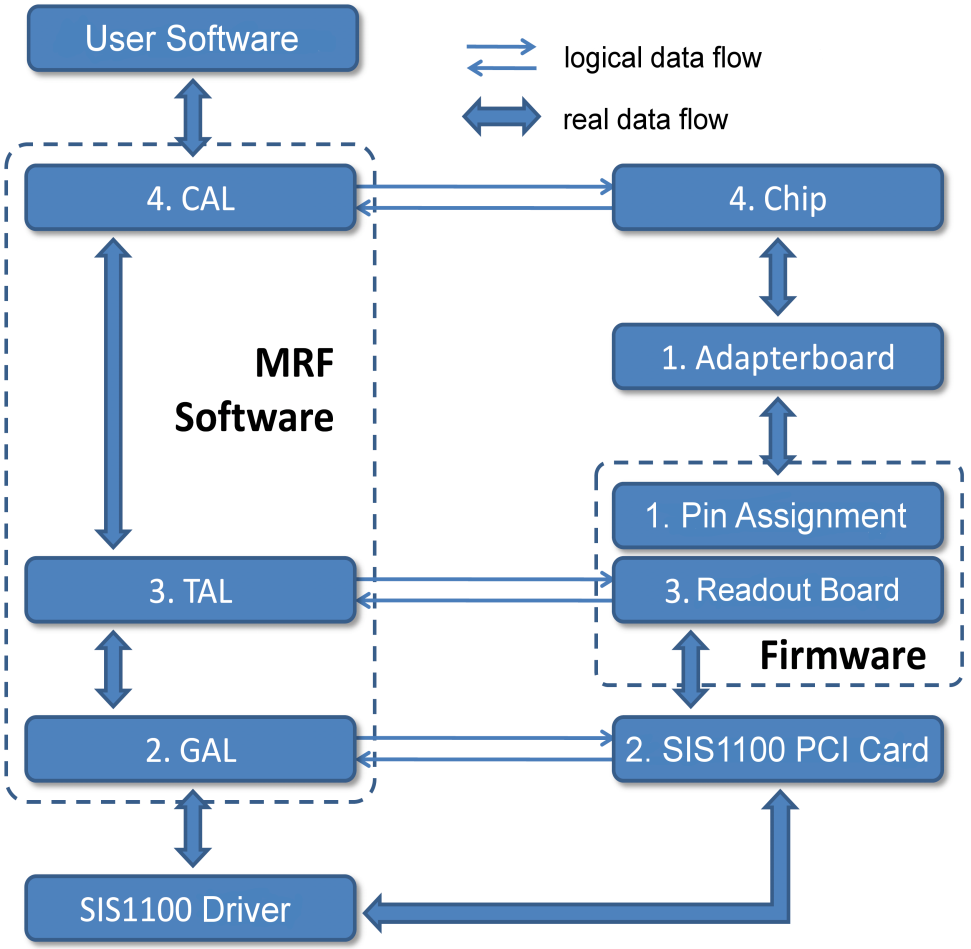


Digital Readout Board



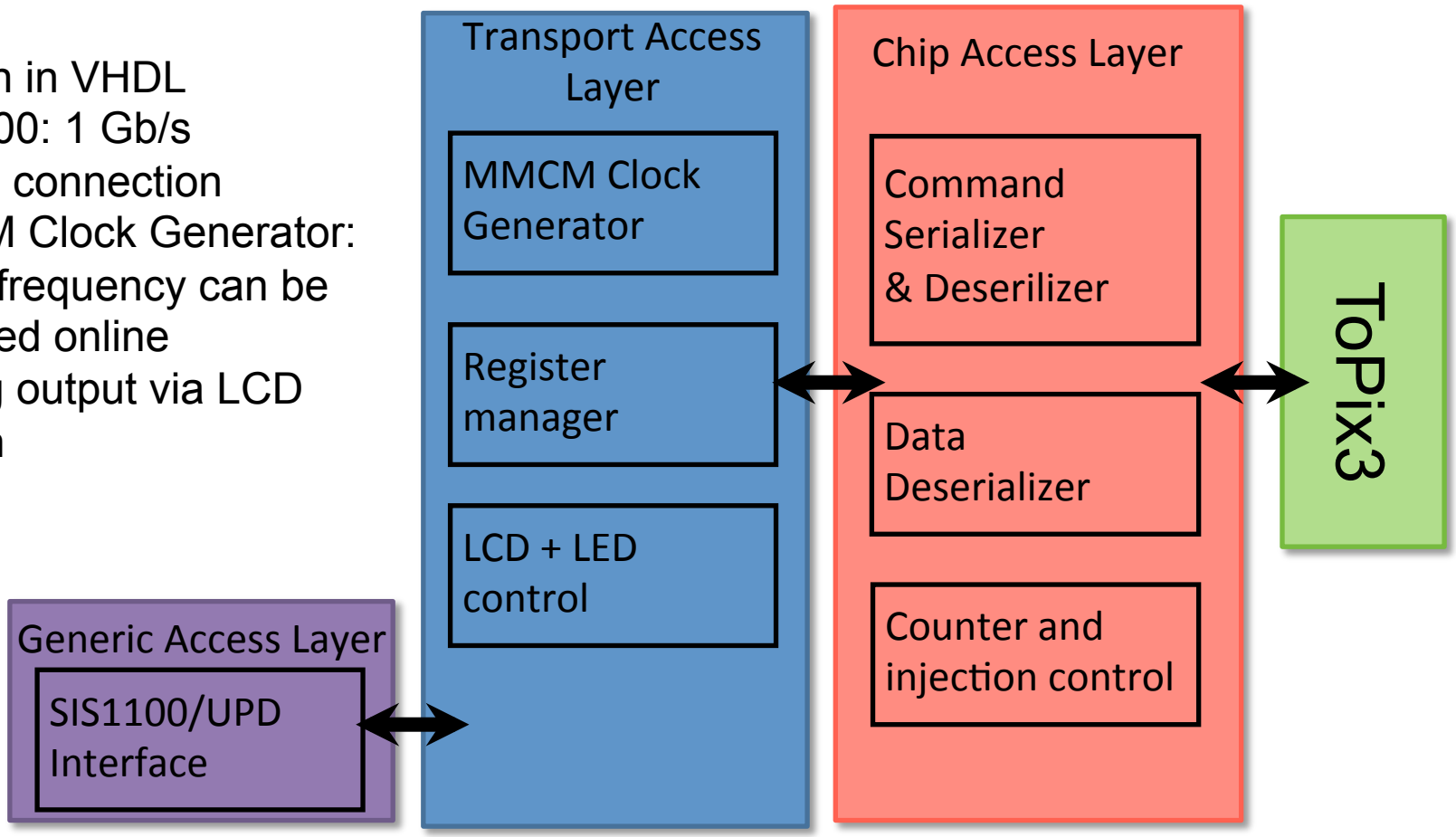
Software Framework

- MVD Readout Framework (MRF)
- Written in C++
- No external dependencies except STL
- Defines four communication layers:
  - **Physical Layer** : Establishing signal connection
  - **Generic Access Layer** (GAL) : Communication between FPGA board and readout PC
  - **Transport Access Layer** (TAL): Access to functionality of the readout board
  - **Chip Access Layer (CAL)**: Communication with the DUT



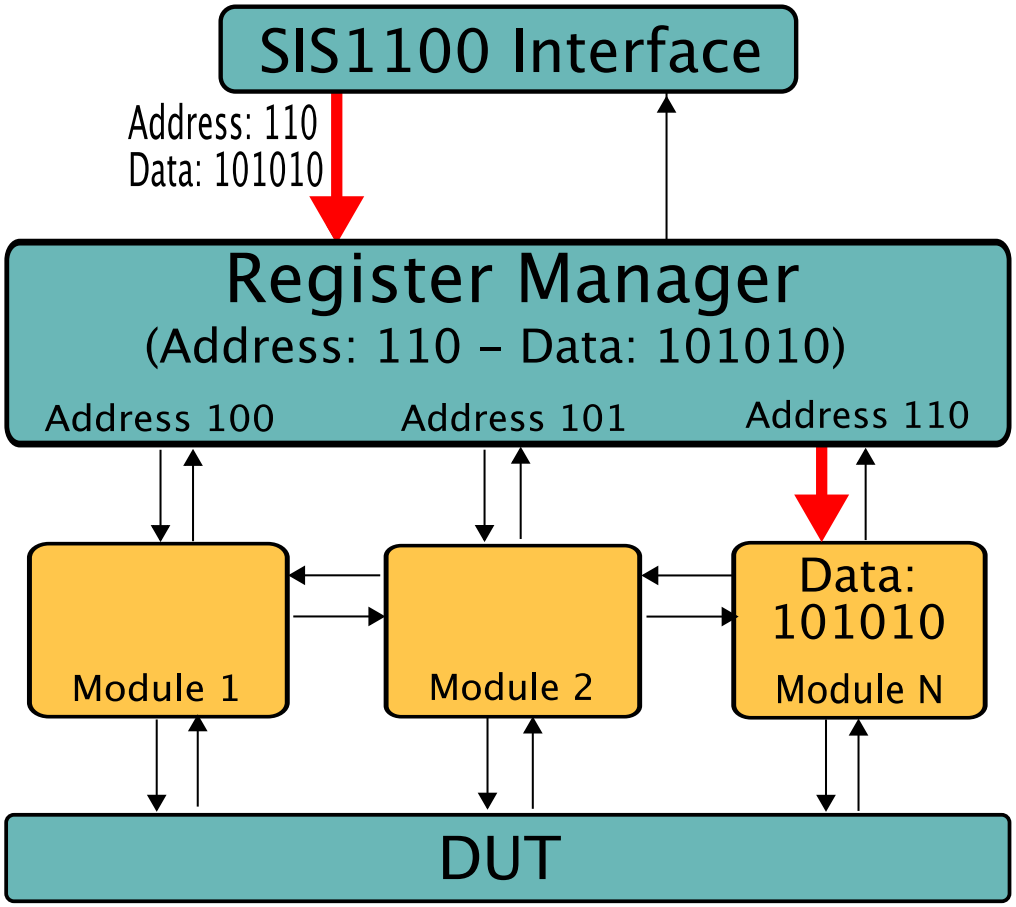
Firmware

- Written in VHDL
- SIS1100: 1 Gb/s optical connection
- MMCM Clock Generator: Clock frequency can be changed online
- Debug output via LCD screen



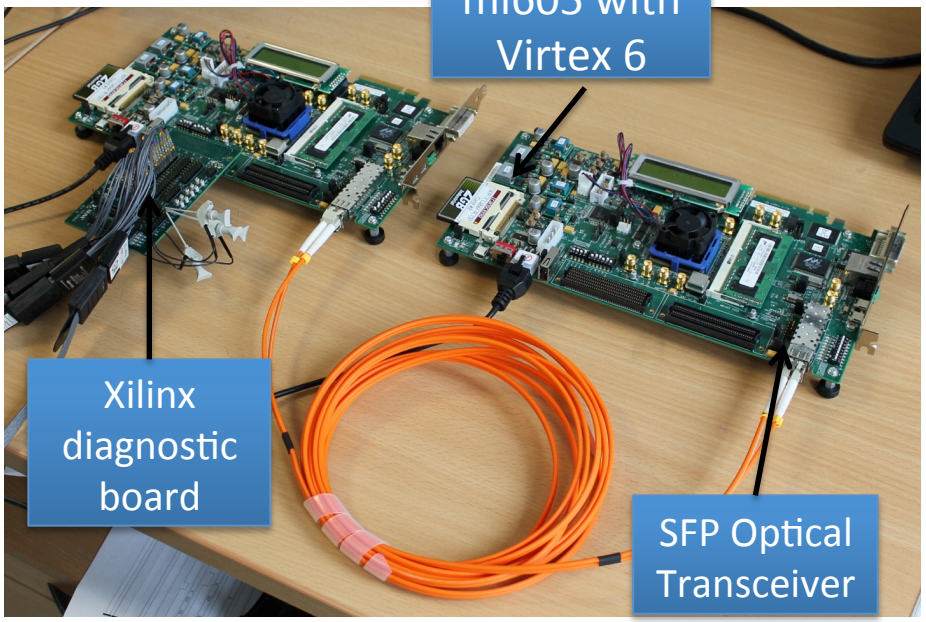
Register Manager

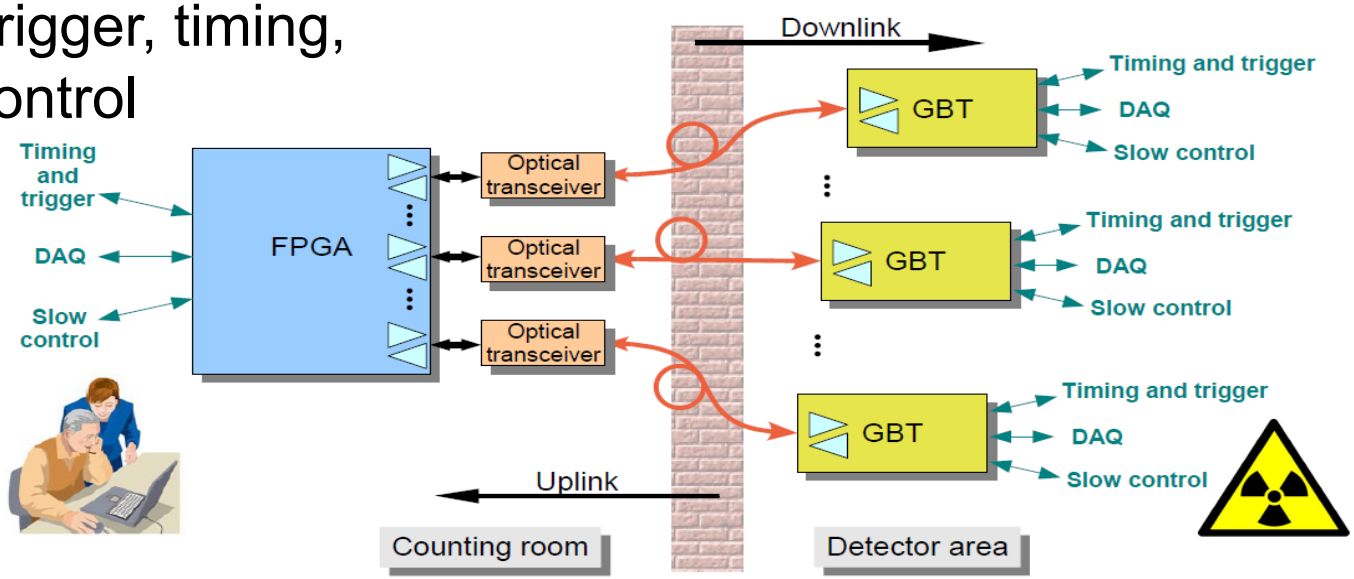
- Packages formatted in address-data pairs
- Register manager distributes the data depending on the address to the concerning modules.
- Modules have different functionality:
  e.g. Module-1 writing configuration to DUT



Implementation of GBT

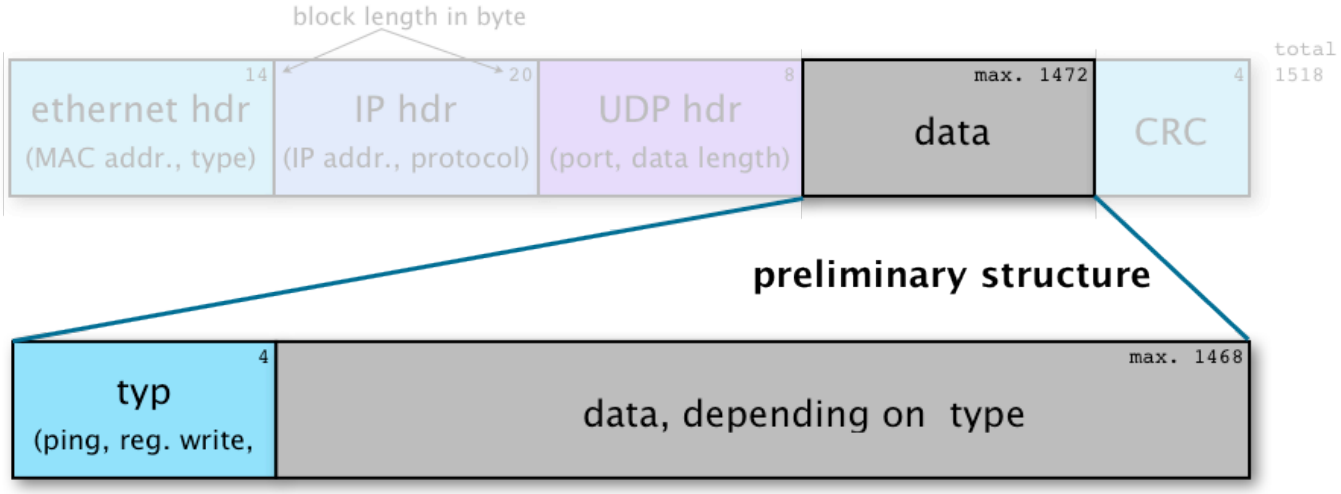
- GigaBit Transceiver, developed at Cern for SLHC upgrade
- Development of a radiation hard bi-directional optical link
- Line rate: 4.8 Gb/s. User data rate: 3.36 Gb/s
- Combined transmission of physical data, trigger, timing, fast and slow control





Implementation of UDP link

- Ongoing development: Implementation of communication via UDP
- Additional communication link
- Standard hardware can be used



Example: writing a value to an FPGA internal register

Summary

- The Jülich Digital Readout System has been developed to characterize different ASICs for the development of the PANDA detector.
- The system includes hardware, firmware and software developed with a modular approach for easy adaption to new interfaces.
- The Readout System is successfully working with the MVD Pixel front end prototype ToPix2 and ToPix3
- A UDP link implementation is under development
- A GBT link implementation into readout system is under development to interface the next prototype ToPix4

Dankeschön

Thank you for your attention