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The Juelich Digital Readout System for $\overline{\text{P}}$anda development

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The $\overline{\text{P}}$anda detector is one of the main experiments at the upcoming Facility for Antiproton and Ion Research in Darmstadt (FAIR). The fixed target experiment will explore $\overline{\text{p}}$p annihilation with intense, phase space cooled beams with momenta between 1.5 and 15 GeV/c.
For the development of the Micro Vertex Detector (MVD), the innermost tracking detector of $\overline{\text{P}}$anda, the evaluation of prototypes and detector parts is very important. Different prototypes of the pixel front-end chip ToPix (Torino Pixel) need to be tested and characterized under similar conditions to improve the development.
To control these devices unter test (DUT) and to save the taken data a suitable readout system is necessary.
To have similar conditions for different prototypes a modular concept of a readout system is required which can be adapted in a simple way to the specific interface of different types of electronics.
To meet the requirements of an upcoming full size ToPix prototype and online analysis an upgrade of the Juelich Digital Readout System was developed.
The Xilinx ML605 evaluation board with the Virtex 6 FPGA is the main harware component of the upgraded system providing a 1 GBit/s optical connection and 2Gb DDR3 RAM. The DUT can be connected via a 160 pin free configurable connector to the FPGA.
An overview about the system componentens and measurements of the ToPix prototype with the new readout system will be shown.

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