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The ATCA based Compute Node and its application in the Belle II PXD-DAQ

Monday, December 3, 2012 3:45 PM (25 minutes)

In this talk we present the Compute Node, an ATCA carrier board and AMC board design based on Virtex-4 FX60 and Virtex-5 FX70T FPGAs.
The system is designed to perform data acquisition of 22 GB/s and data reduction by a factor <10 at the Belle II pixel detector,
which is supposed to start operation in 08/2015. The firmware programming comprises buffer management with pointer lookup tables,
DDR2 memory access using NPI (native port interface), optical link data transfer using GTX transceivers and Aurora 8B/10B,
SERDES links and custom UDP and TCP/IP interfaces.
A parallel region-of-interest (ROI) algorithm performs data reduction of the PXD data based upon charged track extrapolation
from the high level trigger and silicon strip vertex detector, arriving with a large latency and out of order.
In addition, PXD cluster charge analysis will be performed on the compute nodes for identification of slow pions from D* decays.

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