Session Program

Dec 3 – 4, 2012

Topical Workshop: FPGAs in Research - Applications, Technologies and Tools

Talks TUE1

Zentralinstitut für Elektronik, Forschungszentrum Jülich, Room 110 in Building 2.5

Tue, December 4

11:00 AM

Talks TUE1

Session | **Location:** Zentralinstitut für Elektronik, Forschungszentrum Jülich, Room 110 in Building 2.5

11:00 – 11:25 **FPGA Programming Methods - An Overview**

Speaker
Diana Goehringer

11:25 – 11:50 **Matlab/Simulink and HDL-coder**

Speaker
Mr Renhai Xiong

11:50 – 12:15
Parallelisation potential of image segmentation in hierarchical island structures on hardware-accelerated platforms in real-time applications

Speaker
Mr Sergey Suslov

12:15 PM