HELMHOLTZ

RESEARCH FOR
GRAND CHALLENGES

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ST1 – Sensing

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- Sensing part of “Detection and Measurement”
- Participating institutes: GSI, KIT, DESY
- Milestones from proposal:
  - ***DTS-1*** *Establish and commission the Distributed Detector Laboratory [2025]*
  - **DTS-2** Establish availability of sensors with high spatial (20 µm) and time resolution (20 ps) for charged particles [2024]
  - **DTS-6** Establish availability of high-performance sensors covering the entire X-ray spectrum [2026]
- Updates on the objectives (right) on the next slides

Objectives and Approach

ST1 – Detection and Measurement: ST1 investigates sensors, as an essential building block of any detector system, and the intimately linked custom readout circuitry (ASICs). We will push the development of advanced **silicon sensors for greater time, energy, and position resolution.** Prominent examples are low-gain avalanche diodes (LGADs). They have already attracted great interest as particle tracking and timing detectors in high-energy physics. LGAD devices provide a large signal, excellent time resolution of 20–30 ps and potentially a spatial resolution down to 20 µm. This would enable fully four-dimensional tracking detectors of unprecedented performance [DTS-2, DTS-3]. Enhanced lateral drift sensors (ELADs) promise improved spatial resolution by increasing charge sharing. This technology has high potential, and provided the production technology can be established, it could be an attractive sensor choice for future collider detectors. Development work in MT-DTS on LGADs, ELADs, and other silicon sensors includes sensor design, R&D on the processing of these devices with several industrial partners, prototype production, and characterization in the laboratory and at test beam facilities.

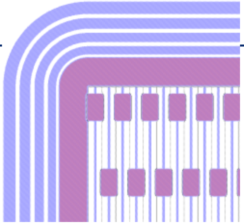
We will develop infrastructure for **thinning and post-processing silicon sensors** to make these technologies readily available for tailoring sensors to different applications. In particular, back-illuminated CMOS sensors and pixelated LGADs with thin entrance windows could greatly improve detection of soft X-rays in photon science. This, along with continued collaboration with industry to develop **high-*Z* sensors** for hard X-rays, would make it possible **to cover the full spectrum of X-ray energies** at synchrotron and FEL beamlines [DTS-6].

We observe a surge of opportunities for **superconducting sensors** across several fields of research. For instance, metallic magnetic calorimeters (MMCs) offer uniquely high energy resolution, which makes them ideally suited for applications in neutrino physics, dark matter searches, spectroscopy, astrophysics, atomic physics, molecular physics, and more. Together with the Universität Heidelberg, we will establish superconducting sensor production capacity in MT-DTS.

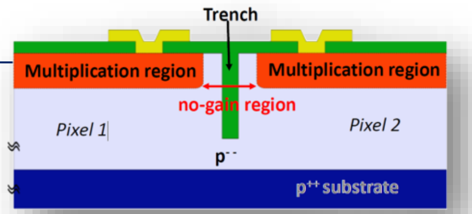
During PoF III, **depleted monolithic CMOS sensors** have reached a level of maturity that has made them a viable choice for future particle, hadron, and nuclear physics detectors. They will also find application in astrophysics and photon science. Our R&D will address the ever-increasing challenges of improving granularity, timing, data rate, and radiation hardness. This development will require the expertise in both sensor development and integrated-circuit design available in MT-DTS.

Silicon sensors for greater time, energy, and position resolution

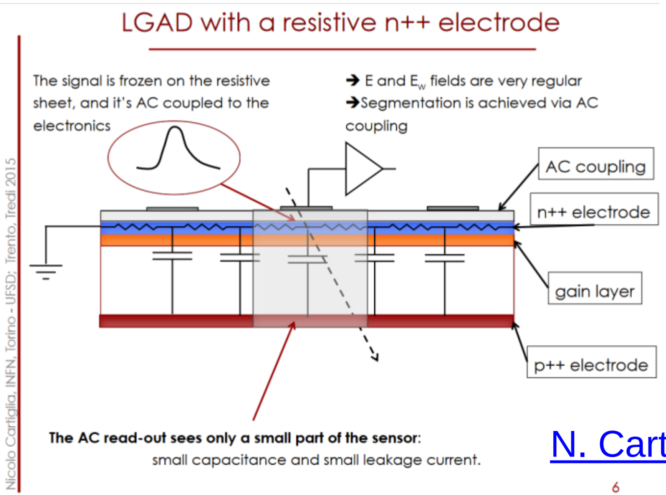
- Low Gain Avalanche Detectors (LGAD)
  - Time resolution down to tens of ps possible
  - Spatial resolution with **trench isolation** about 25µm
  - Further improvement by **resistive layer** and AC coupling (incl. higher fill-factor)
  - Edgeless design by using deep trenches
- R&D together with FBK and CERN RD50
  - TI-LGAD wafer batch submitted in May 2020, delivery date expected in beginning 2021
- TANGERINE (WP2)
  - 4d tracking with LGADs and embedded AI
  - project supported by Helmholtz Innovation fund



TI-LGAD
Microstrip sensors
50 × 3000 µm²



Trench isolated LGAD structure
no-gain region of ~ few µm



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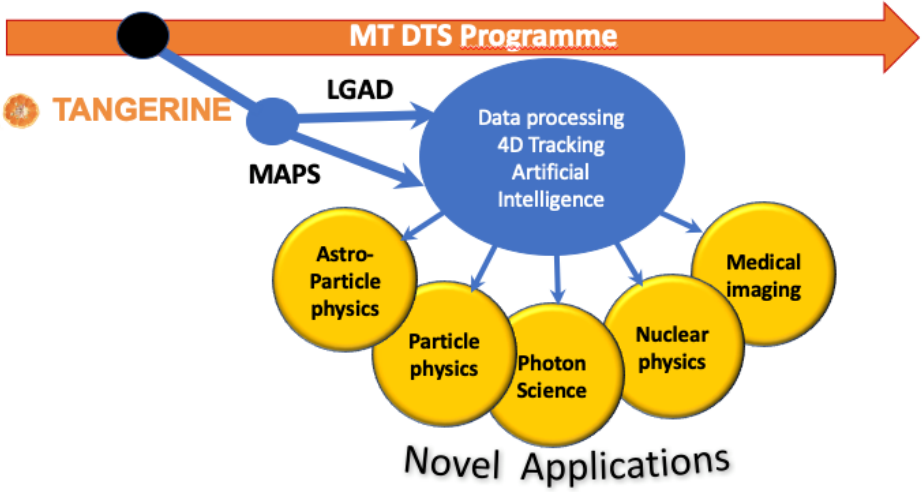
TANGERINE
- Towards Next Generation Silicon Detectors

Tangerine aims to push detector technologies to a new level exploiting the full potential of **newly available semiconductor technologies** as well as recent developments of **machine-learning approaches embedded in hardware**

- Deep-submicron process technologies
- Data processing circuits on-chip
- Monolithic Active Pixel Sensors (MAPS)
- Silicon pixel detectors
- In-pixel logic
- Low Gain Avalanche Detectors (LGAD)
- Machine-learning in hardware

The opportunity to drive these developments is now!
The resources required, the technologies, as well as the potential impact significantly exceed the MT-DTS ideas and framework.

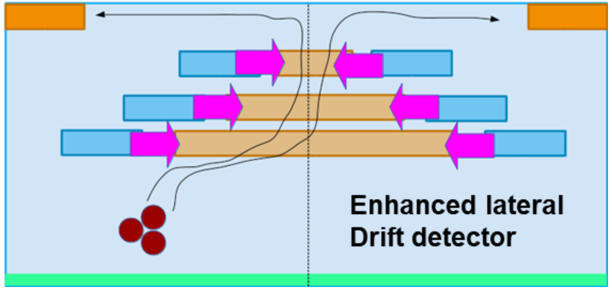


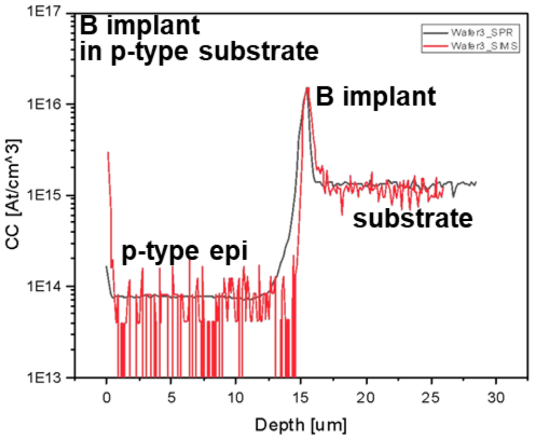
Silicon sensors for greater time, energy, and position resolution

- Enhanced Lateral Drift Detector (ELAD)
  - Wanted: Thin & fast & precise pixel detectors
  - Goal: Reach theoretical limit of position resolution at given pitch/SNR/threshold
  - How: Linear charge sharing
  - Solution: Dedicated charge sharing mechanism by engineering the E-field
  - Req.: Layer-by-layer process combining epitaxy and ion beam implantation

    → Innovative concept in silicon technology

    → High-risk/high-gain project
- Process development at Fraunhofer EMFT* done
- Now start of production





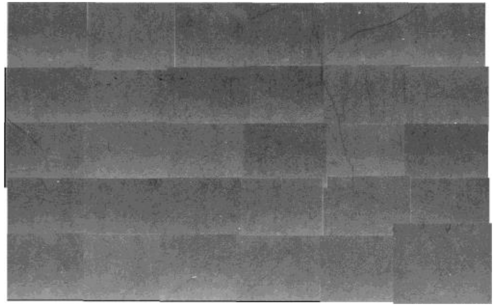
* Fraunhofer-Einrichtung für Mikrosysteme und Festkörper-Technologien

Cover the full spectrum of X-ray energies

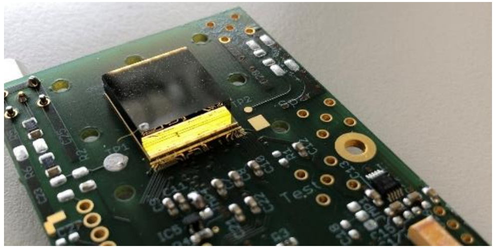
- Thinning and post-processing silicon sensors
  - High-purity, low-temperature processes; thinning, delta-doping, filters …
  - Not started without molecular beam epitaxy (MBE) facility, which is part of DDL
- Highly granular Ge and thick Si(Li) sensors
  - *Development mainly at Jülich/GSI; status unclear*
- High-Z sensors
  - Challenge: availability and size of sensor grade material
  - Development of GaAs detectors:
    - Collaboration with Fraunhofer ISE* Freiburg
    - Designing of x-ray detectors with p-i-n structure
    - Growth of GaAs epitaxial films using MOCVD
    - Characterization of films (I-V, WBSXT, detector meas.)
  - Development of CdZnTe crystals:
    - Crystal growth of CdZnTe crystals by Travelling Heater Method
    - Characterization of crystals (I-V, XRD, detector meas.)
    - Processing of detectors (planar technology)

Figure 13. The 384-strip germanium detector wire-bonded to 12 MARS ASICs.

DOI: 10.1088/1748-0221/13/04/C04030



White Beam Synchrotron Topography image of a GaAs crystal



CdZnTe detector measurements with Timepix

* Institut für Solare Energiesysteme

Superconducting sensors

- New groups at KIT
  - New Fachgruppe at IPE: “Cryogenic sensors and superconducting electronics” (Ch. Enss)
  - New Professor (S. Kempf) at Institute of Micro- and Nanoelectronic Systems at KIT
- Metallic magnetic calorimeters
  - Moving to large arrays
  - Detectors for massive particles
  - New soft x-ray detectors
  - R&D for advanced readout technology
- Establish superconducting sensor production capacity
  - Currently evaluating procurement of first machines (in 2021) to establish technology (during 2022ff.)
  - When large cleanroom space available (DDL) complete machinery and ramp up production

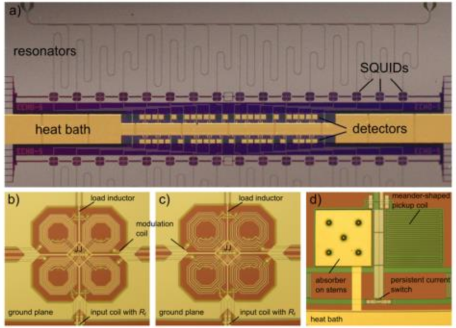
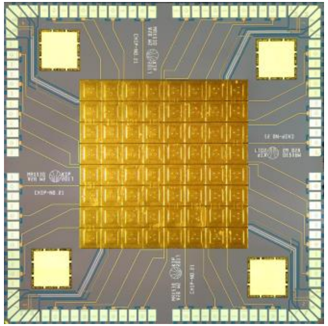


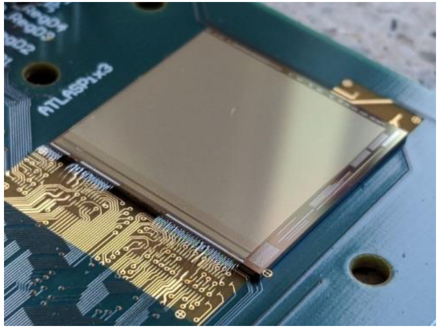
FIG. 2. Photographs of the detector array with on-chip, integrated μMUX: a) Overview of the upper two-thirds of the device. b) SQUID formed by four continuous washers connected in parallel. c) SQUID formed by four slotted washers connected in parallel. d) Two-pixel detector for which only one meander-shaped pickup coil is equipped with a temperature sensor and an absorber.

https://doi.org/10.1063/1.4973872

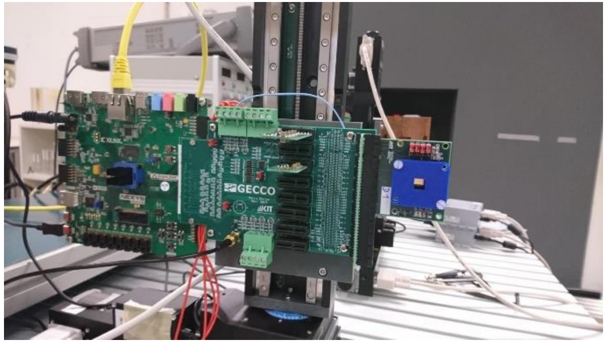


Depleted monolithic CMOS sensors

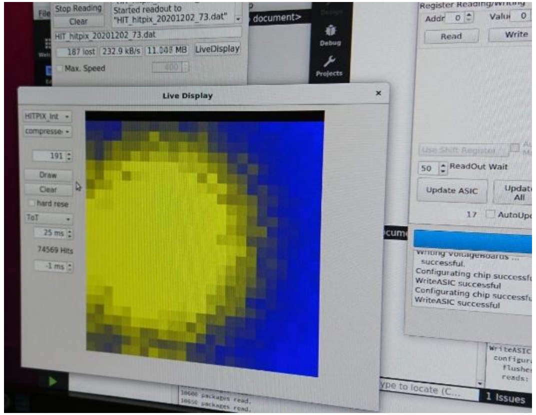
- Current new developments at ASIC and Detector Lab (I. Peric)
  - ATLASPix3: full reticle detector for LHC environment fully functional [timing ~25ns, pot. rad. hard < $5x10^{15} n_{eq}/cm^2$]
  - HITPix: particle counting chip for extreme particle rates as required for therapeutic particle beam monitoring [particle rate > 10^9 p/s, rad. hard design to be evaluated]
  - Also working on timing down to 100ps (BiCMOS) and high dynamic range (dE/dx measurements)
- TANGERINE (WP1)
  - explore 65nm CMOS imaging process and add in-pixel intelligence



Full-reticle ATLASPix3



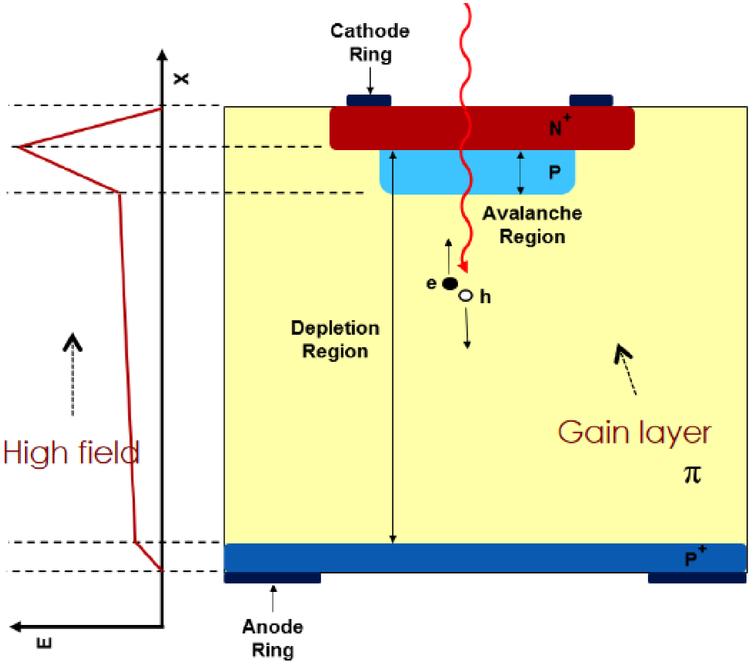
HITPix at HIT beam line



Online monitor of HITPix

SPARES

LGAD Concept



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TANGERINE

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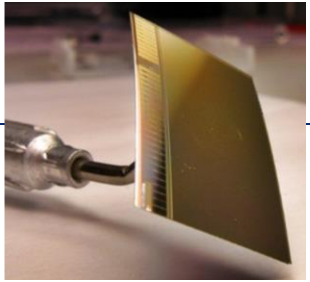
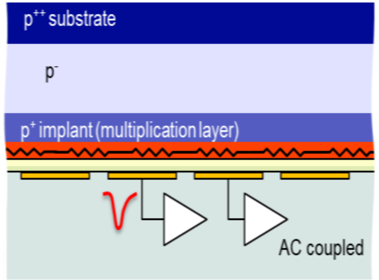
Michael Deveaux, Jerzy Pietraszko, Christian J. Schmidt - **GSI**
Erik Bründermann, Michele Caselle, Andreas Kopmann – **KIT**



Monolithic Active Pixel Sensor



Low Gain Avalanche Detector

- **WP1: A Monolithic Pixel Detector in a Novel CMOS Imaging Technology (DESY, GSI)**

  Work package leader: Simon Spannagel (DESY)

  - **Develop a fine pitch pixel** sensor in a brand-new small-node quadruple-well CMOS imaging technology allowing for high logic density
  - **Evaluate** integrated circuits for intelligent pattern recognition, hit classification, cluster-shape analysis and data compression algorithms suited to perform data reduction already on chip

- **WP2: Large area, fast 4D tracking system based on LGAD and RSD sensors (GSI, KIT)**
  Work package leader: Michele Caselle (KIT)

  - Combine **4D tracking** with fast LGAD sensors and embedded artificial intelligence (AI) in two steps:
    - Large area (>100 cm^2) demonstrator based on optimized LGAD strip sensors
    - Develop a novel concept based on Resistive Silicon Detector (RSD) LGADs for pixel detectors

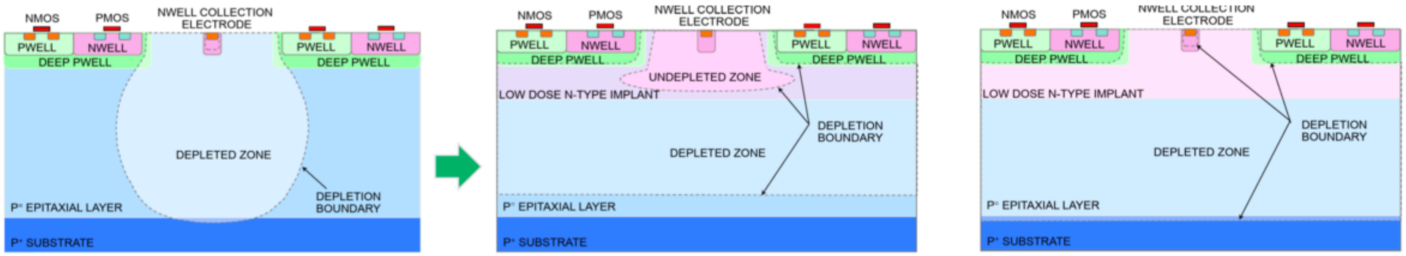
- **WP3: Pixel Detector Innovation Platform (DESY, GSI, KIT)**
  Work package leader: Michael Deveaux (GSI)

  - Establish a strong pixel-detector network between the Helmholtz centers sustainable beyond the projects lifetime
  - Goal: Train the next generation of silicon experts, establish schools/workshops to profit from cross-center knowledge and attract young scientists

65nm CMOS

TANGERINE WP1:

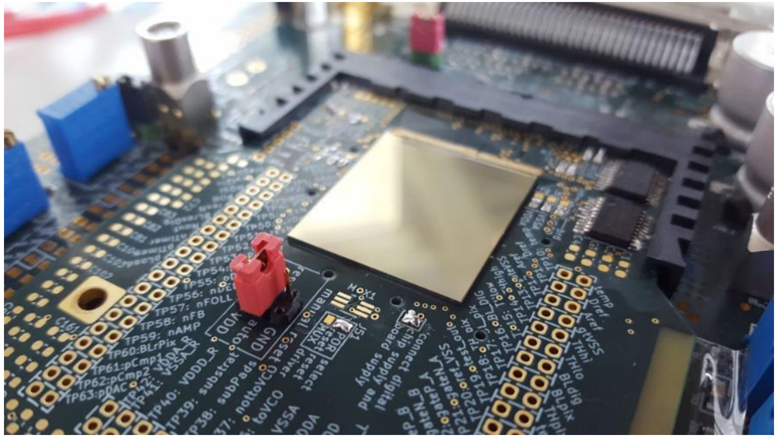
- explore 65nm CMOS imaging process
- develop ‘detector-on-chip’ (in-pixel intelligence using higher logic density)
- collaboration with CERN's EP R&D Work Package 1.2 (CMOS sensors)
  - many members associated with ALICE ITS3 upgrade
  - very open to participation from us, regular participation in design meetings
- development based on experience with modified 180nm porcess
  - relying on deep p-well implant and n implant



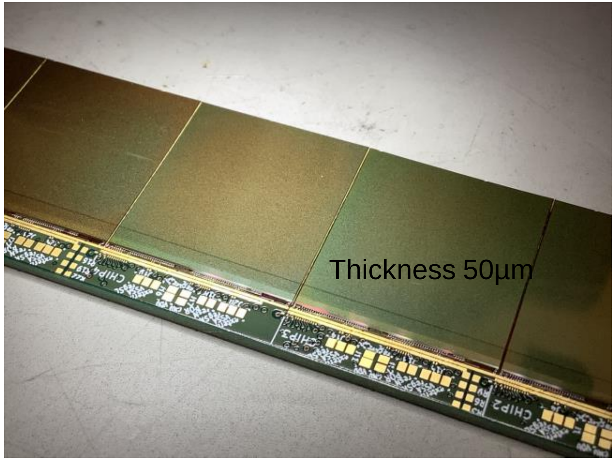
Standard, not fully depleted — Not fully depleted at low reverse bias — Depletion at higher reverse bias

  - first attempt to understand process and its capabilities and limitations
  - CERN focus on fast but simple front-ends
  - DESY layout of an amplifier with Krummenacher feedback - basically a first draft for an actual front-end in this technology
  - submission imminent

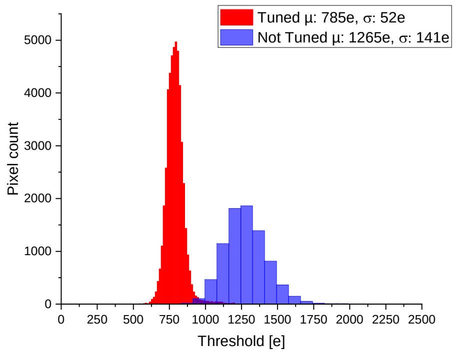
- MUpix10 [2] is a reticle size sensor produced in TSI 180nm HVCMOS process on 200-400Ωcm substrates
  - 256 x 250 pixels of 80x80µm^2 size. The chip area is 20.66mm x 23.18mm.
  - Pixels contain charge sensitive amplifiers
  - Connected to hit digitizers
  - Two comparators one for time- and one for hit-detection
  - The hit digitizers receive time stamp signal with variable frequencies. Hit time and amplitude can be measured. The chip contains power supply voltage generators that can be used for serial powering scheme. 4 data links (4 x 1.28GBit/s), possible to process 120MHits/s
- Tested in beam with very good results

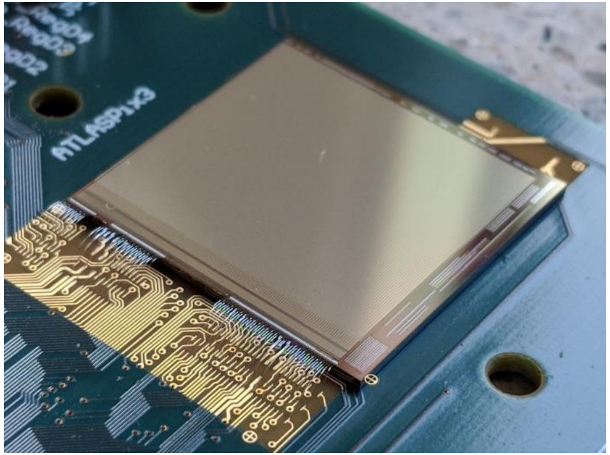


MuPix10 demo ladder for Mu3e pixel detector



- ATLASpix3 [3] [4] is a reticle size HVCMOS sensor implemented in 180nm HVCMOS process of TSI.
- The chip is designed for quad module construction
  - High resistivity substrates of 200-400Ωcm used.
  - 19.8mm x 18.6mm pixel matrix.
  - Chip size 20.2mm x 21mm.
  - Pixel size is 150µm x 50µm.
  - Pixel contains amplifier, comparator and DAC for threshold tuning. The digital part supports triggered and continuous readout. The digital interface uses only two lines command in and data out. Only 3 external voltages are required
- ATLASpix3 is currently being characterised with excellent results. Detection efficiencies of 99.5% have been measured in beam (DESY and PSI). The time resolution after time-walk and binning corrections is 4.5ns sigma. The production yield is about 85% and the power consumption is of the order of 140mW/cm^2



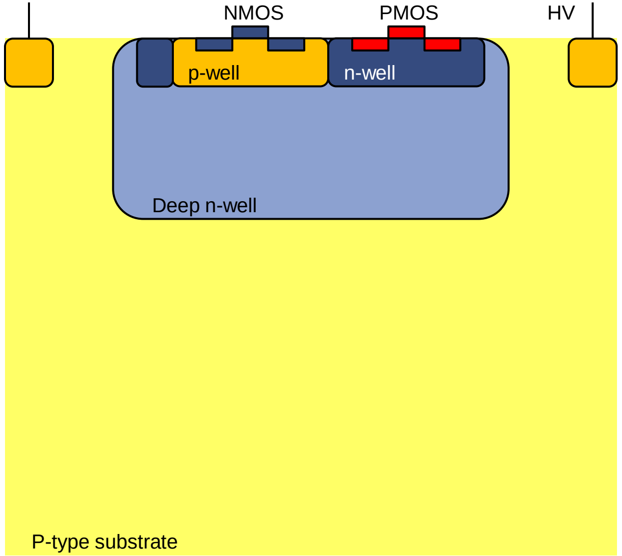


References

- [1] I. Peric, "A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology," Nucl. Inst. Meth. A 582, pp. 876-885 (2007)
- [2] H. Augustin et al., "The MuPix sensor for the Mu3e experiment," Nucl. Inst. Meth. A 979 (2020)
- [3] M. Prathapan et al., „ATLASpix3: A high voltage CMOS sensor chip designed for ATLAS Inner Tracker“, in Proceedings of Science, vol. 370, TWEPP 2019, 2-6 September (2019)
- [4] R. Schimassek et al, Test results of ATLASPIX3—A reticle size HVCMOS pixel sensor designed for construction of multi chip modules, Nucl. Inst. Meth. A 986, 11 January 2021, 164812, https://doi.org/10.1016/j.nima.2020.164812

- HVCMOS pixel sensors [1]
- Radiation tolerant
- Can be implemented in standard IC-processes -> not expensive
  - Engineering run ~ 100k€, processed wafer (thinned) mit 40 chips (each 4cm^2) ~ 1.9k€
- Can be thin
- Can have a high time resolution

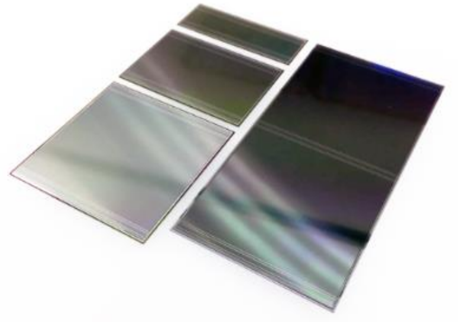
HV-MAPS

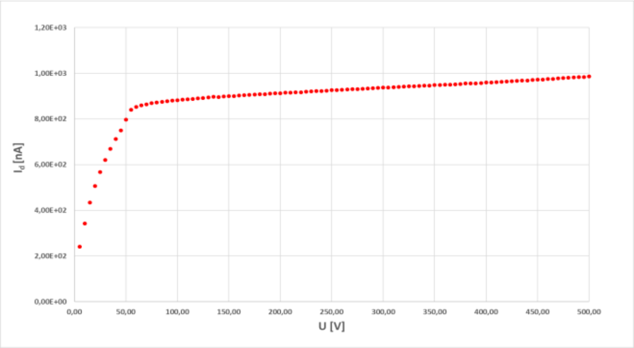


- Implemented in standard (HV)CMOS bulk process with triple well structure
- Pixels consist of large electrode with embedded readout electronics
- The deep-n-well fulfils two tasks:
  - 1. Local substrate for electronics (isolated from p-substrate)
  - 2. Charge collecting electrode
- Biasing of substrate with high voltage possible (typically |V| >= 50V)
  - Example: 300Ωcm substrate and 50V bias => 30µm depletion
- Electron-hole pairs generated by particles are separated quickly in strong E-field.
  - => Strong and fast signals when compared to standard MAPS
- HVCMOS sensors are compatible with many standard processes
  - Implemented in following 8 processes: UMC 65nm, AMS 350nm and 180nm, TSI 180nm, Globalfoundries 130nm, Lfoundry 150nm, IHP SG13S 130nm
  - Uniformly doped substrates with resistivity >=10Ωcm have been successfully used

Sensors of the CBM-STS:

- double-sided Si microstrip sensors
  - produced in 2019 - 2020,
    all produced (>1000 pcs)
  - testing close to be finalized
  - generally speaking: sensors operational up to U_{bias} = 500 V





<u>4 sizes available:</u>

- (62 x 22) mm^2
- (62 x 42) mm^2
- (62 x 62) mm^2
- (62 x 124) mm^2