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Multi-core Computing in High Energy Physics

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Even though the miniaturization of transistors on chips continues like predicted by Moore's law, computer hardware starts to face scaling issues, so-called performance 'walls'. The probably best known one is the 'power wall', which limits clock frequencies. The best way of increasing processor performance remains now to increase the parallelization of the architecture. Soon standard CPUs will contain many dozen cores on the same die. In addition, vector units become again standard. To not to waste the available resources, application developers are forced to re-think their traditional ways of software design.

This talk will explain some of the common problems, and some ways of solving them. It will summarize the on-going parallelization activities in the field of high-energy physics software and as well give an outlook for what to expect in the coming decade.

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