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Electrical active defects caused by threading dislocations in Ge-rich GeSi heterostructures integrated on Si(001)

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Ge-based devices have numerous applications in the field of photonics and optoelectronics. These include Ge as alternative channel material for high-performance MOSFETs [1], as near-infrared integrated light sources [2] and as active material for THz quantum cascade lasers (QCL) [3]. A CMOS-compatible fabrication requires the integration of Ge-based heterostructures on Si substrates. In this case, the lattice mismatch between Ge and Si (4%) leads to plastic relaxation and, therefore, the formation of threading dislocations (TDs). These extended defects can negatively influence the electrical properties of Ge-based optoelectronic devices.

Previous investigations of the electrical active defects caused by TDs in either n- or p-doped Ge(Si) films were carried out on devices with threading dislocation densities (TDDs) in the range of 107 to 1010 cm-2 including processing-induced defects [4,5,6]. By means of the recent reported reverse graded buffer technique using a benficial second interface in GeSi/Ge/Si heterostructures it has become possible to tune the TDD in Ge0.96Si0.04 layers in a wide range down to the low 106 cm-2 range by keeping thickness and degree of plastic deformation constant [7]. Since material physics as well as practical considerations such as fabrication cost can be expected to impose limits on a further reduction of the TDD, it is particularly important to obtain a quantitative understanding of the impact of TDs on device performance in the low density regime. This is at the focus of our investigation.

Here, we study undoped Ge-rich GeSi epitaxial layers featuring different values for the TDD ranging from 3·106 to 2·108 cm-2 grown on Si(001) using a Ge buffer. We present a comprehensive analysis of the influence of TDD on the vertical leakage currents in buried n+-p homojunctions. Here, the influence of TDs oriented parallel to the current path on device characteristics in as-grown Ge0.96Si0.04/Ge/Si heterostructures can be investigated without the introduction of processing-induced defects e.g. by implantation and annealing. The correlation of leakage currents and TDD shows a stronger than linear dependency and temperature dependent current-voltage (I-V) measurements reveals an electric field dependent carrier generation inside the diodes. In addition, capacitance-voltage (C-V) profiling of MOS capacitors fabricated on similar heterostructures gives information on TD related background doping in the studied Ge0.96Si0.04 layers. Associated DLTS measurements indicates an unintentional carrier concentration in the order of 3x1015 cm-3 above 175K and provide information on the included defect level characteristics.

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Category

Solid State (Experiment)

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