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Hot Carrier Injection and Bias Temperature Instability in SiC Transistors

Saturday, November 26, 2022 4:00 PM (2 hours)

N- and p-channel metal oxide semiconductor field effect transistors (N-MOSFETs, P-MOSFETs) have a wide range of applications today but have their limits to operate in harsh environments with temperatures above 300℃ or with high rates of radiation. Transistors realized with Silicon Carbide (SiC) as compound semiconductor are candidates to overcome these issues and have been used as power semiconductors for years already. Current research efforts focus on microscopic degradation mechanisms in SiC transistors, known as Hot Carrier Injection (HCI) and Positive Bias Temperature Instability (PBTI) in NFETs and negative BTI (NBTI) in PFETs. We investigated the reliability of SiC NFETs and PFETs with respect to HCI, NBTI and PBTI degradation models by adapting stress voltage levels and temperature.
The JEDEC standards describing the procedures for measuring the degradation mechanisms in Si integrated transistors were used to set up the corresponding measurements for SiC transistors. This allows the comparison of the degradation behaviour between the two different materials.
The results so far show interesting differences in the aging especially the Hot Carrier Injection in NFETs compared to equivalent sized silicon based transistors.
The derived models are able to be used in SPICE models to depict the physical behaviour of SiC Integrated transistors in IC simulation software.

Category

Other

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