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Development of Microfabrication processes for a scalable Multilayer Surface Electrode Ion Trap Quantum Computer

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Ion traps are promising candidates towards scalable quantum computer. One of the possible designs is the multilayer surface electrode ion traps[1]. The different processes involved in realising it are UV photolithography, Electroplating, Reactive Ion etching and more. Research and development towards the scalable quantum computer is tried with TSVs (through substrate vias) and Flip Chip Bonding for packaging. A solder free thermocompression method is proposed in [2] using gold stud bumps for flipchip bonding, but it brings a risk of damaging the ion trap. An approach with gold micrograss structures in the place of stud bumps is tested for damage free ion trap while bonding.

[1]A. Bautista-Salvador et al. New J. Phys. 21, 043011 (2019), Patent DE 10 2018 111 220 (2019)

[2]M. Usui et al., "Opto-electronic hybrid integrated chip packaging technology for silicon photonic platform using gold-stud bump bonding, (ICEP-IAAC) pp. 660-665 (2015)

Category

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