MAX PLANCK SEMICONDUCTOR LABORATORY

TRISTAN SDD

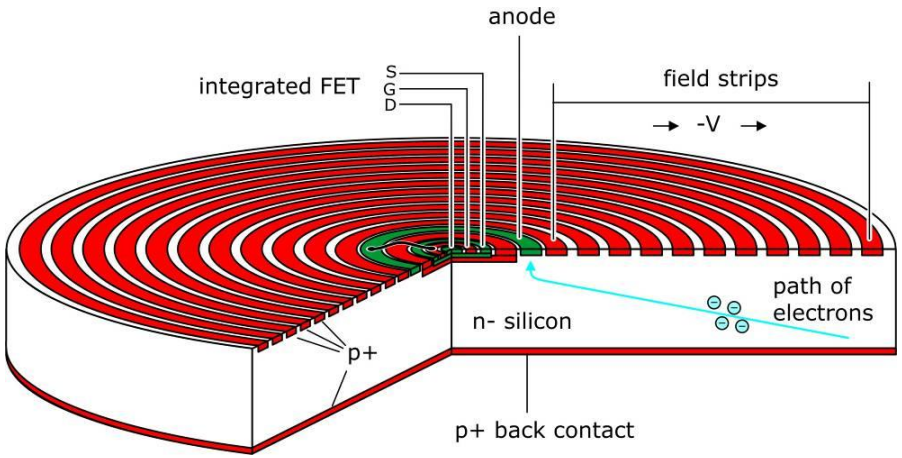
S. Jansen, P. Lechner, A. Mayatska,
D. Mießner, G. Schaller, F. Schopper

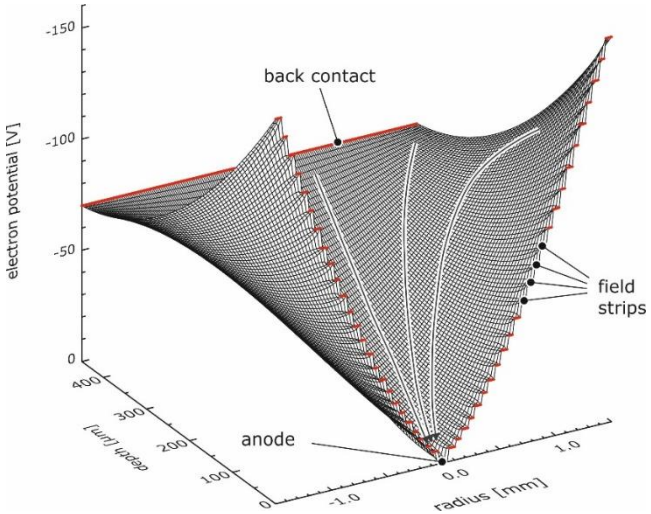
MPG Semiconductor Laboratory

TRISTAN Workshop, KIT, 06.07.2022

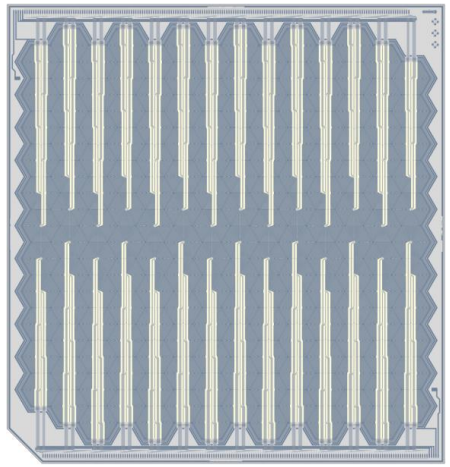
TRISTAN

- requirements
  - ▷ spectroscopy → good energy resolution — < 300 eV FWHM @ 20 keV (25 el. ENC)
  - ▷ minimal energy loss → thin entrance window — < 100 nm dead layer
  - ▷ beam dimension → large area coverage — Ø ~ 20 cm focal plane, ~ 300 cm²
  - ▷ high count rate → segmentation — Ø ~ mm cell size, ~ 1.000 cells
- detector choice: Silicon Drift Detector SDD
  - ▷ small capacitance & large cell area



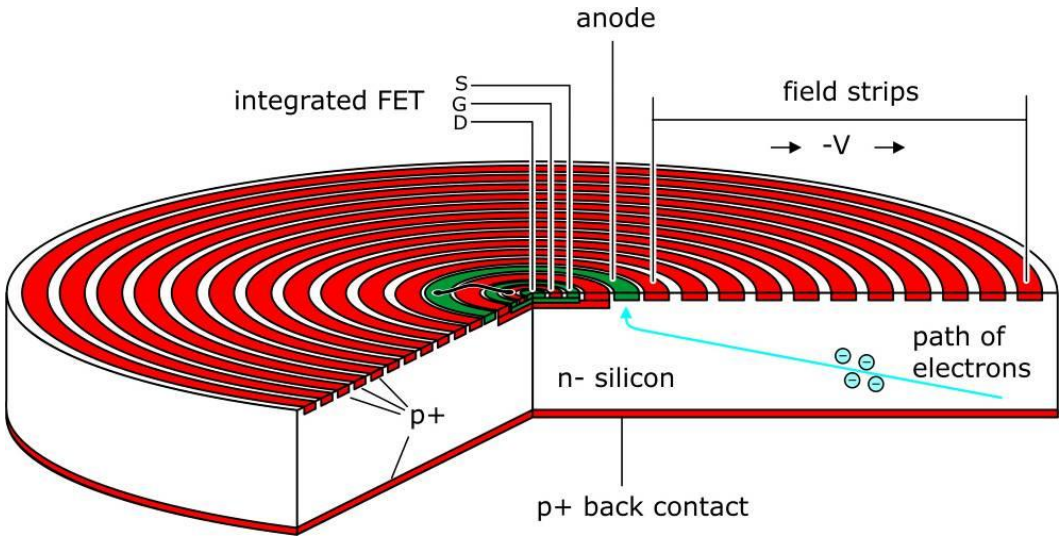


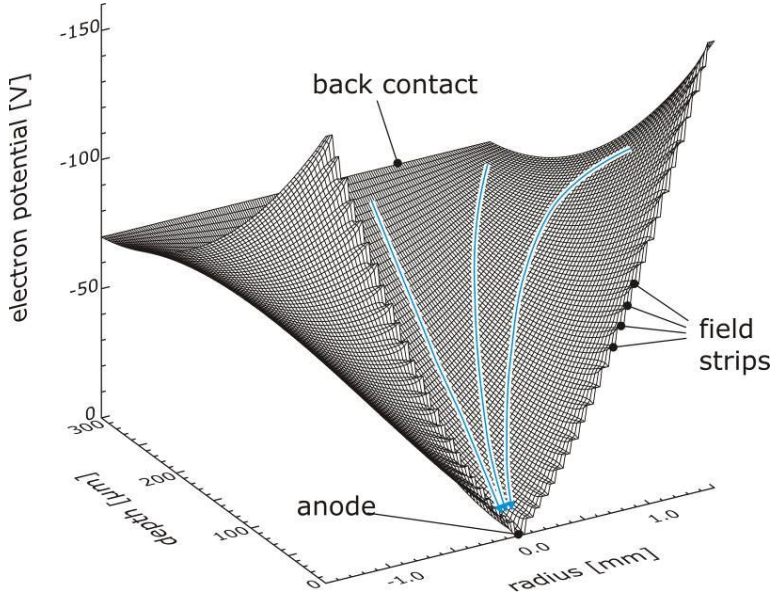
  - ▷ multi-channel option



SILICON DRIFT DETECTOR (SDD)

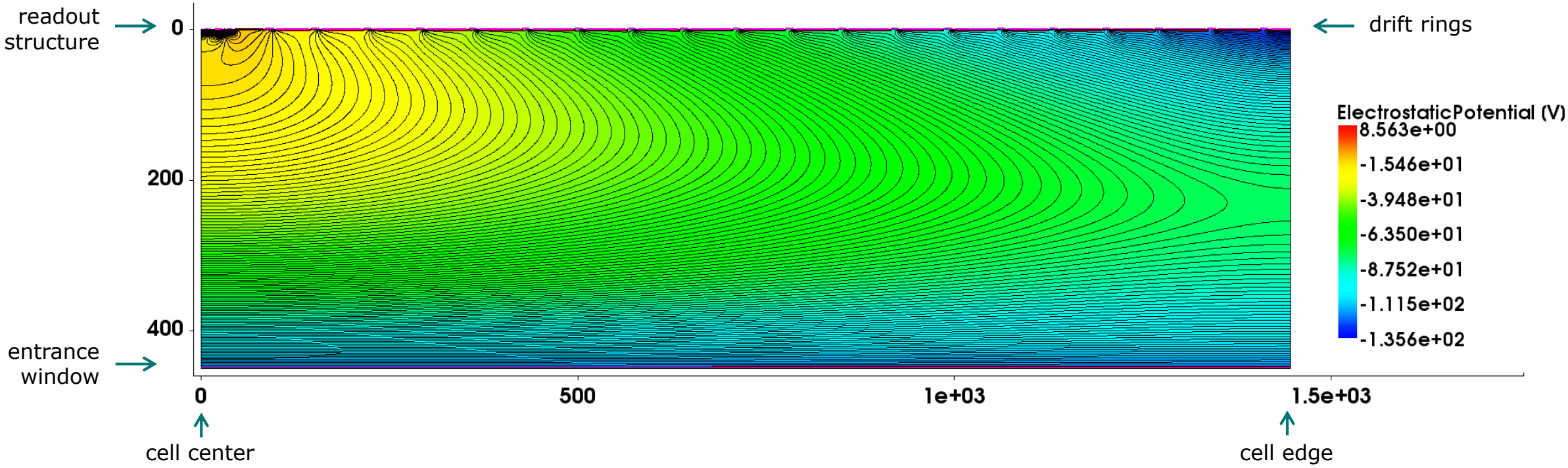
- principle
  - signal charge collection on small readout node by internal static electric field
  - X-ray & particle spectroscopy
- large area
  - 5 mm² … 1 cm² (… wafer scale)
- small capacitance
  - low noise, high count rates
- fully depleted and sensitive
  - efficiency @ high energies
- backside illuminated, uniform thin window
  - efficiency @ low energies
  - peak/background ratio
- integration of 1st amplifying FET
  - further capacitance reduction
  - no pickup, no microphonic noise





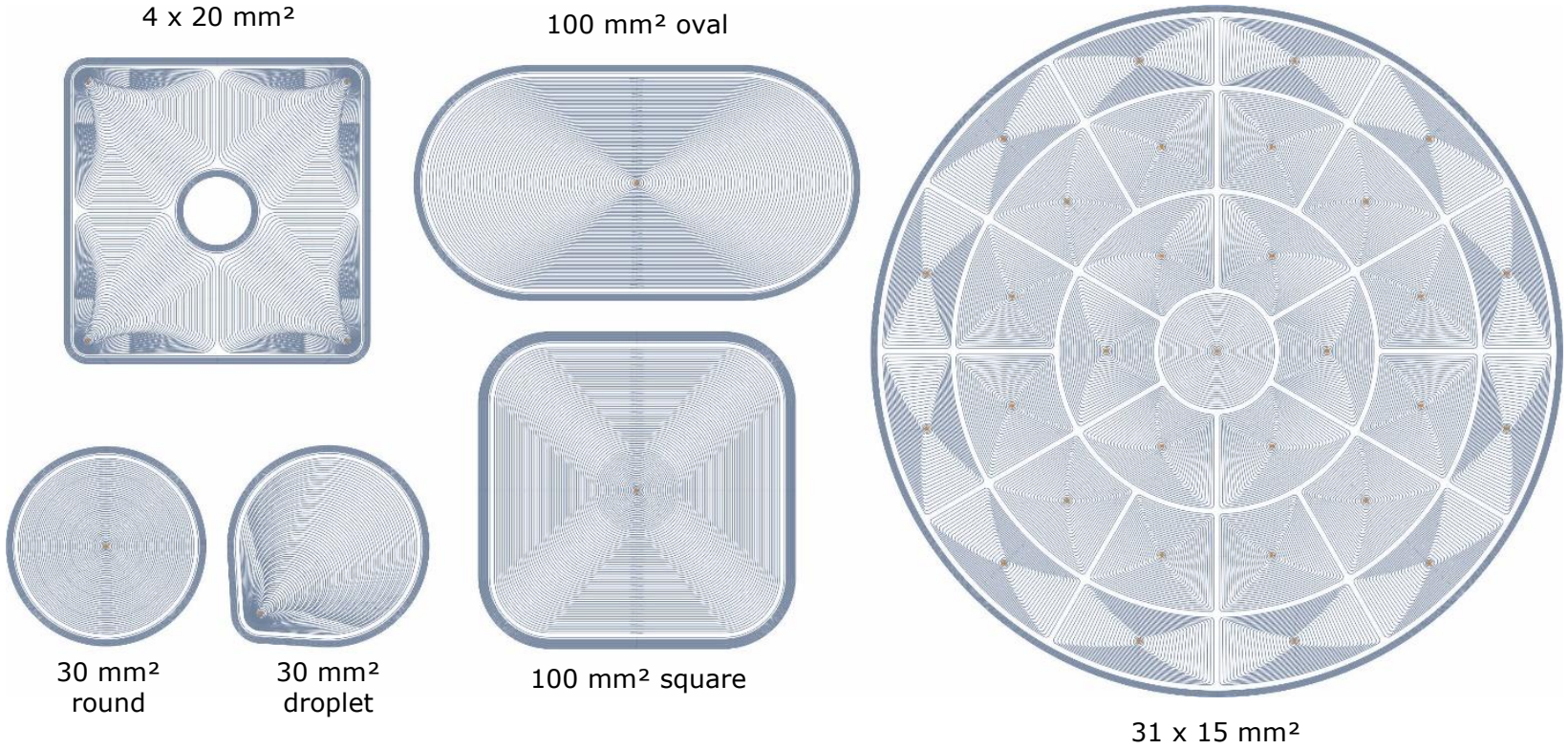
SILICON DRIFT DETECTOR (SDD)

- simulated electrostatic potential
  - equipotential lines ΔV ≈ 1V
  - strong E-field ⊥ surface, weak E-field || surface
    - → fast vertical drift to 1D potential minimum
    - → 'slow' horizontal drift to readout structure
  - two saddle points (vertical minimum & horizontal maximum)
    - cell edge
    - barrier of readout structure
      - → "field-free" regions



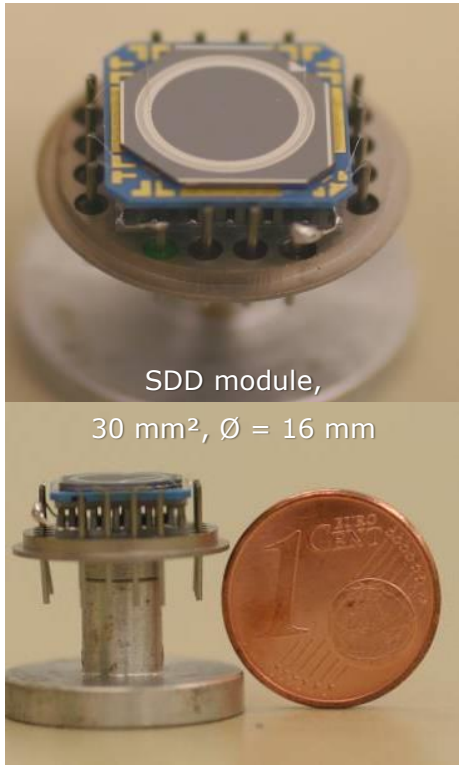
SILICON DRIFT DETECTOR (SDD)

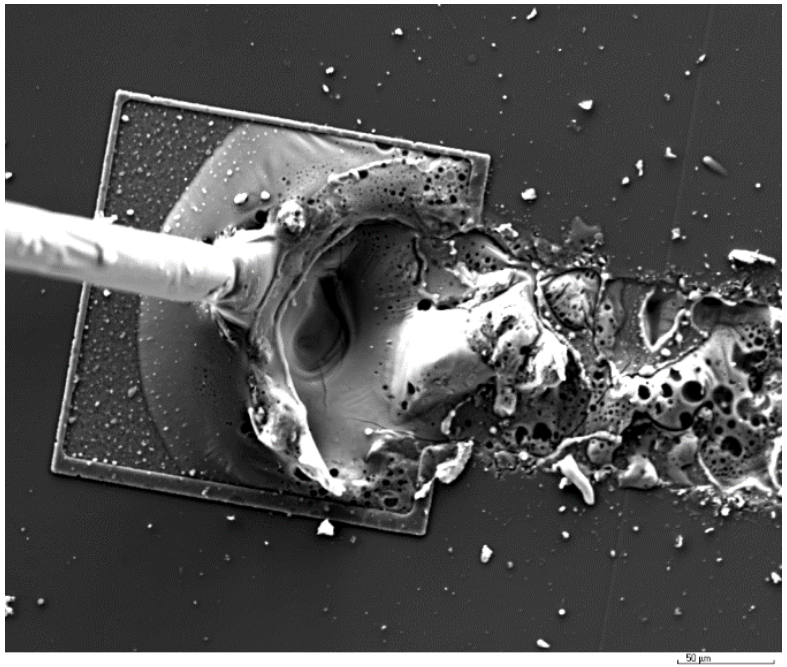
- flexible size & shape
  - cell sizing by number & width of field strips
  - cell shaping by bended field strips
  - any 2D geometry
  - multi-cell option



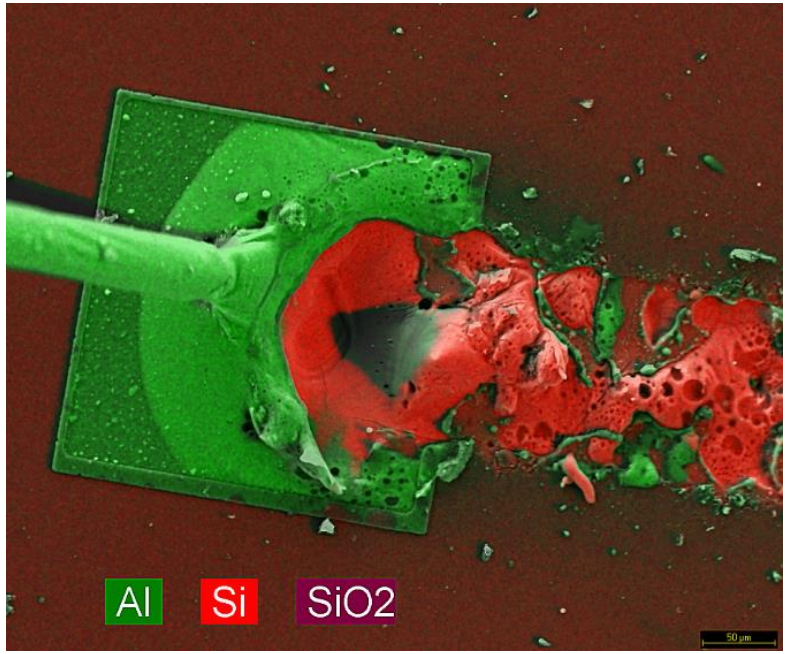
SILICON DRIFT DETECTOR (SDD)

- numerous fields of application
  - commercial products
    - electron microscope EDX
    - X-ray fluorescence XRF





exploded pressure sensor – SEM image



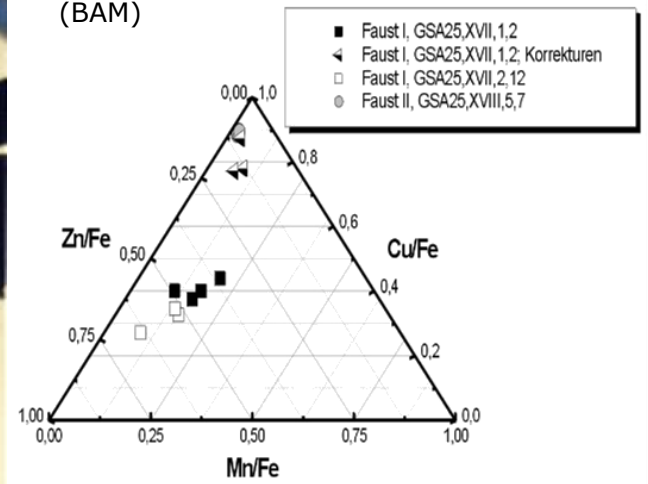
elemental mapping by EDX SDD

SILICON DRIFT DETECTOR (SDD)

- numerous fields of application
  - ▷ scientific experiments

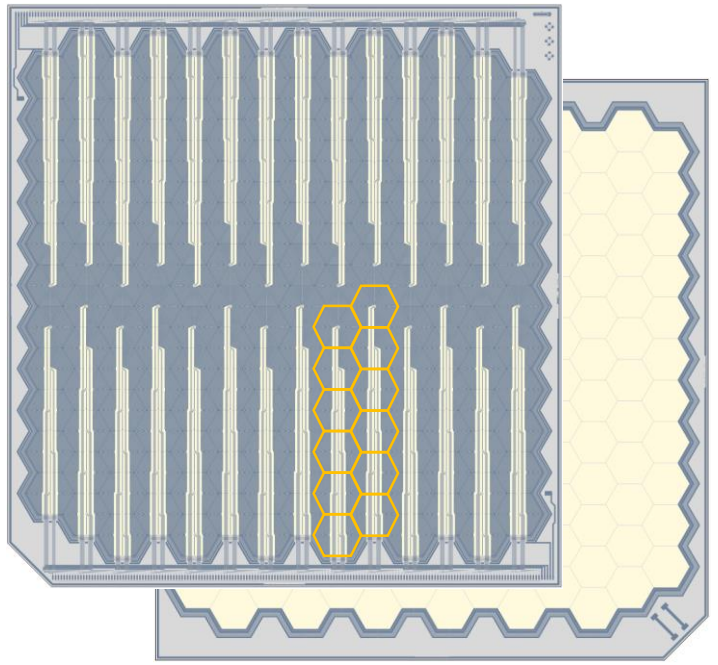
Goethe‘s original manuscript
of Faust II

ink analysis
(BAM)

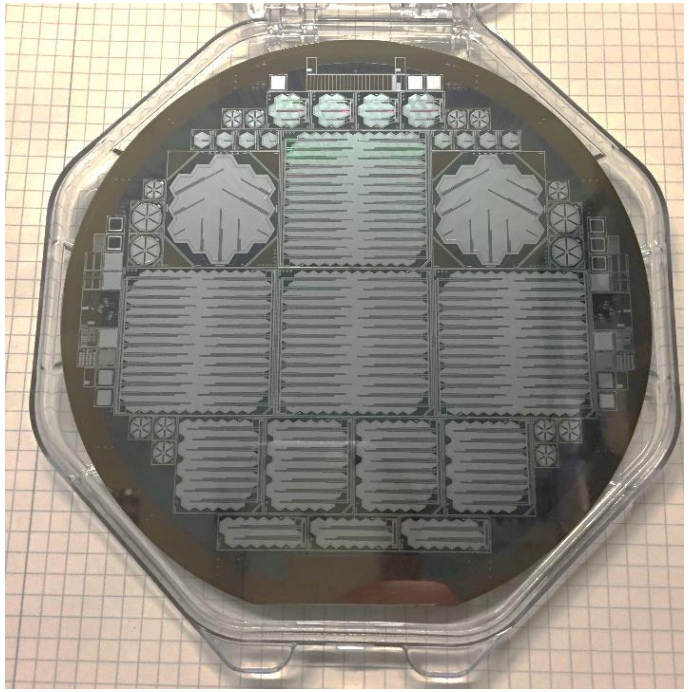


TRISTAN SDD

- production SDD33
  - volume 6 (+2) wafers
  - SDD with integrated FET
  - 166 cell device (~ 14 x 12 array)
    - 120 "full" cells
    - 46 edge cells for event reconstruction
  - cell size Ø ≈ 3 mm, A ≈ 7 mm²
  - chip format 38 x 40 mm²
  - organized in 14 groups of 12 (11) cells
  - 2 rows of ~ 180 bond pads
  - cut corner for back side bonds
  - smaller formats 8 x 6 cells
    2 x 6 cells
    7 cells
    1 cell



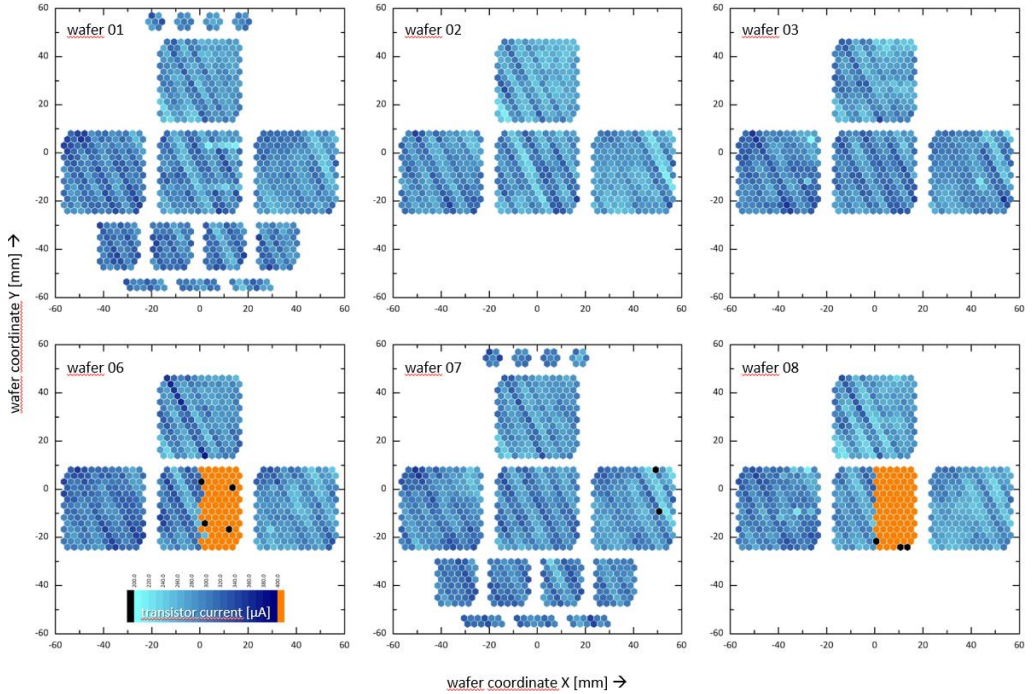
layout of 166 cells TRISTAN SDD



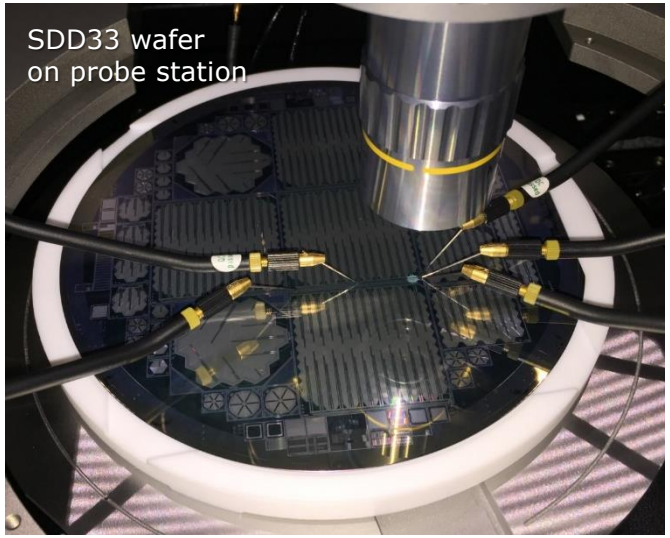
SDD33 dummy wafer

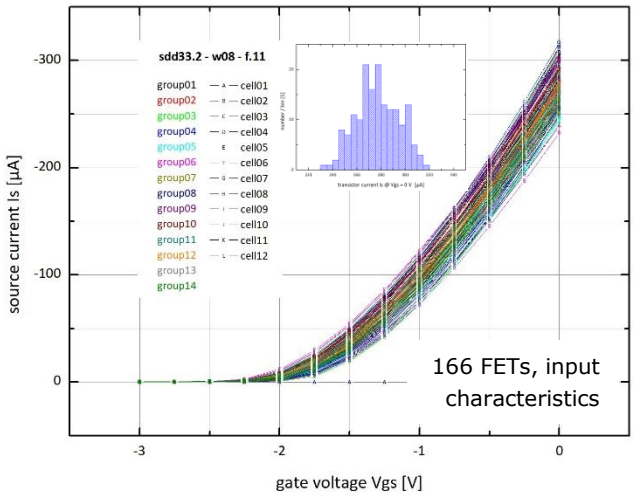
TRISTAN SDD

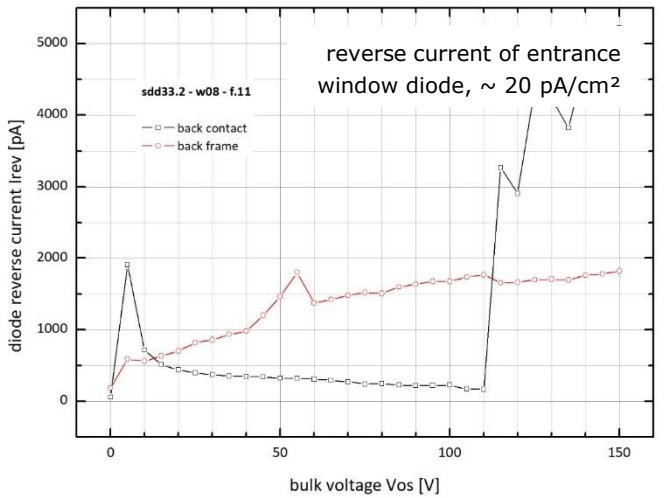
- wafer & die level test
  - semi-automatic stepping & test function
    - stability of diodes
    - integrity of insulating layers
    - characteristics of integrated voltage divider
    - characteristics of integrated FET
    - leakage current
  - high yield, expected performance figures



wafer maps of FET currents

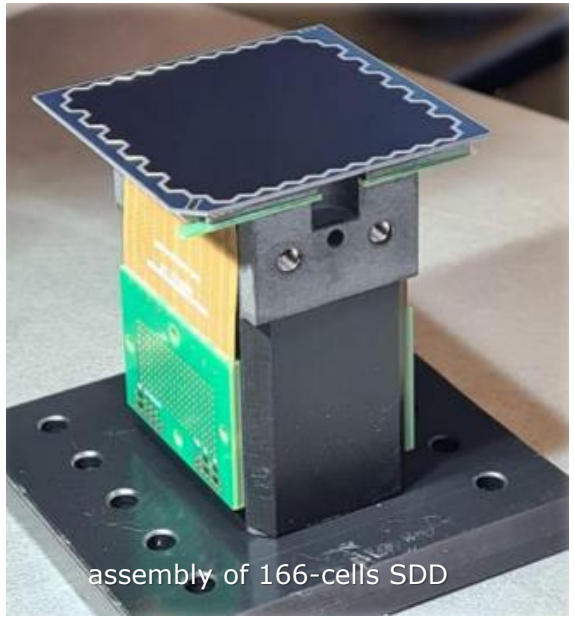






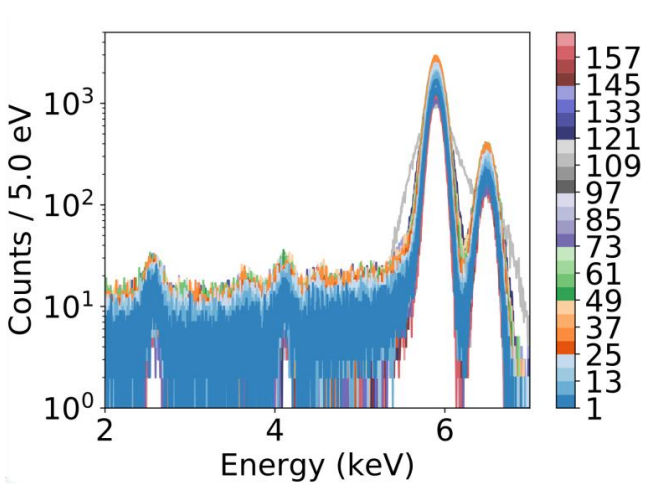
TRISTAN SDD

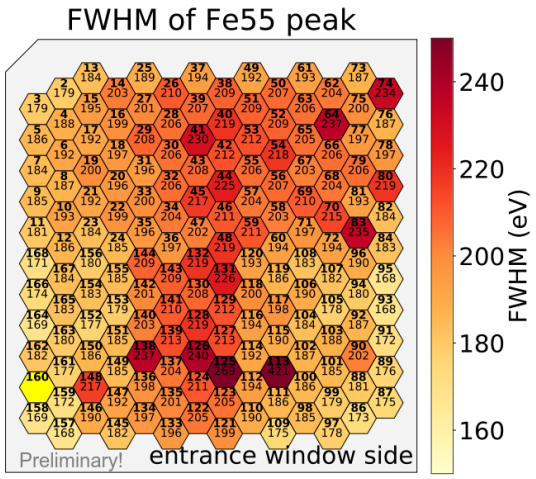
- module concept
  - 4-side buttable
  - perpendicular orientation of
    - mechanical structure
    - thermal connection
    - signal & supply lines



- performance
  - ≥ 2 working modules (165 of 166 cells)
  - energy resolution 195 eV FWHM @ 5.9 keV (-50 °C)
  - room for improvement
    - homogeneity
    - noise
    - crosstalk
    - entrance window

} mitigation tested on 2 wafers (SDD33.3)

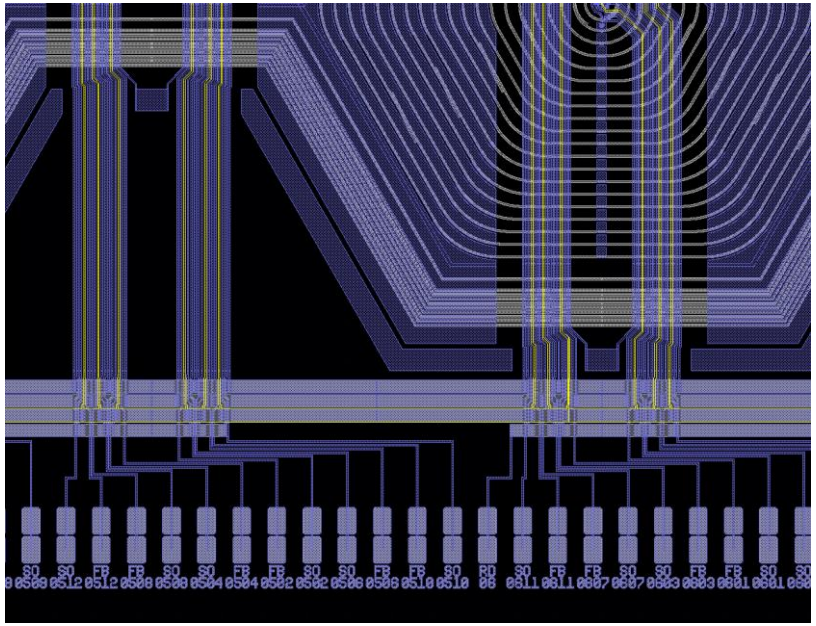


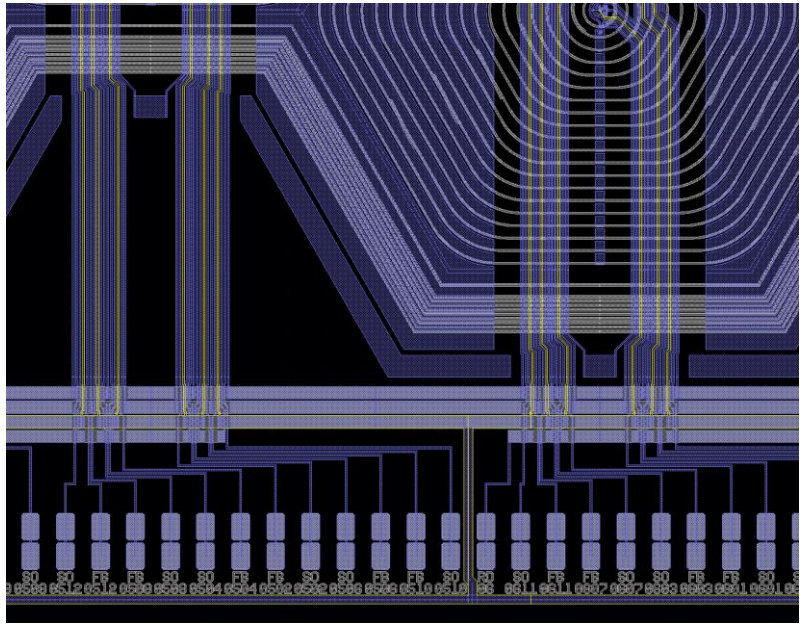


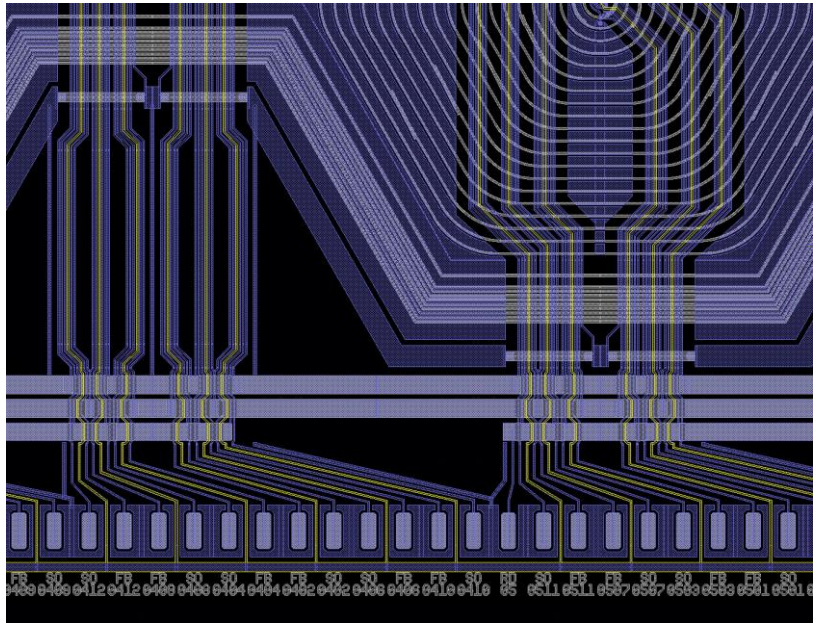
plots from D. Siegmann's IWoRID poster

TRISTAN SDD

- drain series resistance
  - SDD33.2
  - voltage drop ~ 1 V
  - caused by polySi bus pieces
  - SDD33.3
  - parallel metal line
  - bus support
  - SDD35
  - all-in-metal drain bus

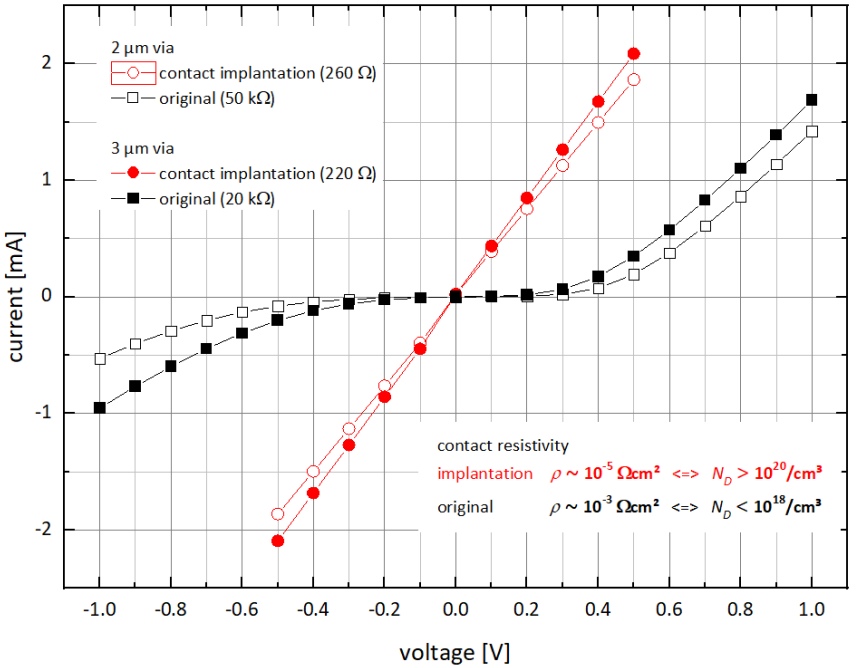






TRISTAN SDD

- noise
  - contact resistance
    - repaired by additional shallow n-implantation
    - now standard process routine
    - positive effect confirmed
  - white noise & random telegraph signal
    - caused by traps
    - reason unclear
    - DLTS analysis effort without concrete result
    - unknown from previous & parallel productions
    - rely on one-time occurence

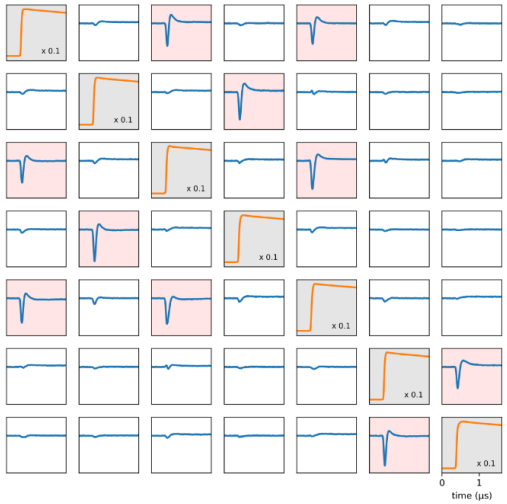


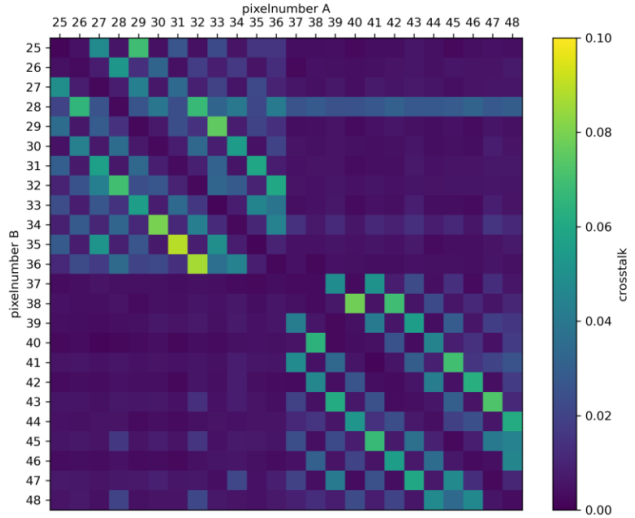
TRISTAN SDD

- crosstalk
  - capacitive coupling of signals source ←→ feedback lines of different cells
  - correlation with length of parallel connection lines inside the cell array

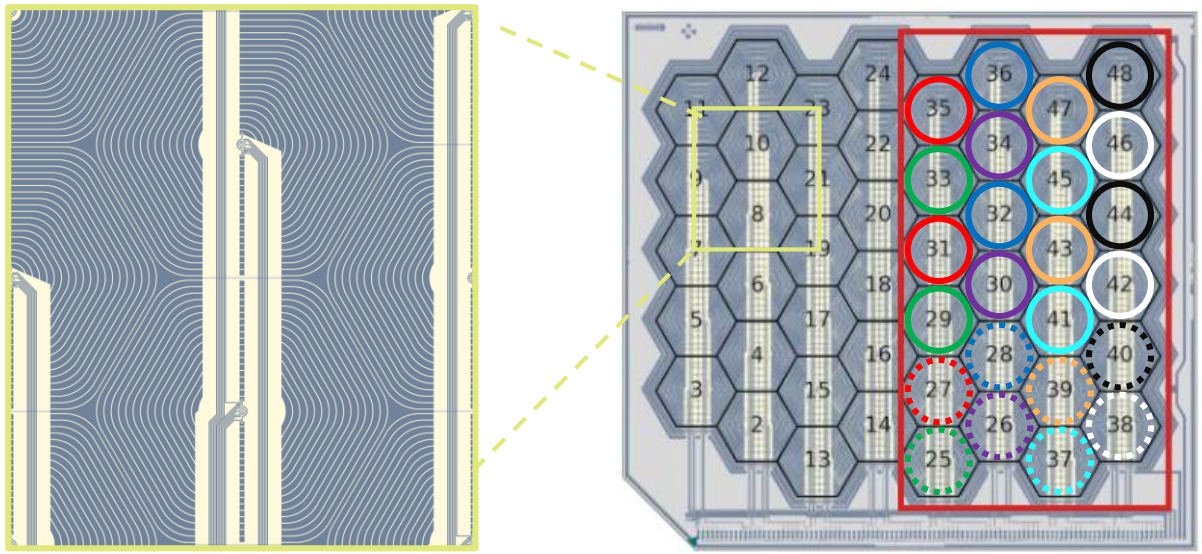
    e.g. **#36 – #32 – #28**
  - additional contributions from outside the cell array

    e.g. **#36 – #33**



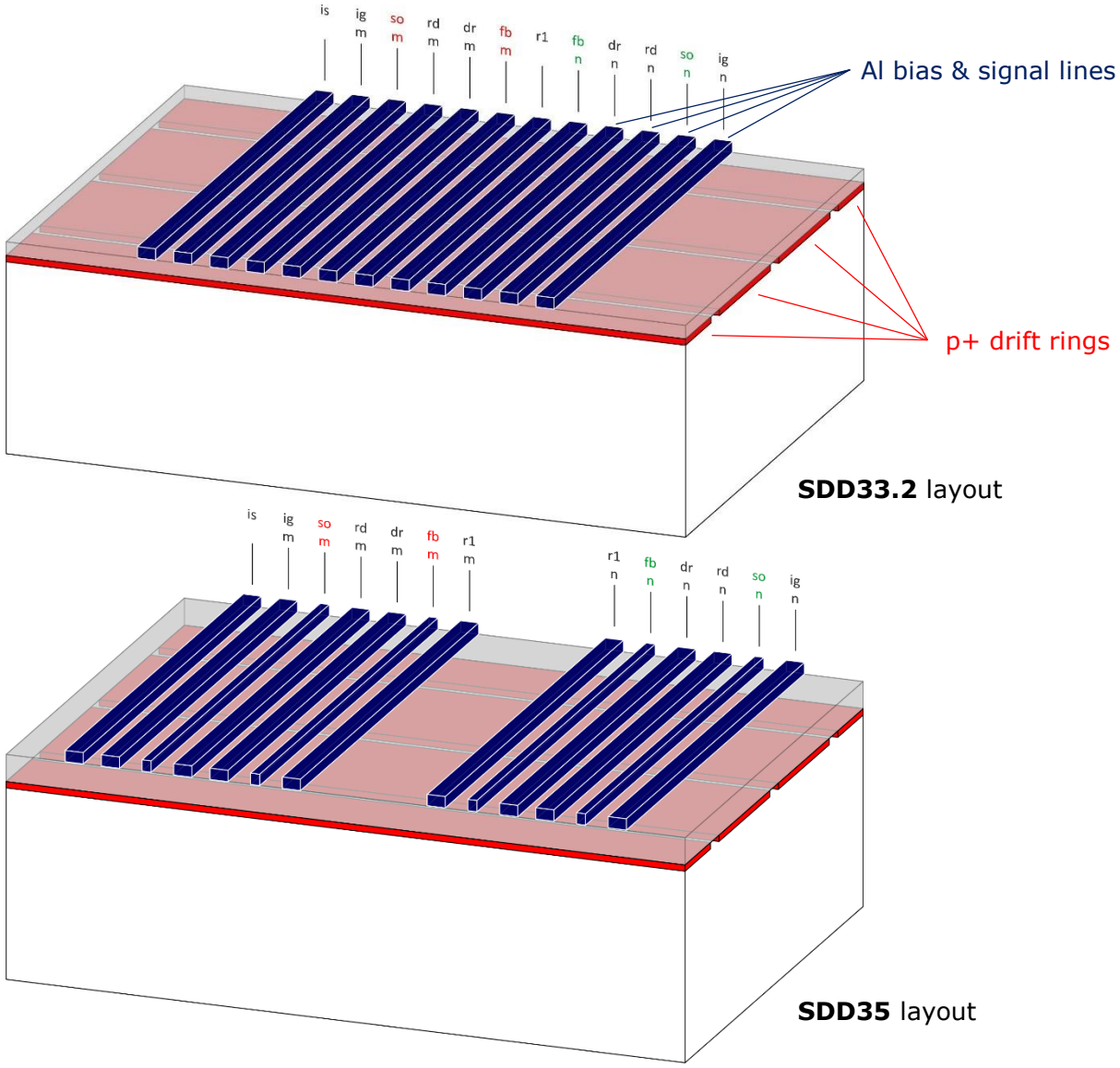


crosstalk measurements by K. Urban



TRISTAN SDD

- crosstalk inside of the pixel array
  - assumption
    - → transmitted via high-ohmic connected drift rings
  - simulation not practicable
  - intuitive approach
    - → reduction of coupling capacitance by
      - thick insulator
      - distance between cell connections
      - narrow signal lines
      - capacitive clamping by ground plane
  - in parts confirmed by SDD33.3

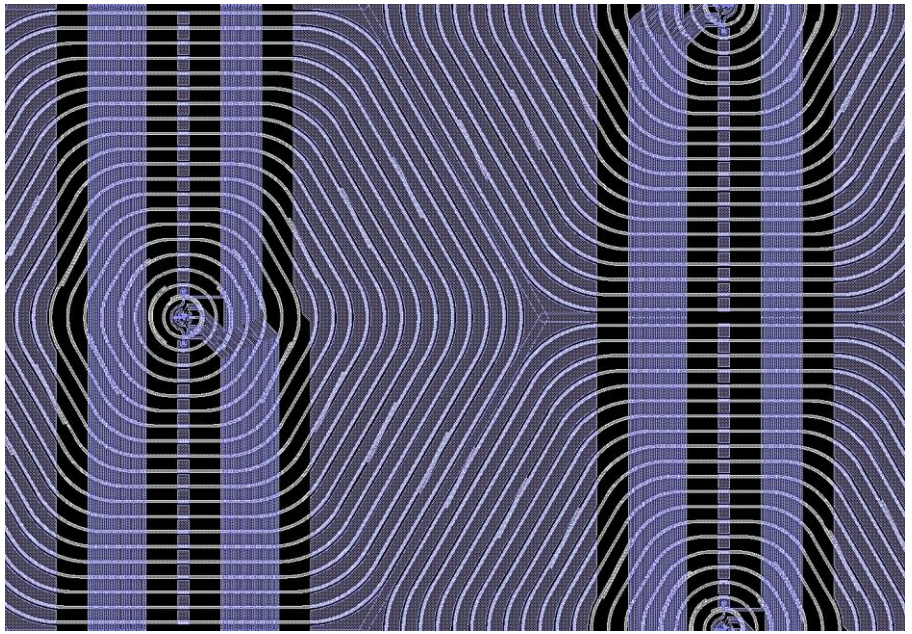


TRISTAN SDD

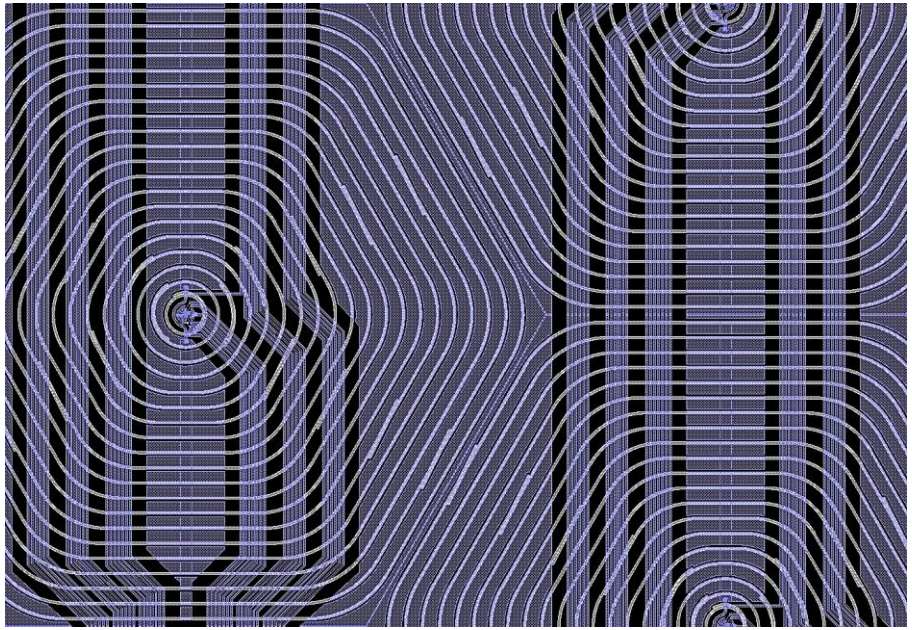
- crosstalk inside of the pixel array
  - layout & process modifications
    - thick insulator

      SDD33.2 SDD33.3 **SDD35**

      400 nm → 800 nm → **1400 nm**
    - distance between cell connections
    - narrow signal lines, 20% width reduction
    - (capacitive clamping by ground plane)



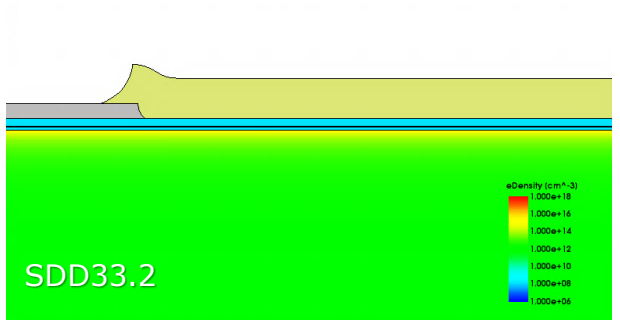
signal & supply line routing
SDD33.2

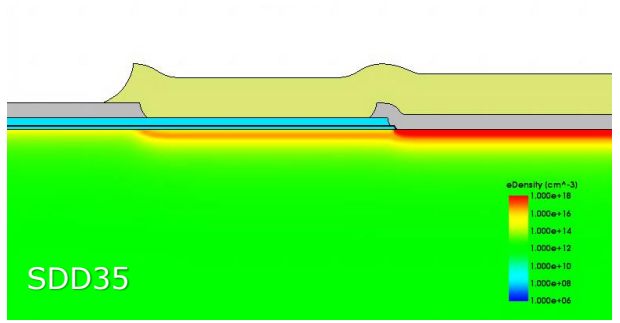


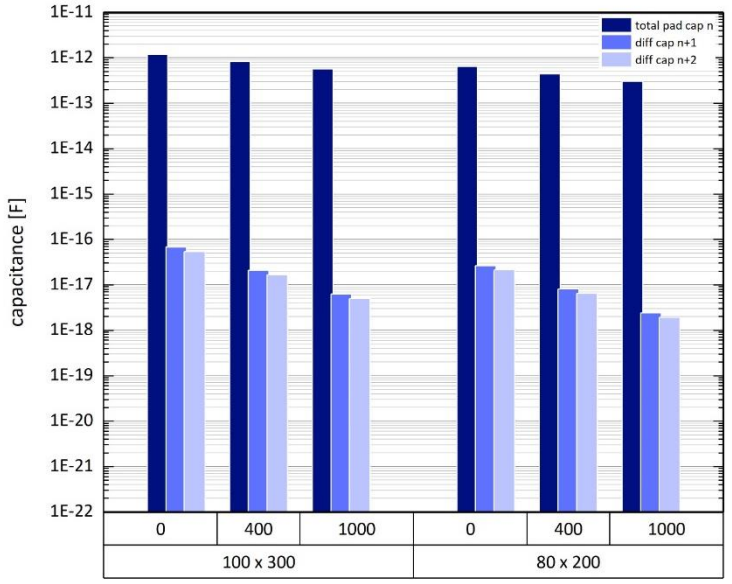
signal & supply line routing
SDD35

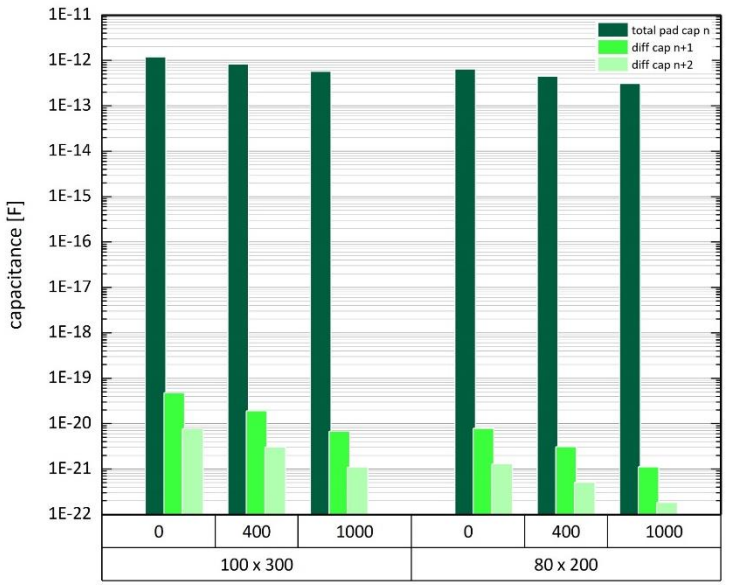
TRISTAN SDD

- crosstalk via bond pads
  - assumption
    - → transmitted via loosely connected bulk
  - device simulation
    - → reduction of coupling capacitance by
      - thick insulator
      - smaller bond pads, larger gaps
      - bond pads enclosed by ground frame



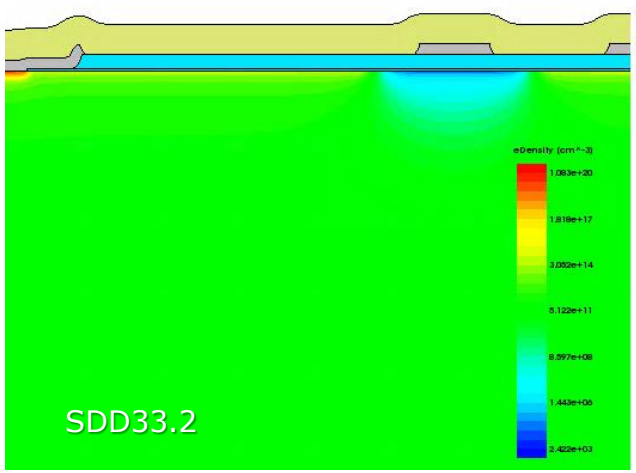


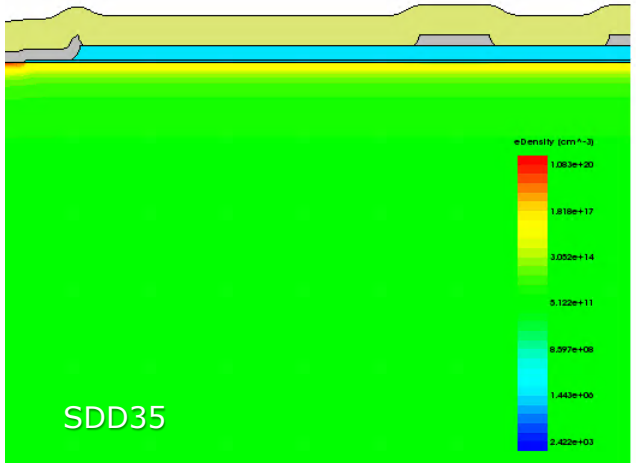


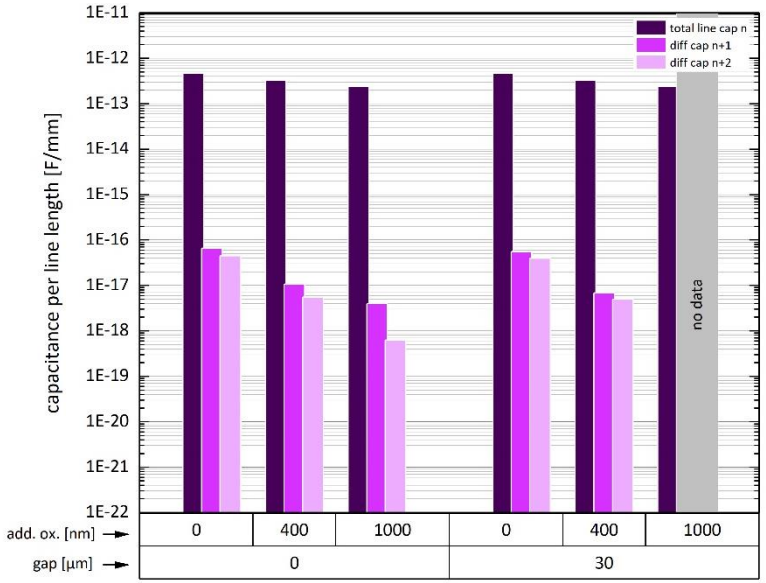


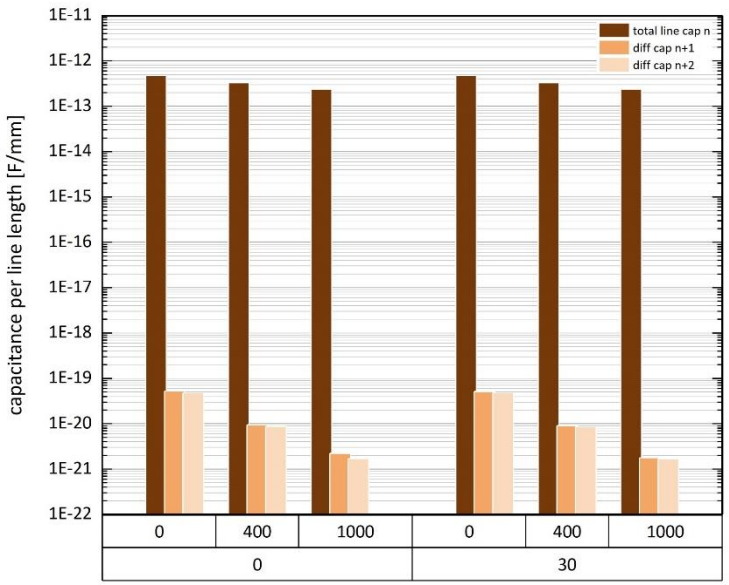
TRISTAN SDD

- crosstalk via bond pads
  - assumption
    - → transmitted via loosely connected bulk
  - device simulation
    - → reduction of coupling capacitance by
      - thick insulator
      - gap between cell connections
      - grounded deep n-implantation









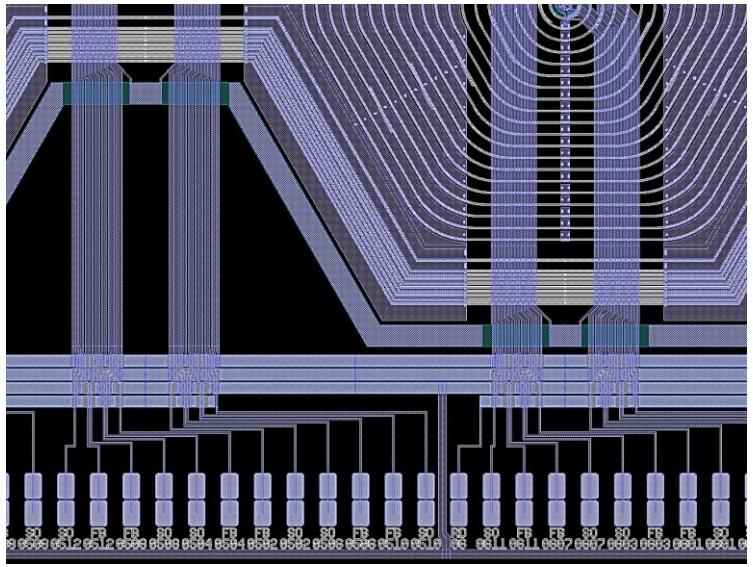
TRISTAN SDD

- crosstalk outside of the pixel array
  - ▷ layout & process modifications
    - ◇ thick insulator

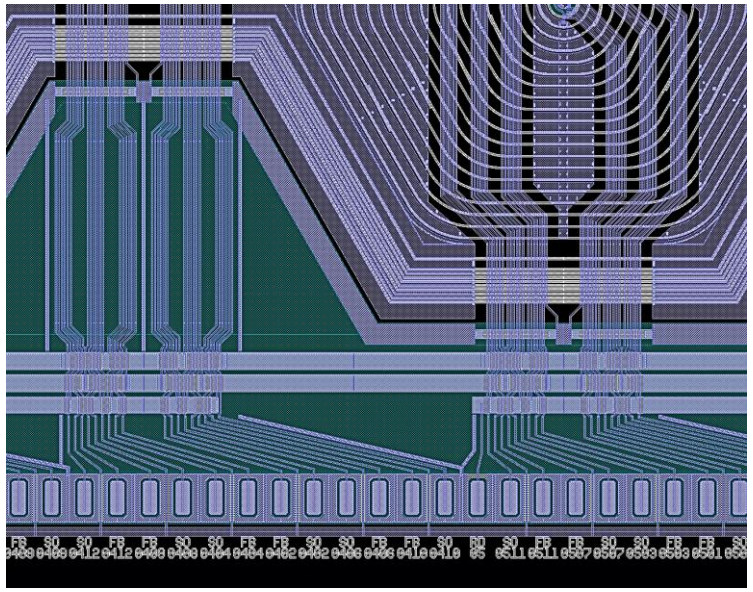
      SDD33.2 SDD33.3 **SDD35**

      400 nm → 800 nm → **1400nm**
    - ◇ small bond pads

      100 x 300 µm² → **80 x 200 µm²**
    - ◇ deep n-implantation & substrate contact
    - ◇ gap between cell connections
    - ◇ fan out of connection lines



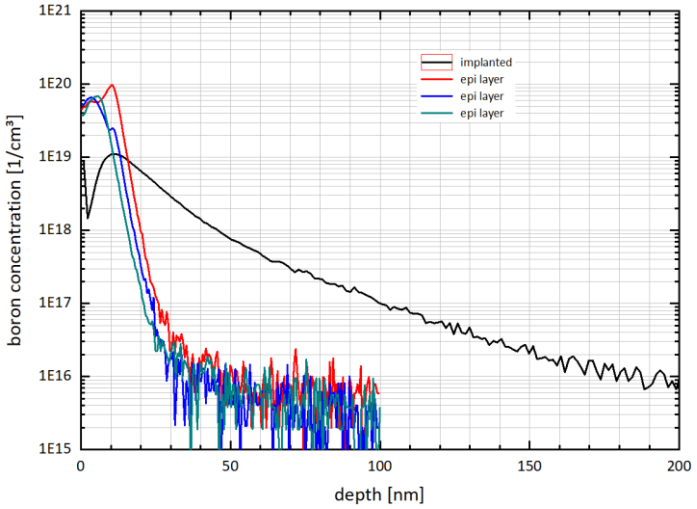
signal & supply line routing
SDD33.2



signal & supply line routing
SDD35

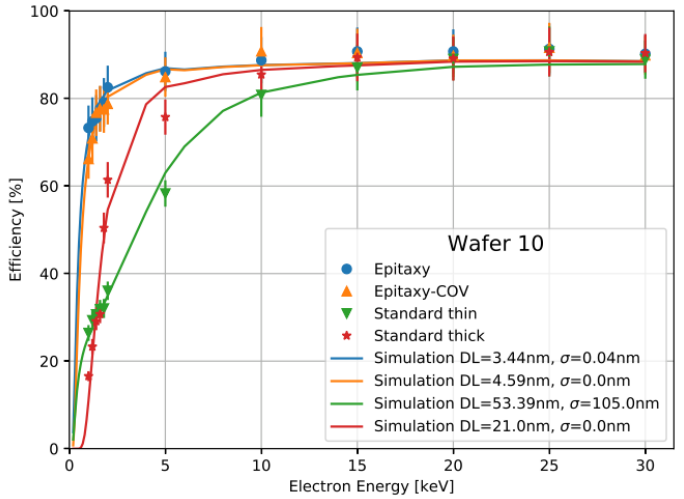
TRISTAN SDD

- entrance window
  - implanted diode
    - minimum energy & dose
    - min 'dead layer' thickness limited by profile diffusion @ thermal treatment for B activation
  - molecular beam epitaxy (MBE)
    - growth of B-doped Si
    - shallow profiles
    - external service by partner lab
    - tested on diode level
    - confirmed by e-beam current measurements
    - tbd: no. of wafers for MBE process



SIMS measured boron profiles

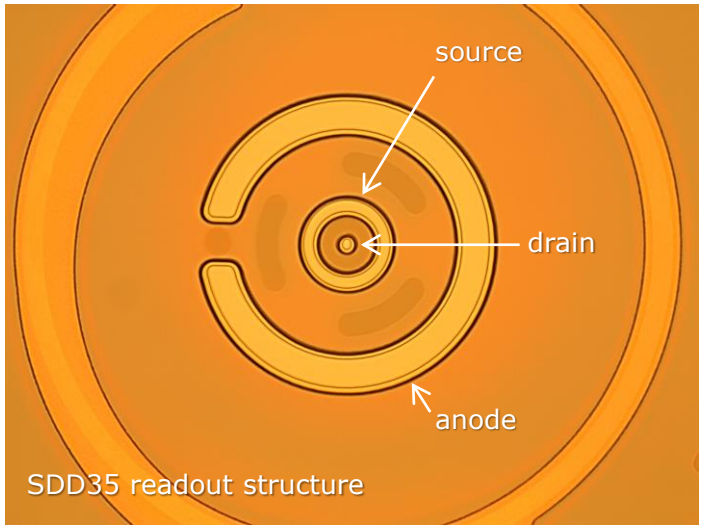
- implanted entrance window
- epitaxial grown layer(s)

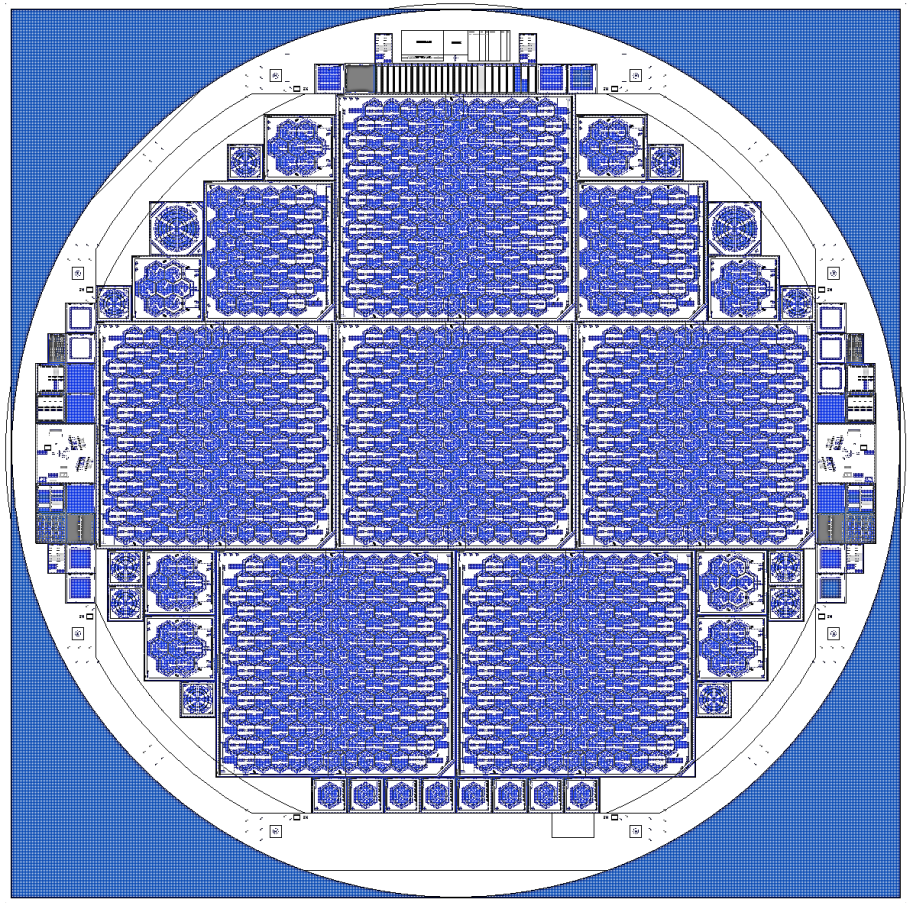


charge collection efficiency by monoenergetic electron beam current (thesis M. Lebert)

TRISTAN SDD

- new production SDD35
  - volume 10 wafers
  - chip count 6 x 166 cells
    2 x 47 cells
    8 x 7 cells
  - status jul22 lithography n^+ implantation
  - e.t.a. q1 of 2023





SDD35 wafer layout