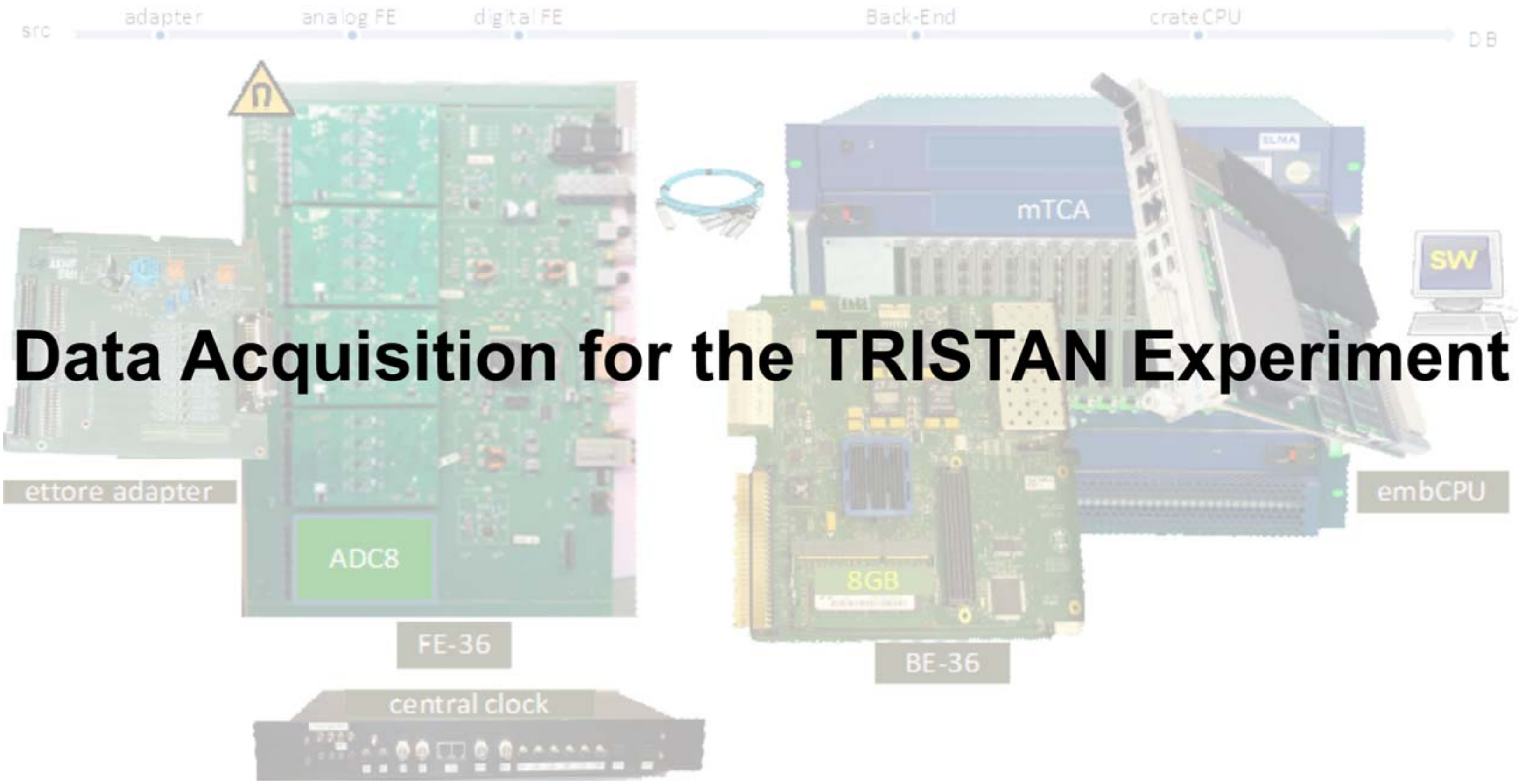
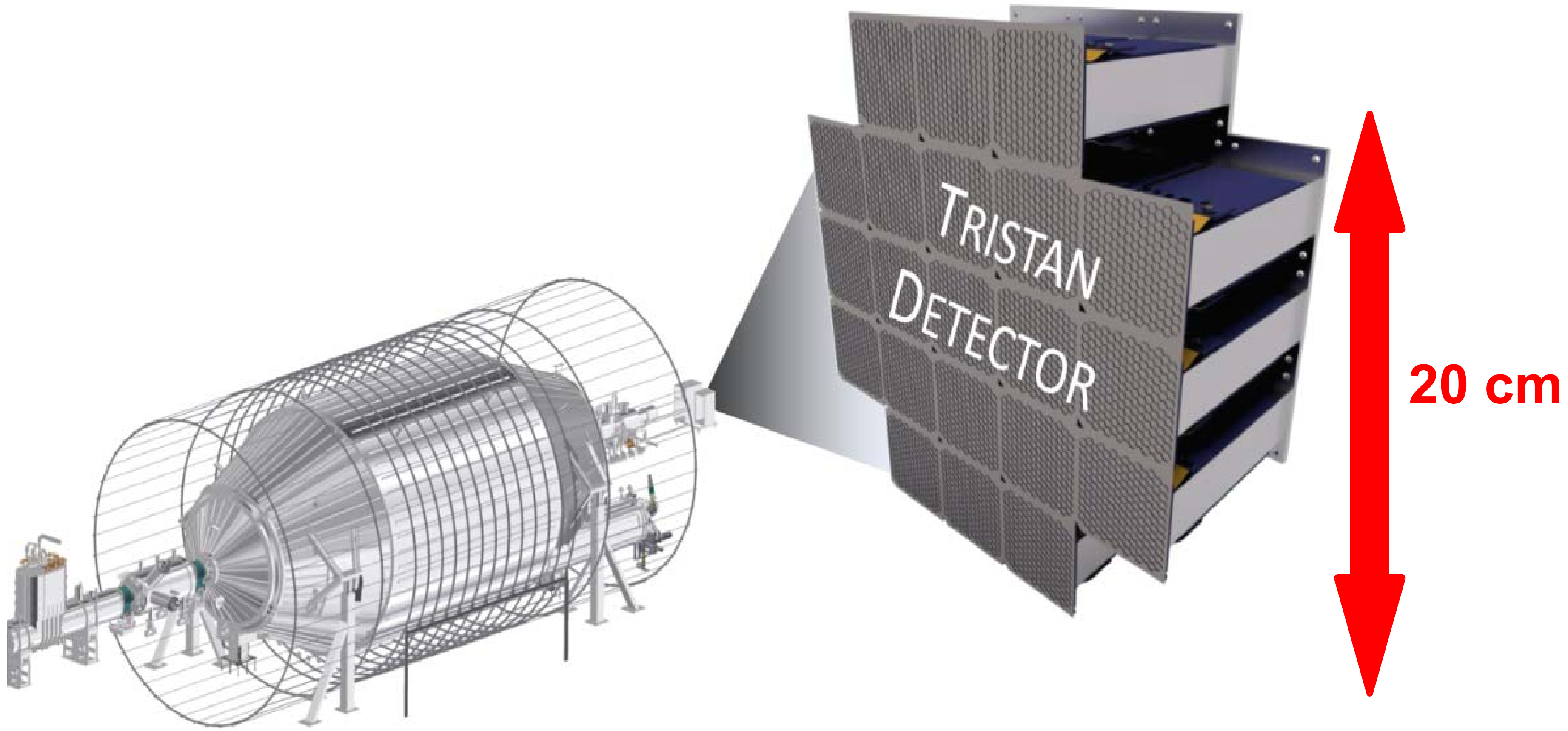
Data Acquisition for the TRISTAN Experiment



Overview

- Basic requirements for the TRISTAN detector DAQ
- Concept of the “remote” (detached) ADCs
- Phase 0 DAQ
- Phase 1 and 2 DAQ concept
- Readout Modes
- Status
- To Be Defined (open points in the DAQ specification)......

TRISTAN Final (Phase 2) Detector: 3486 Channels + Magnetic Field + P/A High Voltage



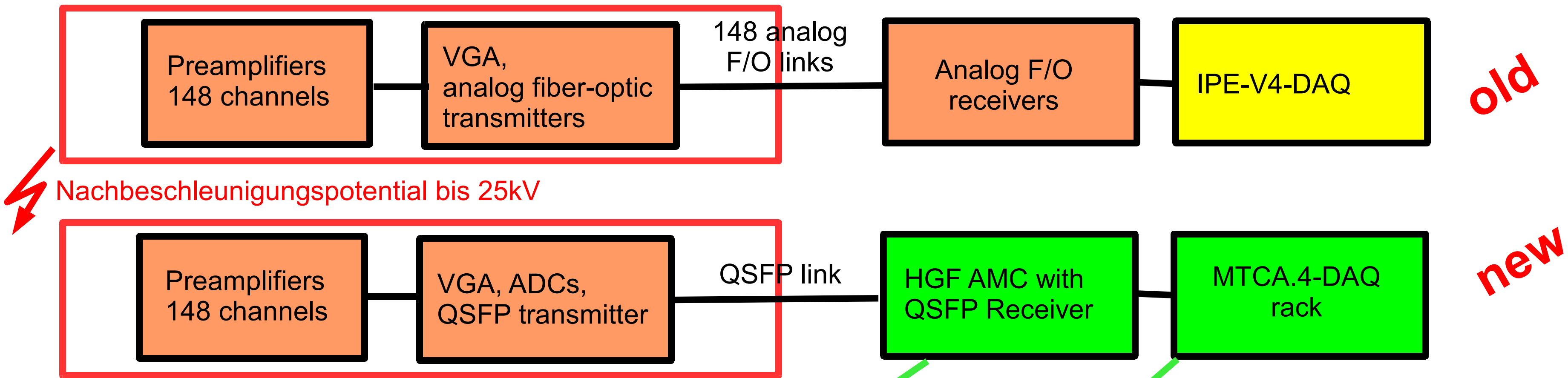
(Zeichnung: Gruppe S. Mertens)

Requirements for the TRISTAN DAQ

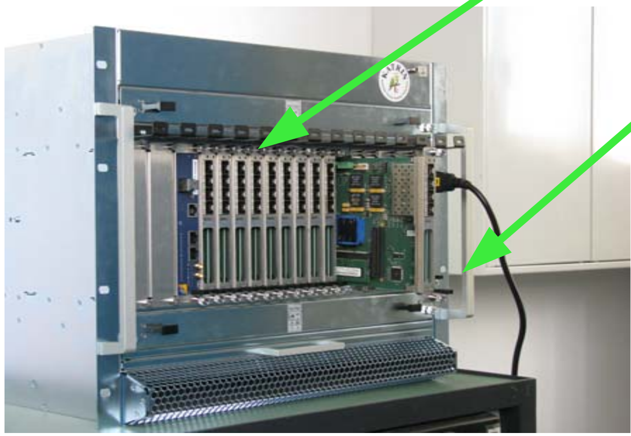
- Phase 2 full 21-tile concept: 3486 channels (166 ch. per tile)
- High rates (100 kHz per pixel)
- High-impedance DC-coupled inputs for the "Ettore" ASIC output signals
- Magnetic field compatible (100mT...1T)
- Front-end on post-acceleration potential (25kV)
- Adequate sampling of 30ns rise time signals
- Support energy resolution of <140eV
- Freely programmable, exactly reproducible digital waveform processing
- Complex trigger and event building schemes (coincidence, neighbouring pixel readout, etc.)
- **Management of the complex biasing scheme of the SDD (10 voltage settings, 15 voltage & current readbacks)**

"Remote" (detached) ADCs

- Concept developed at the IPE for the KATRIN "standard" focal plane detector
- DAQ requirements have grown (more complex digital preprocessing would be helpful, better gain stability, etc.)
- => early digitization, ADCs move close to the signal source



- projekt-specific
- partially multi-project
- multi-project



- Only one new board design required for retrofitting the KATRIN FPD with the new concept

Advantages and Challenges of the “Remote ADC” Structure

- Minimizing the analog signal path (interference pickup!)
- Easy high-voltage isolation through commercial digital fiber-optic media
- Simpler wiring
- Less project-specific building blocks

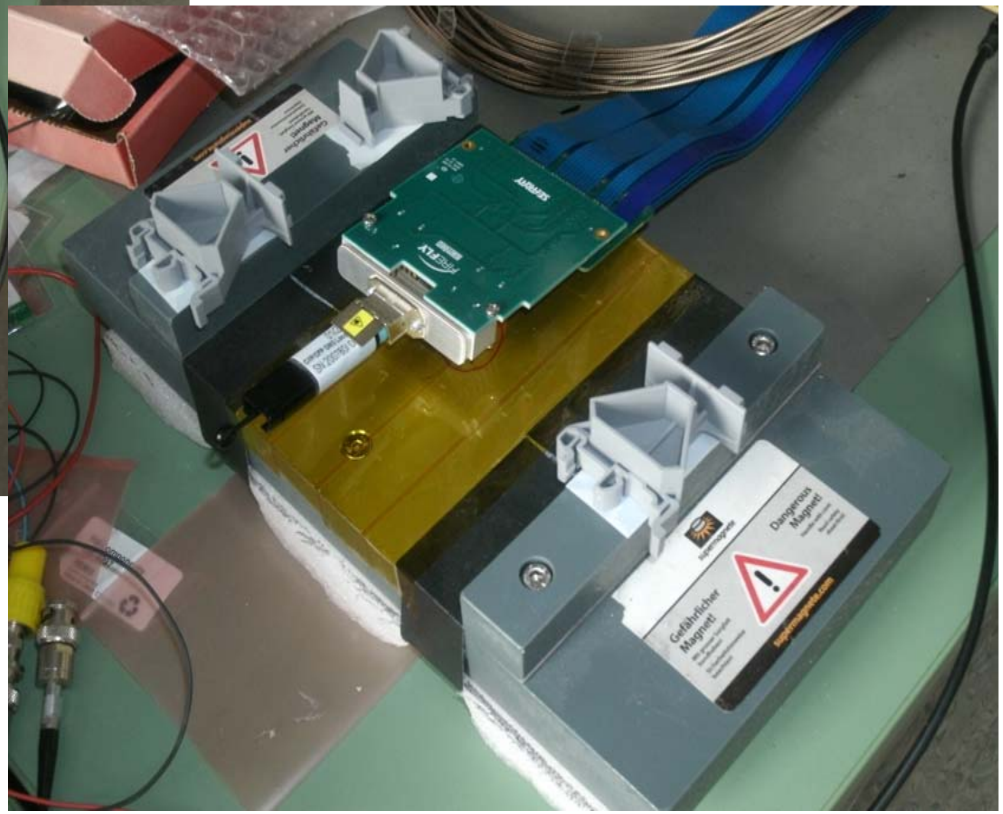
However:

- **DC/DC converters** required due to high power requirements
  - management of DC/DC stray fields
  - air-core inductors in DC/DC converters required (magnetic field!)
- DC/DC converters and high-performance digital circuitry close to analog inputs
- Magnetic field compatibility of commercial fiber-optic transceivers must be verified
- Complex sampling clock management:
  must be synchronous across whole distributed system
  => central timing unit (GPS clock etc.), PLLs
- Increased power dissipation compared to conventional (purely analog) front-ends

Karlsruhe Institute of Technology

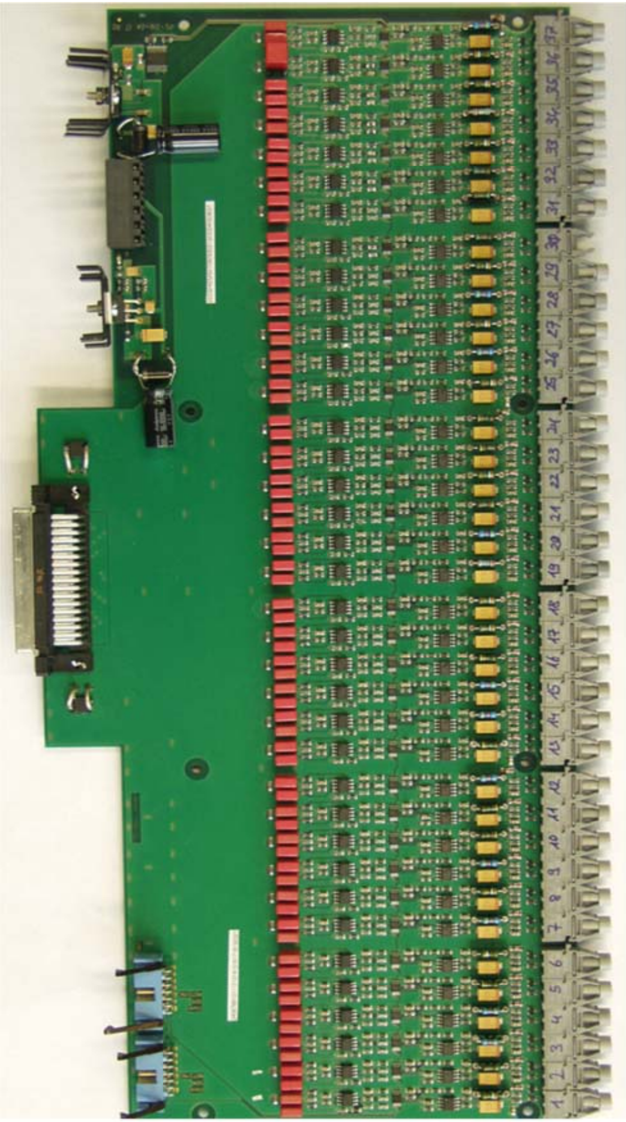
Magnetic Field Test for Commercial F/O Transceivers BER = f(B) ?

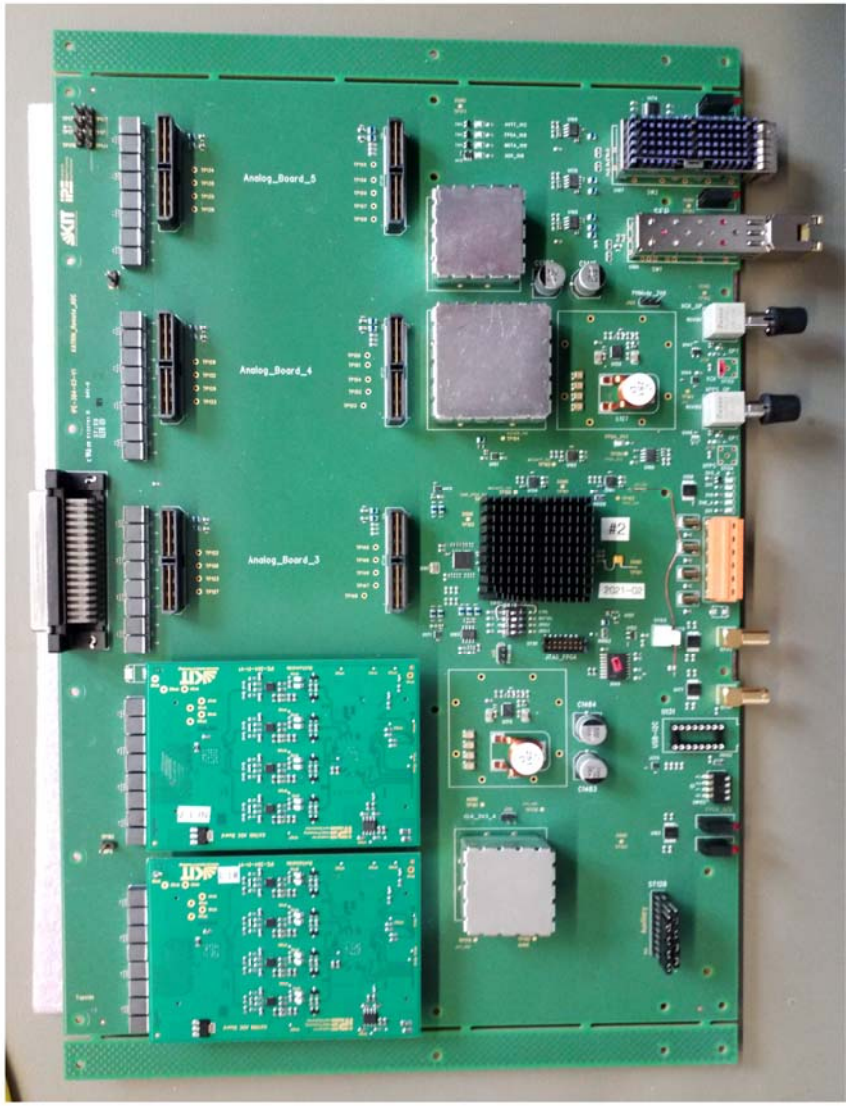
Test chamber, 400mT,
Neodymium ”Death Magnets”



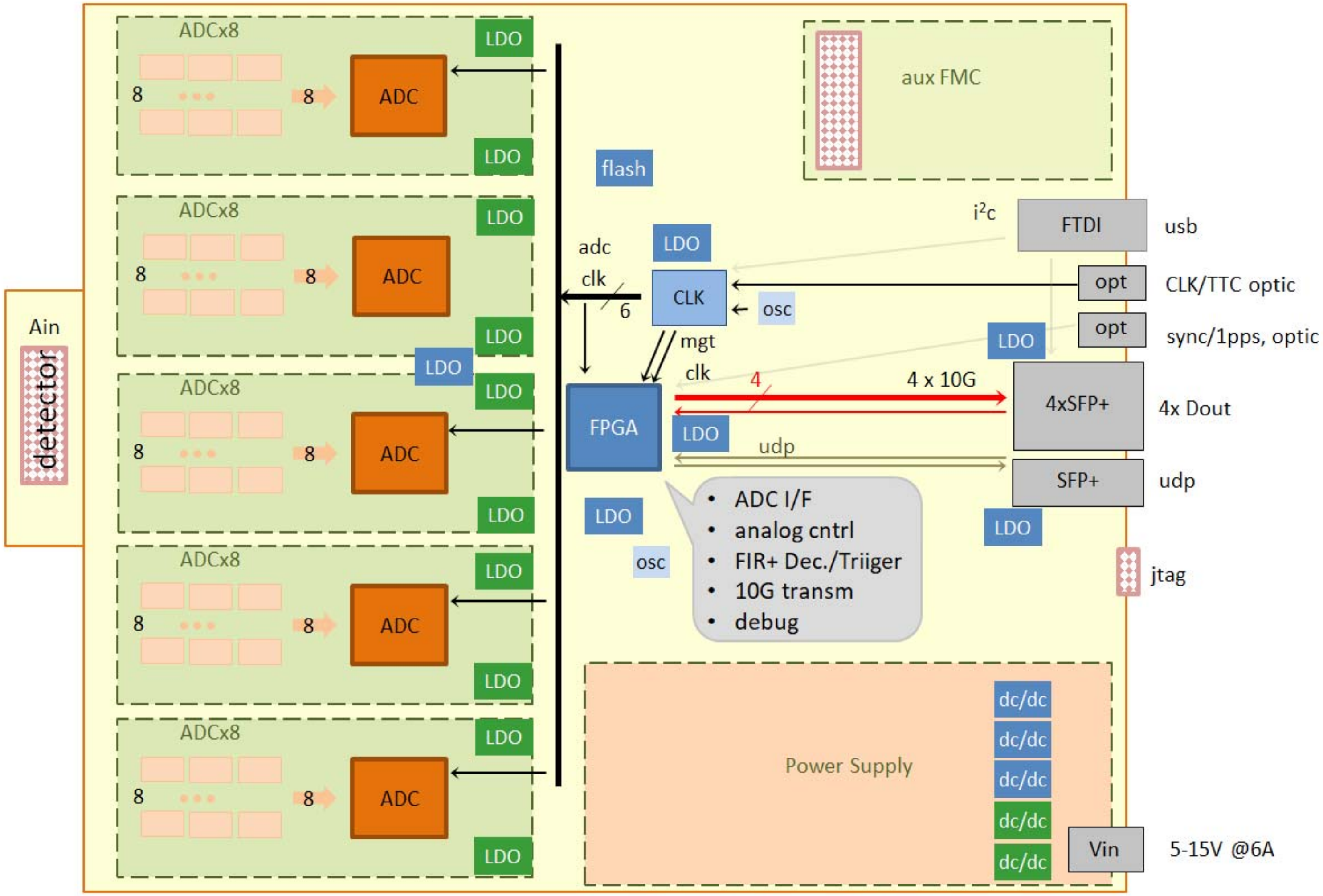
(Bilder: J. Hartmann)

“Remote” ADCs for the KATRIN FPD (37 Ch OSB → “RADC-40”) and TRISTAN Phase 0 (5 x RADC-40)





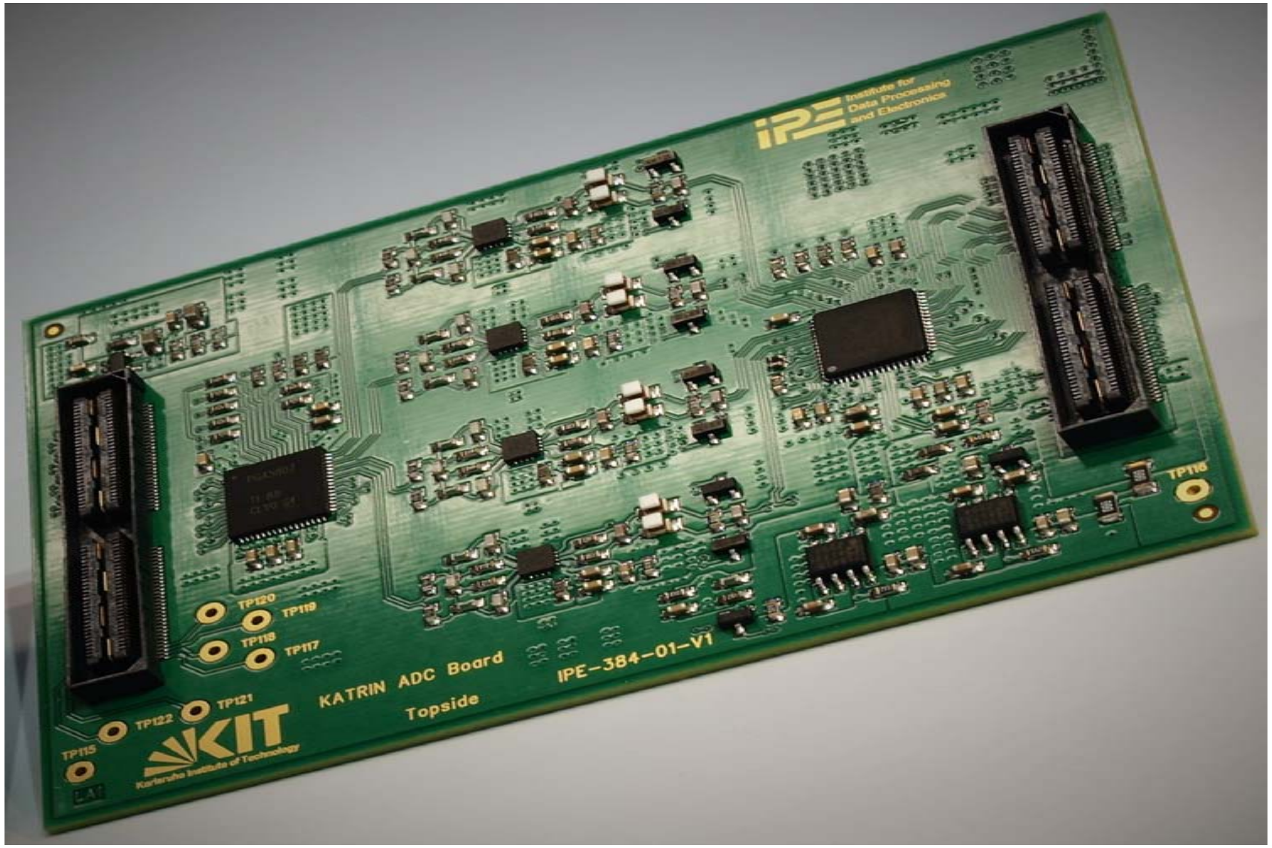
Phase 0: The RADC-40 Front End Board



(Skizze: D. Tcherniakhovski)

8 Channel ADC Module

- PGA, AA Filter (ceramic core inductors), ADC
- Fully differential analog signal path
- 65 MSps, 14 Bit
- 1,5 W

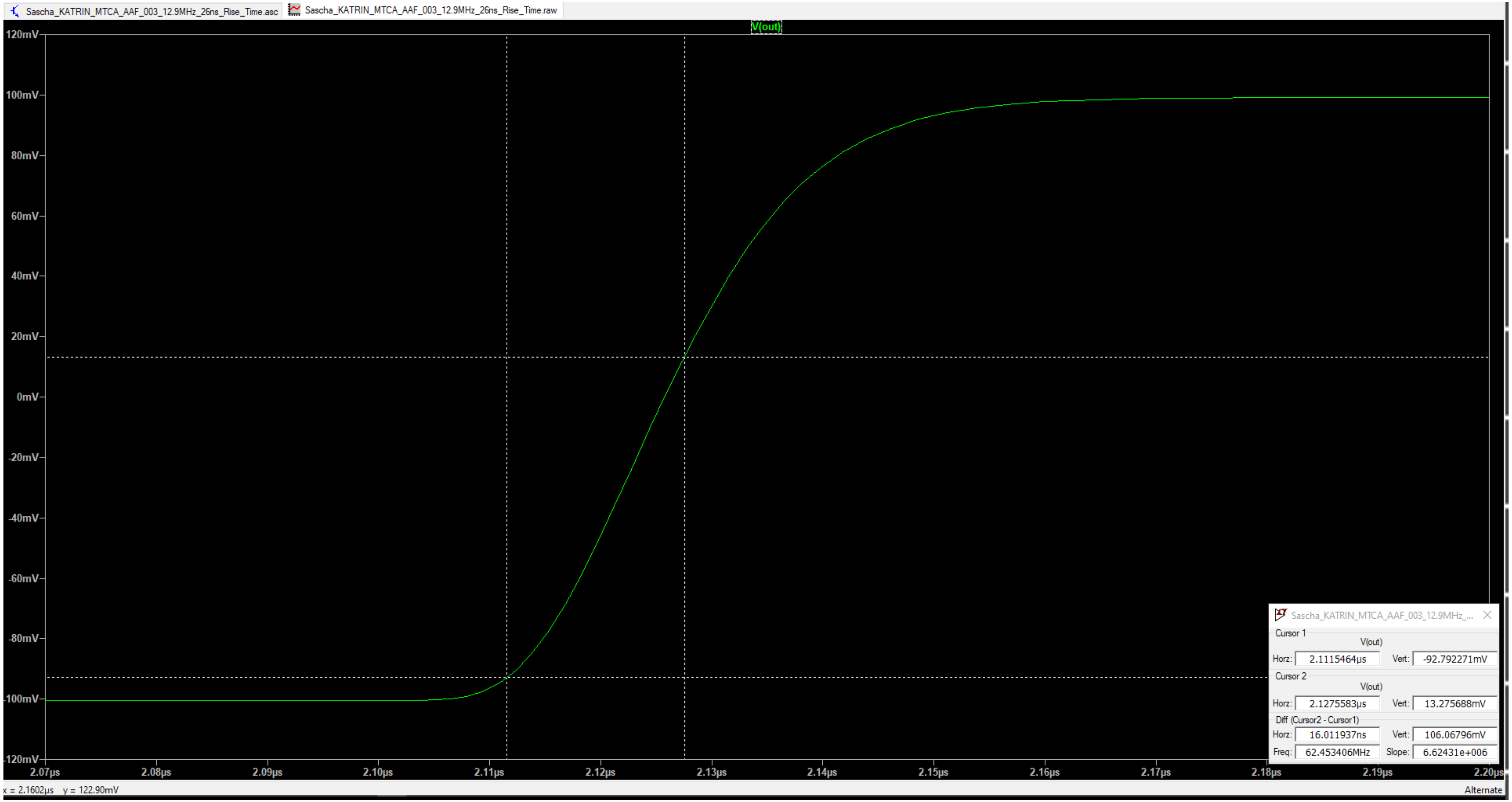


(Bild: Marc Schneider)

Basic Data of the 8 Channel ADC Module

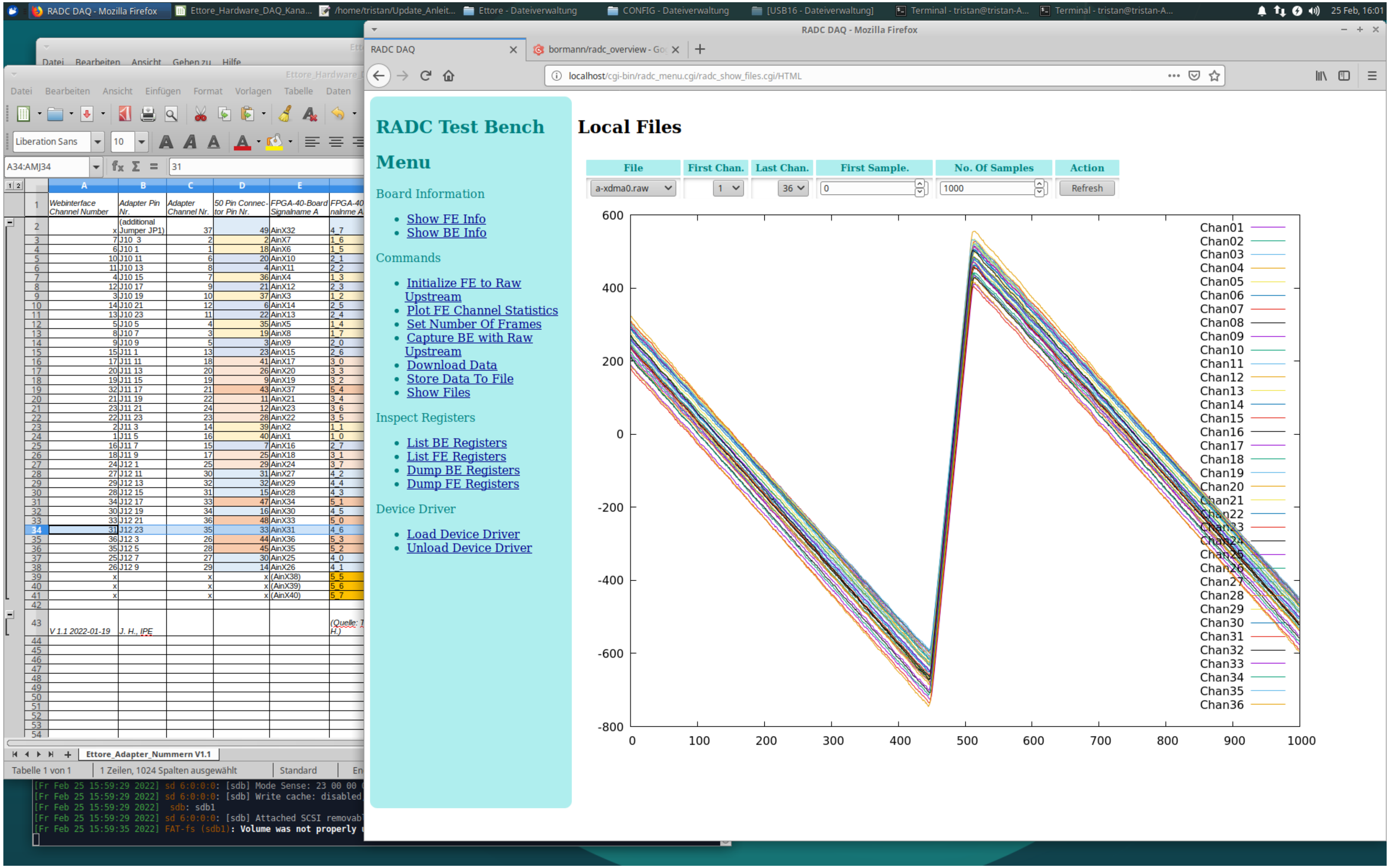
Betriebsspannung 1 (PGA, AAF)	3,6 V, ca. 170 mA
Betriebsspannung 2 (ADC)	2,3 V, ca. 310 mA
Verlustleistung	ca. 1,5 W
Anti-Aliasing-Filterung	Bessel (gutes Impulsverhalten), 5. Ordnung
Anti-Aliasing -3dB-Grenzfreq.	12,9 MHz
Anti-Aliasing-Dämpfung bei 31,25 MHz	14 dB
Analog-Verstärkung	12…30 dB (4x … 32x) in 3 dB-Schritten
Vorgesehene(s) Abtastrate/-intervall	62,5 MHz / 16 ns
FSR am Eingang	63 mVss … 0,5 Vss
Analogeingang	differentiell, hochohmig, DC-Kopplung
Common-Mode-Bereich	1,9 V … 2,3 V

Step Response of the AA Filter

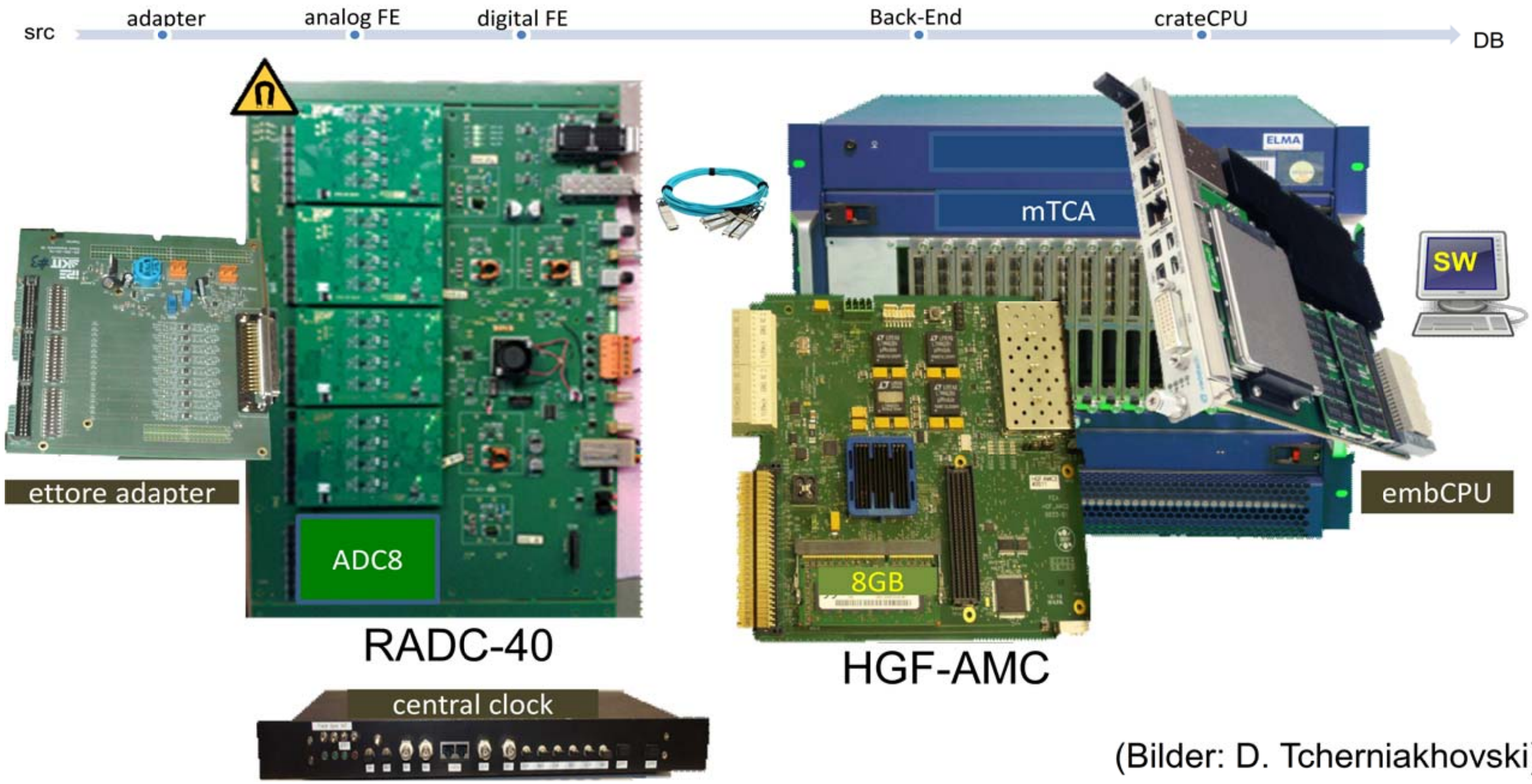


Marker spacing 16ns (1 sampling interval)

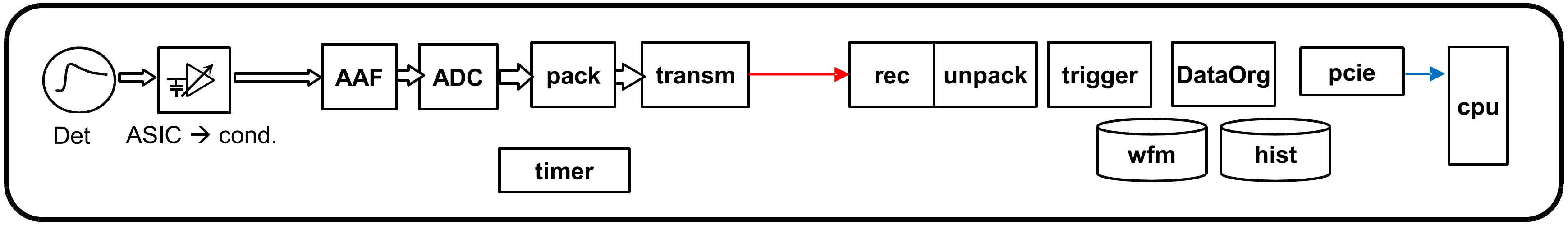
GUI for RADC-40 Testing



The Phase 0 DAQ Structure

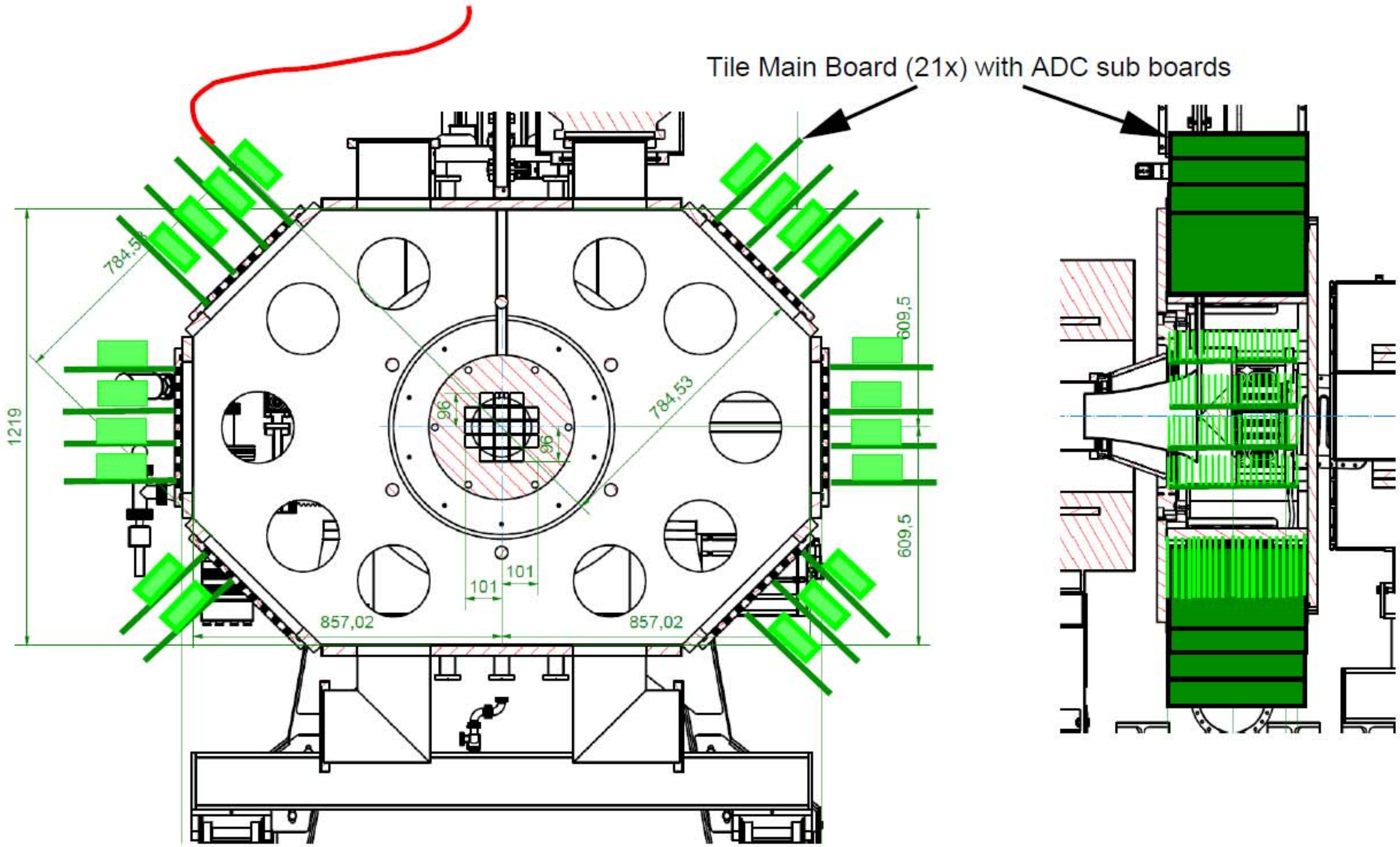


(Bilder: D. Tcherniakhovski)



Phase 0 DAQ Hardware
(1 of 5 RADC-40 fitted)

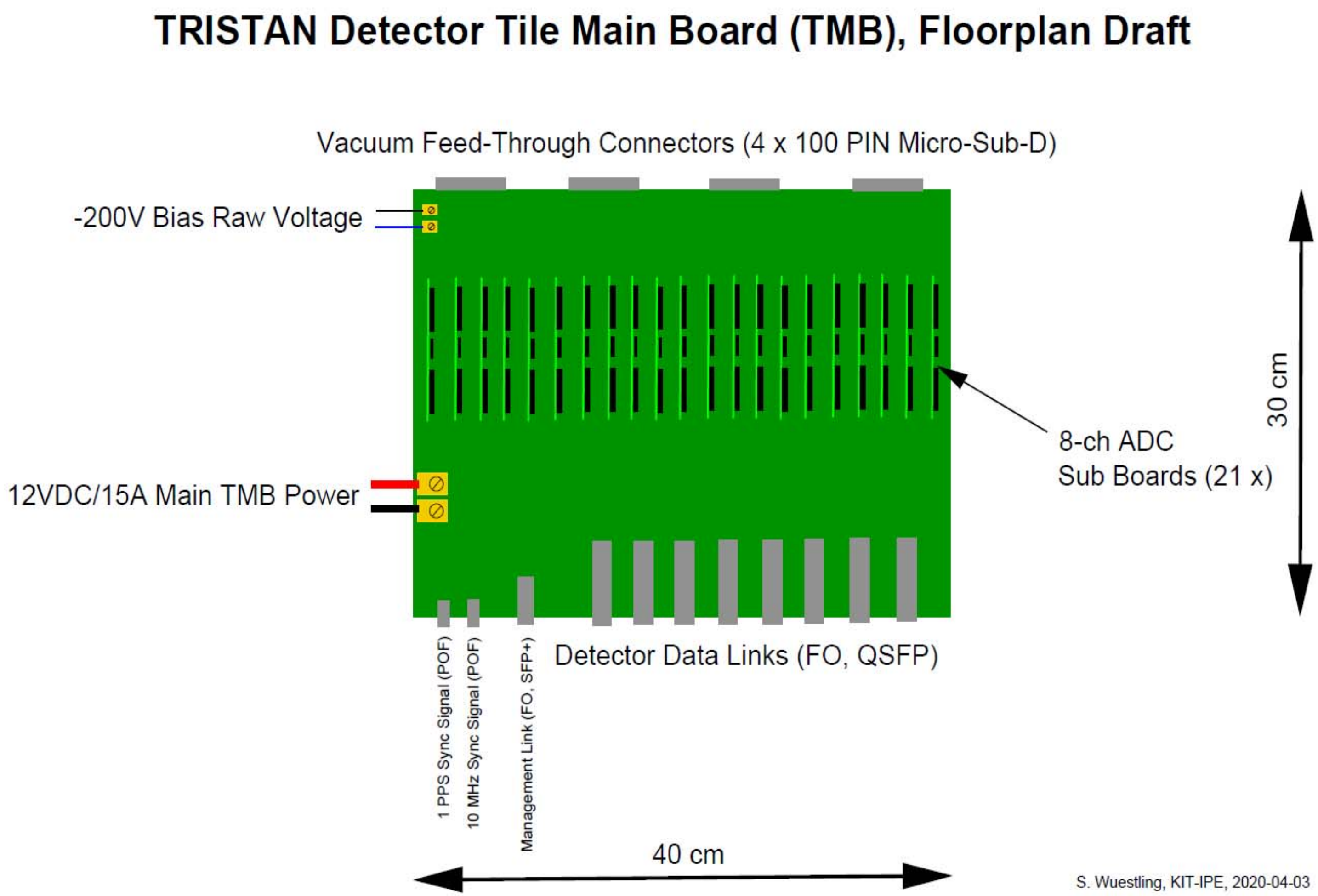
Phase 2 Concept for the Front-End Electronics Arrangement



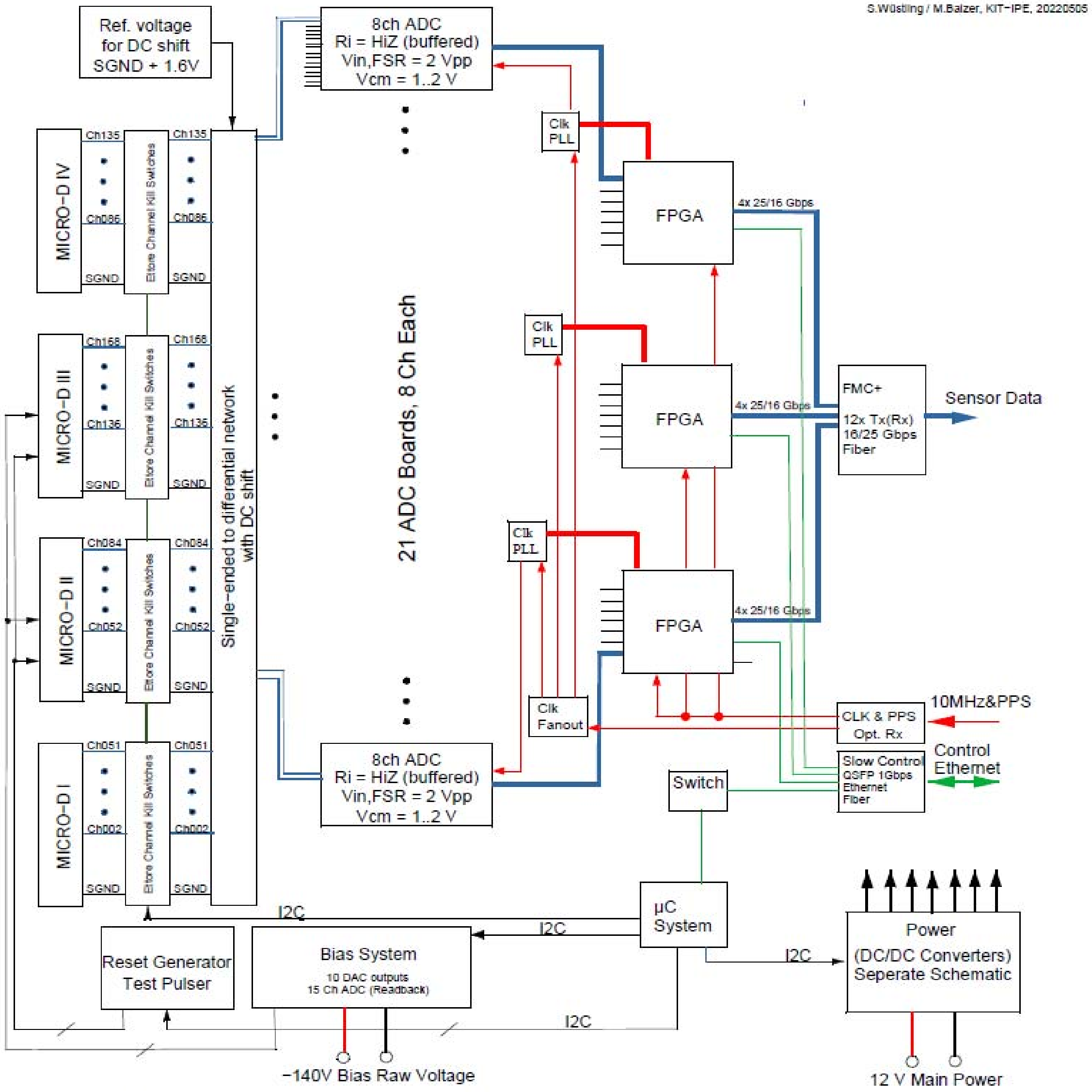
TRISTAN Detector Ambient Air Electronics (Draft), S. Wuestling, KIT-IPE, 2020-04-03

Not shown in the drawing: PCB support frames, FO harnesses, power cable harness

TRISTAN Detector Tile Main Board
a. k. a. “RADC-168”



Tile Main Board Block Diagram



TRISTAN RADC-168 Digitizer Board ("Tile Main Board"), Block Diagram

Tile Main Board Sub Modules

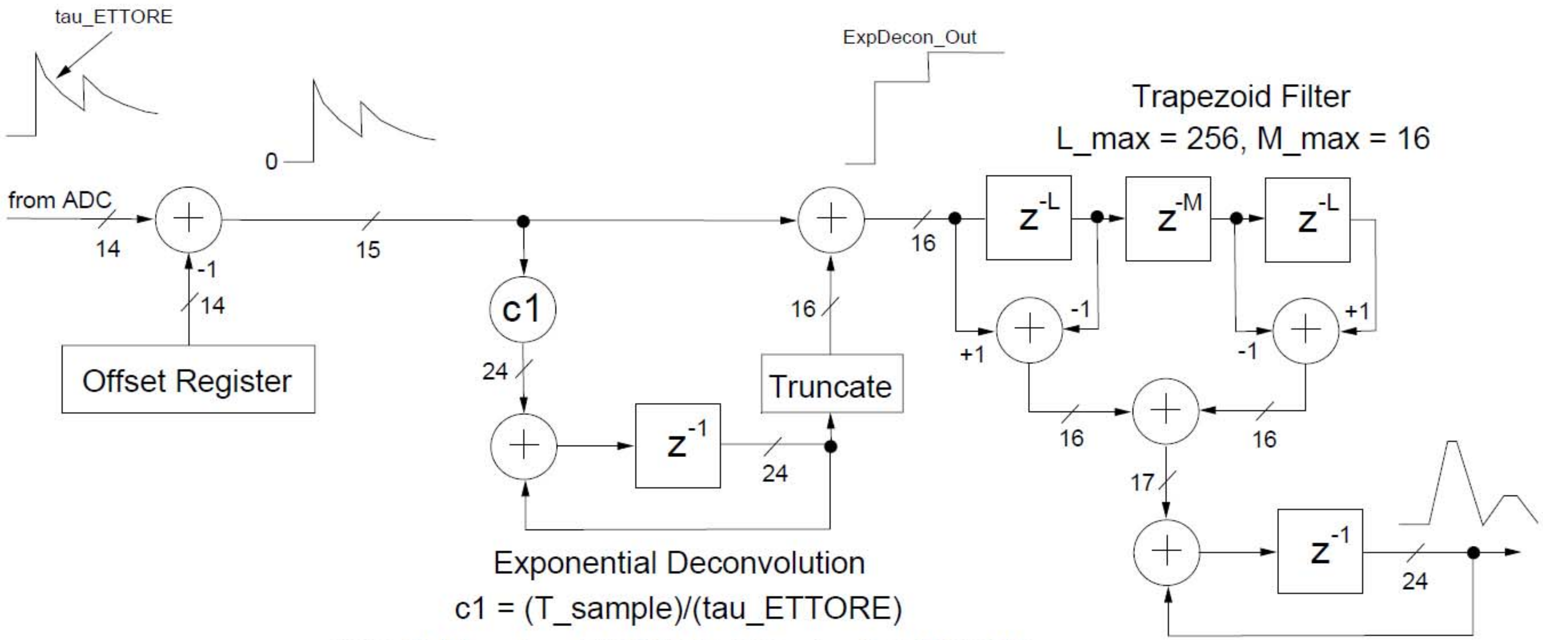
Purpose of sub-boards:
space savings, design risk reduction, future improvements

- 21 x ADC board (8 channel)
- Power Module, 6 DC/DC converters (all air-core inductors), 82 W in total (!):
  5V / 1.5A for Ettore 3.3V
  2.3V / 6A for ADC 1.8V
  3.3V / 3A for ADC 3.0V
  3.5V / 4A for 3.3V digital power
  1.8V / 12A for 1.8V and 1.2V digital power
  0.85 / 18A FPGA core
- Bias Board
  10 adjustable SDD & Ettore bias & supply voltages
  15 readback channels
- uC-Board for slow control purposes (voltage settings & readbacks)….
- Reset Board (to be defined)

TRISTAN Phase 2
DAQ “Backend”
3486 Channels

- 3...4 IPE CMS “Serenity” boards in a ATCA rack
- provide FPGA power for the waveform & event processing

Exponential Deconvolution
a. k. a. Pole Zero Compensation



ExpDecon integrator width: during L (???) samples, ExpDecon_Out must remain within FSR/2

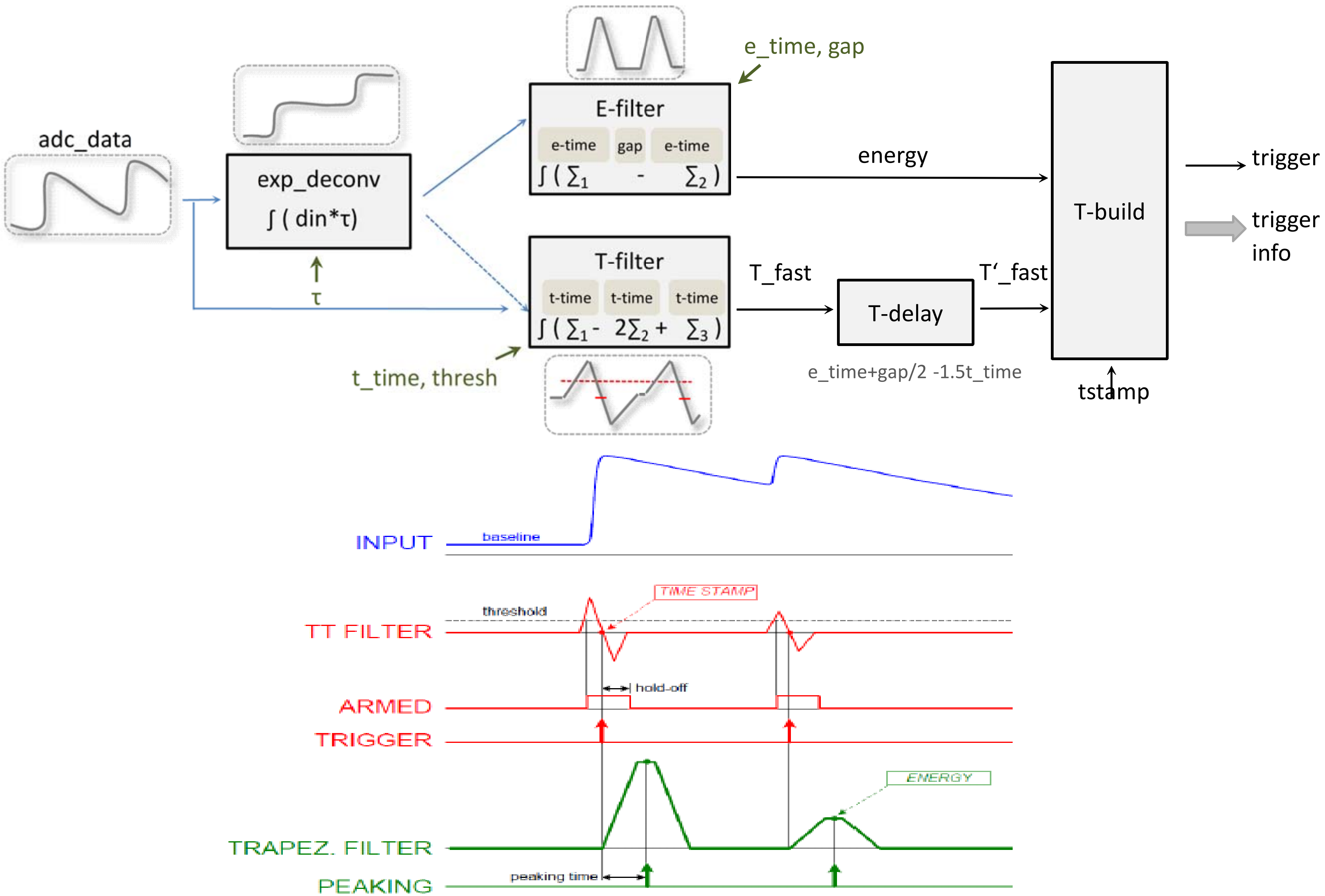
This is true as long as the shaping time (L/f_sample) < tau_Ettore/2 (to be confirmed)

Offset register adjustment: without events, trapezoidal output should be zero (ExpDecon_Out=const.)

ExpDecon (c1) adjustment: energy-rate dependency must be zeroed

TRISTAN Waveform Processing, S. Wuestling, KIT-IPE, 2022-01-31, rev. 03

Trigger and Energy Filters



Readout Modes

- **Waveform mode:** manually triggered waveform capture
- **List Wave Mode:** triggered waveform capture
- **Energy Mode:** triggered event capture
- **Histogram Mode:** Histogramming of triggered events
  - Golden
  - Silver
  - Pile-up
  - Multiplicity
  - etc.
- Phase 0 (Monitor Spectrometer):
  Waveform Mode, List Wave Mode, Energy mode
- Phase 1 and 2:
  Waveform Mode, List Wave Mode, Energy mode, Histogram mode

Status of the DAQ Task

- a number of **“RADC-40” boards manufactured and tested**, operative at MPP München and KIT-IPE, AC and DC coupled variants
- Adaption to the “Ettore” output signal range: a number of **“Ettore-Anpassboard” manufactured and tested**
- **Hardware for phase 0 ready** (1 of 5 RADC-40 due to delivery delays)
- Schematic design of phase 1 and 2 ADC board complete, connector defined (commonly available PCIe edge connector 168 pin)
- Bias board for phase 1 and 2 schematic design almost complete, connector defined (DIN 41512 64 pin)
- Power board for phase 1 and 2 component selection complete, power supply sequencing yet to be defined, connector selection to be confirmed
- FPGA firmware and DAQ PC software for phase 0 measurements ready

To Be Defined

- “Gatti Slider” ADC nonlinearity mitigation.
  Current idea: Single offset DAC for all channels
- Built-in ADC nonlinearity diagnostics methods
  Current idea: Detector leakage current sawtooth from Ettore preamp output (LED illum. may be required when detector cooled)
- Reset methods: fixed frequency, first overflowing channel resets all, etc.