The Data & Infrastructure Density Challenge in Ultra High Speed Imagers

- with CoRDIA as example –

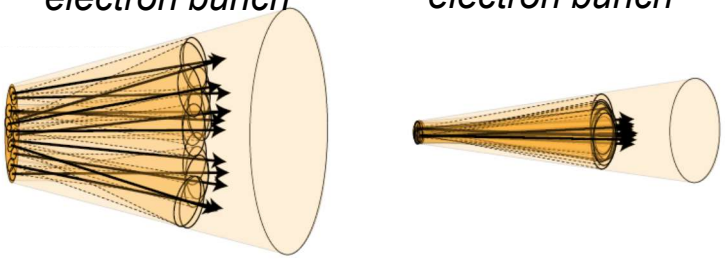
Ulrich Trunk | DESY FS-DS | 17.03.2022

CoRDIA–Motivation: Coming Source Upgrades

PETRA-IV: Upgrade to a diffraction limited ring (2028)

PETRA-III electron bunch

PETRA-IV electron bunch

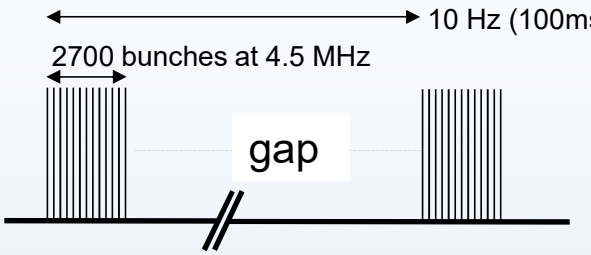


- 100-1000 fold improvement in brilliance and coherent flux
- Frame rate requirements in some experiments increase from kHz to >100 kHz (continuous) readout

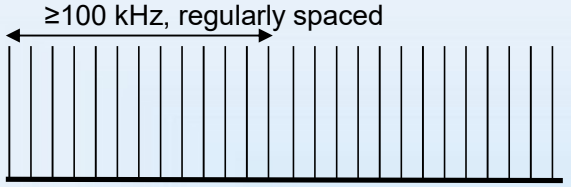
common need for:
- continuous readout
- > 100kHz frame rate

European XFEL: CW mode operation (20??)

Current Eu.XFEL



CW operation

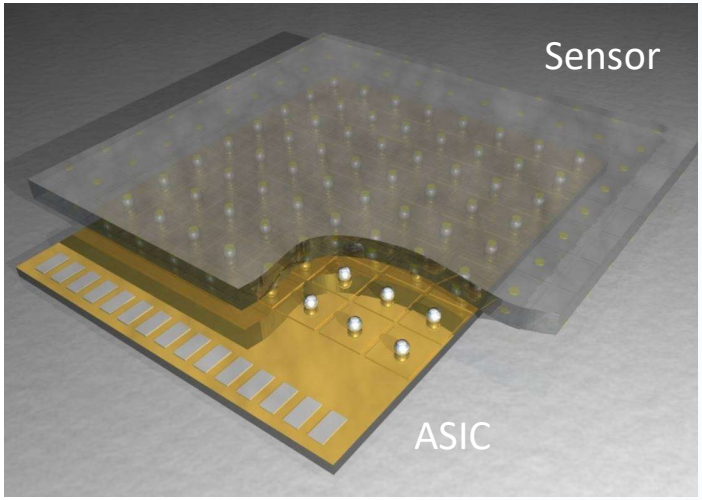


many more [O(1)] bunches per second
no gap for burst-readout of internal storage

CoRDIA – Continuous Readout Digitising Imager Array

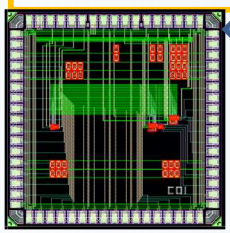
CoRDIA – **Co**ntinuous **R**eadout **D**igitizing **I**mager **A**rray - is…

- Targeted to DL Synchrotron sources (like PETRA IV)
- CW FELs (future CW Mode of European XFEL)
- Collaboration of Bonn University & DESY



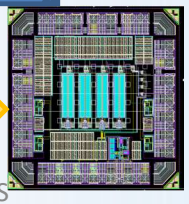
CoRDIA is…

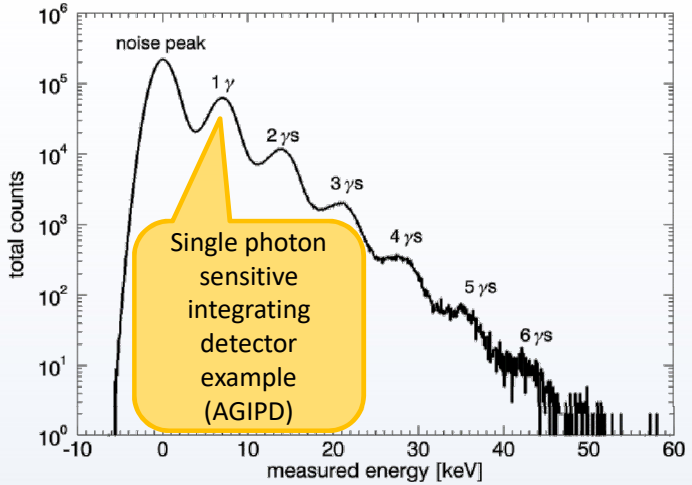
- A Hybrid Pixel Detector
- Charge Integrating
- Pixel size 100µm × 100µm
- Continuous Frame Rate f_{FR} ≈ 150kHz (≥100kHz)
- On-Chip Digitisation @ ≥ 10 bit
- GWT Data Transmission (based on Timepix4 Implementation)
- Dynamic Gain Switching (à la AGIPD) -> +2 bit



CoRDIA 0.1 (analogue) &

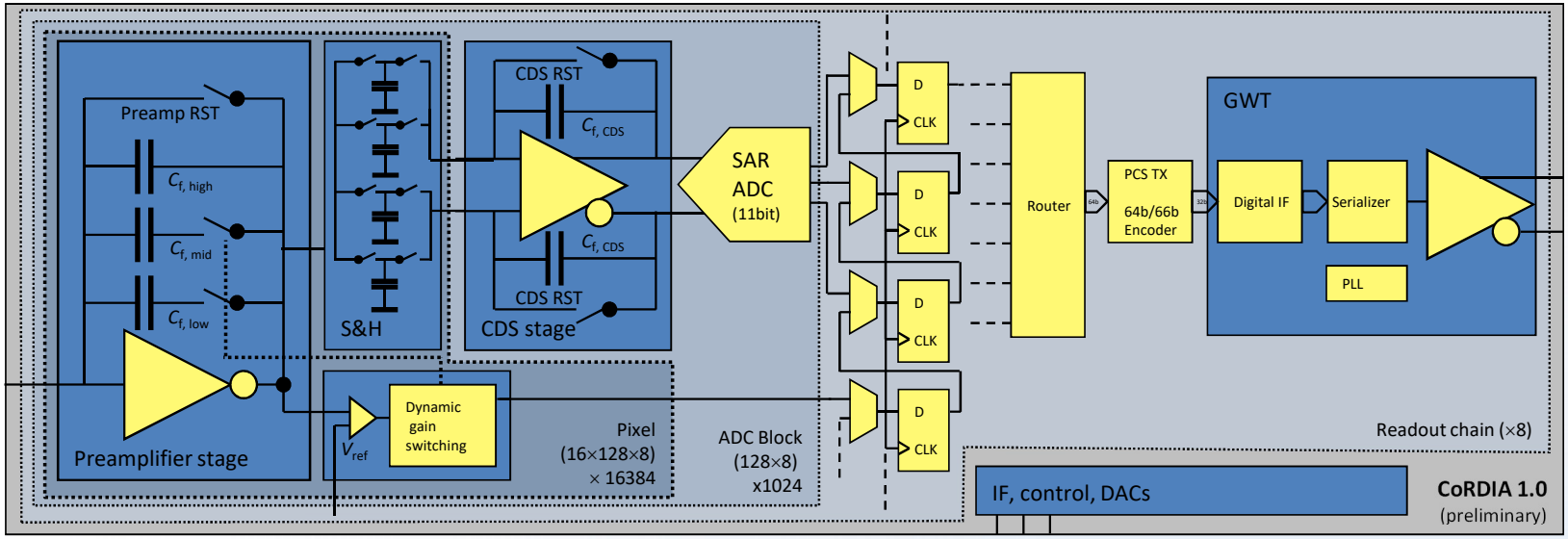
SAR ADC test chips





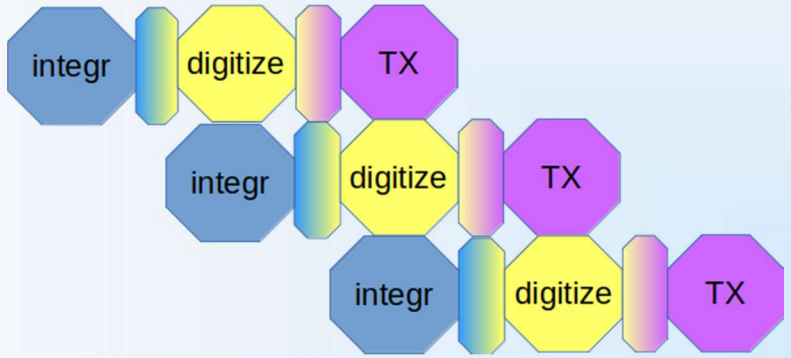
- Single-Photon Sensitive (@ ≤12keV)
- ≥ 10k Photon Dynamic Range
- Dead-Time free Pipelined Operation
- Targeted at Electron-Collecting Sensors:
  - Si for hard (12keV X-Rays)
  - High-Z materials for E > 15keV
  - Active (LGAD) Sensors for low E
- Little or No Dead Area

CoRDIA – Architecture & Signal Path



CoRDIA Architecture

- CW
- Pipelined operation
- Small dead time due to reset of integrating preamp

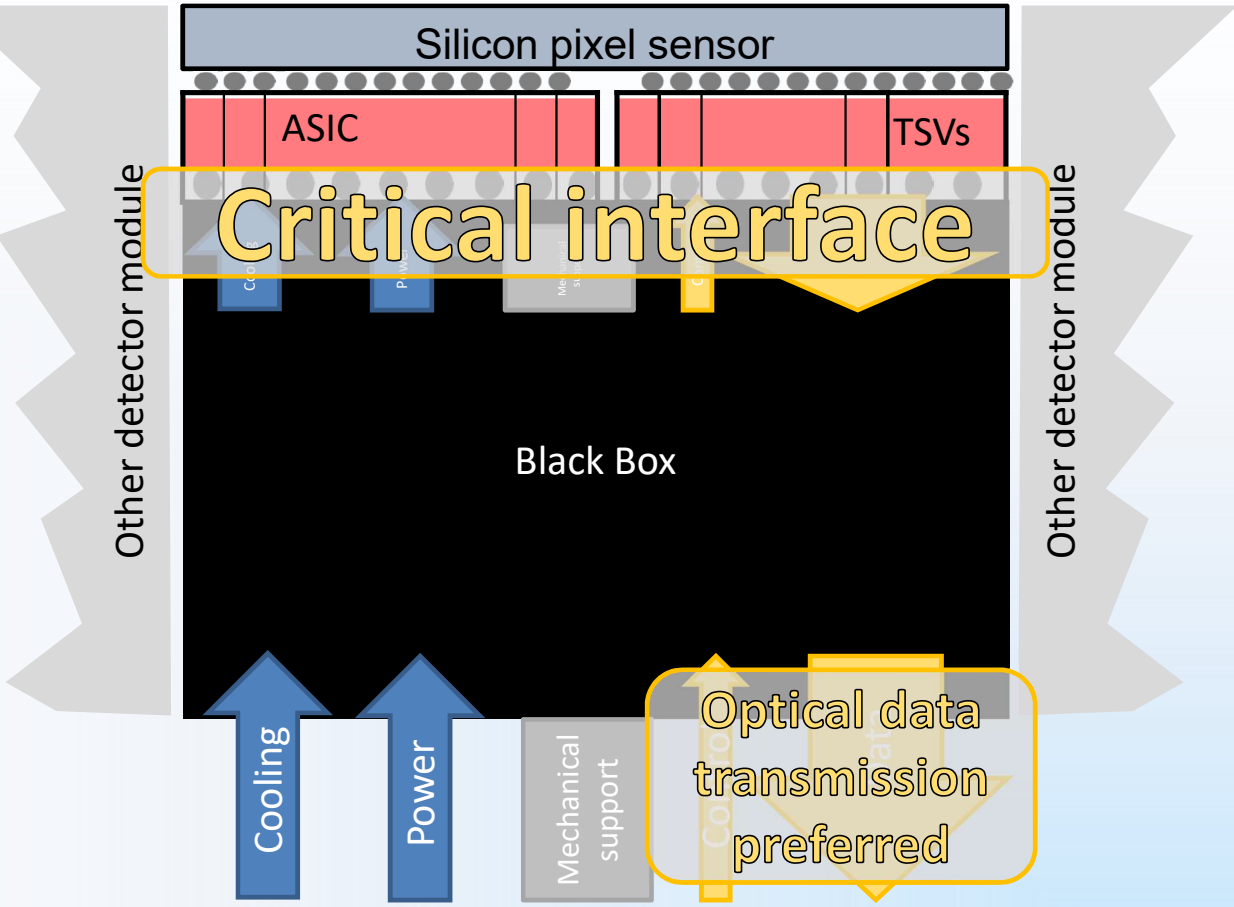


A Black Box…to be filled

Any hybrid pixel detector needs a
- Mechanical
- Thermal
- Electrical (i.e. power supply)
- Data (i.e. control & readout)

Interface to the outside world.

Some boundary conditions:
- The interface is never completely “dumb” or passive. Intelligence may range from
  - Power supply control to
  - Data reformatting to
  - Calibration
- Electrical and optical components should be commercial of the shelf components (COTS) to minimize development effort.
- The hybrid detector itself is a “”wear part” due to radiation damage and should be easily exchangeable
- Operation in vacuum is required for single photon sensitivity
- Optical data transmission to the outside world is desireable



A little Math……
…… is where the Trouble starts!

CORDIA

Per Pixel:
- 11 bit from ADC resolution
- 2 bit from gain encoding

- 13 bits/(image▪pixel)
- 150 kHz frame rate

- 1.95 Mbit/(s▪pixel)

Per ADC Block:
- 16 pixel/ADC

- 31.2 Mbit/ADC block

Per MGBT Link:
- 128 ADC blocks
- 2048 pixel
- 64b/66b encoding

- 3.9935 Gbit/(s▪link) input

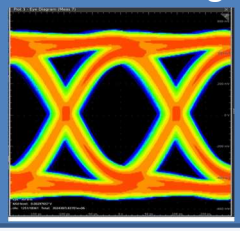
- 4.1184 Gbit/(s▪link) output ☺

ASIC :
- 100µm × 100µm pixel size
- 128 × 128 pixels

- 12.8mm × 12.8mm size
- 16384 pixels
- 8 MGBT links ☹

- Low enough to work with the Timepix4 GWT transceiver (IP block)
- Some margin to run faster than 150 kHz
- Lower requirements on PCB design

Timepix4
GWT @5 Gbit/s
X. Llopart,
On behalf of the Medipix4 Collaboration
11 th February 2022
CERN seminar



- Too many!
- 128 MGBT links for an AGIPD-sized (8×2 chip) Module
- FPGAs with SoC are all ≤96 GTH/GTY TX
- Only Xilinx VU13P has 128 GTH/GTY TX, but no SoC

Sensor & 8×2 chip module

Readout board (w. SoC FPGA)

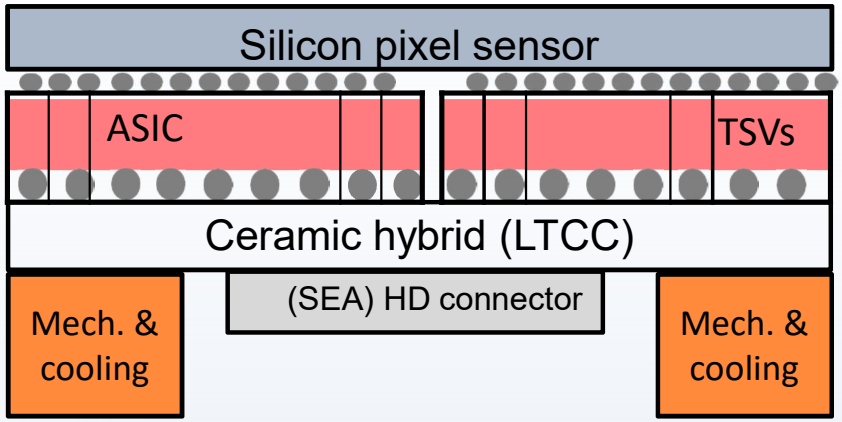
A few things to consider…

Sensors and ASICS are usually mounted on a ceramic hybrid (LTCC):

- For matching of thermal expansion coefficients
- For thermal conductance

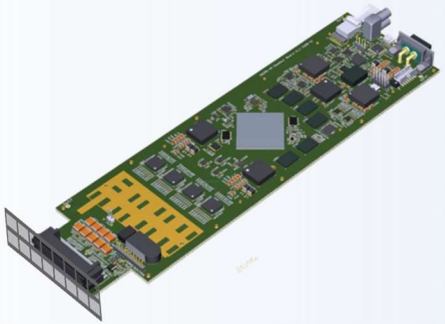
- Design rules are difficult
  - Impedance matching and
  - Routing recommendations may not be fulfilled

- The same may hold true for the RDL on the bottom of the ASICs



Components are characterised/qualified under optimal conditions:

- Signal integrity may be compromised by
  - A sequence of connectors
  - Routing areas with sub-optimal impedance control
  - Crosstalk in congested areas



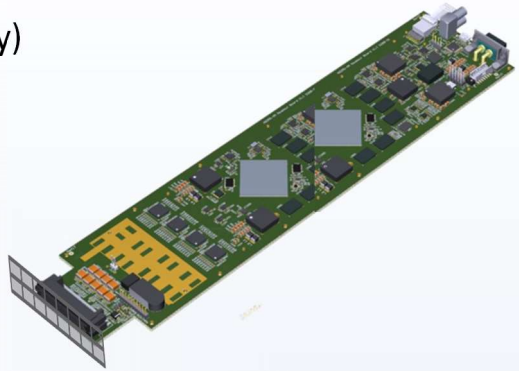
Power consumption is non-negligable

- Estimated 1.0..1.5 W/cm² (30cm²)
- Substantial area needed
  - Contact surfaces
  - Thermal vias
  - MC cooling

Inside the Black Box….

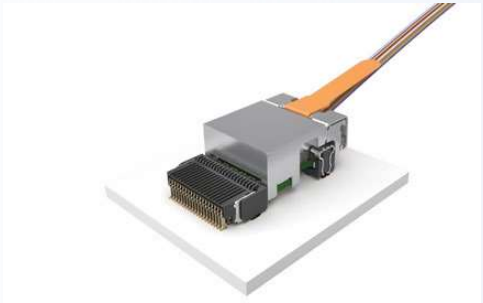
AGIPD-like FPGA based RoB not desireable:

- Operation in vacuum (Single-photon sensitivity)
- Power consumption (2 FPGAs!)
- Routing of multiple MGBT signals via (SEA) HD connector
- Signal integrity?



Ideal: Optical data transmission

- Ideally on back of FEM LTCC
- Fire Fly:
  - 12 channels
  - Footprint: 11mm × 22mm
- 2 CoRDIA 1.0 ASICS:
  - Footprint: 25.6mm × ~14mm
  - 16 channels ☹



Current solution(s):

- Bite the bullet
  - Use 2 FPGAs and
  - invest in a good cooling system
- Technology extrapolation
  - Pray for the help of ITRS roadmap and Moore's Law
  - Wait for FPGAs or optical Tx with more links
- "Dumb" RoB with optical Tx

Ideal:

- Anything that integrates data transmission better with other "infrastructures" like
  - Cooling
  - Power supplies
- 2.5D or 3D integration
- MC cooling