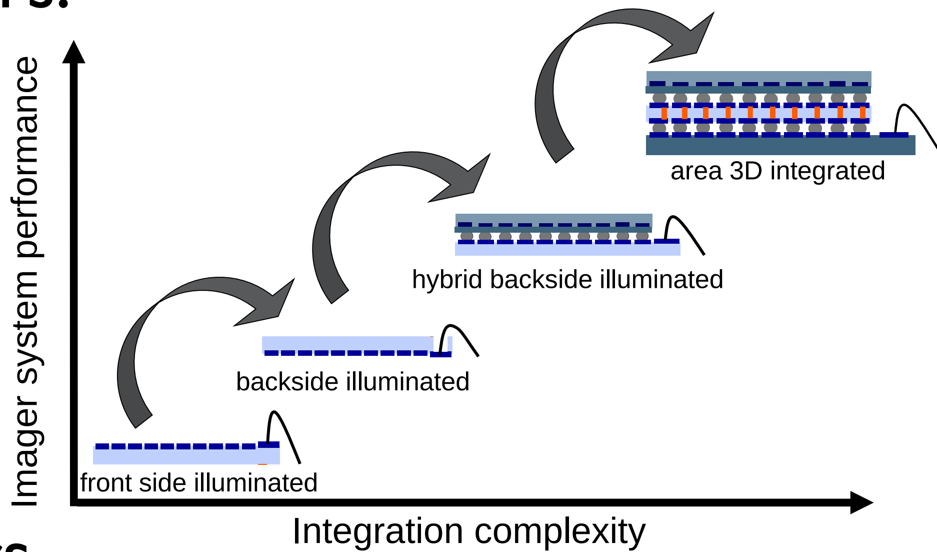
SPECIALTY IMAGERS AT IMEC

PIET DE MOOR

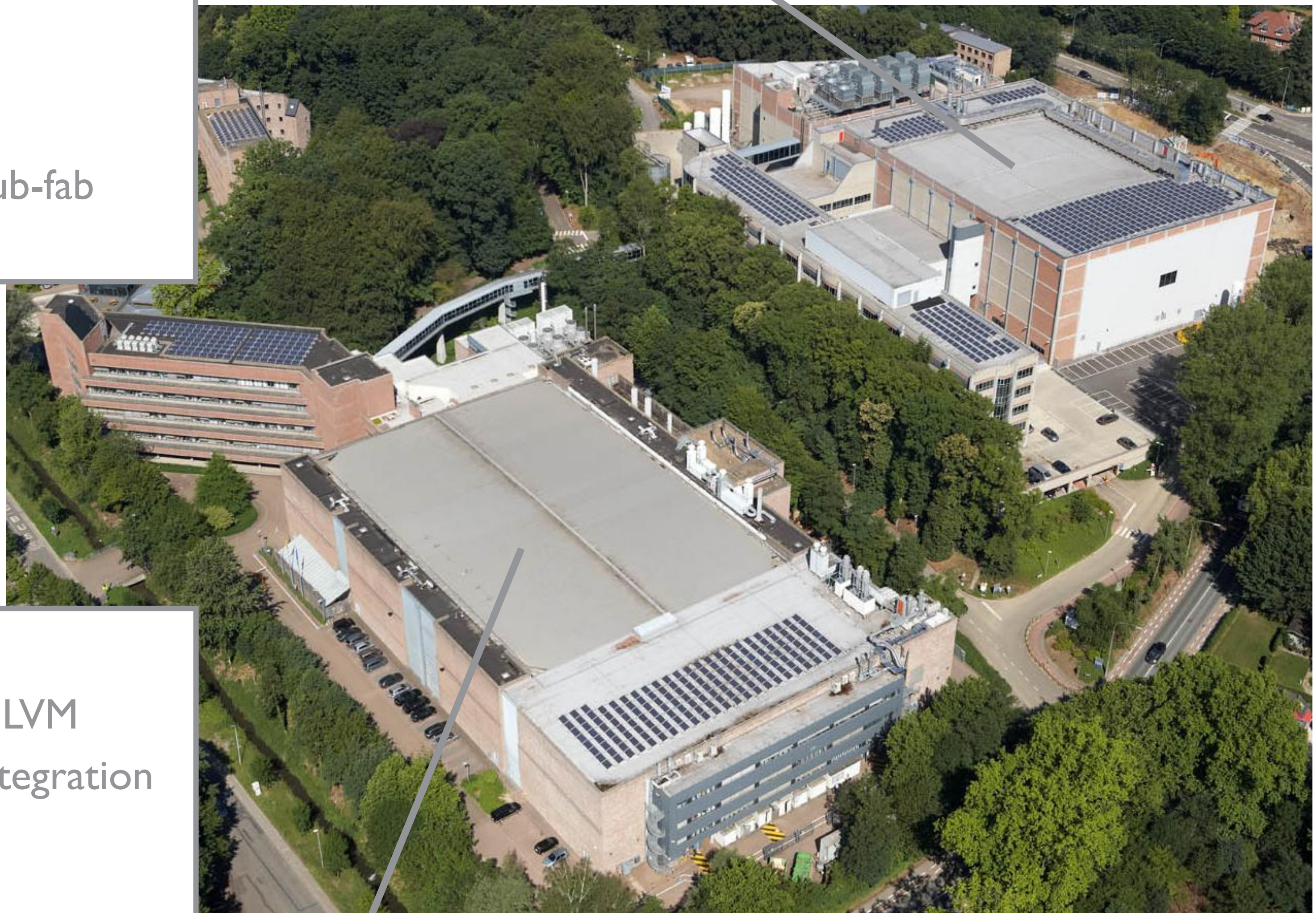
OVERVIEW

- Frontside illuminated imagers:
  - Competences
  - (E)UV detectors
  - 4k2k imager
  - eCCD
  - Hyperspectral imaging
- Backside illuminated imagers
- Hybrid backside illuminated imagers
- 3D stacked imagers
- Applications & imec offering



$10{,}000m^2$ CLEAN ROOM

300mm pilot line
450mm ready
Sub-22nm CMOS
Ball room, clean sub-fab
$3200m^2 + 1200m^2$

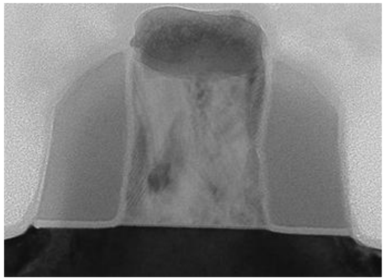


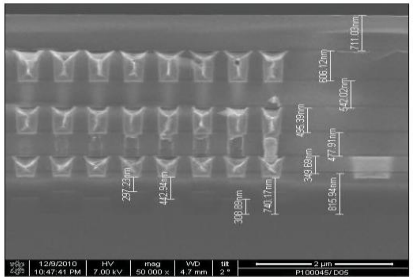
200mm pilot line
R&D, prototyping, LVM
Heterogeneous Integration
CMORE
$4800m^2$

CMOS PLATFORM

200mm Process Technology

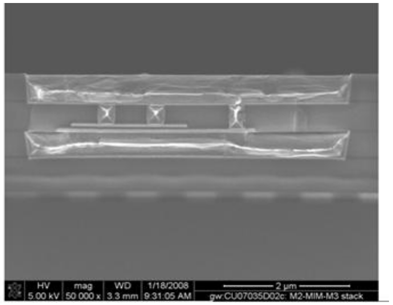
- ✓ 130nm CMOS
- ✓ 1.2V & 3.3V I/O
- ✓ ESD, Analog features (R, MIM,…)
- ✓ PDK and basic design IP available
- ✓ Packaging capabilities

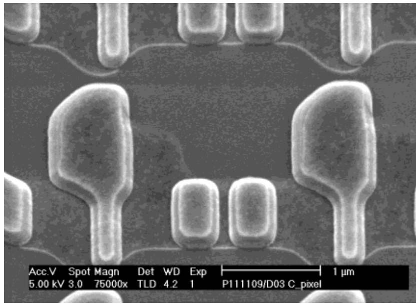




Operations

- ✓ Runs 24/7
- ✓ Trained operator personnel
- ✓ Computer controlled MES:FAB300
- ✓ Contamination control
- ✓ Quality control: SPC, Cp/Cpk
- ✓ Volume: 30.000 lot moves/yr
- ✓ Cycle time controlled
- ✓ QA & low volume production





Engineering

- ✓ High flexibility in process design
- ✓ Calibrated TCAD
- ✓ Test & characterisation
- ✓ Reliability engineering

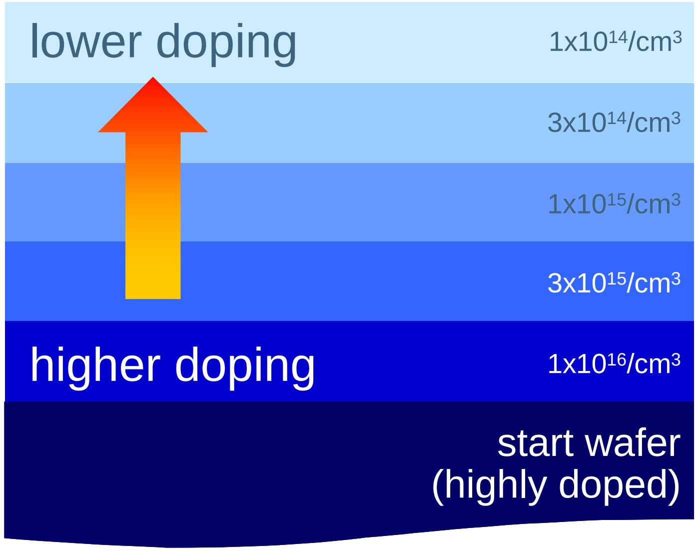
IMEC USP/DIFFERENTIATORS

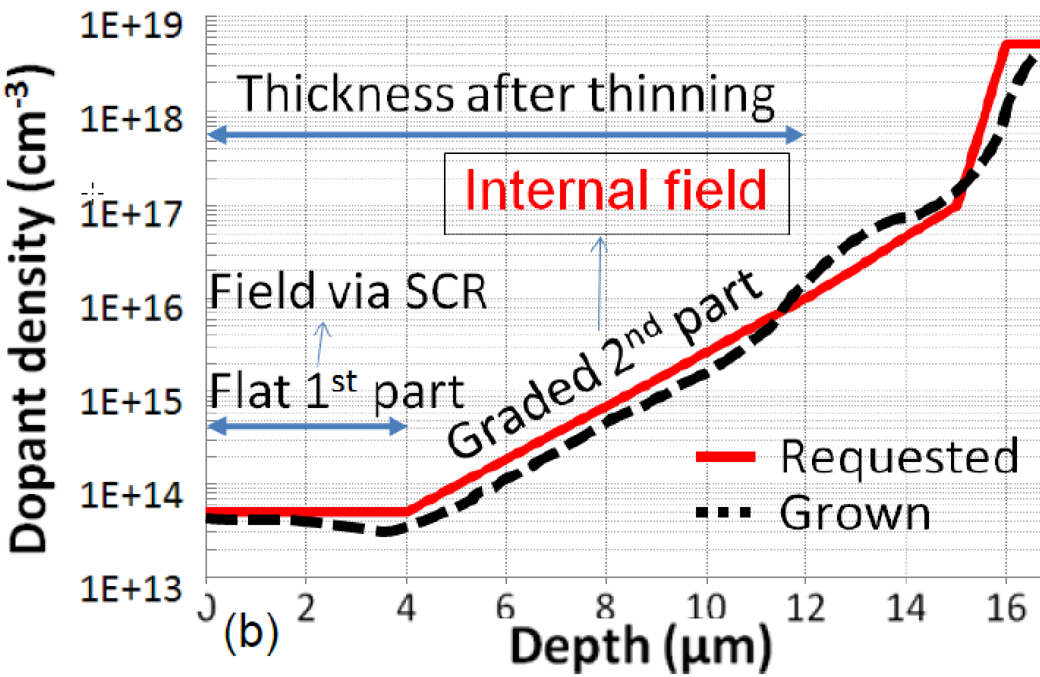
- **Custom technology development**:
  - Adaptations of technology to meet specific requirements
  - Is typical not possible at standard foundries
  - Is required for (some) high-end imagers:
    - E.g. ultra low noise, ultra-fast, non-visible, combination with microfluidics, hyperspectral filters, ...
- **Co-design: close interaction between designers and technology integration**:
  - Is not obvious in fabless design + foundry model (foundry gives no process details)
  - Enables reaching best specifications:
    - E.g. Advanced low noise pixels, use of special epi substrates, ...

SPECIAL SUBSTRATES

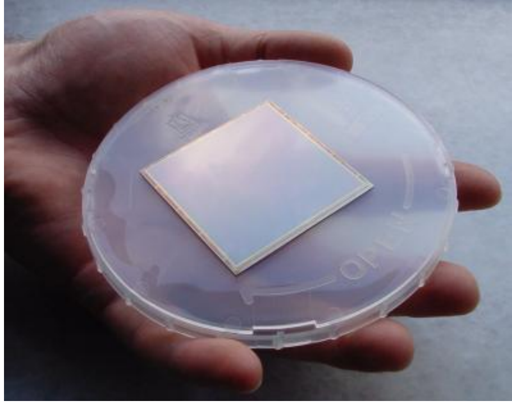
- Epitaxial layers:
  - Thick:
    - Up to 50 um demonstrated
    - For enhanced red response
  - Graded dopant concentration
    - For directional carrier transport

    = lower cross-talk
- High resistivity substrates:
  - Both n and p-type
  - Resistivity > 1kOhm.cm
  - Solution for chucking in imec fab
- Application: fully depleted imagers for low cross-talk and X-ray direct detection

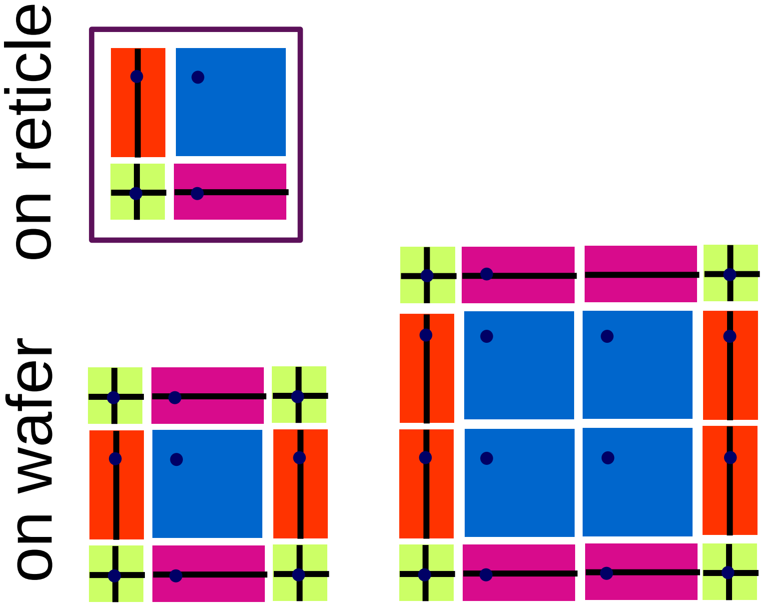


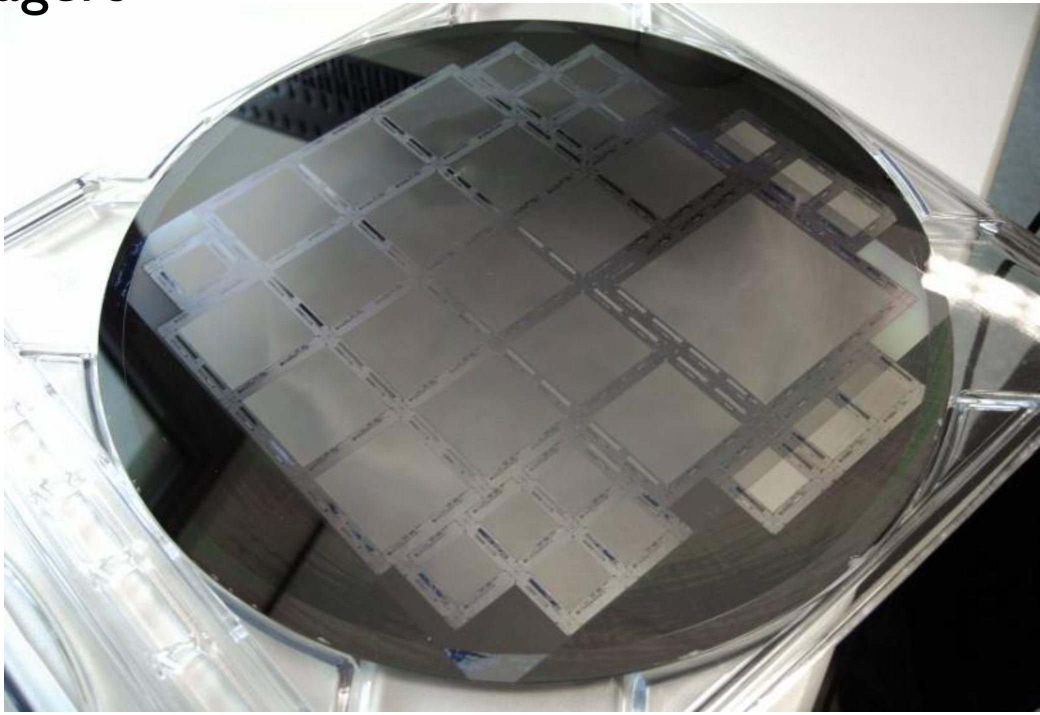


STITCHING

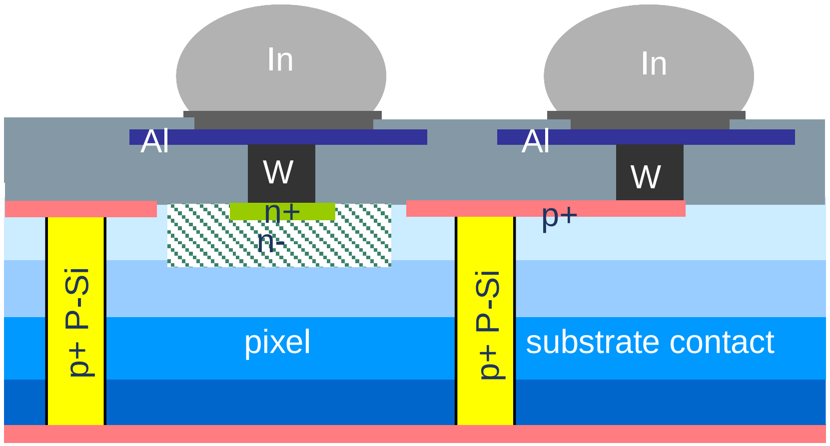


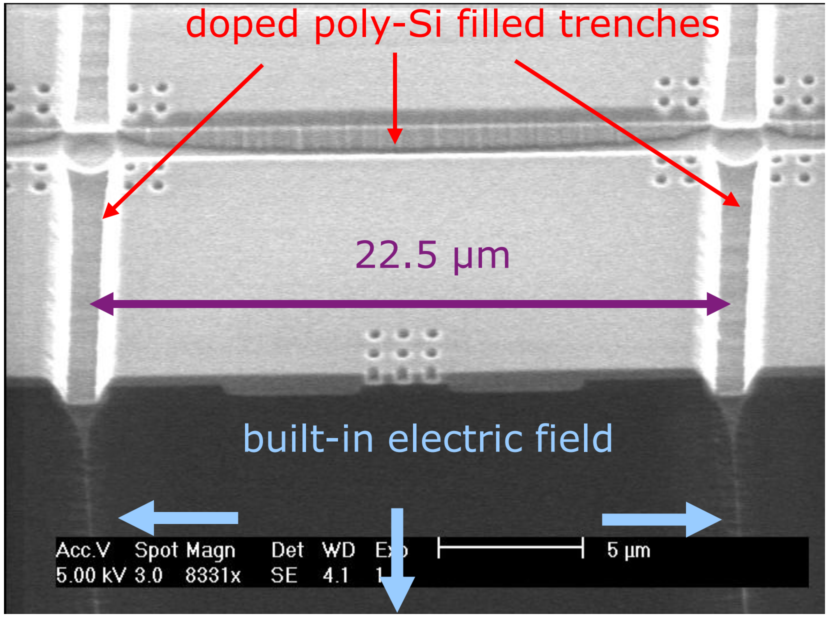
- Stitching allows large area imagers:
  - Up to 1 imager per wafer
- Different imager sizes on one wafer demonstrated:
  - $12x12\ mm^2$, $25x25\ mm^2$ and $50x50\ mm^2$
- Application: e.g. large are imagers





TRENCH ISOLATION BETWEEN PIXELS



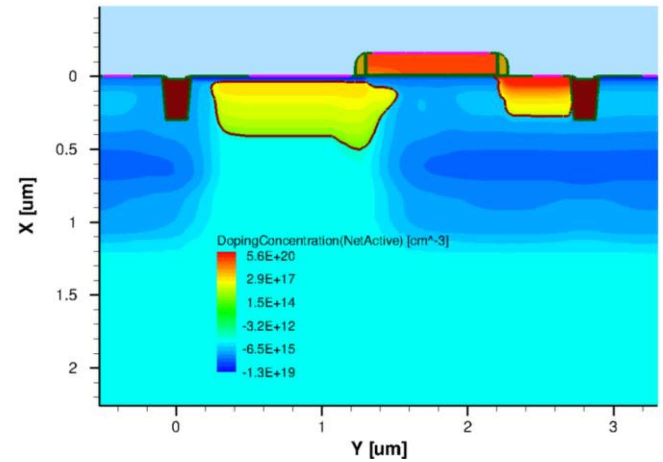


- Doped poly-Si filled trenches for cross-talk reduction: cross-talk due to diffusion of charges eliminated
- Cross-talk reduced to zero
- Lower QE due to recombination at trench sidewall

SMALL PIXEL DESIGN:

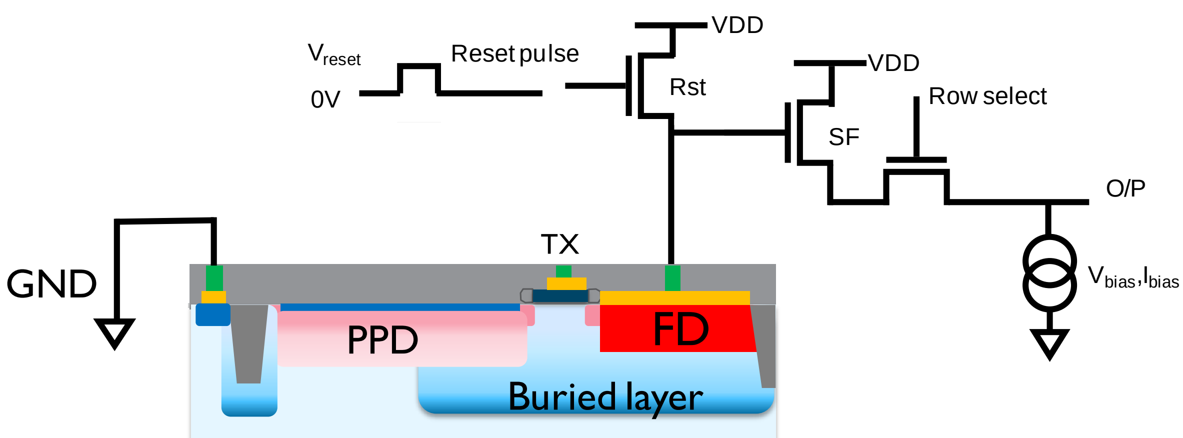
4 Transistor pixel with pinned photodiode:

- ✓ low noise
- ✓ low dark current
- ✓ correlated double sampling compatible
- ✓ shared floating diffusion node

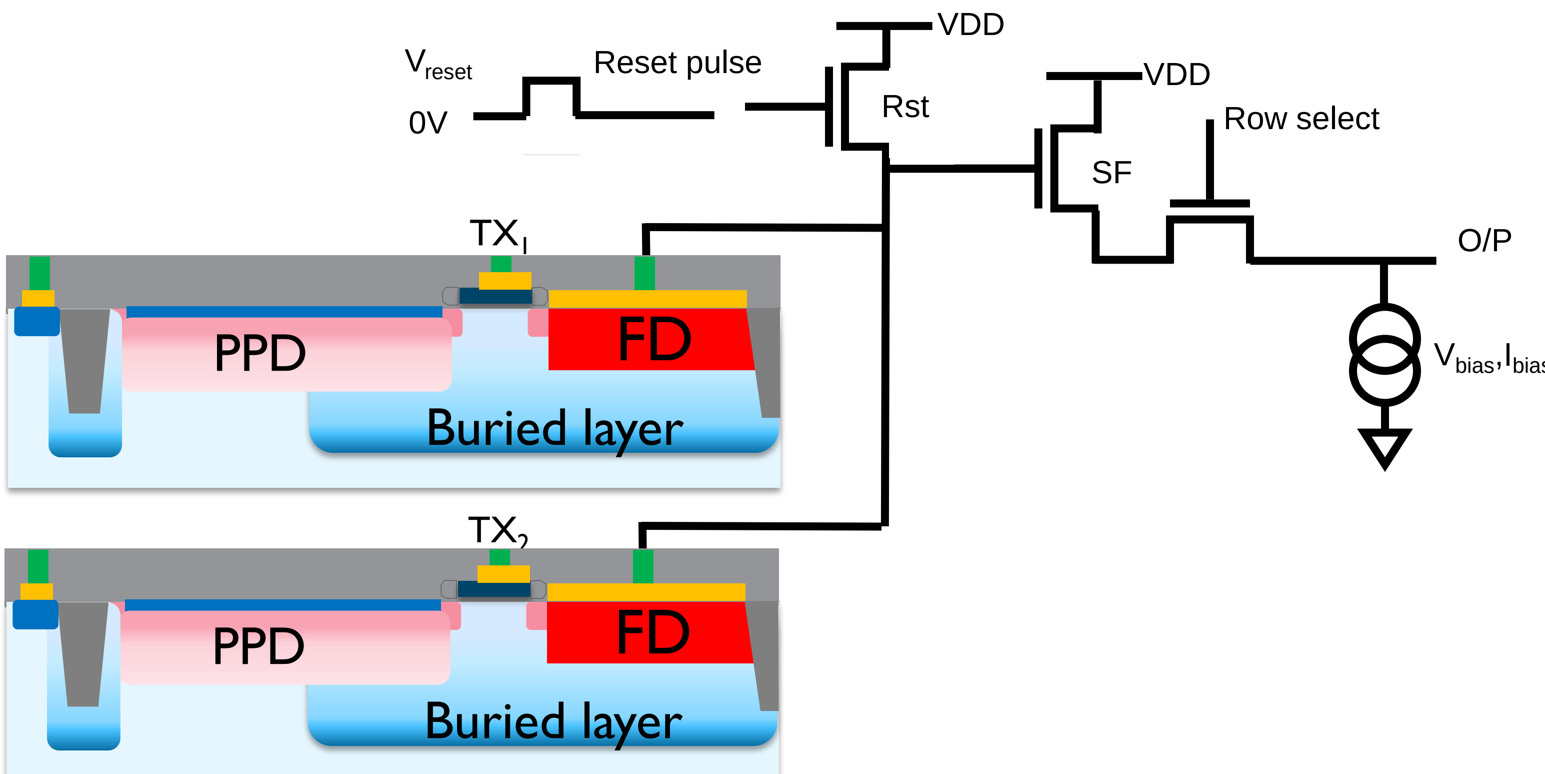


Key technology:

- ✓ custom design and process for:
  - photodiode
  - transfer gate
  - reset and source follower transistors



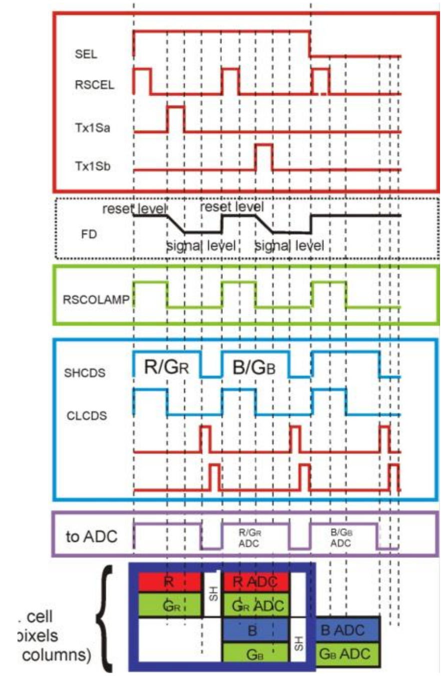
SMALL PIXEL DESIGN:
2.5T PIXEL WITH FD NODE SHARING

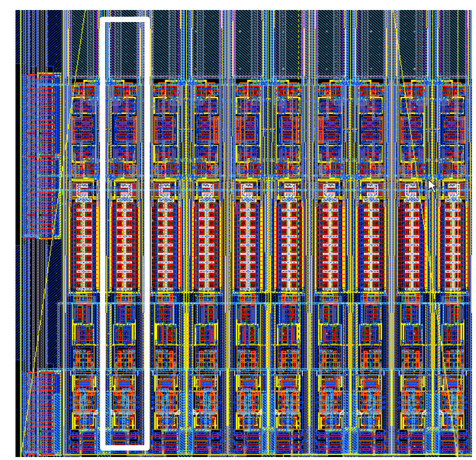


- Shared floating diffusion (FD) node for 2 pixels:
- total # transistors : (2x1T+ 3T)/2 = **2.5 T/pix**

SYSTEM ON A CHIP IMAGERS

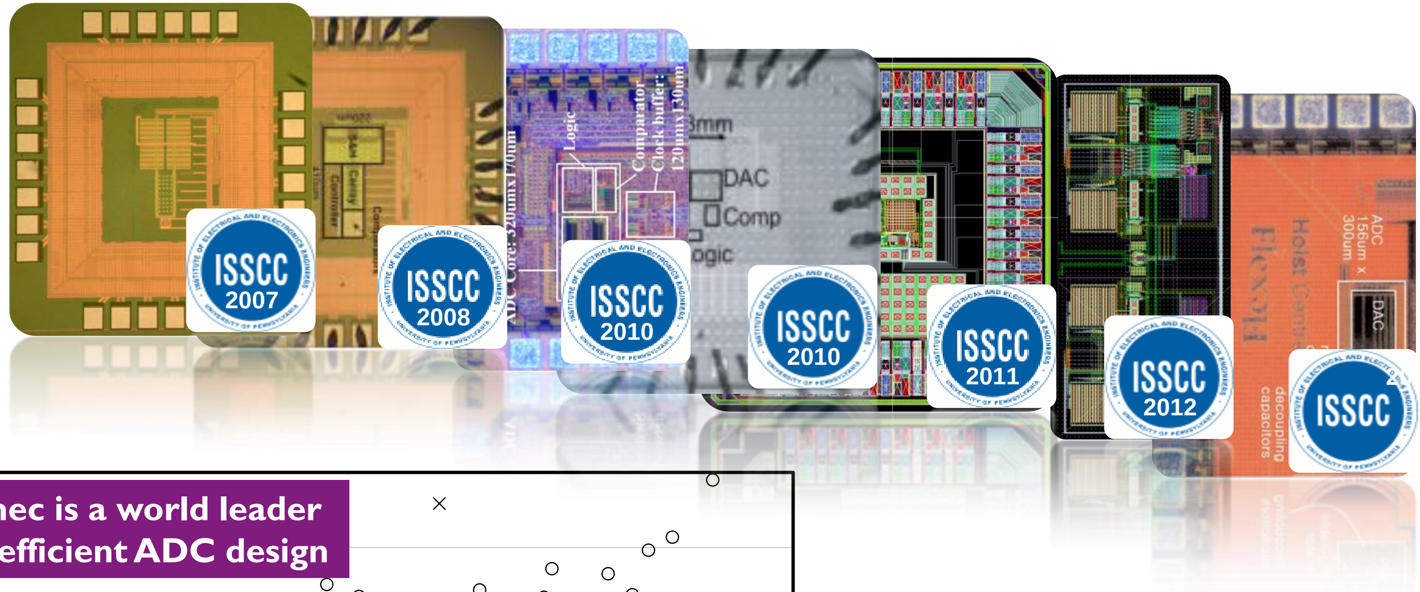
- **Issue**: high-end imagers require complex & fast read-out circuitry:
  - CCD technology cannot integrate complex readout circuit
- **Solution**: CMOS System on a chip imager
- Imec analog and digital **design know-how**:
  - column based fast and low power analog to digital converter

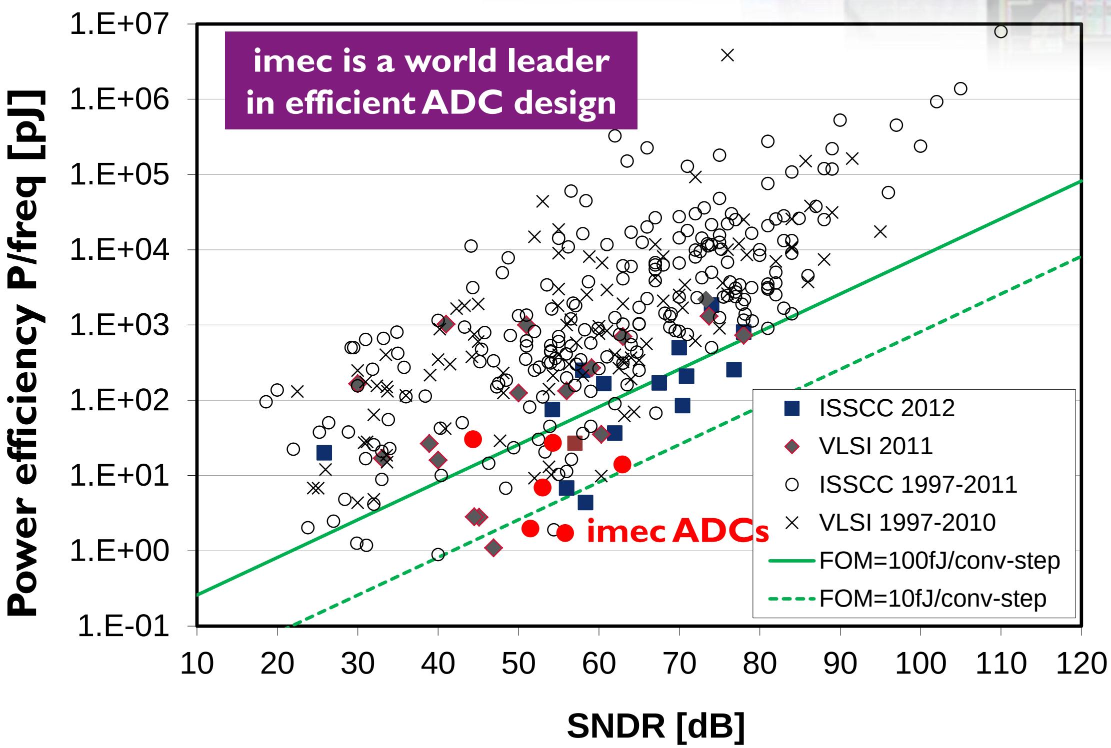




IMEC ADC EXPERTISE

8-12b
4-250MS/s
ADCs





- Low power consumption
- High speed
- High dynamic range

RADIATION HARD DESIGN @ IMEC

- DARE: Radiation-hardened-by-design libraries in standard commercial technology:
  - Developed & enhanced in ESA projects
  - Use = free for European space industry & institutes
  - Library of mixed signal & digital design blocks:
    - DARE180 well supported (UMC 0.18 um CMOS)
    - DARE90 small core & IO library available (UMC 90nm CMOS)
    - XFAB .18 XH started
- Applications: space, high energy physics

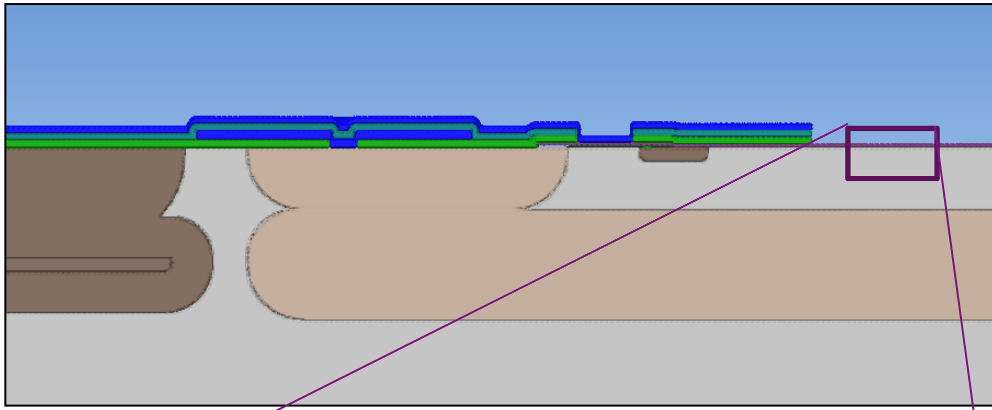
esa

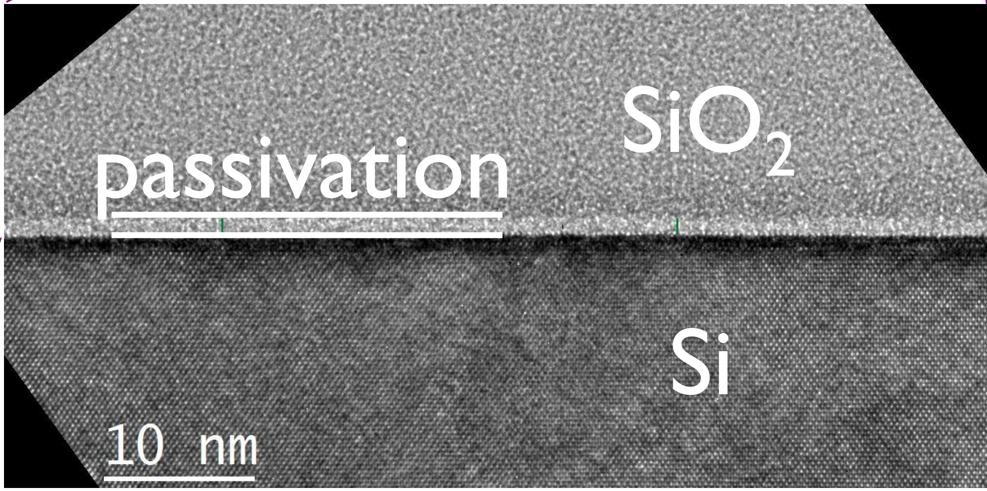
Design
Against
Radiation
Effects

EUROPRACTICE
IC SERVICE

(E)UV DETECTORS

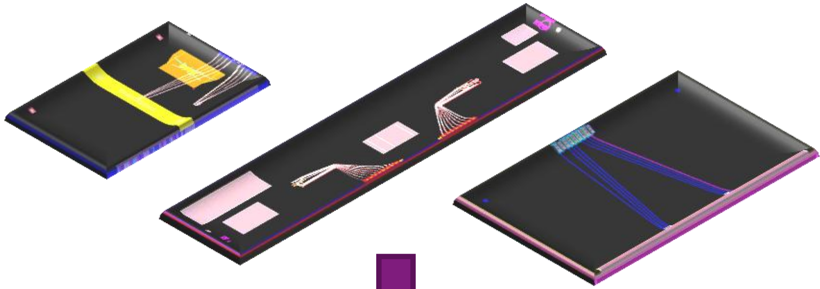
- Direct detection of 13.5 nm (E)UV photons:
  - Single pixels of ~ 1 cm^2
- Dedicated process and design of photodiode:
  - Buried contact
  - Few nm thin Boron surface passivation

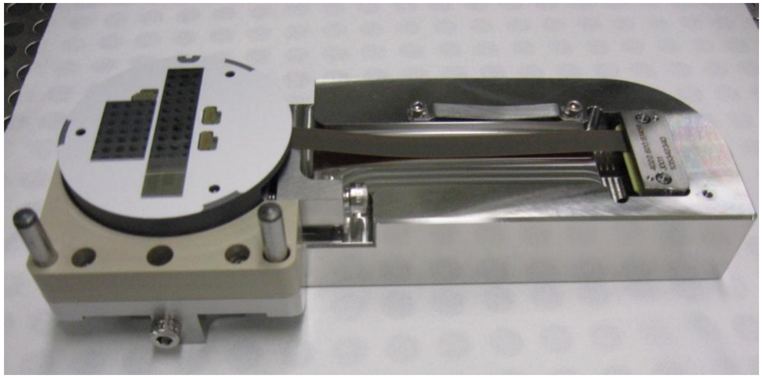




(E)UV DETECTORS

- Application:
  - ASML (E)UV litography tools
- Example of CMORE project:
  - Development-on-demand in 2011
  - Low volume production in 2012: 200 qualified detectors shipped

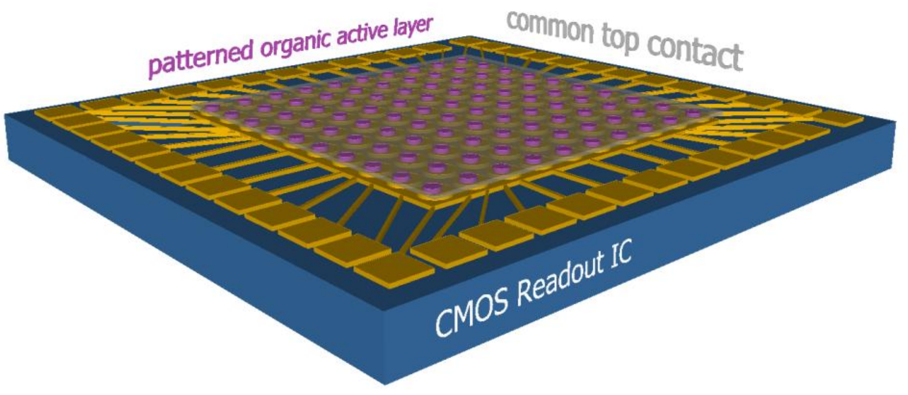




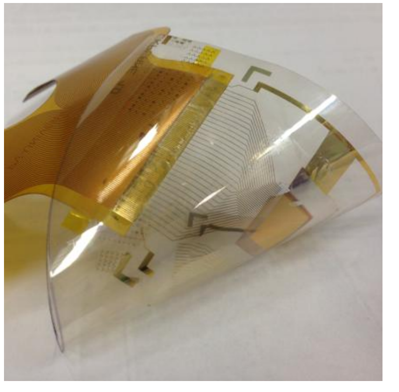
ORGANIC IMAGERS

- Concept:
  - Manufacturing of photodiodes based on organic materials (i.e. non-Si)
  - Two possible routes for integration:

organic imager on Si readout



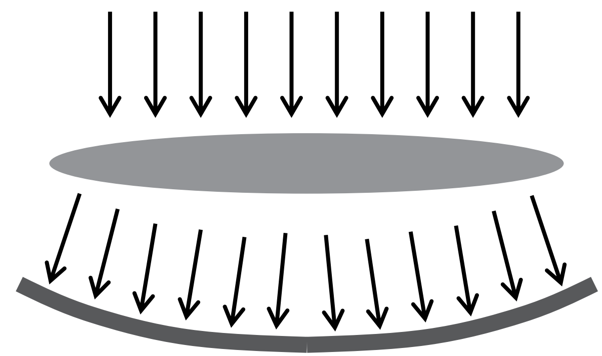
organic imager on foil



- Challenges:
  - Process development
  - Dark current

ORGANIC IMAGERS

- Advantages:
  - Fabrication of active imagers/circuits possible on different (non-planar) non-Si substrates:
    - E.g. **curved/flexible substrates** (e.g. lenses, ...) for much simpler optics
    - Large area/low weight applications



  - High absorption coefficients:
    - Visible + **near infrared**
    - Thin active layer, hence low crosstalk (as compared to Si in red)

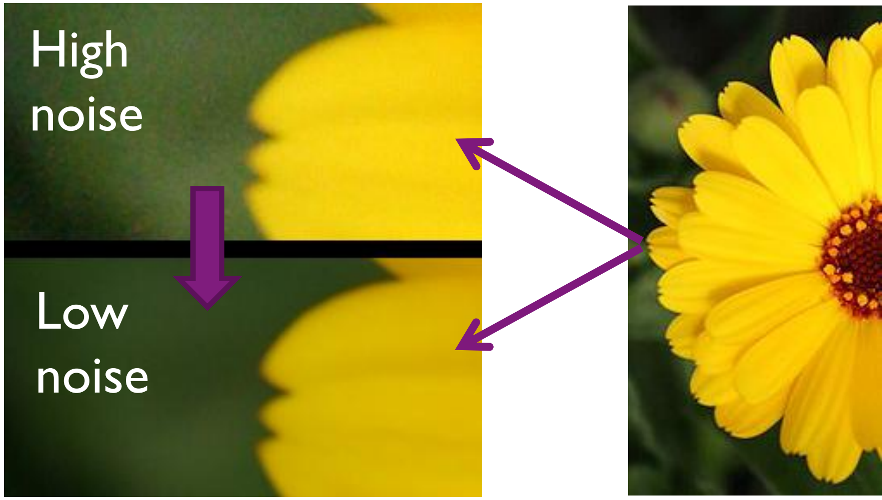
CCD VERSUS CMOS COMPARISON

Parameter	CCD	CMOS
Noise	Very low	Higher
Dark current	Extreme low	Higher
Pixel-to-pixel variation (FPN)	Very low	Higher
Electronics integration (SoC)	Not possible	Possible
Power consumption	High	Very low

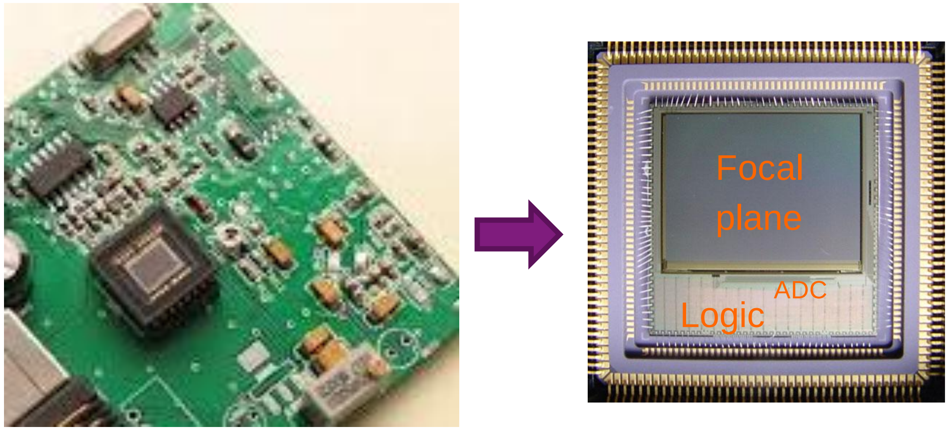
- embedded CCD in CMOS combines best of two worlds

EMBEDDED CCD = CCD + CMOS: BEST OF 2 WORLDS

- **CCD:**
  - ultimate low noise & dark current

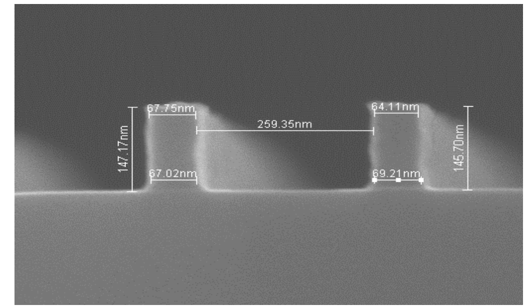


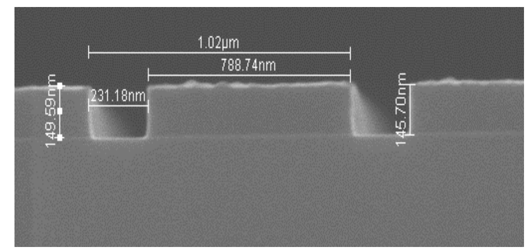
- **CMOS:**
  - system on a chip integration

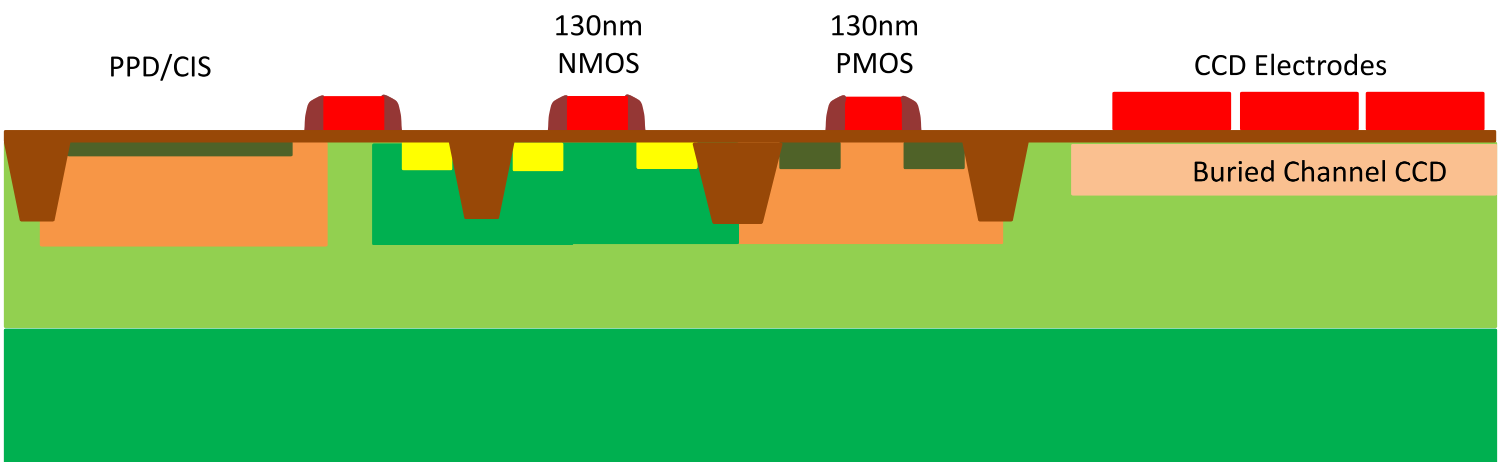


ECCD TECHNOLOGY

- extra module added to imec's 0.13 um CIS/CMOS platform
- CCD pixels:
  - single poly with very narrow gaps for optimal charge transfer
  - leveraging 193nm photo & double patterning

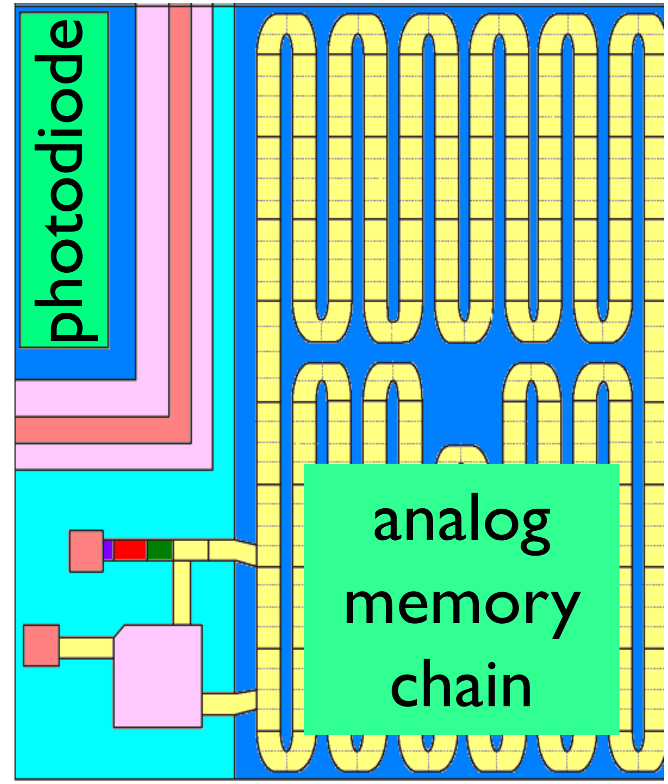




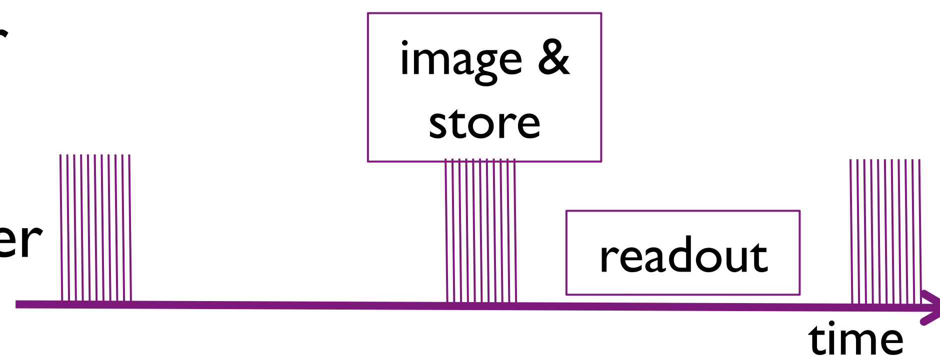


ULTRA FAST IMAGING: USING ECCD

- Design solution:
  - in pixel memories
  - = store a (limited) number of frames inside pixel
  - readout at lower speed
  - allows burst mode of imaging
- embedded CCD:
  - noiseless storage and transfer
- CMOS:
  - Fast & low power data transfer off-chip, ADC's, ...

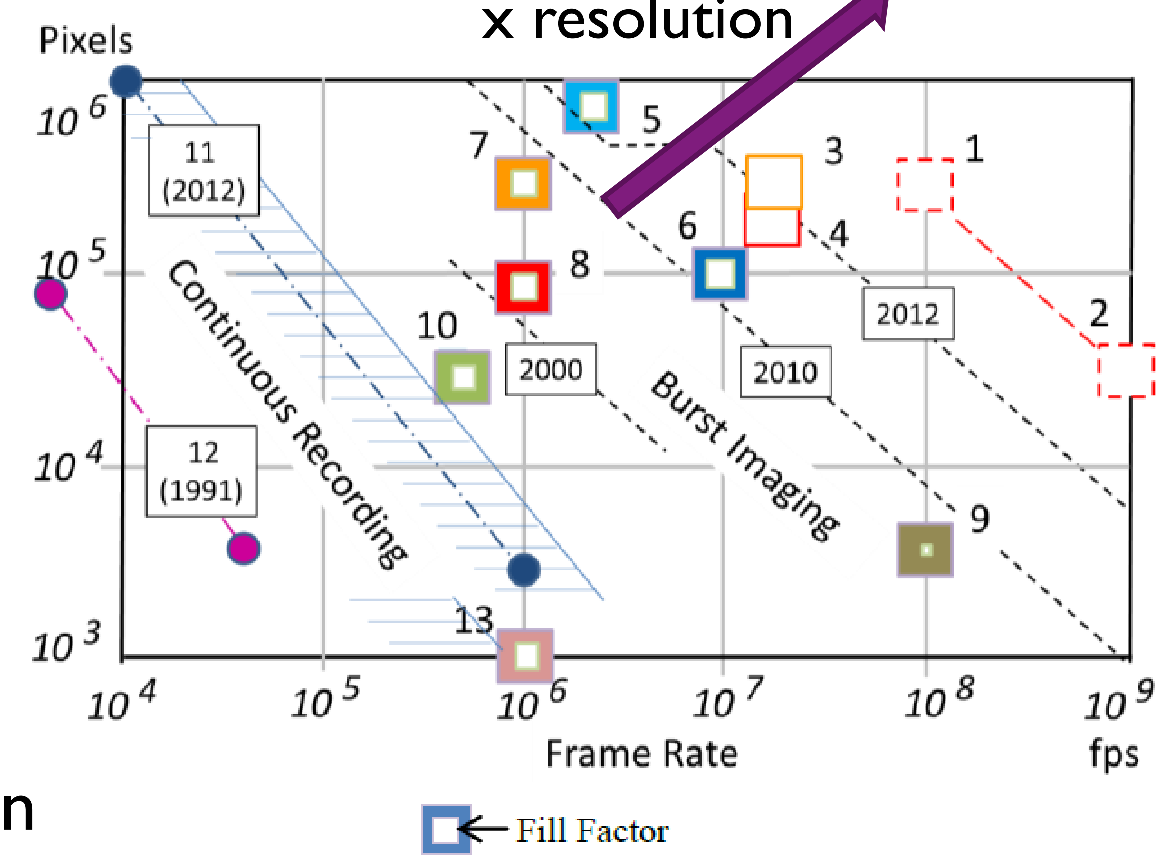


Source: G. Etoh



ISAS ECCD IMAGER: ULTRA FAST IMAGING

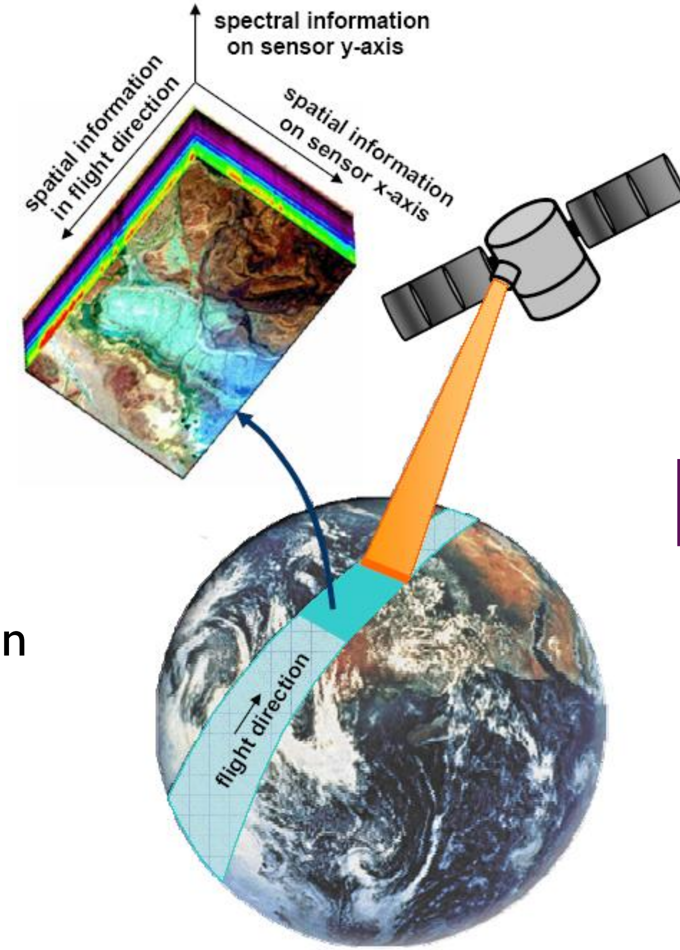
- Specifications:
  - 480 × 640
  - pixel pitch ~ 30 um
  - **4.000.000 fps**
  - ~100 in-pixel **CCD** Memory Element: **~1.5um × 3 um**
  - **Backside thinned**
  - **Dedicated epi**
- Application: neutron camera for JPARC (Japan High energy physics)

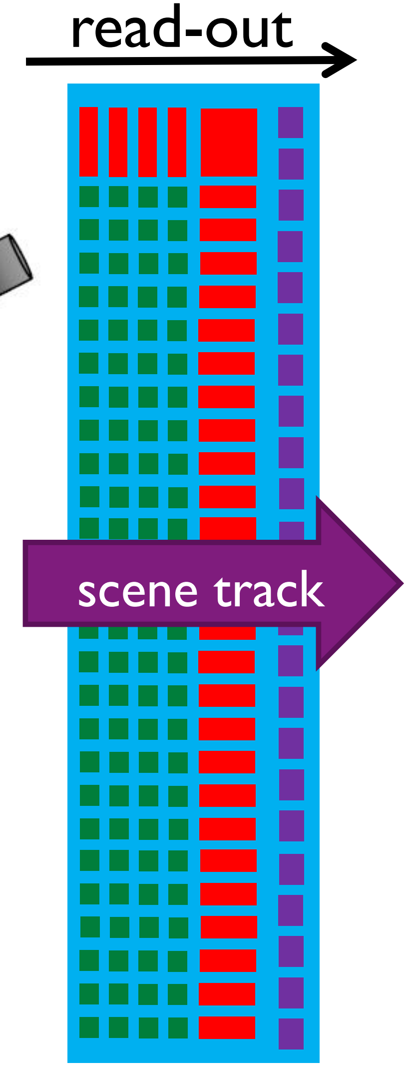


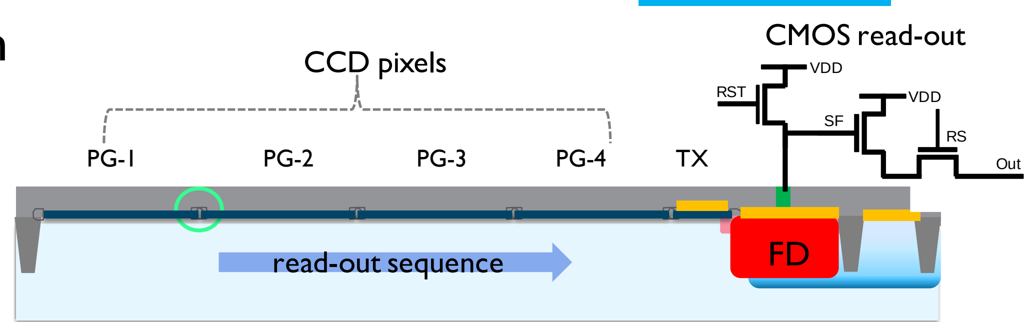
G. Etoh, Dao V.T. Son, T. Yamada and E. Charbon, Sensors 2013, 13, 4640-4658

ECCD TDI

- Time delayed imaging:
  - = synchronized read-out:
  - N times (time delayed) integration of same signal
  - Signal/Noise gain ~ √N
- eCCD approach:
  - TDI CCD pixels: integration in time domain → low noise
  - CMOS column readout → high speed, low power
- Applications:
  - high resolution Earth observation in multiple spectral bands
  - industrial inspection

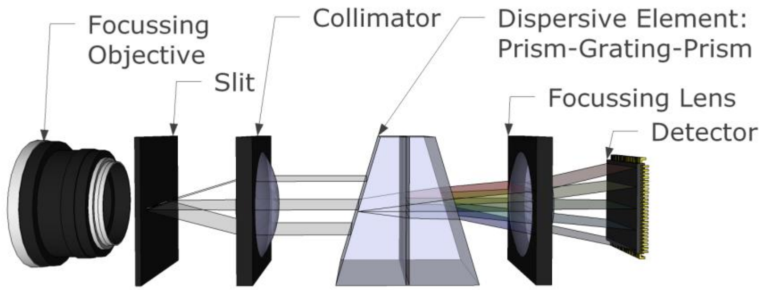


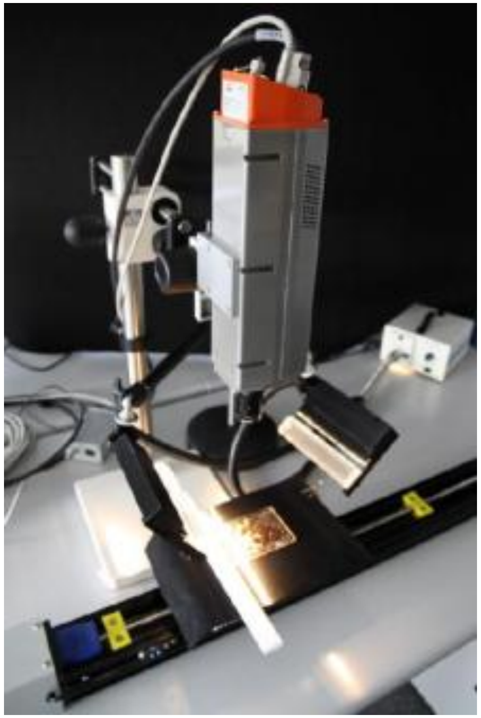




HYPERSPECTRAL IMAGING

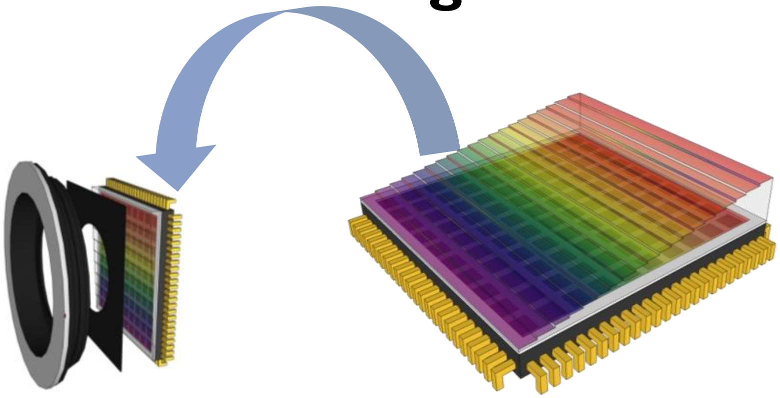
- State-of-the-art:
  - Imager + grating/prism

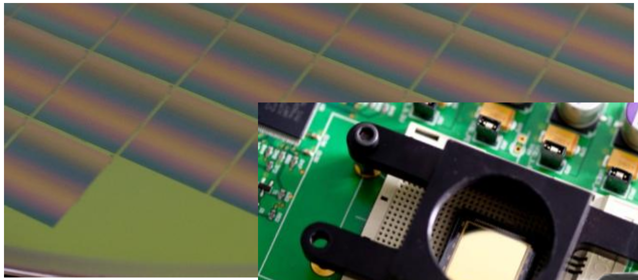


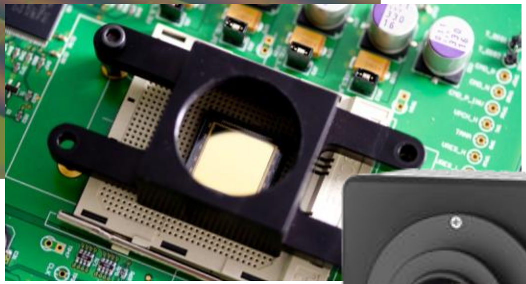


Imec solution:

- **Wafer level filter integration**





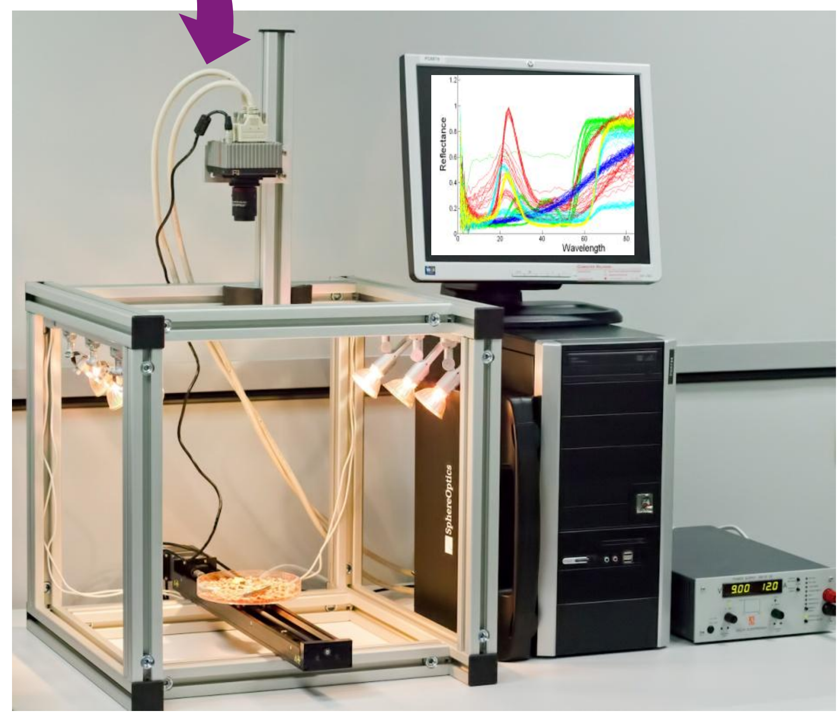


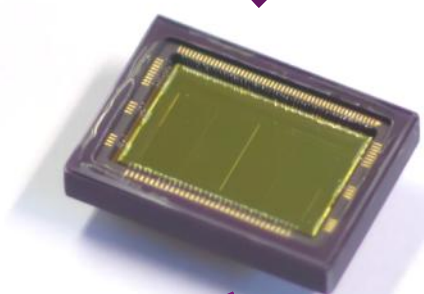
Advantages:

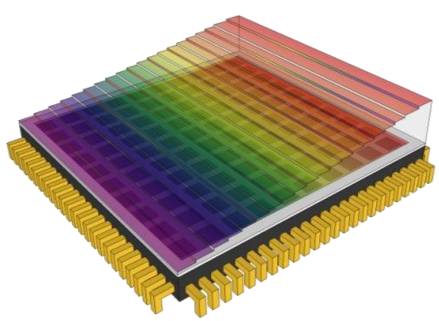
- Extreme miniaturization
- Low cost
- Design optimization possible

HYPERSPECTRAL IMAGING: LINESCAN HSI CAMERA SYSTEM

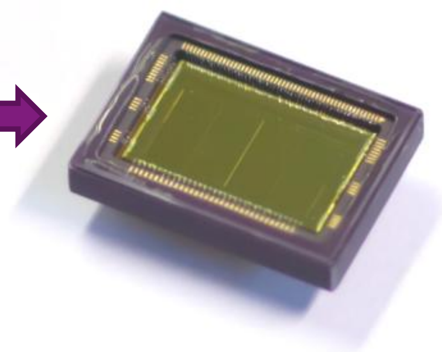
- HSI linescan evaluation system:
  - Camera with HSI imager, translation stage, lighting, software

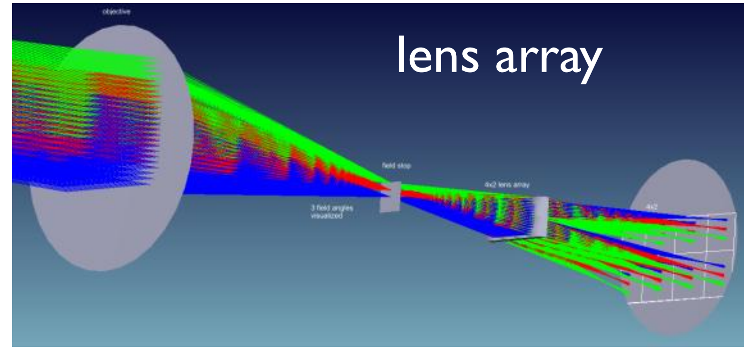


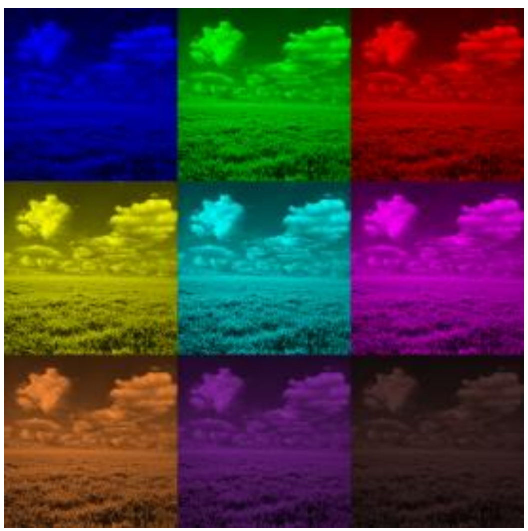




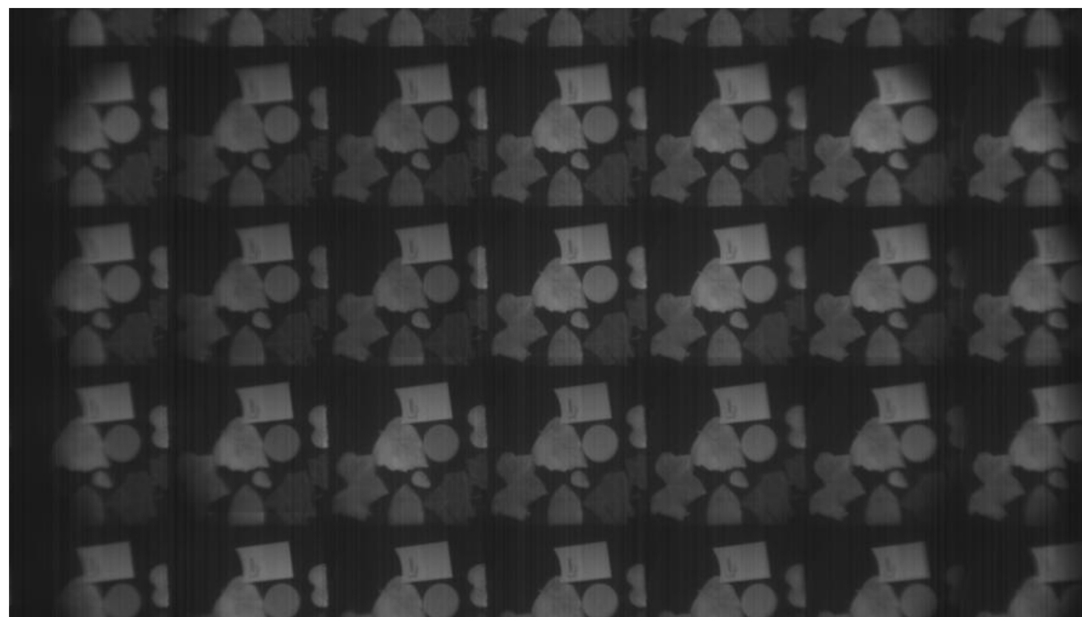
HYPERSPECTRAL IMAGING: HSI VIDEO CAPTURE







Sub-images with hyperspectral filter

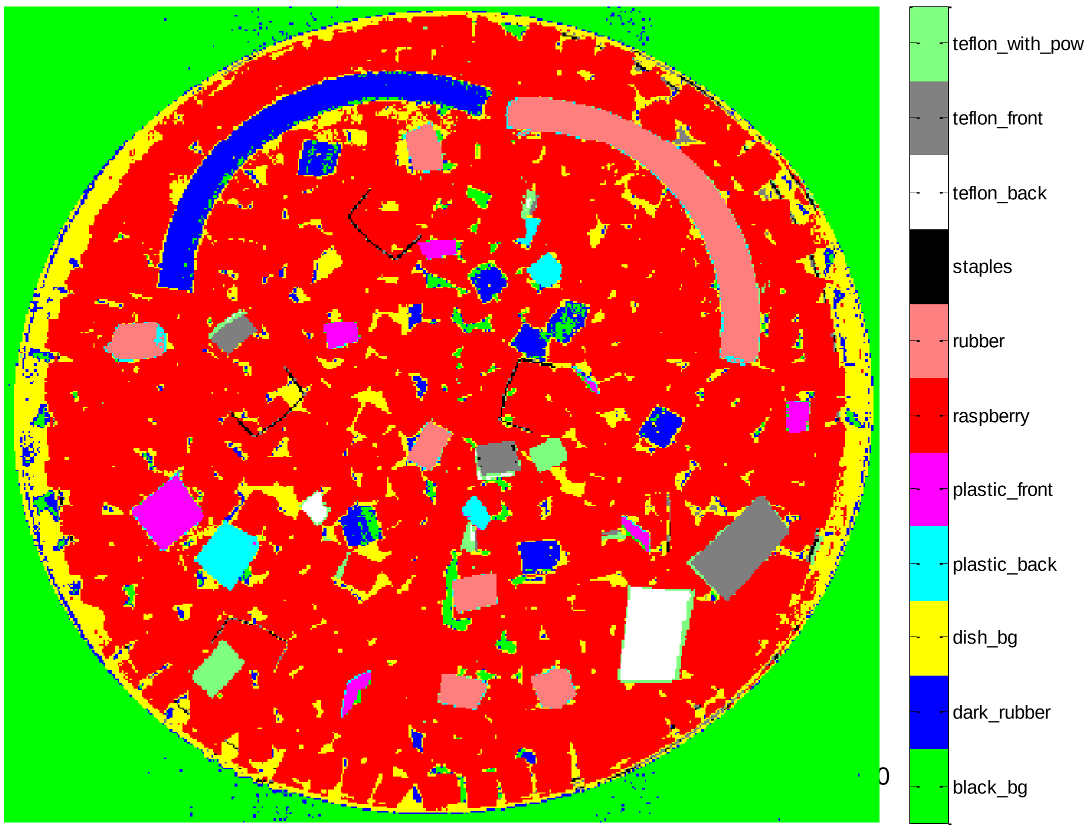


HYPERSPECTRAL IMAGING:
APPLICATION: FOOD INSPECTION

SENSORS FOR FOOD

TAURA NATURAL INGREDIENTS

- TAURA fabricates fruit pieces for the global snack food market
- Hyperspectral imaging allows detection of contaminants

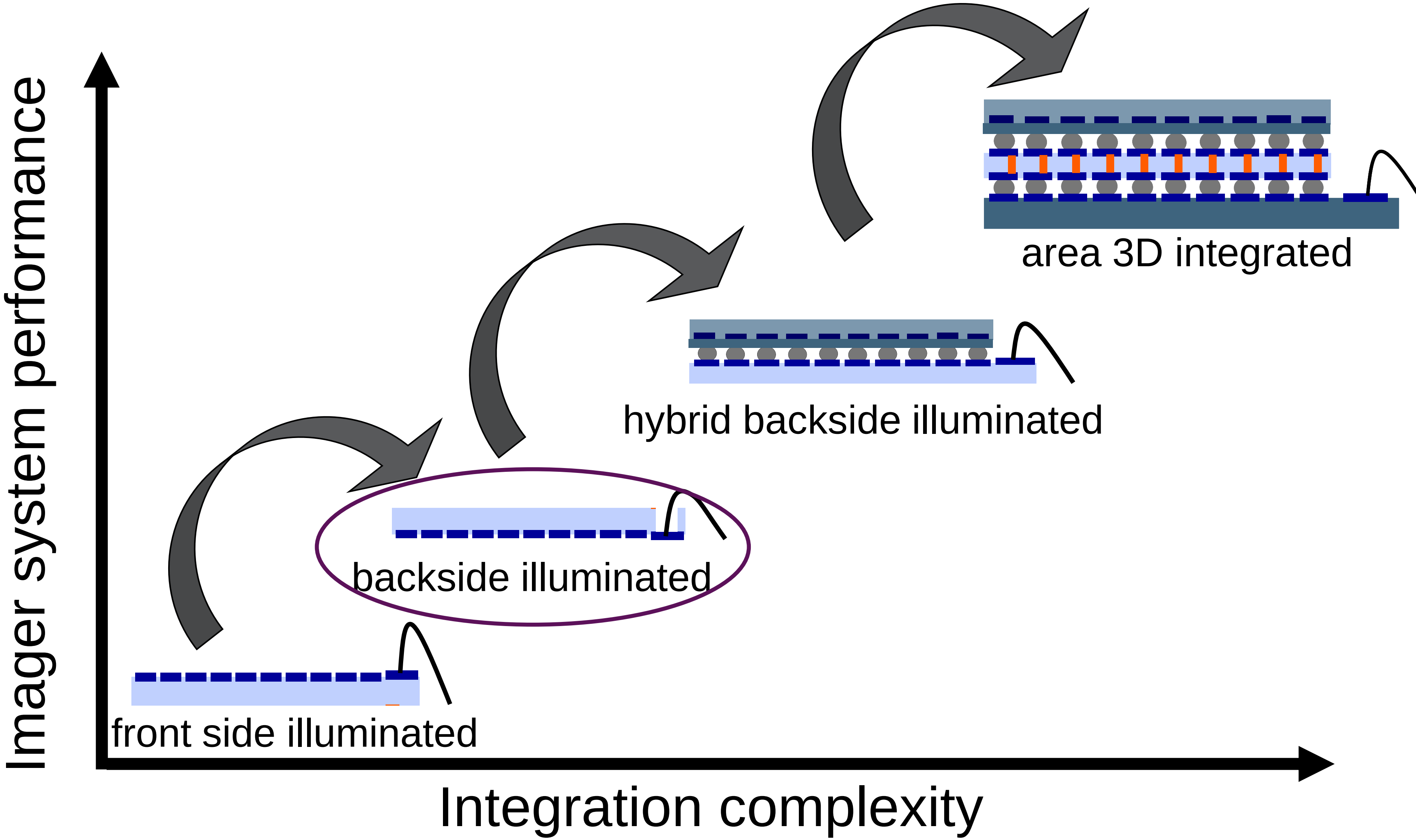


HYPERSPECTRAL IMAGING: APPLICATION: AUTOMATIC WHITE BALANCE

- Optimized white balance correction
- Using hyperspectral pixel signal

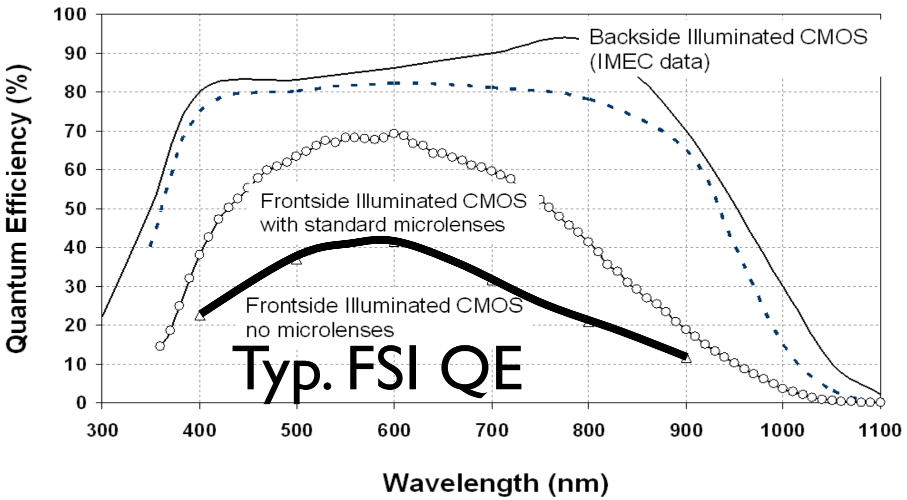
BACKSIDE ILLUMINATED IMAGERS (BSI)

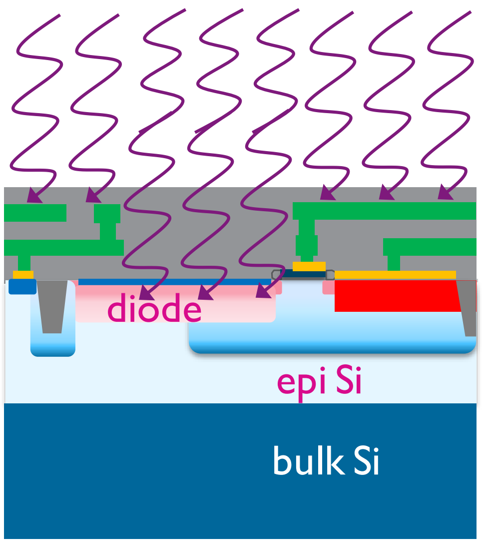
ADVANCED IMAGER INTEGRATION



OPPORTUNITIES & SOLUTIONS: HIGH SENSITIVITY

- front **side illumination** limitations:
  - < 100 % fill factor
  - medium Quantum Efficiency

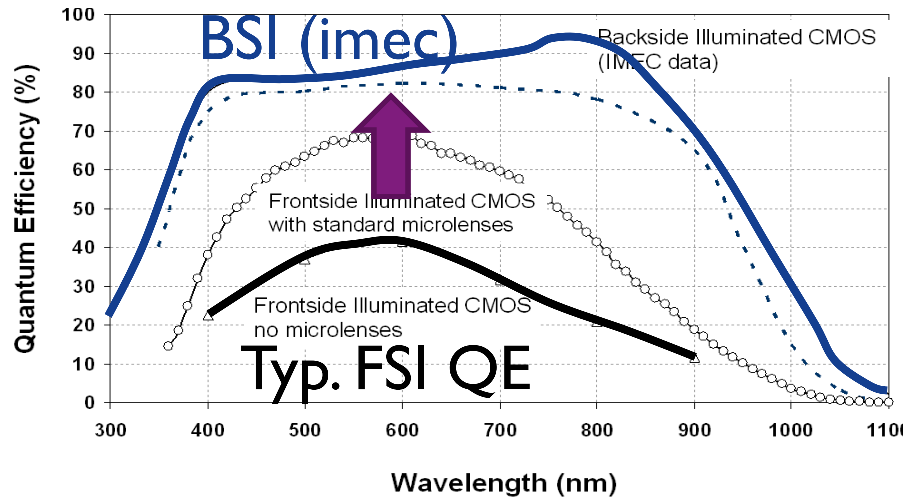


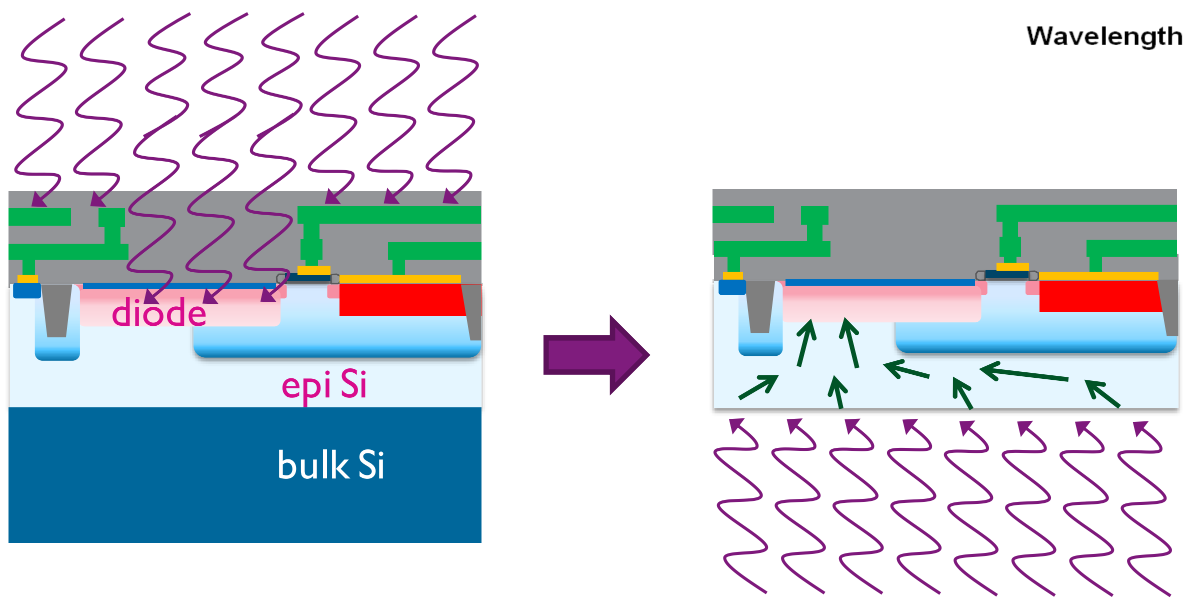


front side illuminated

OPPORTUNITIES & SOLUTIONS: HIGH SENSITIVITY

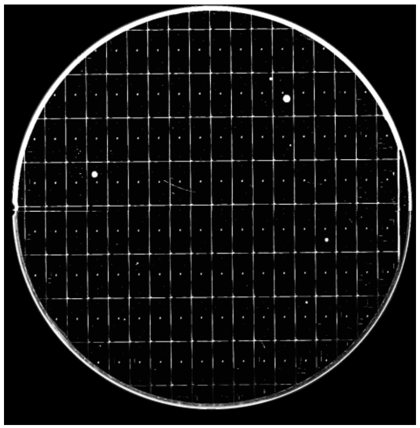
- **backside illumination** enables:
  - 100 % fill factor
  - high Quantum Efficiency (QE)

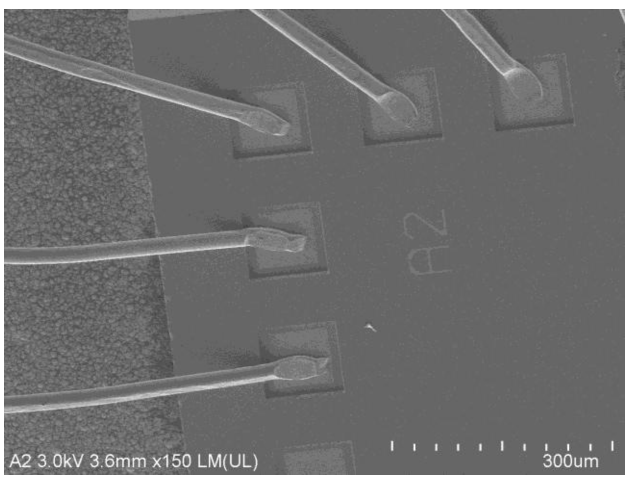


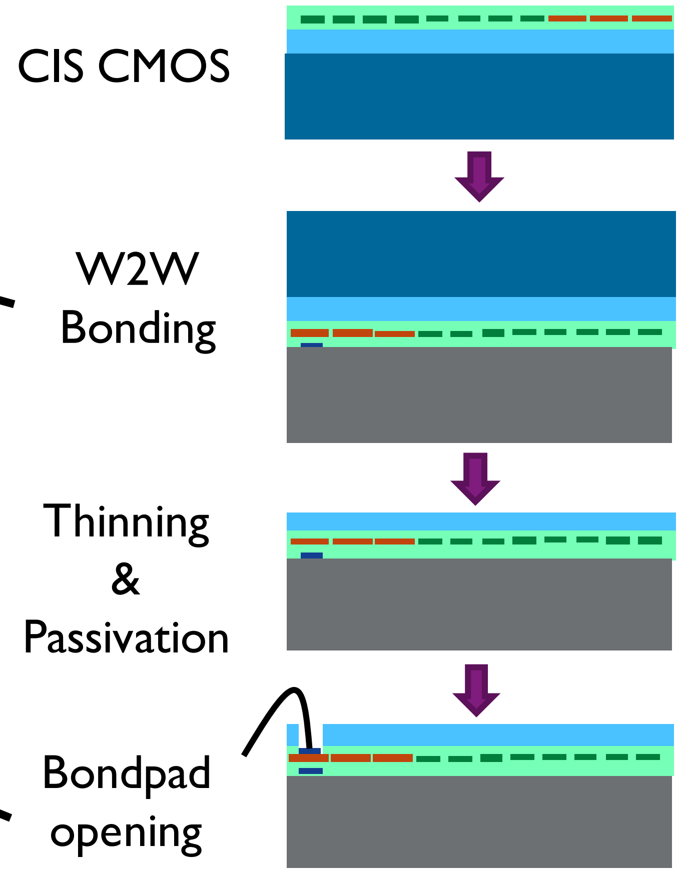


frontside illuminated backside illuminated

IMEC BACKSIDE ILLUMINATED IMAGER PROCESS PLATFORM

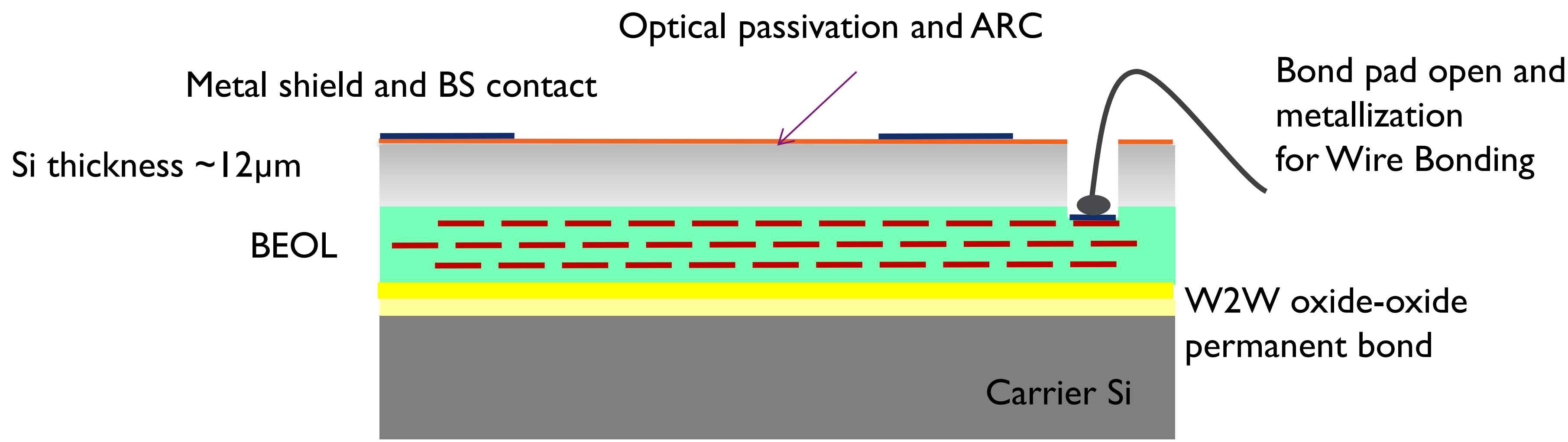






- Investments done, equipment expected ~ Q2 2013

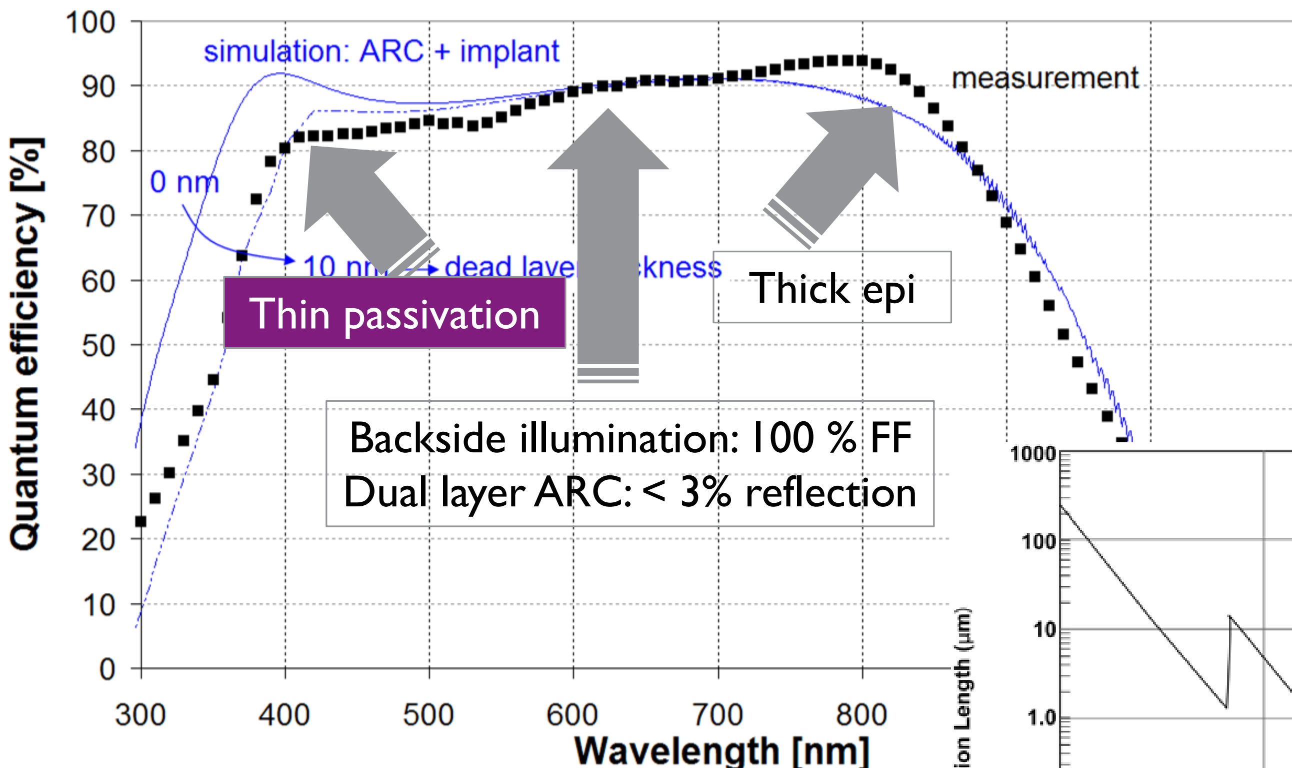
BSI MODULE @ IMEC

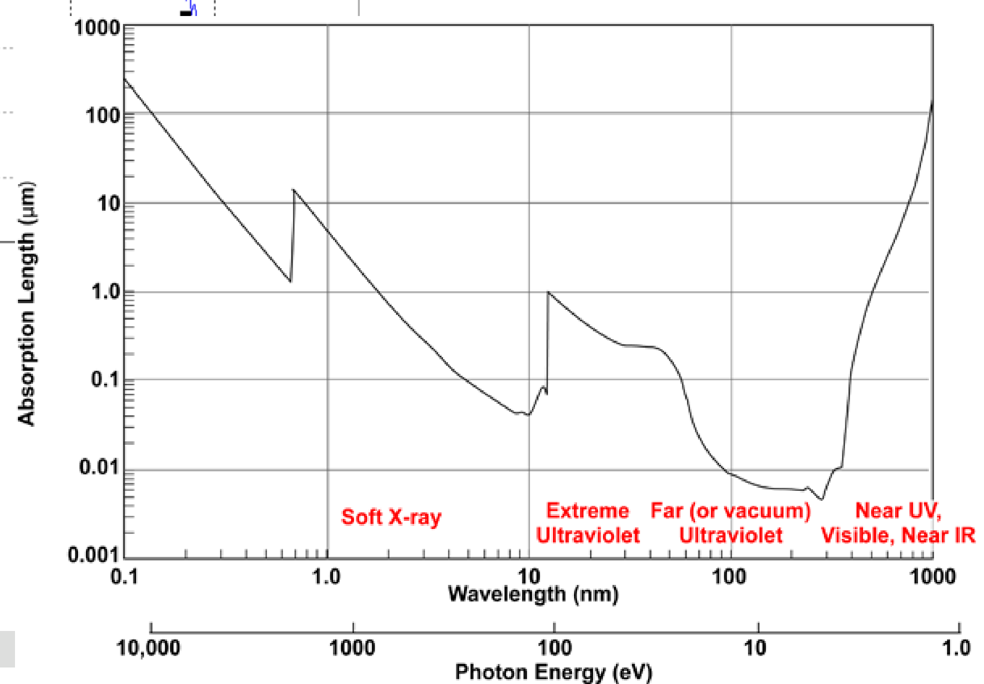


- bulk thinning approach, SOI is possible
  - final thickness & uniformity:
    - in situ measured or selective etch stop
- no TSV but bondpad opening:
  - Etch of Si, insulator deposition & patterning, metallization
- anti-reflective coating (ARC) and backside metal

BACKSIDE ILLUMINATED IMAGERS:
HIGH SENSITIVITY = HIGH QUANTUM EFFICIENCY

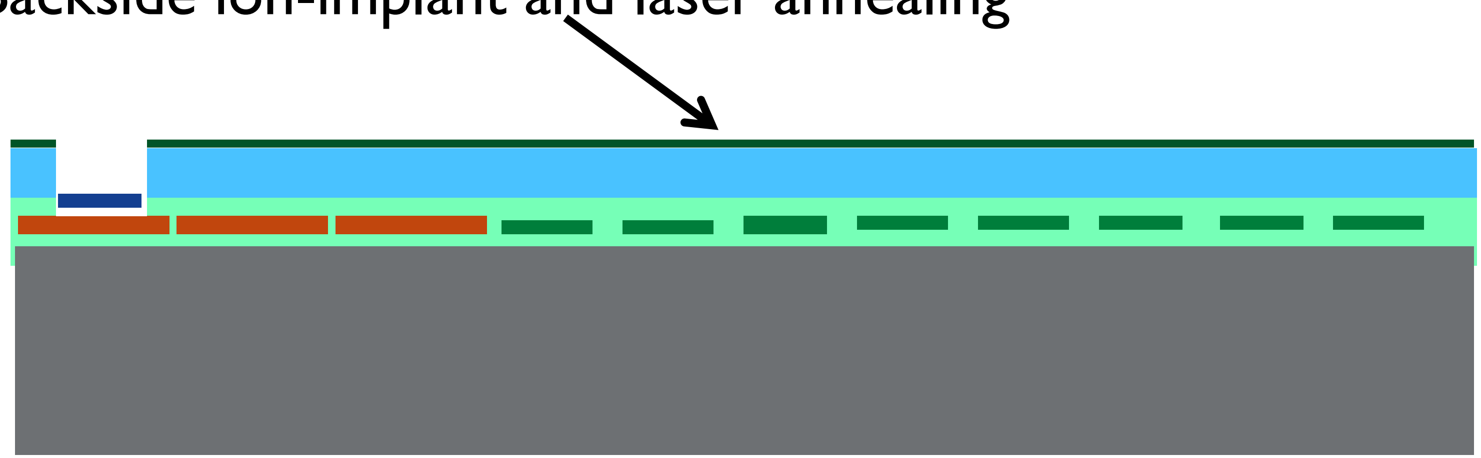
- Excellent broadband QE thanks to:





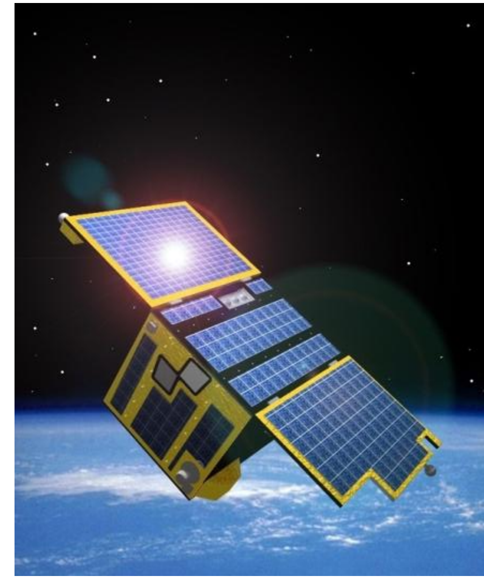
BACKSIDE SURFACE PASSIVATION: PROBLEM AND SOLUTION

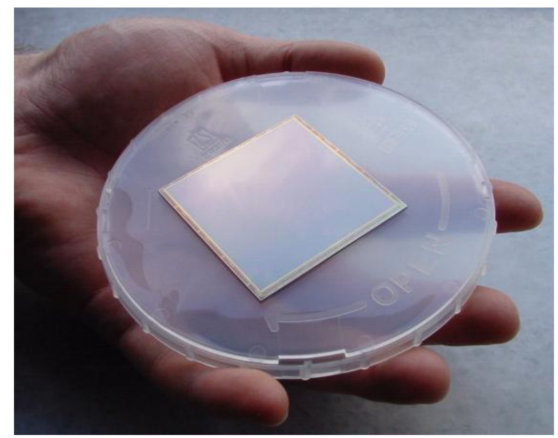
- Problem:
  - Backside interface is low quality: high trap density, potential pockets
  - Impact on imager performance:
    - Reduced quantum efficiency (esp. blue/green)
    - Increased dark current
- Solution: backside surface field:
  - Backside ion-implant and laser annealing



‘EUROCIS’

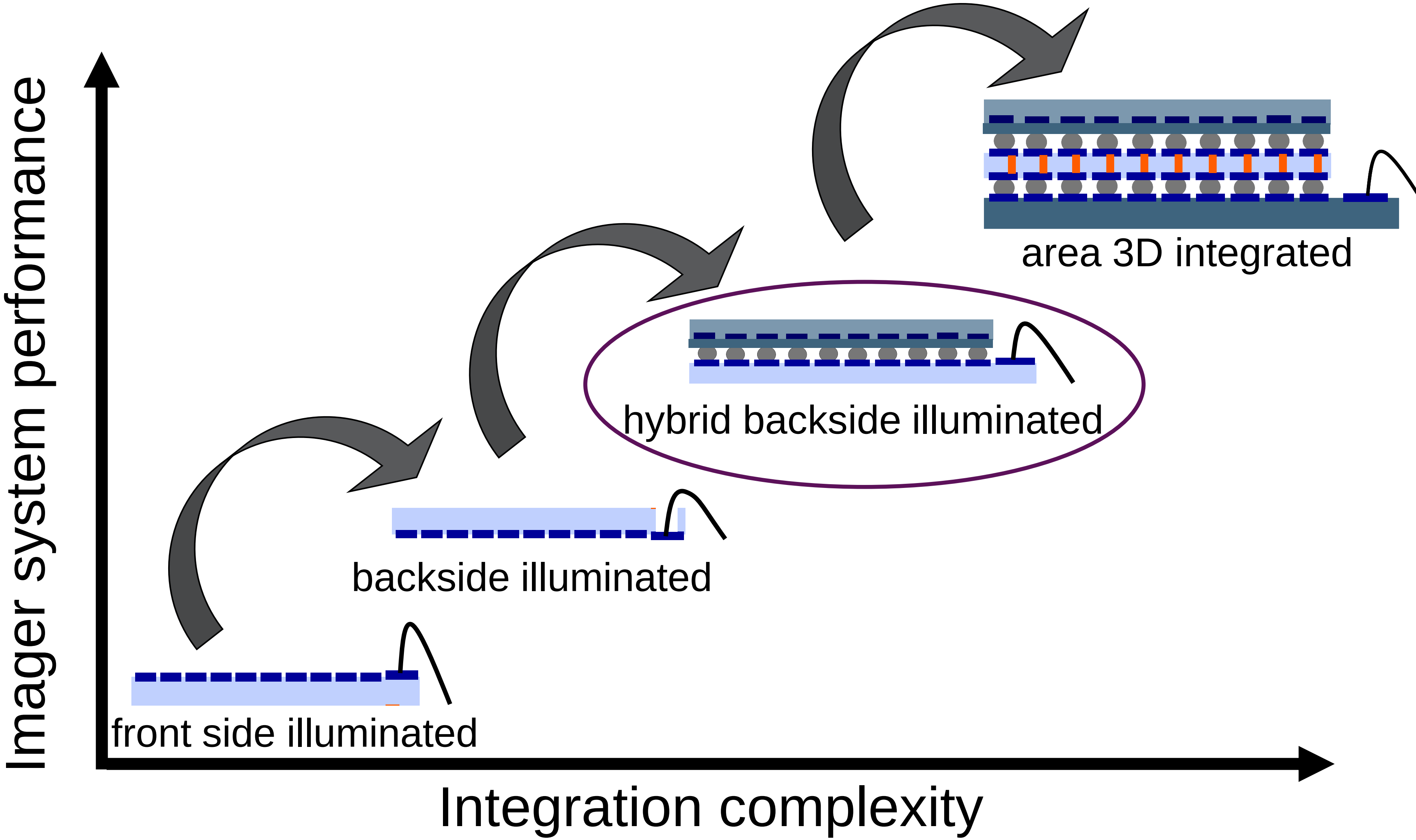
- European source for space imagers
- Requirements:
  - Design & process in imec 0.13 um CMOS
  - Global shutter
  - **Backside illuminated**
  - **Large area (stitched)**
  - **Radiation hard**
- Partners:



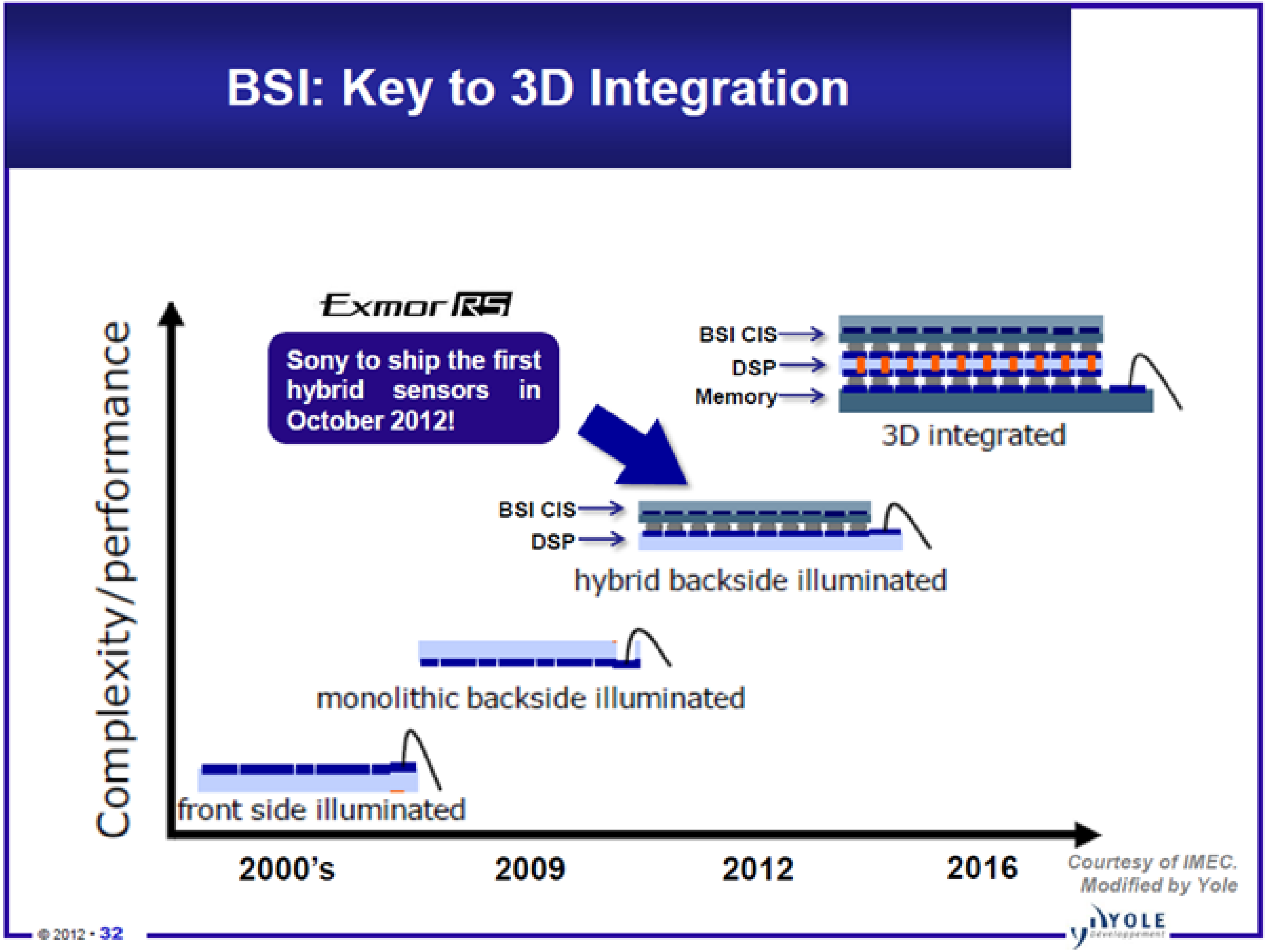


HYBRID BACKSIDE ILLUMINATED IMAGERS

ADVANCED IMAGER INTEGRATION

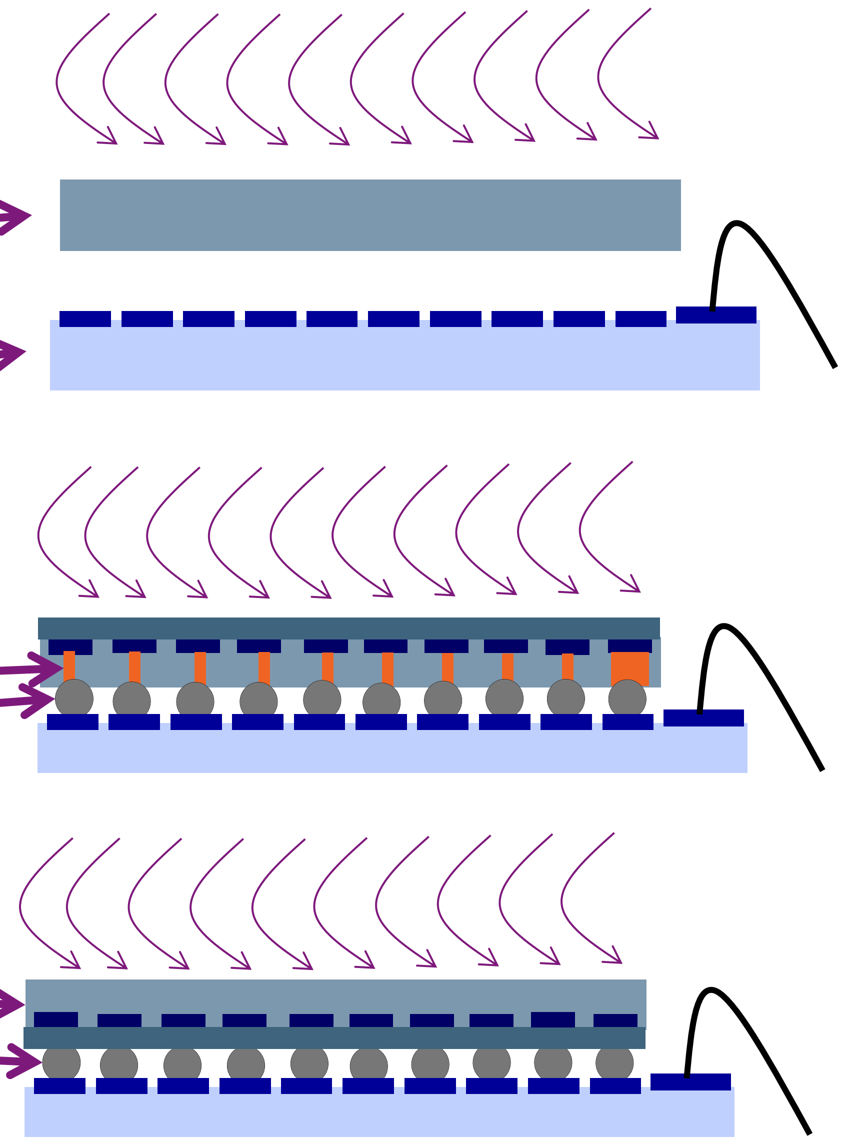


YOLE/IMEC IMAGER ROADMAP



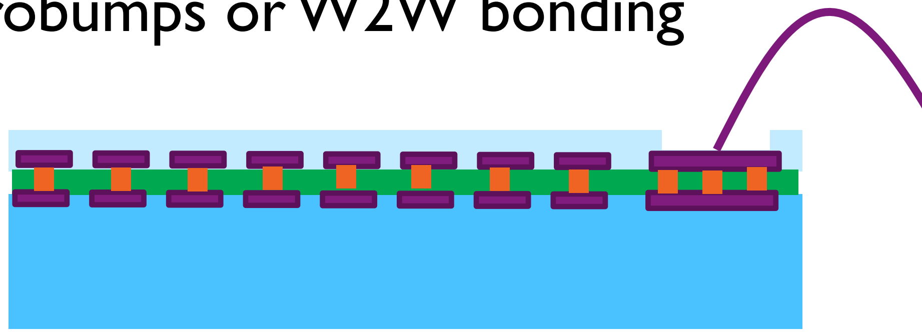
HYBRID IMAGERS: APPROACH

- 2 layers:
  - Detection layer + optional (analog) read-out
  - 2^{nd} read-out layer
- integration options:
  - Front side illuminated::
    - through Si vias (TSVs) + microbumps required
  - Backside illuminated:
    - Backside thinning + microbumps required

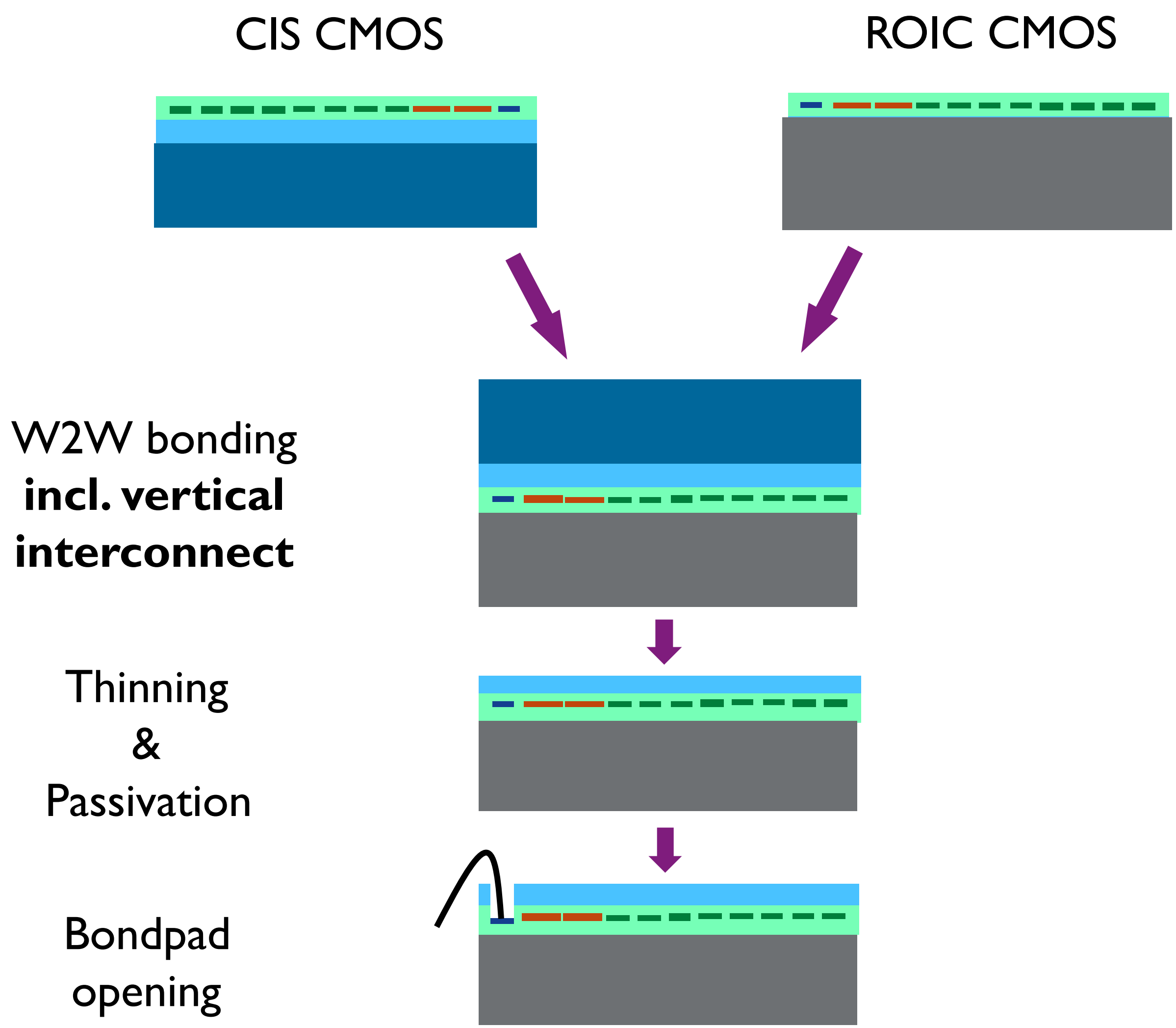


HYBRID IMAGERS:
PIXEL-WISE INTERCONNECT

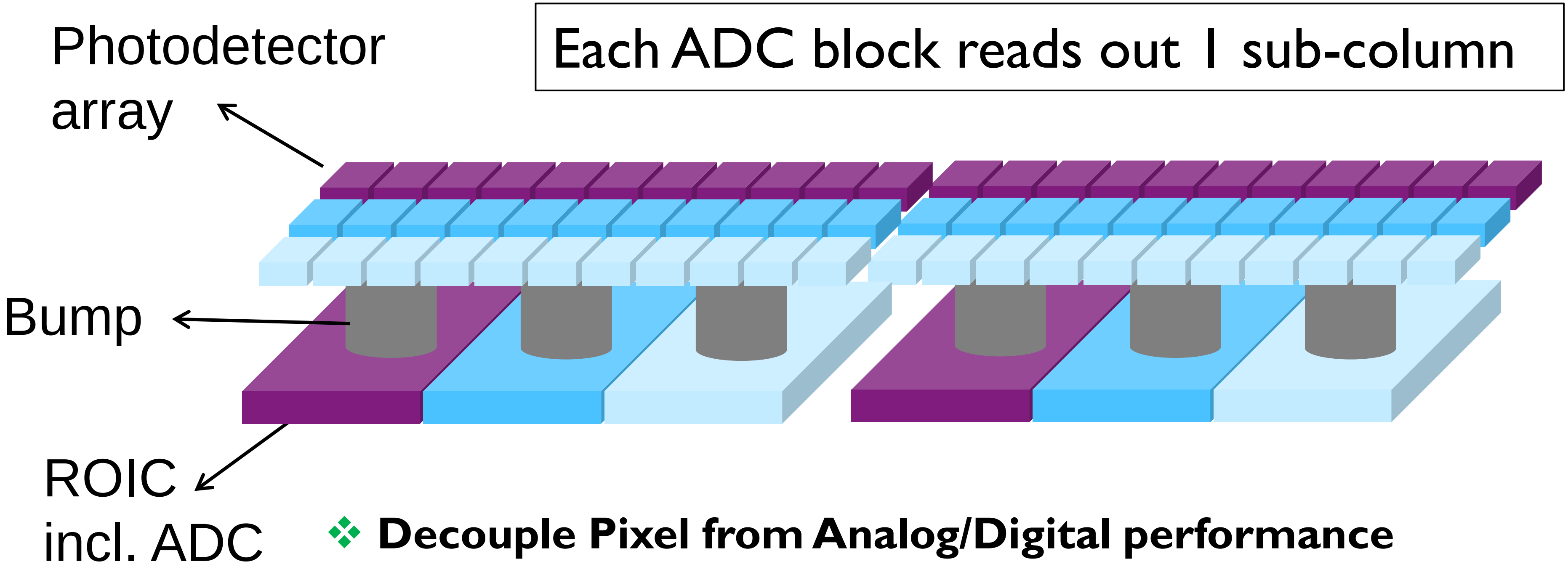
- Concept:
  - Face to face bonding using microbumps or W2W bonding
- Top layer:
  - Photodiodes + active CMOS
- Bottom layer:
  - CMOS read-out circuit (ROIC)
- Advantage:
  - Different CMOS technology top vs. bottom allows separate optimization
- Disadvantage:
  - Yield & cost



HYBRID BSI FLOW



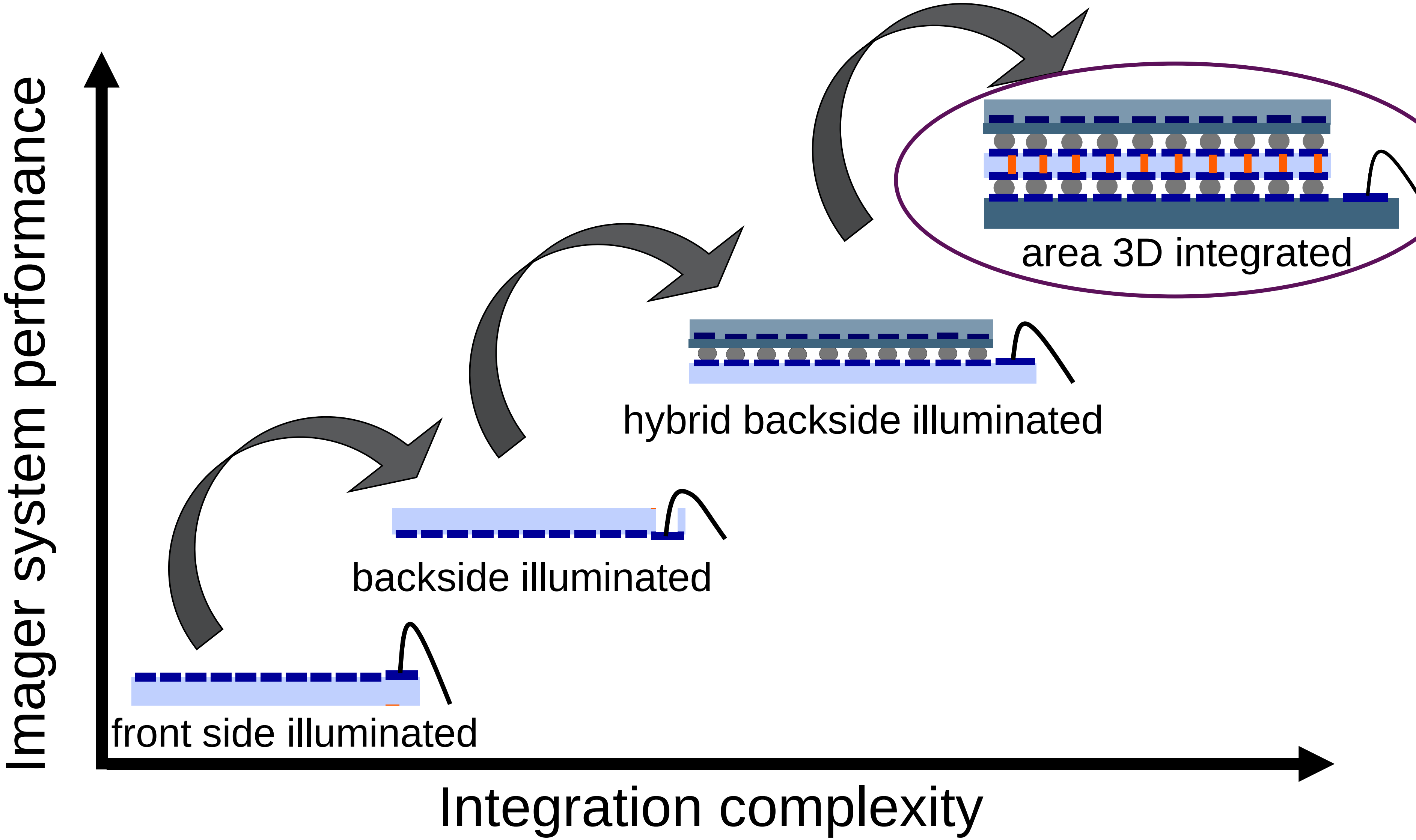
HYBRID IMAGER ARCHITECTURE: 1 ADC PER SUB-COLUMN



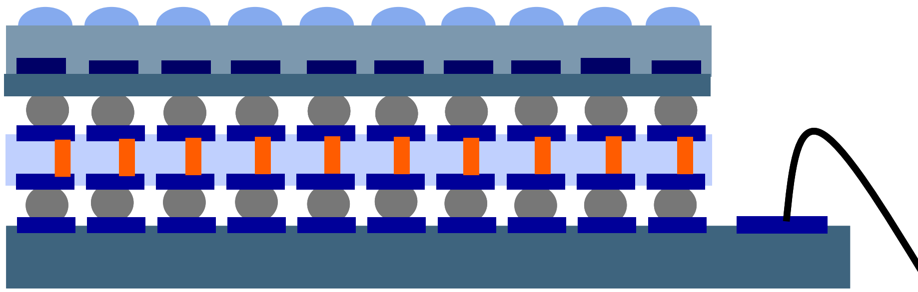
- Decouple Pixel from Analog/Digital performance
- ~ Linear resolution/power characteristics
- High speed parallel readout
- Higher cost

3D STACKED IMAGERS

ADVANCED IMAGER INTEGRATION



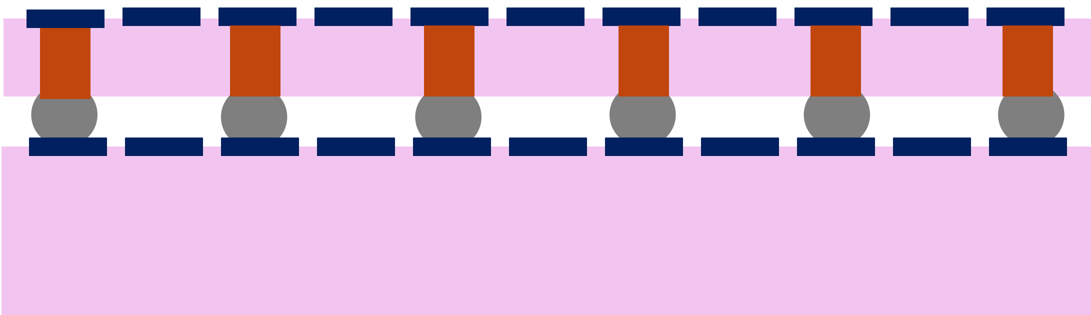
AREA 3D INTEGRATED IMAGERS

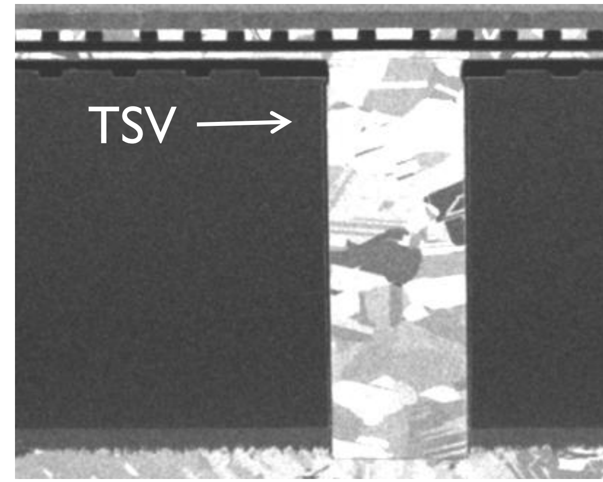


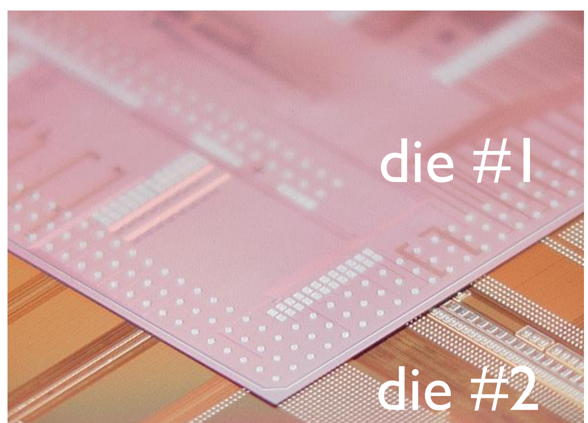
- Concept:
  - Stacking of multiple (>2) layers: detection layer + ROIC layers
  - Using high density bumping + area redistributed TSVs (@ pixel level)
- Advantages:
  - General: optimization of (CMOS) technology for different layers
  - Imager system:
    - Vertical parallel readout chain allows high speed
    - Triple (n-fold) area per pixel allows complex electronics per pixel
    - Low capacitance interconnect to digital image processor allows high speed and low power
- Challenge: system architecture:
  - Optimal split in different layers of functionality and technology

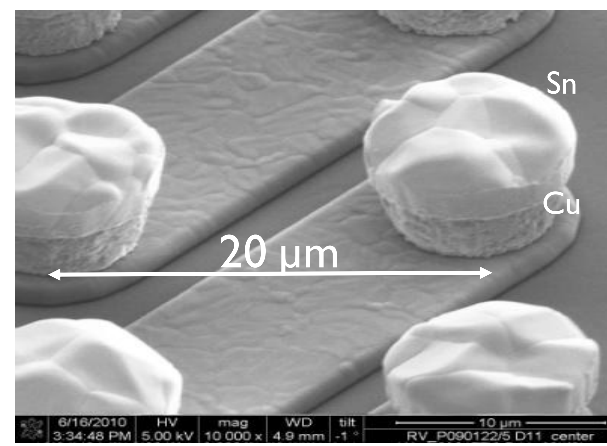
3D INTEGRATION TECHNOLOGY

- leveraging of 3D integration program at imec:
  - through Si Vias (TSVs), wafer thinning
  - high density bumping, advanced assembly



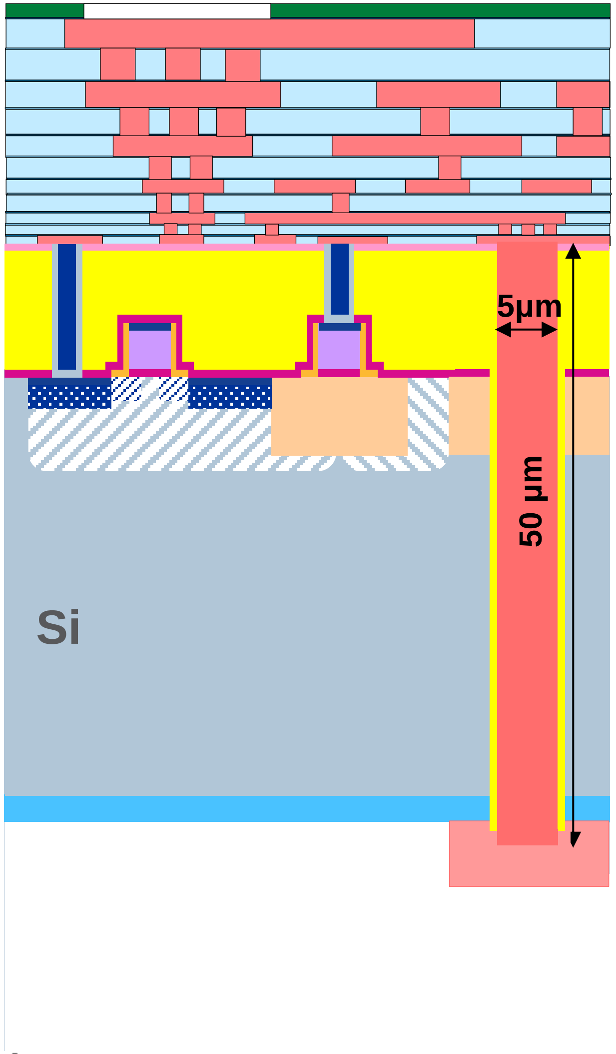






VIA MIDDLE THROUGH-SI-VIA PROCESS

"Via-middle": fabrication TSV's **after FEOL** device fabrication processing but **before BEOL** interconnect.



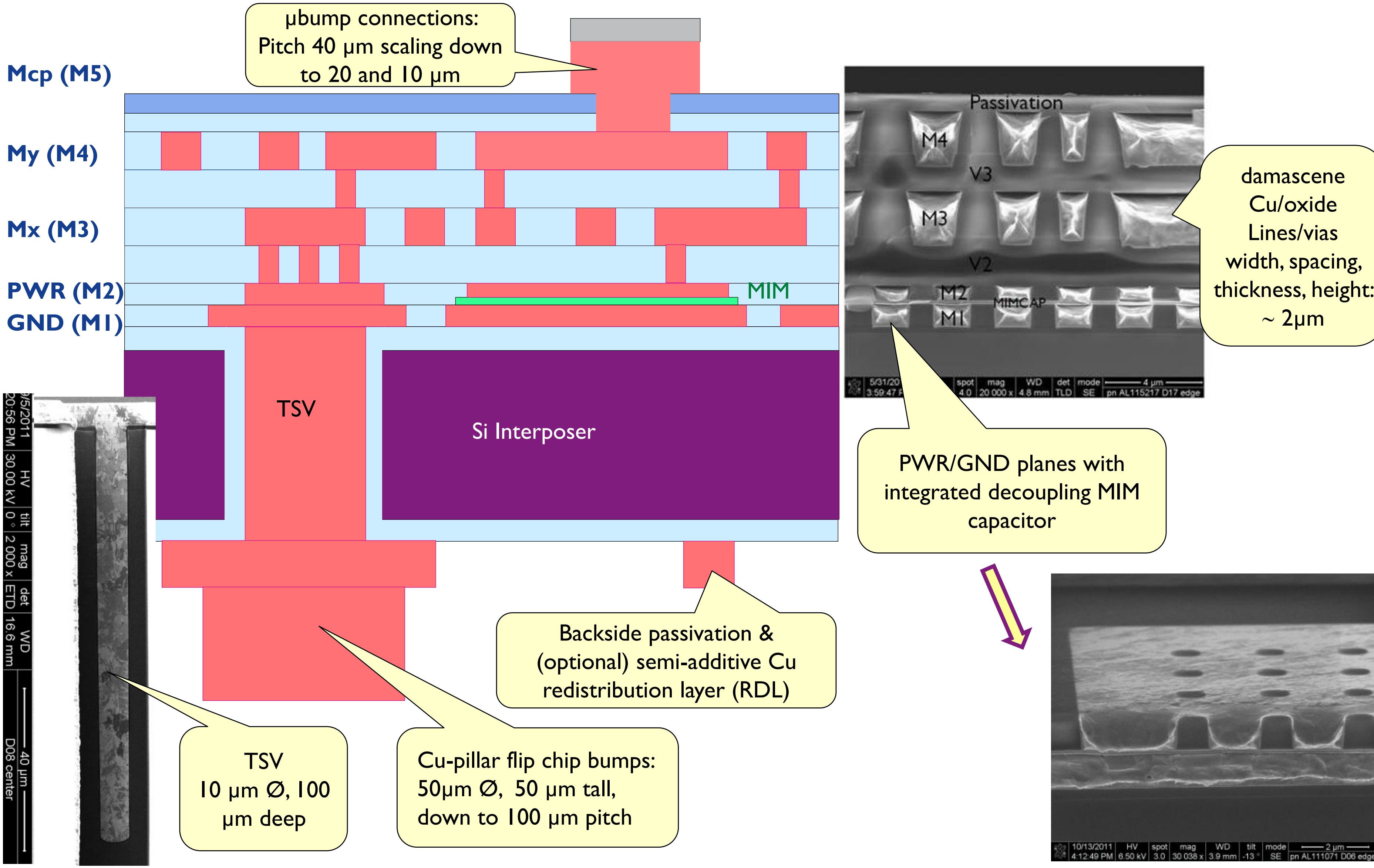
Key features :

- "Cu-nail" process after FEOL, before of BEOL processing
- High aspect ratio Cu damascene technique
- Single litho-step

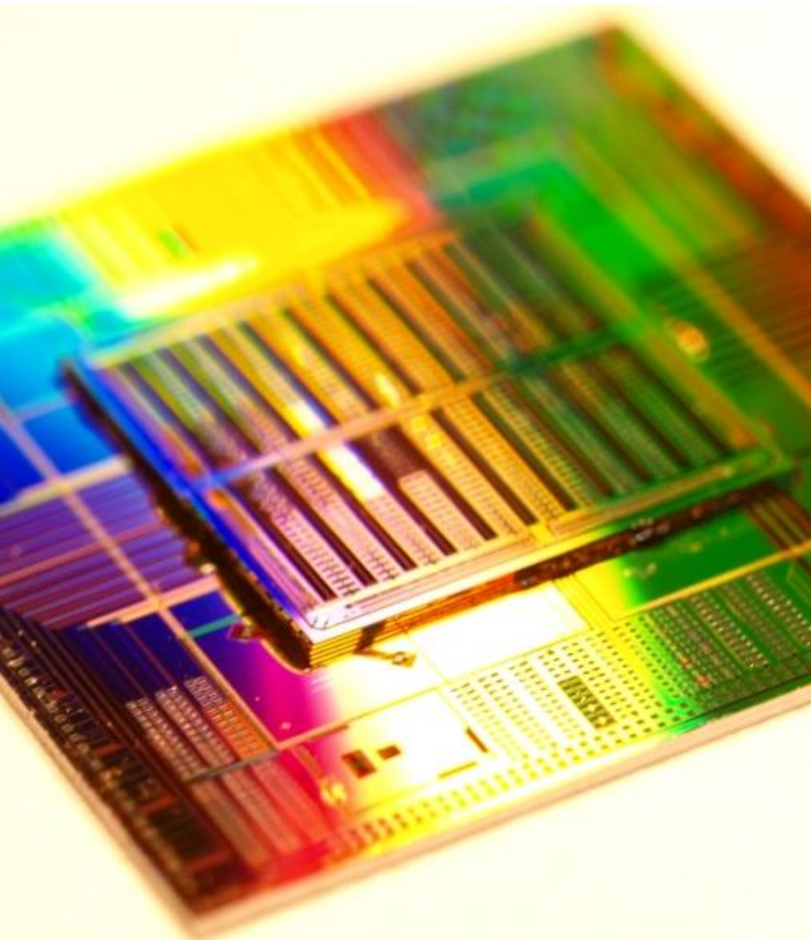
imec POR process:

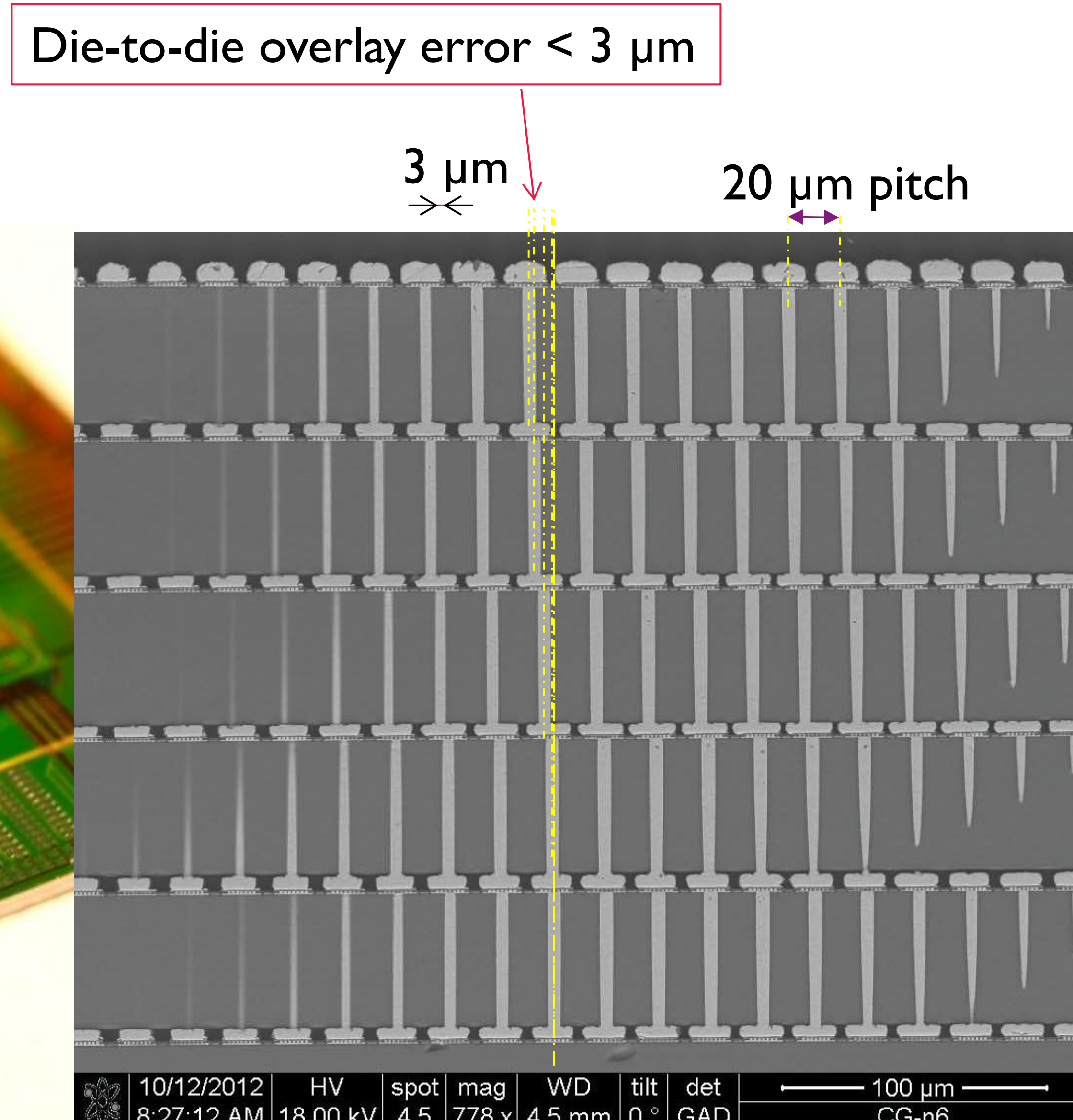
- ***5 µm diameter;***
- ***50 µm deep;***
- ***Aspect ratio 10***

Si Interposer technology development



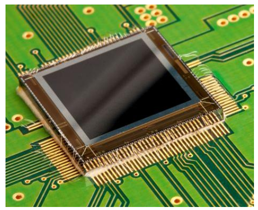
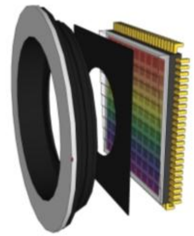
N=6 PTCO/P CU-CU DIE STACKING



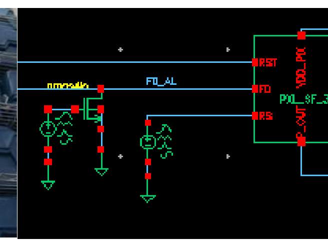
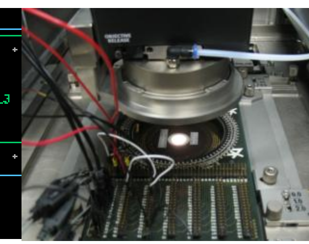


IMEC'S SPECIALTY IMAGERS MISSION

- imec offers **customized specialty imager solutions**


- levering its **competences under 1 roof**:
  - CMOS technology
  - Design & system know-how
  - Characterization

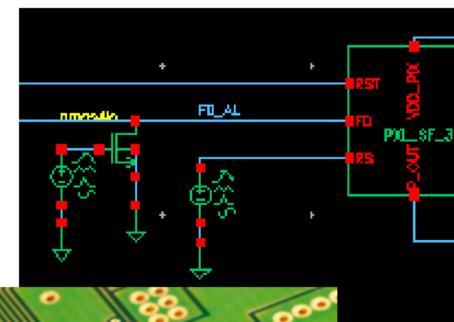




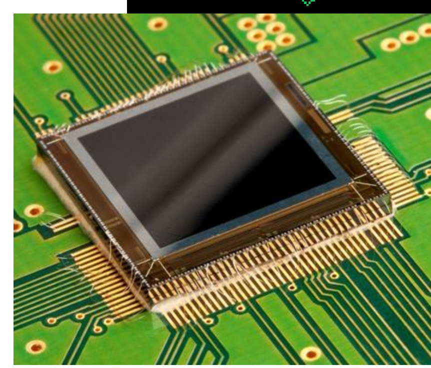
- using a **flexible business model**:
  - From R&D, Prototyping till Low Volume Production

Research & Development → Prototyping → Low Volume Production

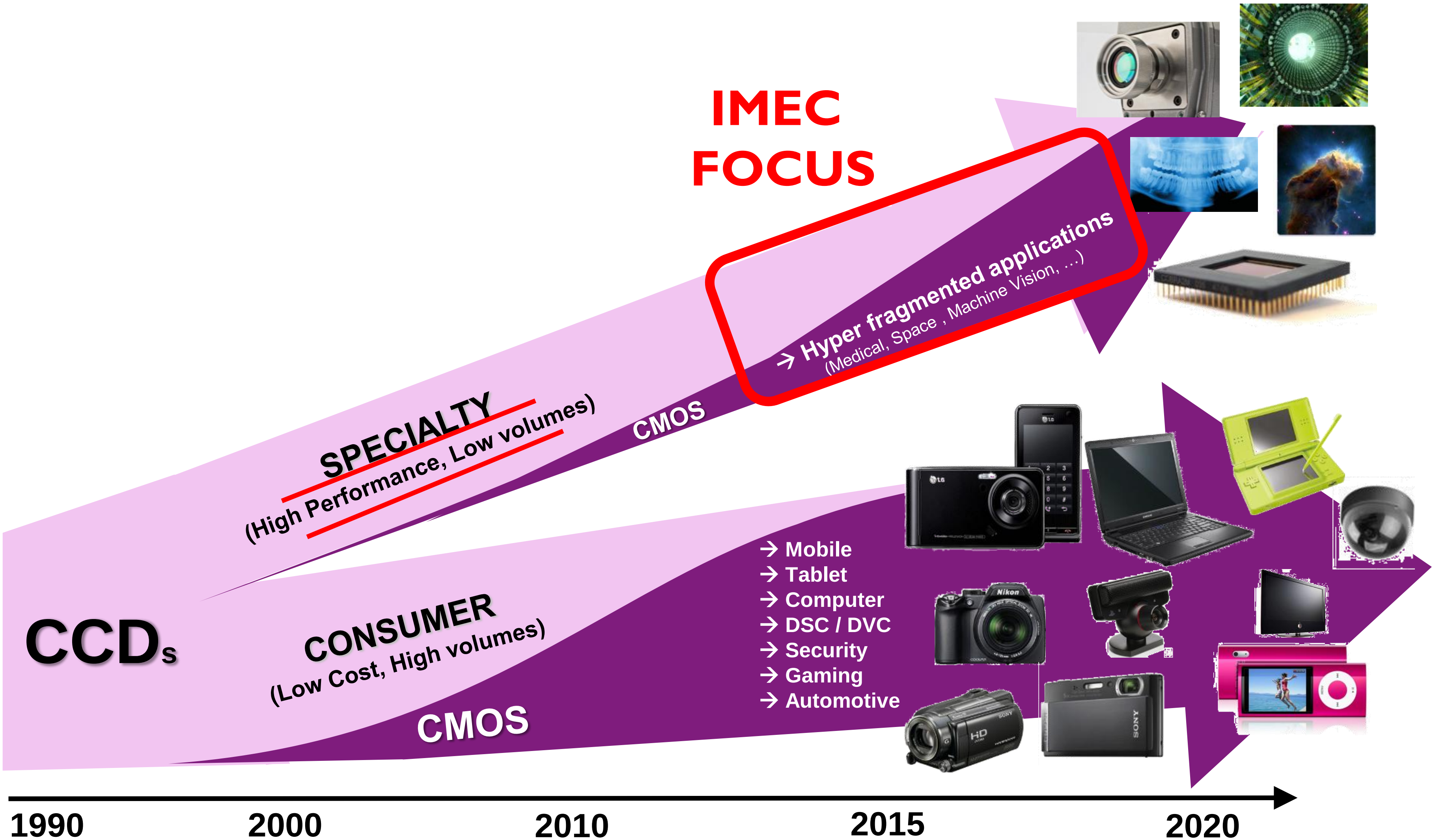
IMEC IMAGER OFFERING

- imec ≠ foundry:
  - No standard technology offering
  - No MPW runs
- imec > foundry:
  - imec offers customized specialty imager solutions
  - Flexible technology & design
  - Based on 0.13 um CMOS platform
  - Imager modules: 4T pixel, BSI, eCCD, 3D ...
  - (Ultra) low volume manufacturing
- Open for collaborations:
  - Fabless design partners
  - Packaging, testing, camera partners





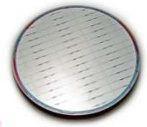
HIGH PERF VERSUS HIGH VOLUME MARKETS
CCD → CMOS TRANSITION

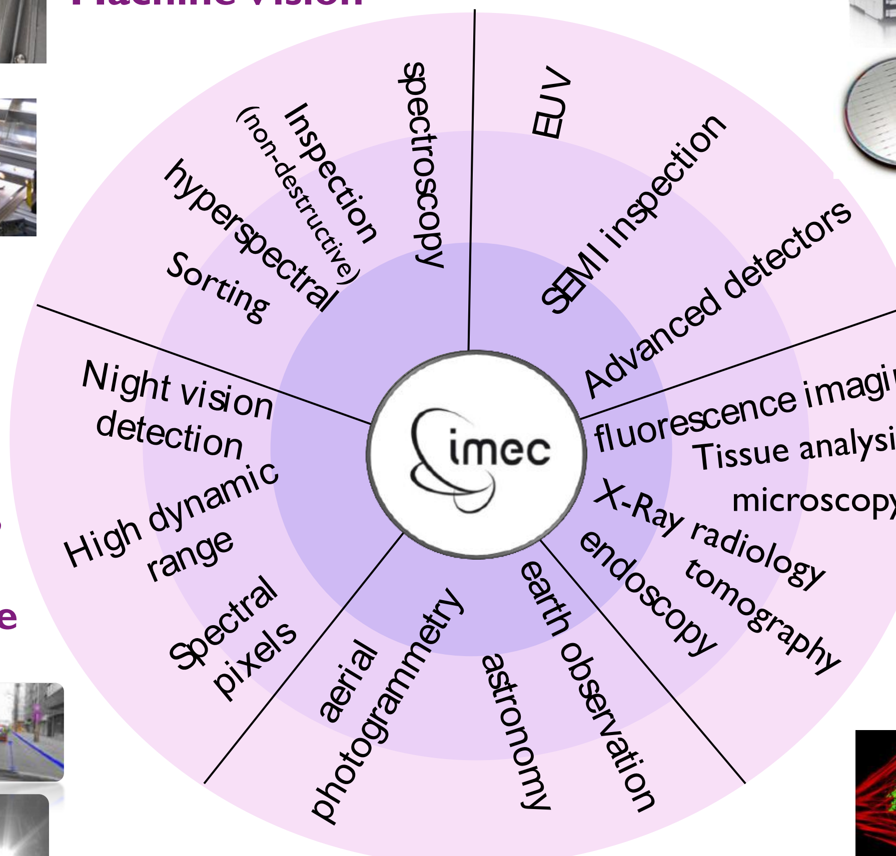


SPECIALTY IMAGING APPLICATION DRIVERS

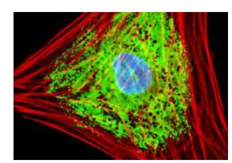
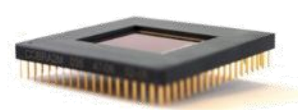

Industrial sorting & Machine Vision

Industrial Instrumentation

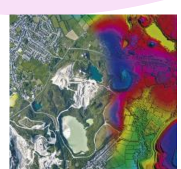



Life-Science & Medical Imaging

High-end **transports, security & surveillance**

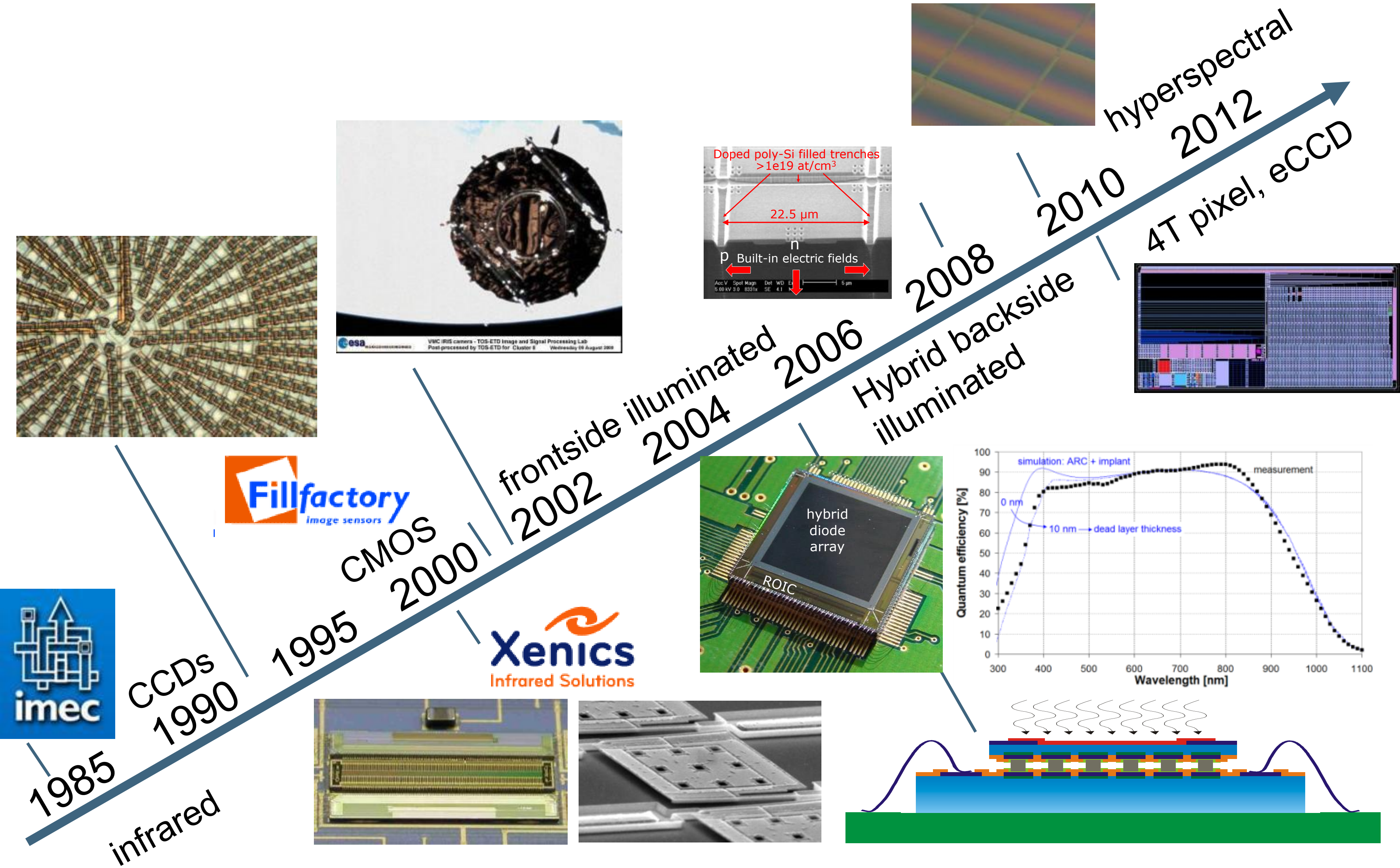
Space, Physics & Scientific




Key features

- High QE
- High speed
- Low noise
- Non-Visible sensing
- Radiation Hard
- Low power
- Spectral Filters/ARC

+25 YEARS OF EXPERIENCE IN IMAGING



ASPIRE
INVENT
ACHIEVE

imec