3D integration of advanced pixel detectors and readout electronics

Università di Bergamo

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Europe/Berlin timezone

The INFN VIPIX collaboration

VIPIX - Vertically Integrated PIXels

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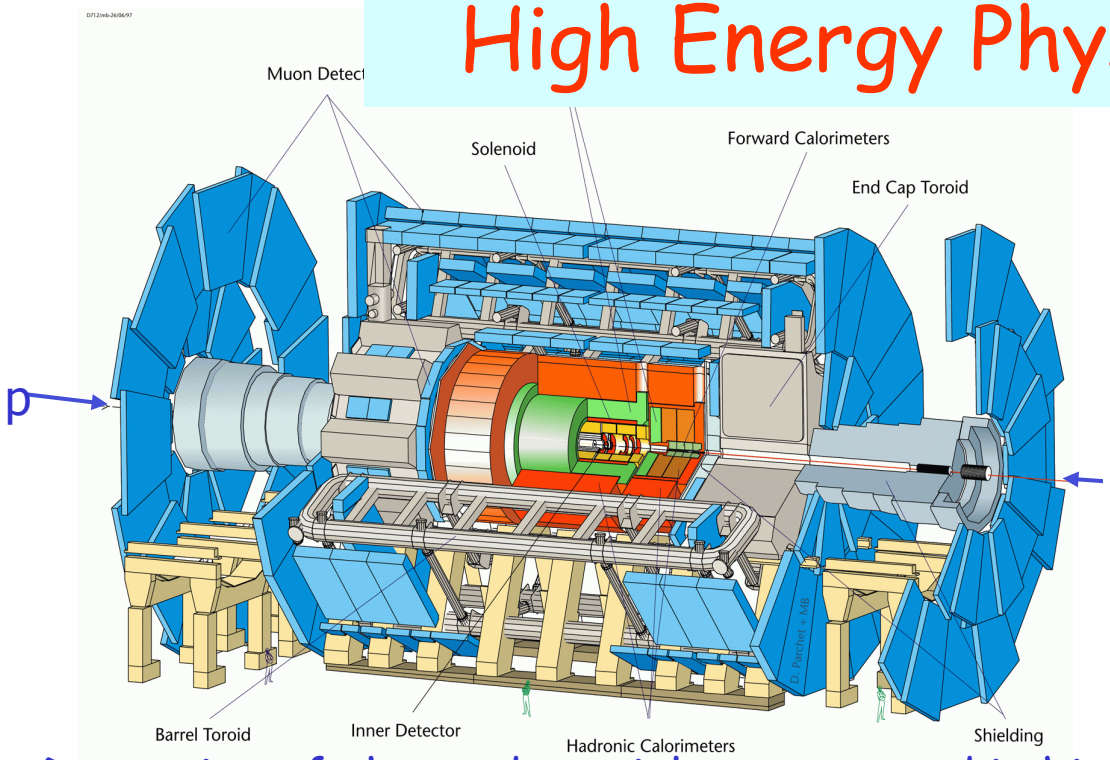
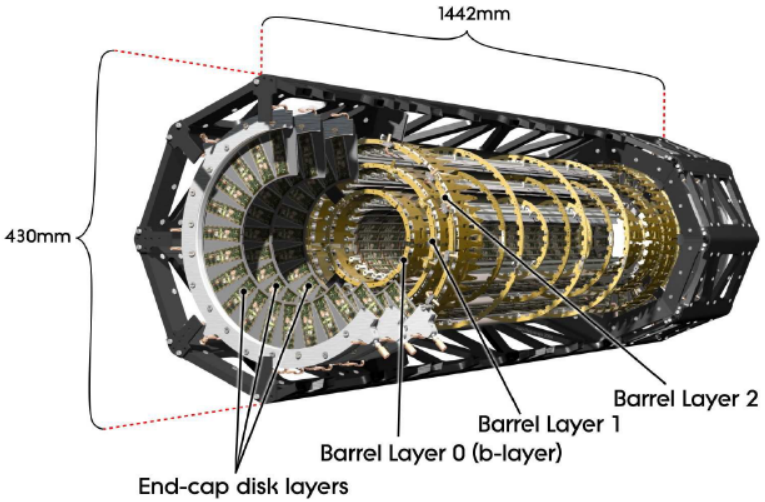
Outline

- What is 3D integration? Why did it triggered a wide interest in our community?
- Evolution from 2D devices to 3D integration for advanced pixel sensors and readout electronics in high energy physics experiments
- Expectations, experience, plans: current status and future promise (a personal view)

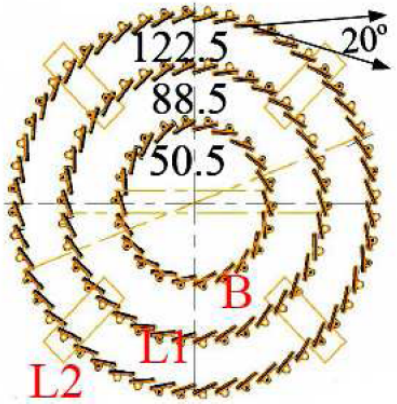
Silicon pixel detectors in High Energy Physics (HEP)





- Detection of charged particles generated in high energy collisions of accelerated proton beams (e.g. LHC - Large Hadron Collider facility at CERN, Geneva)
- Measurement of particle tracks as close as possible to the beam interaction point
- High granularity (80 Mpixels) and high data rate capability (hit rate ~ 50 MHz/cm^2) are necessary to detect multiple tracks with good space and time resolution
- Radiation hardness is also necessary to operate close to beams

Barrel layers cross section (radii in mm)



Advancing the state of the art of pixel sensors for a next generation of HEP experiments

New demanding specifications for experiments at new machines (HL-LHC, International Linear Collider:

- **Improve resolution ⇒ shrink pixel size and pitch**, down to 20 μm or even less

  presently limited to 50 μm by bump bonding technology
- **Preserve or even increase pixel-level electronic functions**

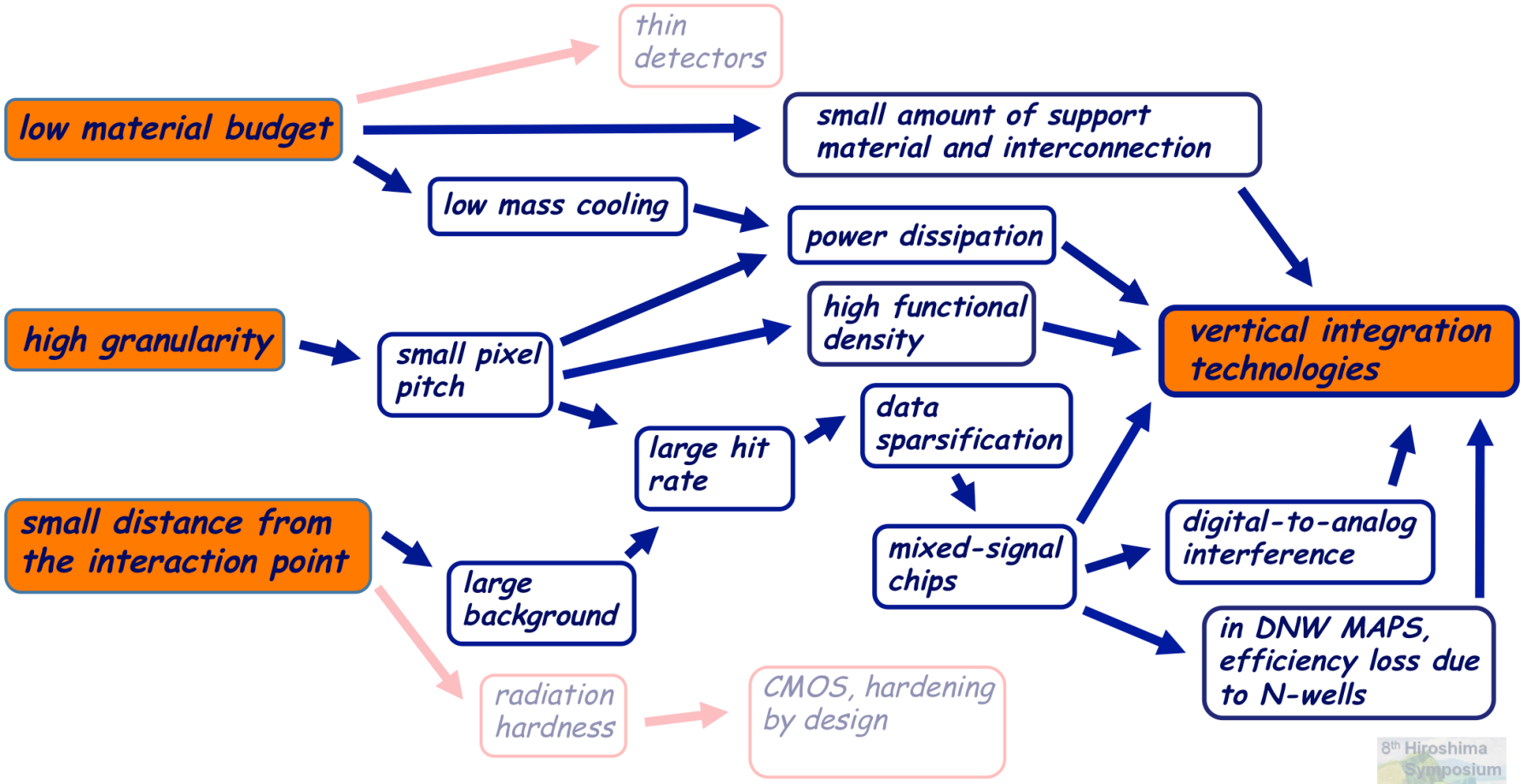
  handling of high data rates (hit rates > 10 MHz/mm^2), analog-to digital conversion, sparsification,…: presently this also contributes to limiting the minimum size of pixel readout cells
- **Decrease amount of material ⇒ thin sensor and electronics** chips, "zero mass" cooling

  Necessary to reduce errors in track reconstruction due to multiple scatterings of particles in the detector system

  50 -100 μm total thickness

Vertex detectors in future HEP experiments

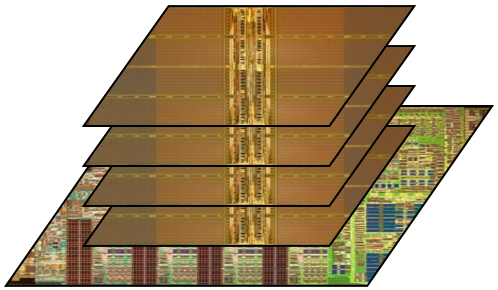
- Experiments at the future particle colliders (or upgrade of present colliders) will set severe requirements for silicon vertex trackers



L. Ratti, "Monolithic and hybrid pixel sensors in 3D CMOS technology", 8th Hiroshima Symposium, 5-8 December 2011

What is 3D integration?

- 3D electronics: "the vertical integration of thinned and bonded silicon integrated circuits with vertical interconnects between the IC layers."[1]



- 3D electronics has the potential of being:
  - Denser (smaller form factor)
  - Faster (reduced delay because of shorter interconnects)
  - Lower power (smaller interconnect capacitance)
  - Lower cost (sizably less expensive than aggressive CMOS scaling)
  - Integration of dissimilar technologies (sensor, analog, digital, optical)

1) Philip Garrou, Christopher Bower, Peter Ramm, Handbook of 3D Integration Technology and Applications of 3D Integrated Circuits, Wiley-VCH, 2008.

Applications of 3D in the semiconductor industry (I)

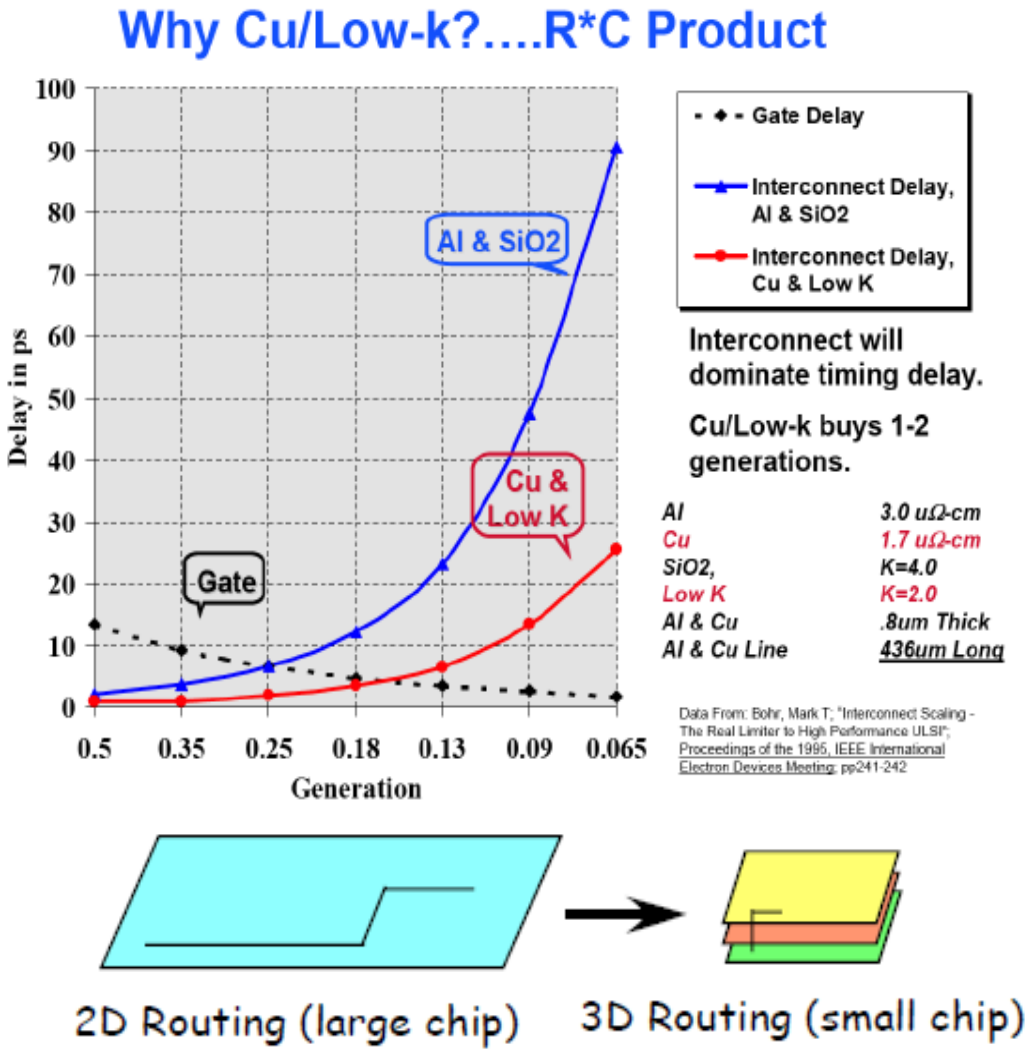
Two examples:

1) Memory

All major memory manufacturers are working on 3D memory stacks. The cost of 3D can be significantly less than going to a deeper technology node for higher density.

A major bottleneck is access time between CPU and the memory. Speed and power advantages are achieved with shorter vertical interconnects.

Initial applications for 3D will use Logic to Memory, and Logic to Logic stacking.



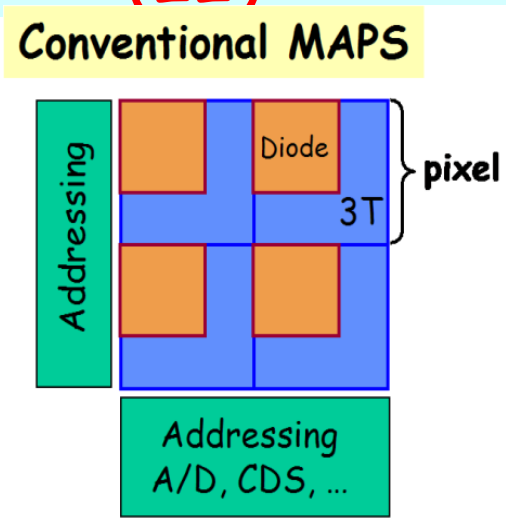
Applications of 3D in the semiconductor industry (II)

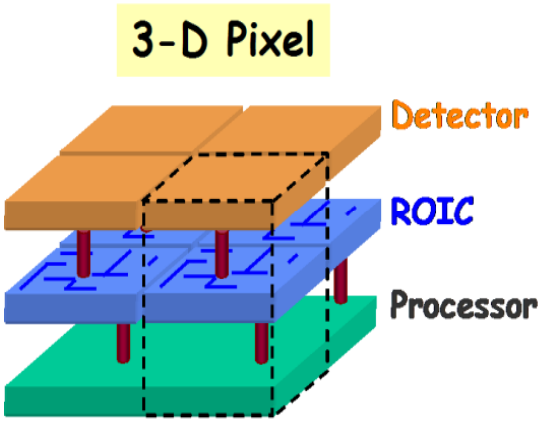
2) Image sensors

Pixel arrays with sensors and readout are well suited to 3D integration since advanced signal processing can be placed close to the sensor and performed at the pixel level. Current 2D approaches cannot handle the data rate needed for high speed imaging.

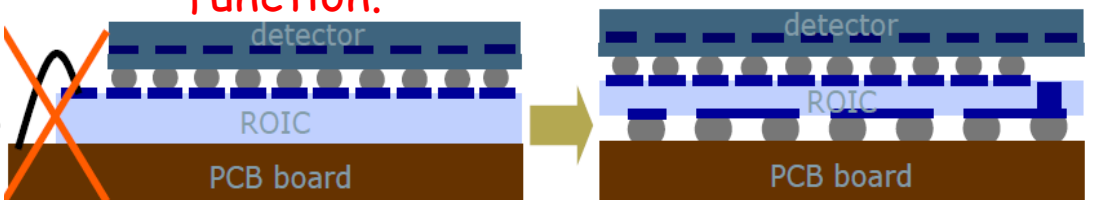
Smaller pixels providing improved resolution can be also designed thanks to 3D integration.

4-side buttable, large area imager with no dead zones are enabled by 3D integration.

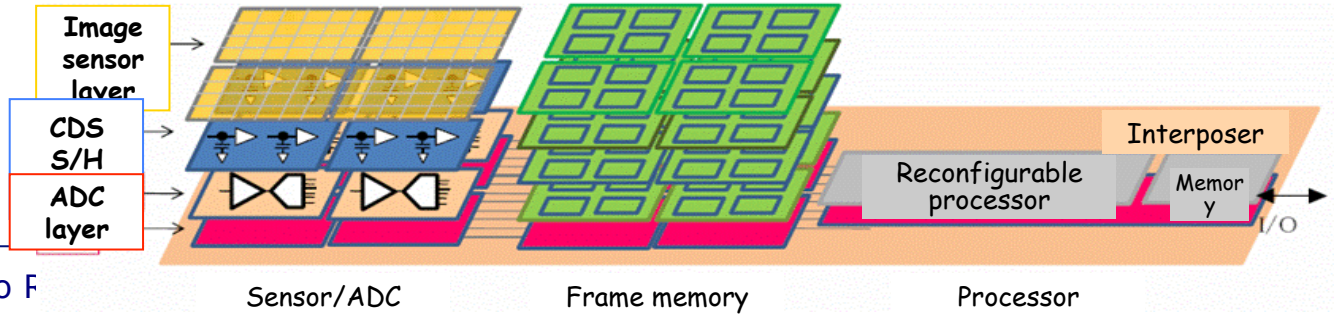




With heterogeneous integration, each layer can be fabricated in a different technology and optimized for a different function.



M. Aoyagi, "Status of 3D-IC Technology Research and Development in Japan", TIPP2011



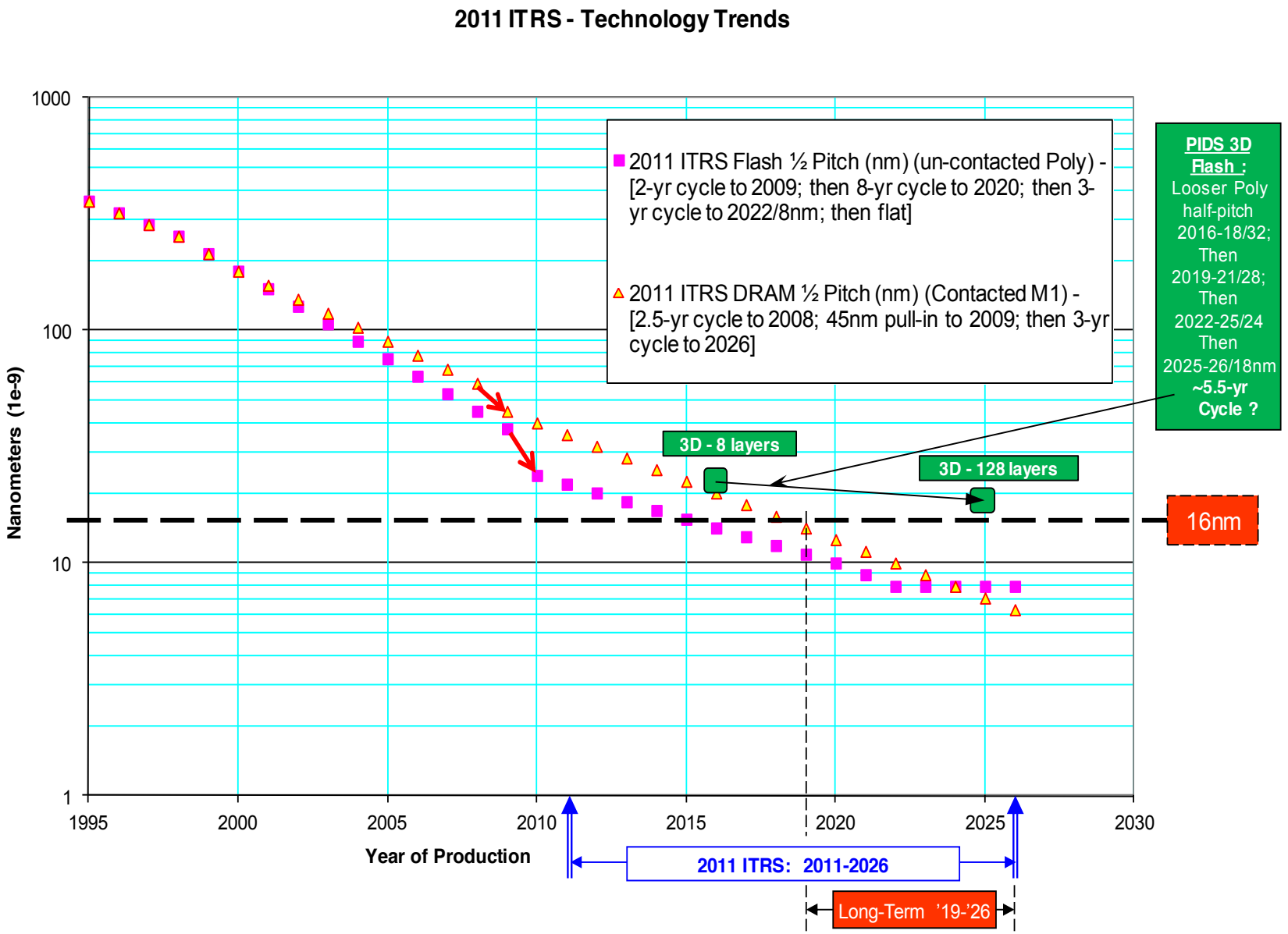
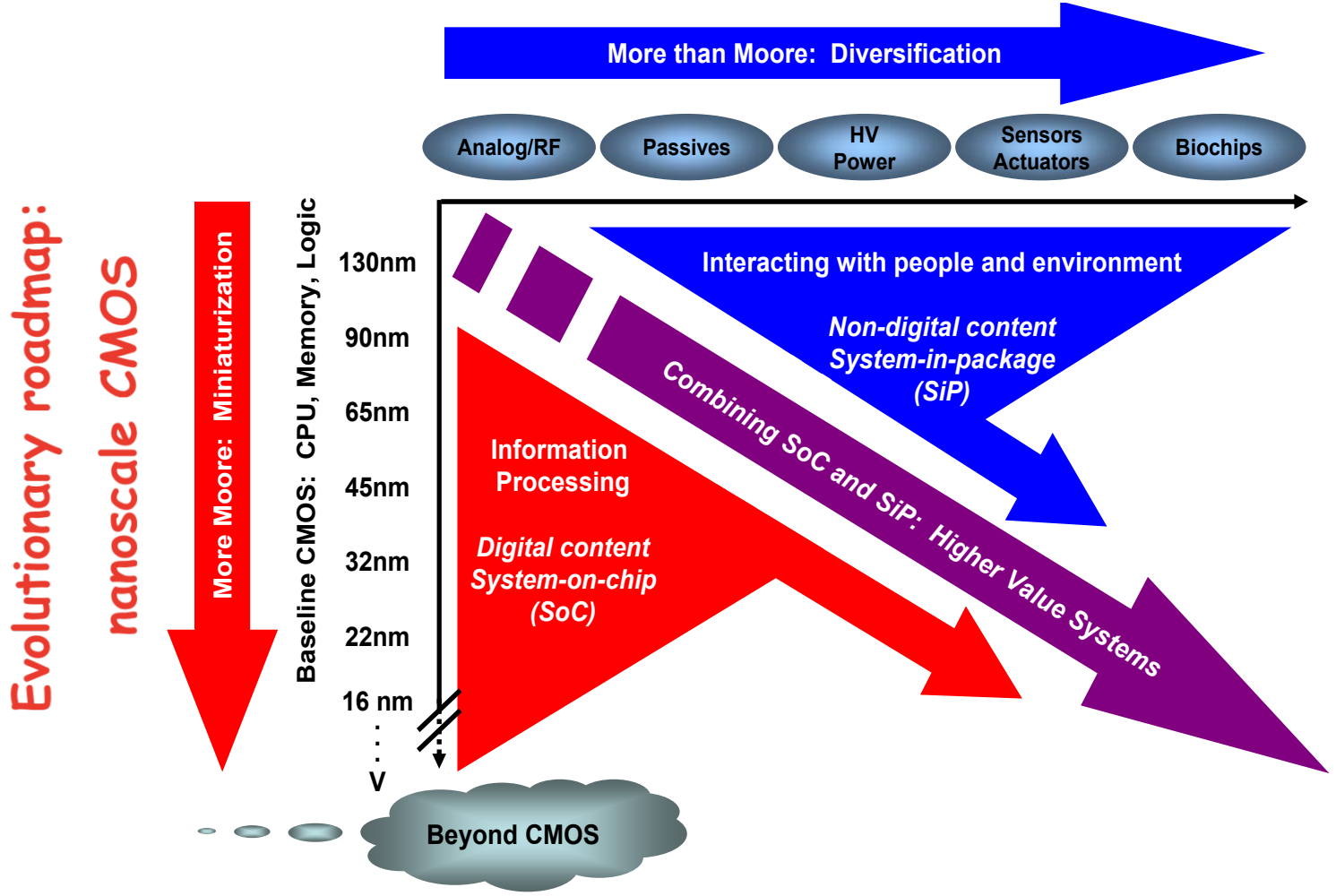


Figure ORTC3 *2011 ITRS—DRAM and Flash Memory Half Pitch Trends*

Evolution of microelectronic technologies

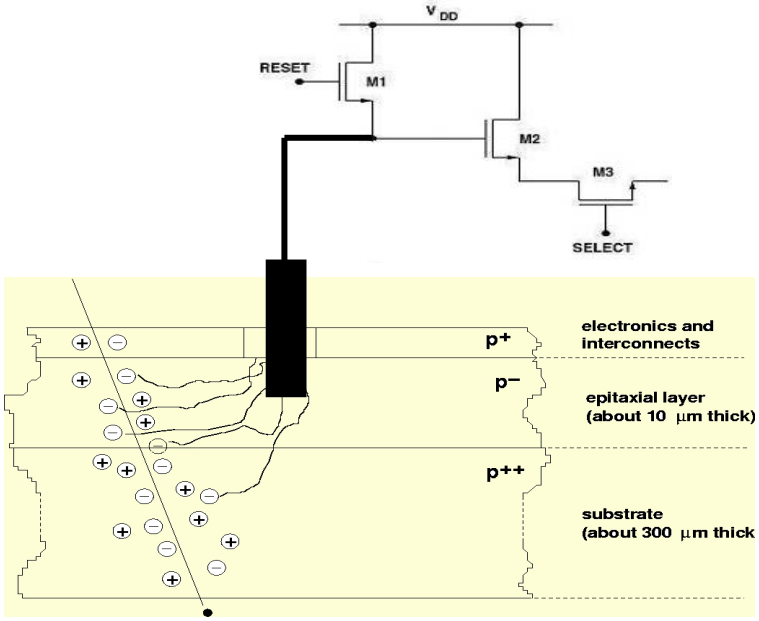
No roadmap, room for new ideas:
monolithic sensors, 3D integration



More than Moore in semiconductor detectors: CMOS monolithic sensors (MAPS)

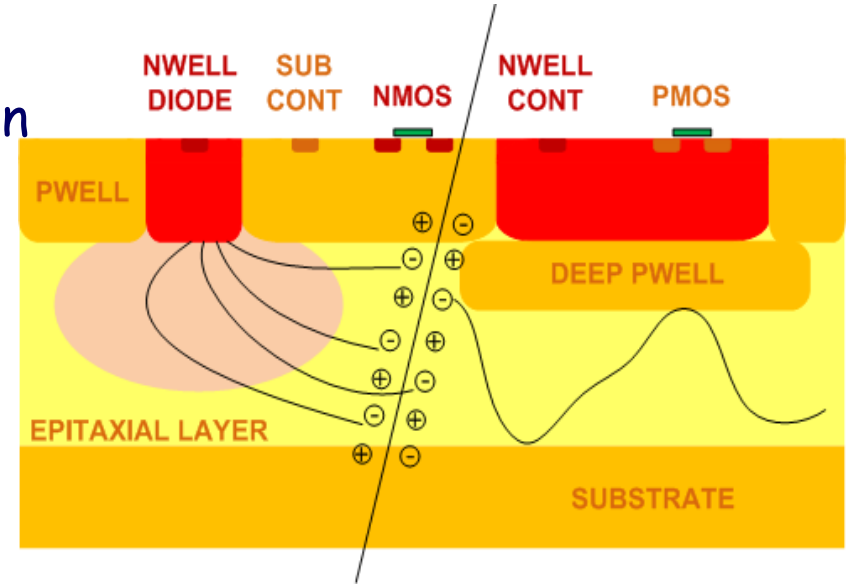
- MAPS can be included in the "more than Moore" family, since besides CMOS electronics they also include sensing electrodes for detecting the charge induced by incident particles.

- In standard MAPS, fabricated in mainstream CMOS processes, the particle-sensitive region (substrate or epitaxial layer) has a relatively low resistivity. This makes these devices sensitive to non-ionizing radiation and displacement damage, with a rather fast degradation of charge collection properties.



The More than Moore evolution of MAPS

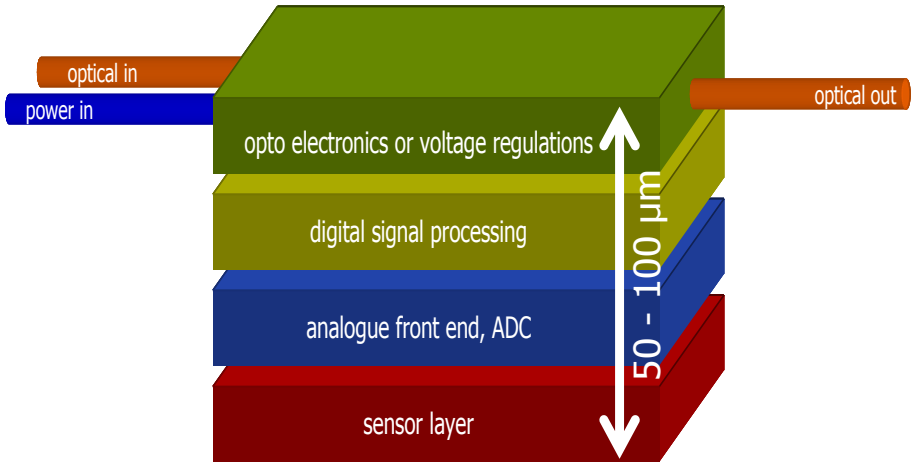
- Advance in MAPS performance does not only involve a reduction of the size of transistors. It can be achieved by optimizing the silicon bulk to increase the signal-to noise ratio and the radiation tolerance
- High-resistivity epi-layers (thickness of 10 – 50 μm) or even substrates have become available in commercial CMOS process
- They can be fully or at least partially depleted, with great potential advantages in terms of tolerance to non-ionizing radiation



A further leap: 3D integration

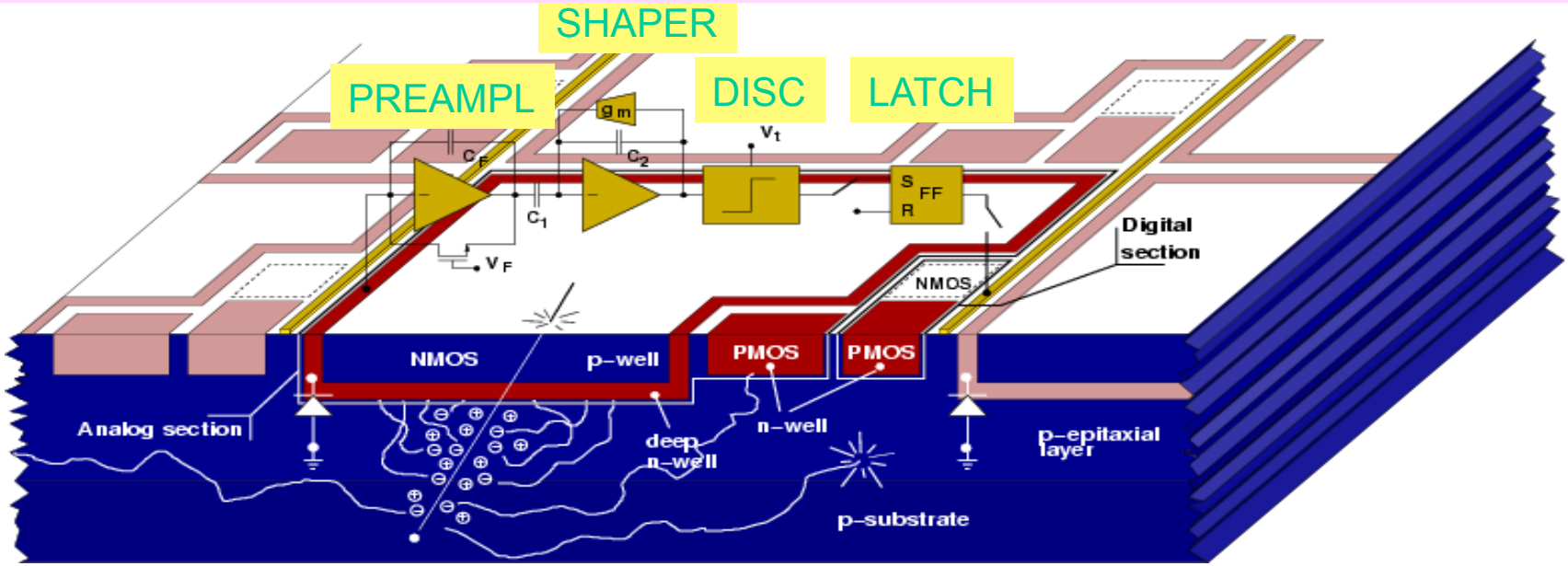
- The microelectronic industry has developed 3D integration of **thinned and bonded CMOS tiers with vertical interconnections through the silicon layers** as an alternative or complementary way to device scaling, with the goal of enhancing memory capacity and microprocessor speed (by reducing length of interconnections) and of improving the performance of image sensors (by including pixel level high-speed signal processing).

- The semiconductor detectors and front-end electronics communities in HEP and photon science plan to take benefit from 3D integration for **new pixel sensor with advanced functionalities, smaller form factor, less material and dead area, separation and optimization of sensing, analog and digital functions,…** New concepts may also be enabled by this technology.



Deep N-Well (DNW) sensor concept

New approach in CMOS MAPS design compatible with data sparsification architecture to improve the readout speed potential



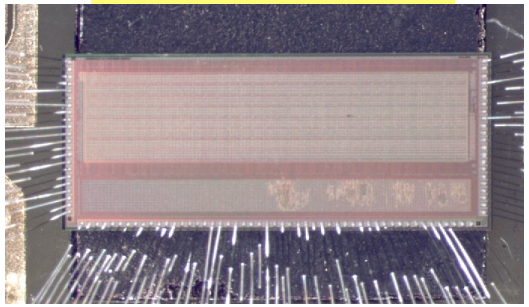
Classical optimum signal processing chain for capacitive detectors can be implemented at pixel level:

- Charge-to-Voltage conversion done by the charge preamplifier
- The collecting electrode (Deep N-Well) can be extended to obtain higher single pixel collected charge (the gain does NOT depend on the sensor capacitance), reducing charge loss to competitive N-wells where PMOSFETs are located

The first generation of CMOS sensors with in-pixel sparsification and time stamping
(DNW MAPS in the 130 nm STM CMOS process)

SuperB

APSEL4D

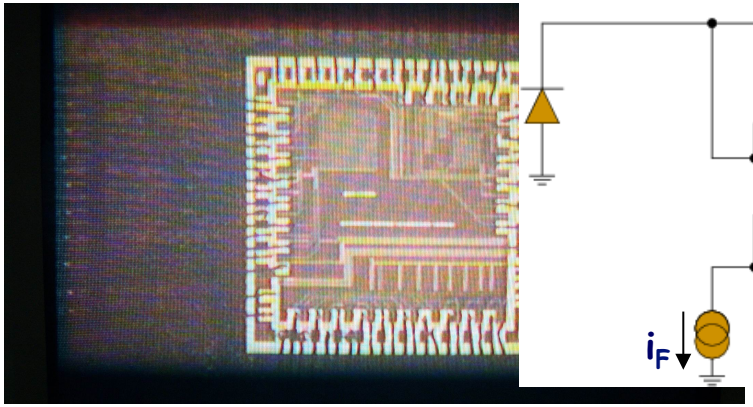


32x128 matrix.
Data Driven, continuously operating sparsified readout
Beam test Sep. 2008

50x50 μm pitch

ILC

SDR0

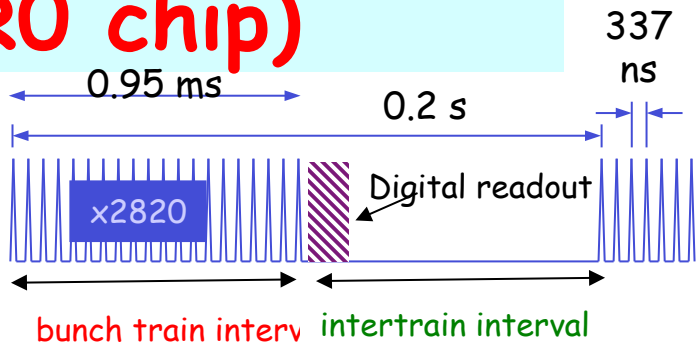


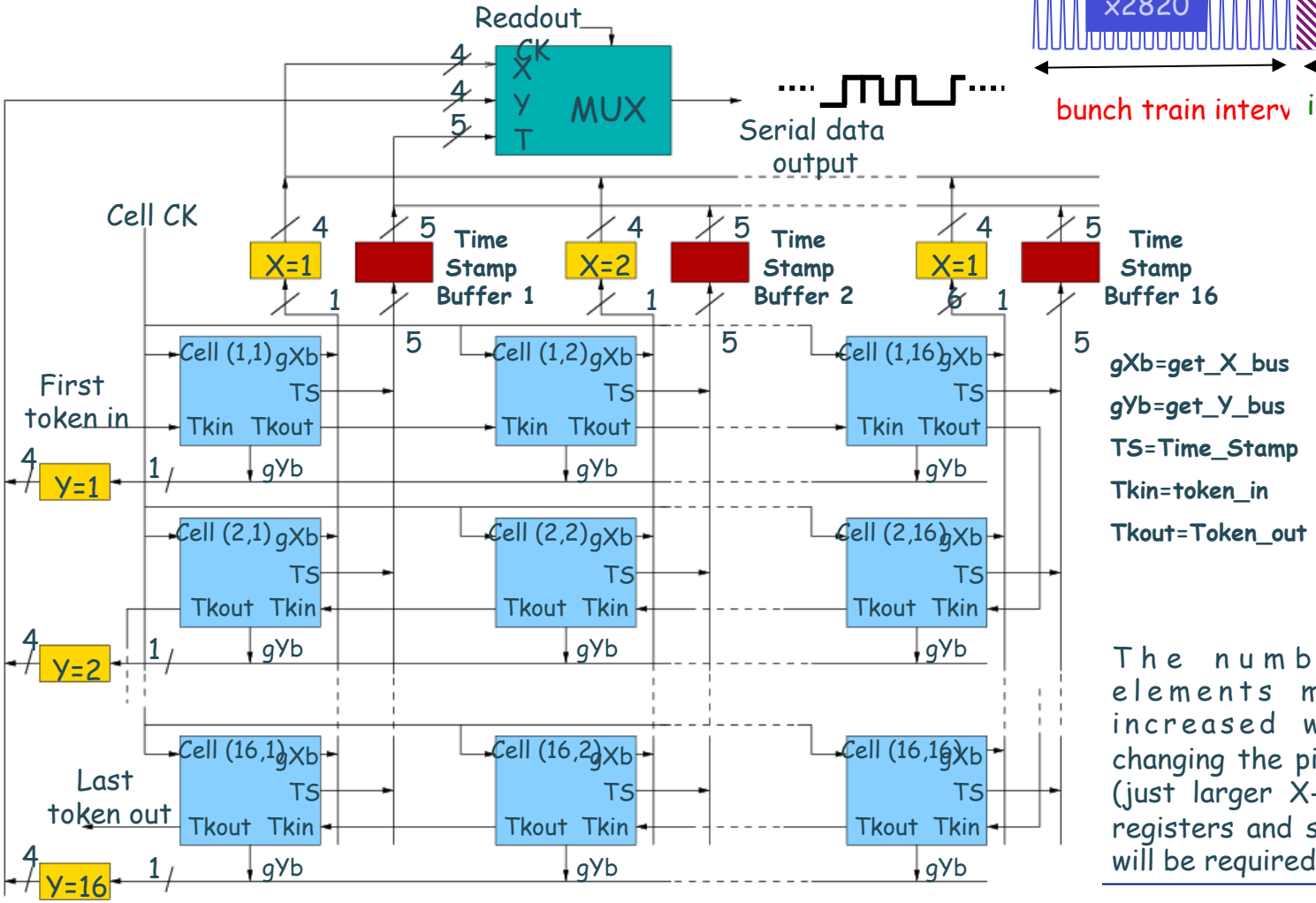
16x16 matrix + smaller test structures.
Intertrain sparsified readout

25x25 μm pitch

Intertrain Readout Architecture for "ILC" MAPS (SDRO chip)

Suggested by FNAL IC design group, first implemented in the VIP chip





gXb=get_X_bus

gYb=get_Y_bus

TS=Time_Stamp

Tkin=token_in

Tkout=Token_out

The number of elements may be increased without changing the pixel logic (just larger X- and Y-registers and serializer will be required)

DNW CMOS sensors: the way forward

Several issues had to be addressed to meet ILC Vertex Detector specifications (pixel pitch, detection efficiency):

- Binary readout: ILC VTX demands a **pixel pitch** < 20 μm to achieve required single point resolution < 5 μm.
- **Detection efficiency** does not meet requirements (> 99 %) because of competitive n-wells (PMOS) decreasing the fill factor
- Capability of **handling multiple pixel hits** has to be included without degrading efficiency and pitch

A further problem:

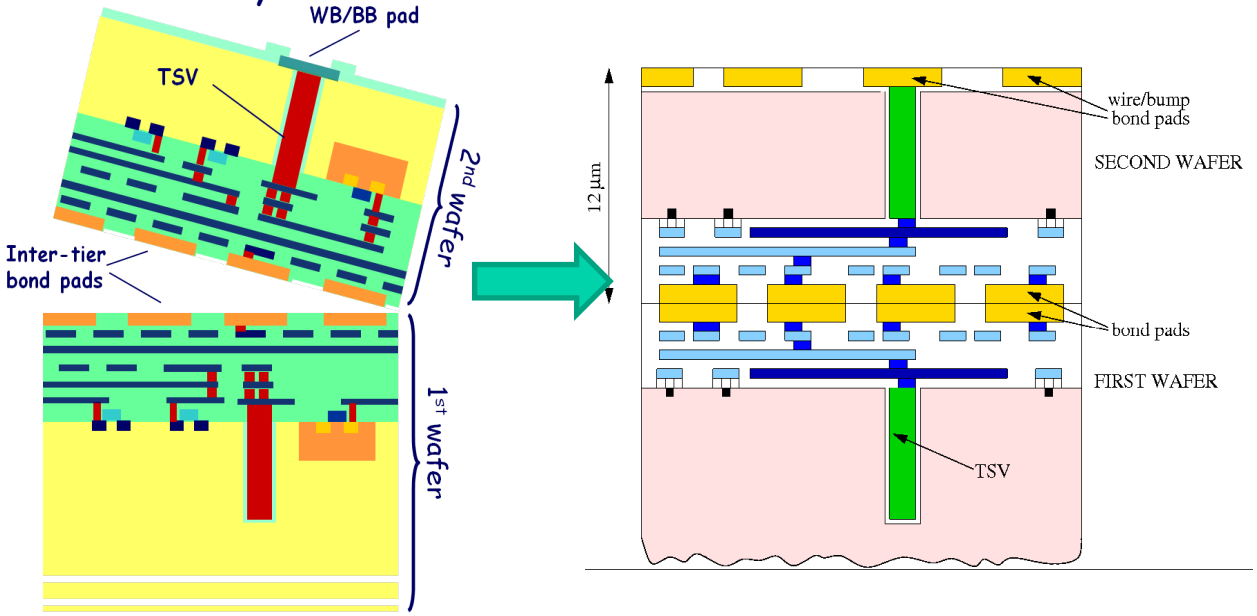
- The performance of the SuperB sensor (APSEL) with continuous sparsified readout was impaired by **digital-to-analog interferences** (digital activity in the same substrate where the sensing electrode is located)

⇒ **3D integration as the technology leap to overcome these problems and tackle the technical issues related to the integration of large sensor matrices.**

A "via first" process as an aggressive variant of 3D integration

Tezzaron 3D process (Fermilab 3D-IC Consortium)

- Through-Silicon Vias (TSV) are etched at early stages of a 130nm CMOS process (after transistor fabrication) at the silicon foundry. High density vertical interconnections are possible. High-density, low-mass bonding of CMOS layer is achieved by a Cu-Cu thermocompression process.
- This is probably the best way to fabricate 3D integrated circuits for pixel readout with a large number of pixel-level interconnections, enabling advanced signal processing architectures, large memory size, digital calibration of analog circuits,...

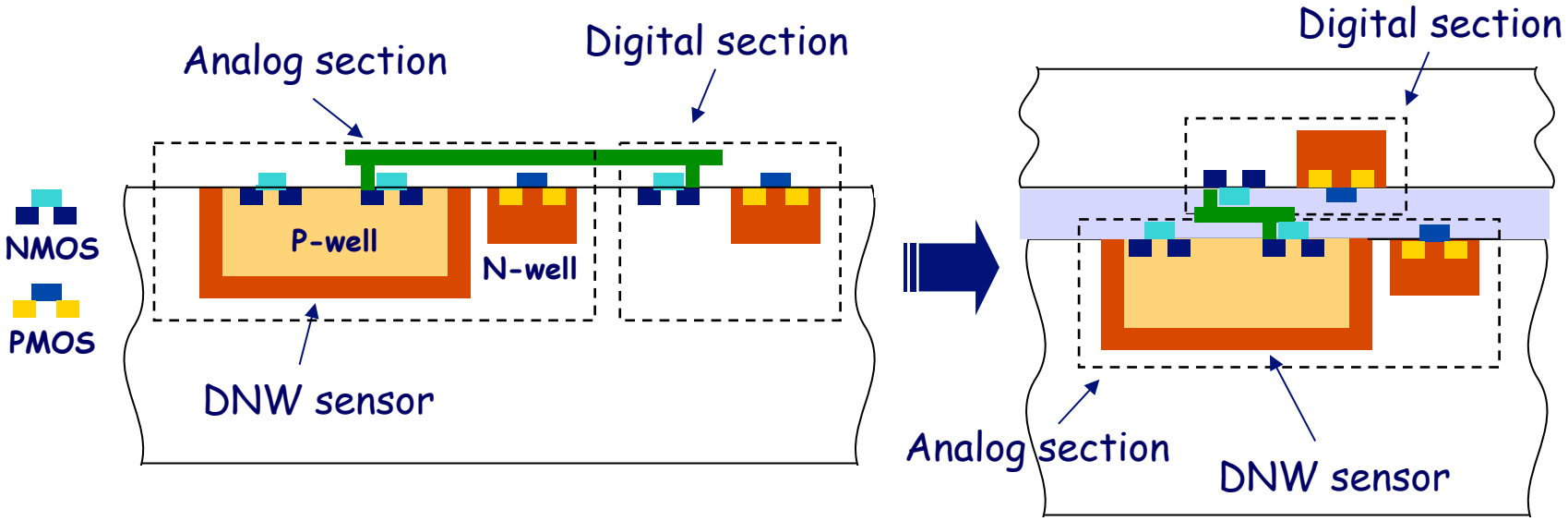


Tezzaron vias are very small: Φ_{via}=1.2 µm, $\Phi_{landing\_pad}$=1.7 µm, d_{min}=2.5 µm

Wafer bonding pads are nominally on a 4 µm pitch

From 2D to 3D CMOS pixel sensors

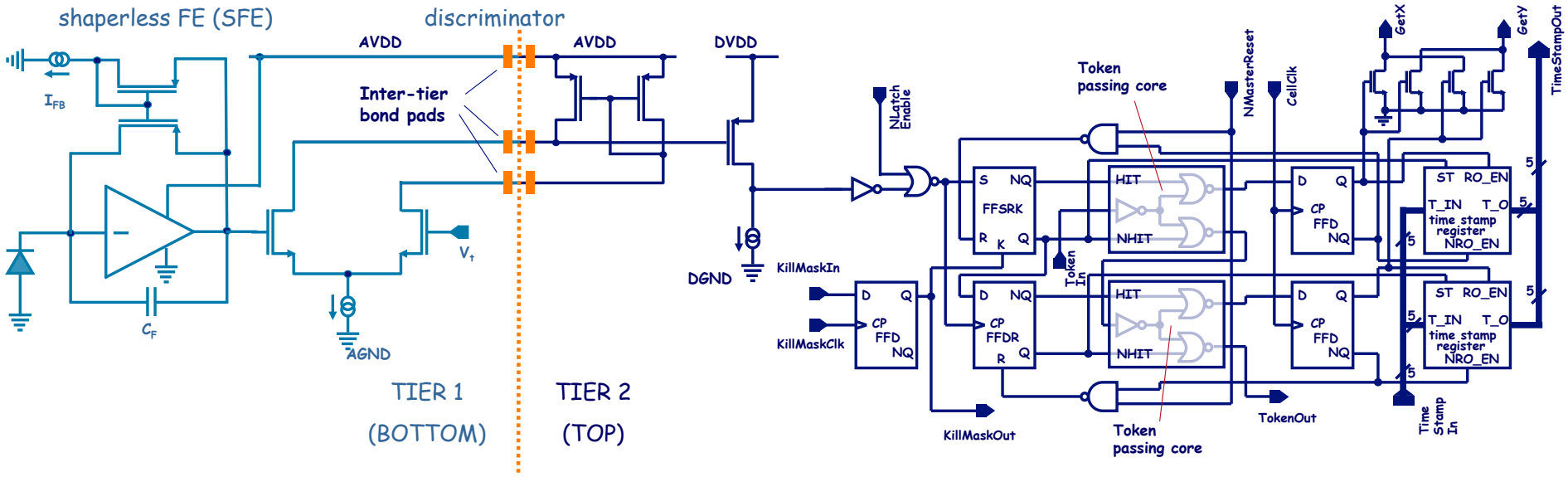
- Guideline: separate analog from digital section to minimize cross-talk between digital blocks and sensor/analog circuits



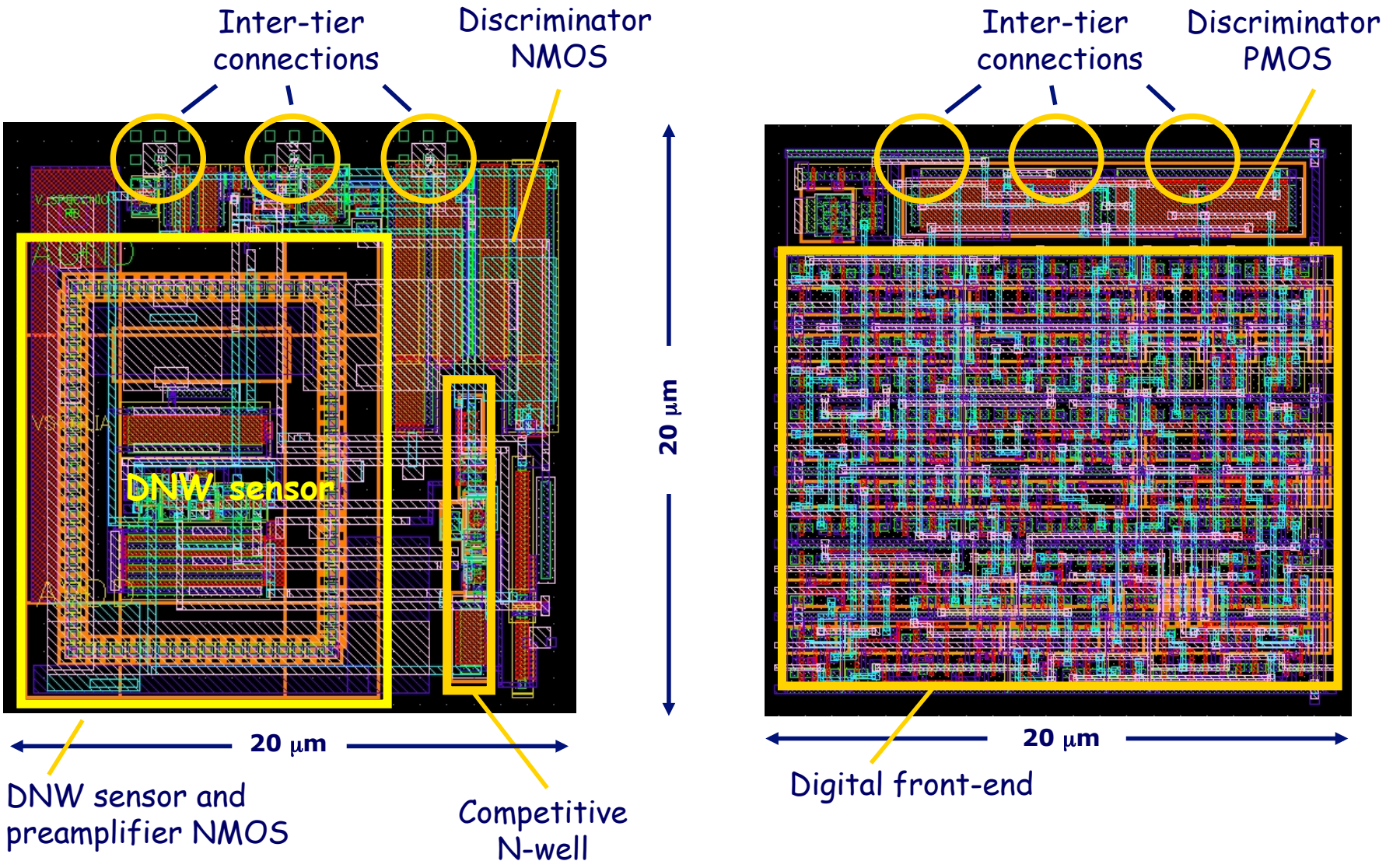
- Tier 1: collecting electrode (deep N-well/P-substrate junction) and analog front-end and discriminator
- Tier 2: digital front-end (2 latches for hit storage, pixel-level digital blocks for sparsification, 2 time stamp registers, kill mask) and digital back-end (X and Y registers, time stamp line drivers, serializer)

Advantages of going 3D

- Pixel-level functionalities: a double-hit detection capability (two flip-flops) is included
- Pixel pitch: reduced from 25 μm to 20 μm
- Pixel "fill factor": increased by a sizable reduction of the area of PMOS N-wells in the sensor layer

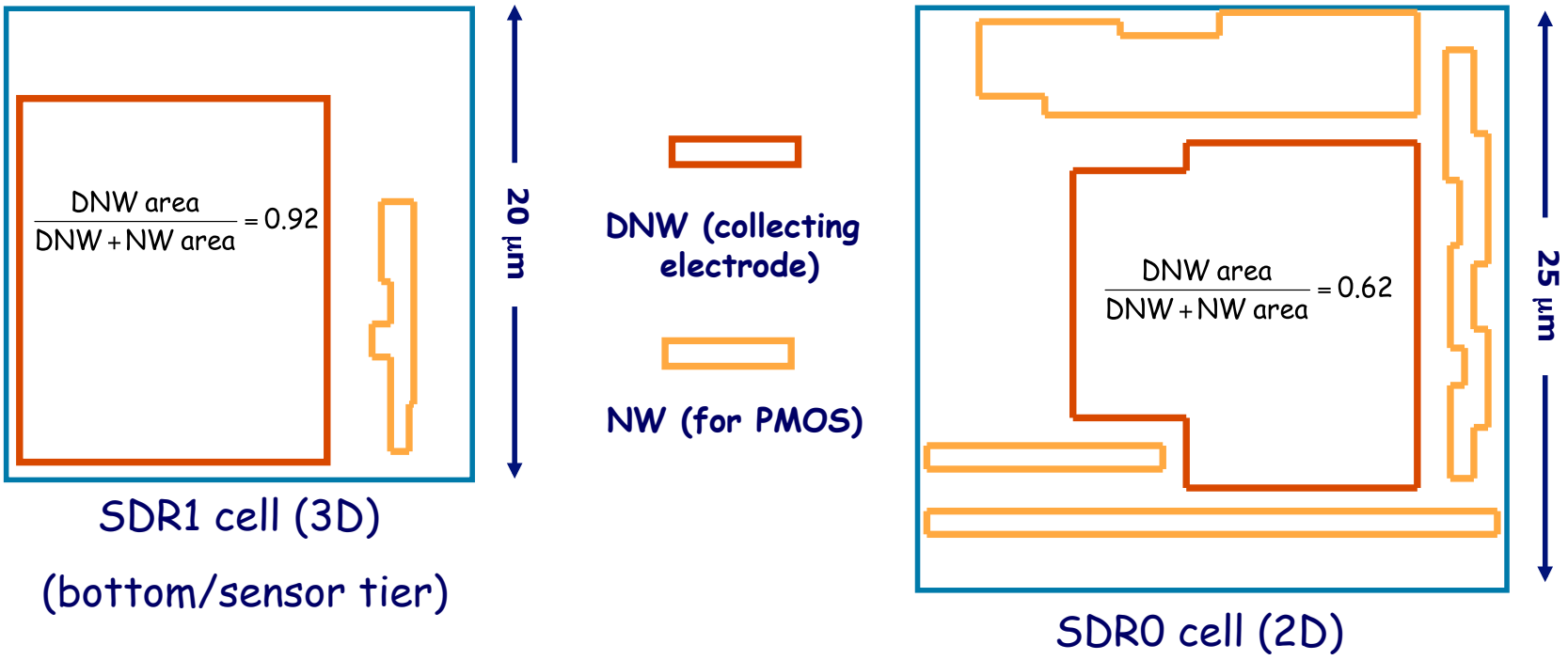


Layout of the 2-tier pixel cell



Collecting electrode layout

- Moving most of the PMOS transistors to the top (digital) tier may significantly improve the detector collection efficiency
- The DNW covers about 35% of the cell area in the SDR0 chip, more than 50% in its 3D release



SDR1 cell (3D)

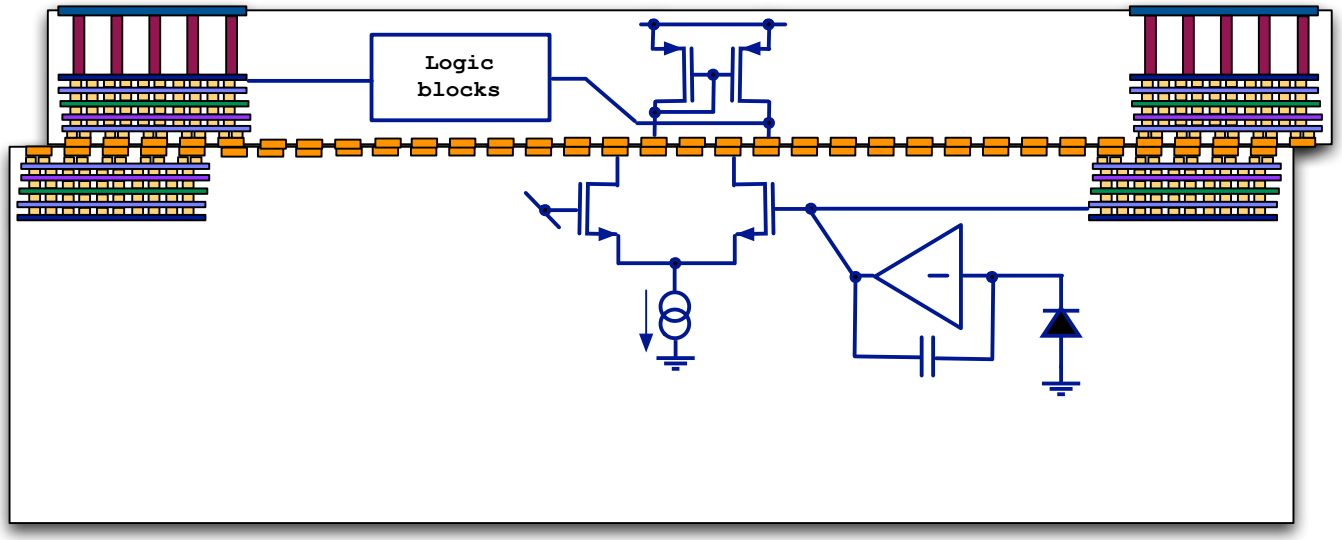
(bottom/sensor tier)

SDR0 cell (2D)

The first 3D DNW CMOS sensors: experimental results

- The processing of 3D devices started about 3 years ago at Tezzaron/ GlobalFoundries and, after many technical problems, only **recently (summer 2012) fully functional chips were delivered**. This is a signature that advanced 3D technologies have not yet reached a full maturity.

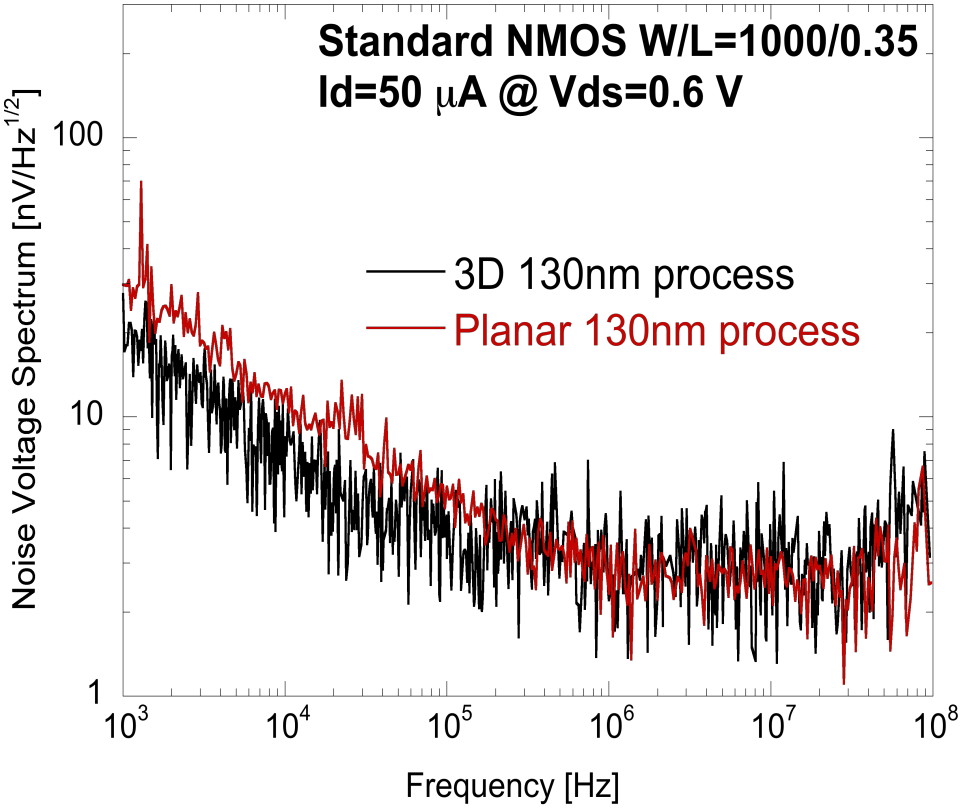
An example of what can go wrong: misalignment in inter-tier connection pads

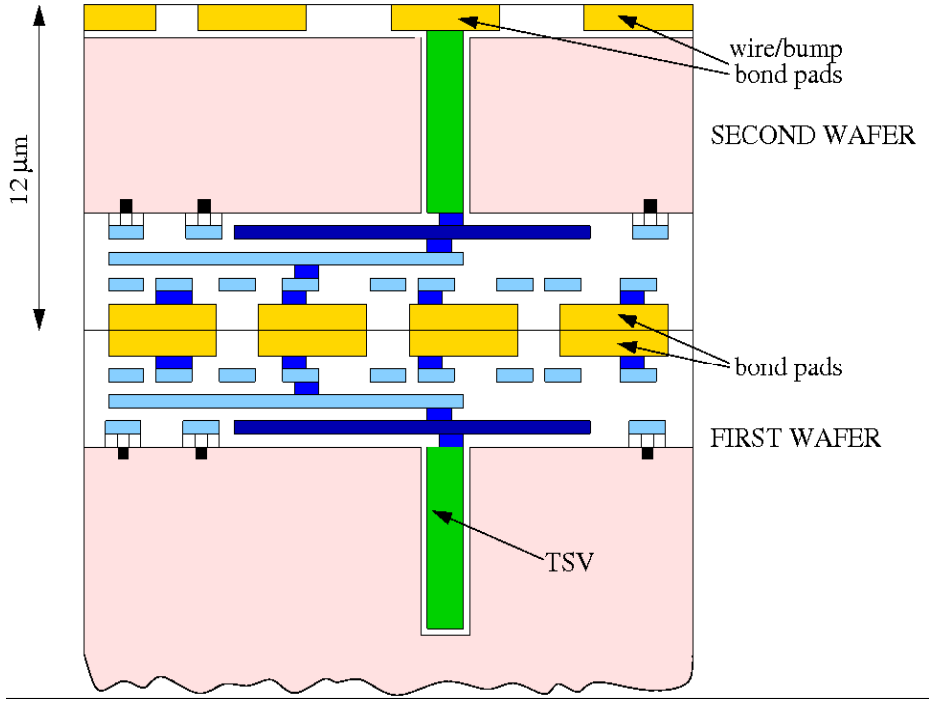


- However, eventually **very good test results on fully working 3D chips provide a demonstration of the potential of 3D integration**, and stimulate further work.

3D processing and MOSFET performance

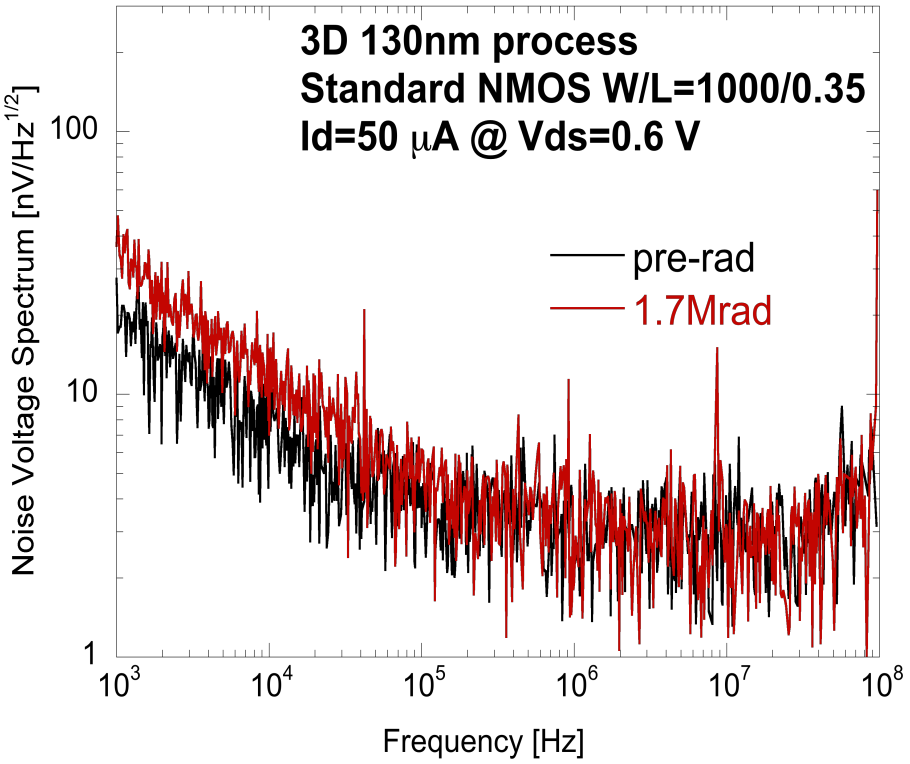
- Processing steps associated to 3D integration involve TSV etching and filling (with mechanical stress on surrounding regions of the silicon bulk), wafer bonding at relatively high temperatures, wafer thinning (12 μm), …
- These steps do not appear to degrade performance of transistors in the thinned layer, with respect to standard CMOS devices in the same 130nm technology node

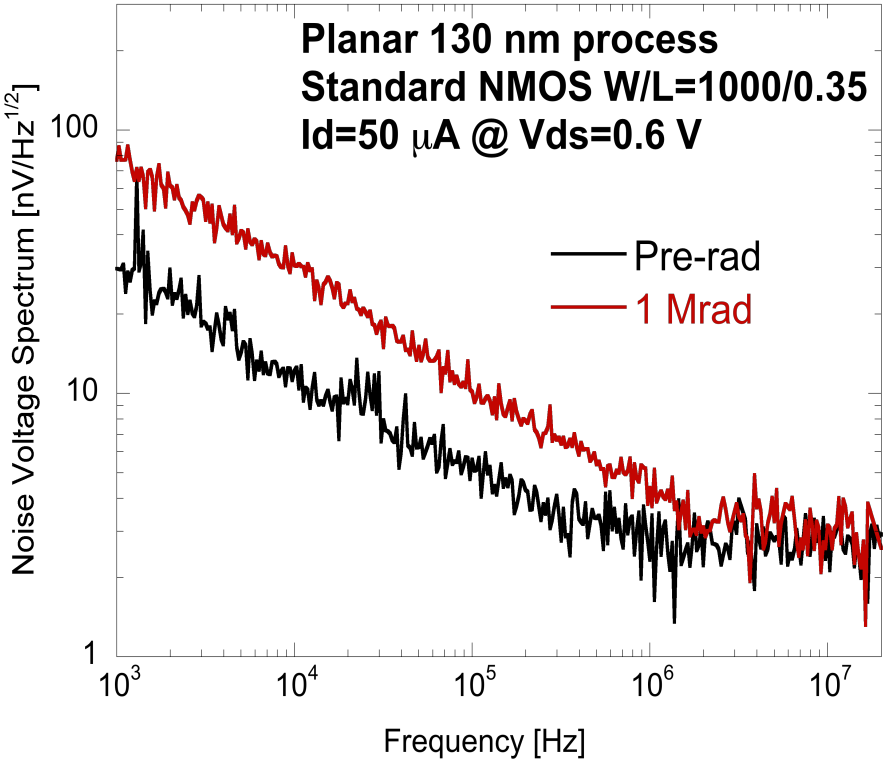




3D processing and MOSFET radiation hardness

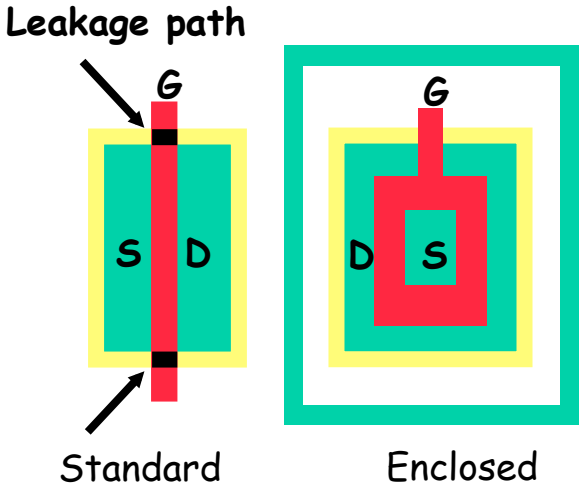
- 3D processing does not appear to degrade MOSFET behavior after exposure to ionizing radiation. On the contrary, the smaller sensitivity (smaller 1/f noise increase in irradiated devices) of 3D-IC NMOSFET could be related to favorable CMOS processing details related to lateral isolation oxides and to bulk doping levels close to STI.

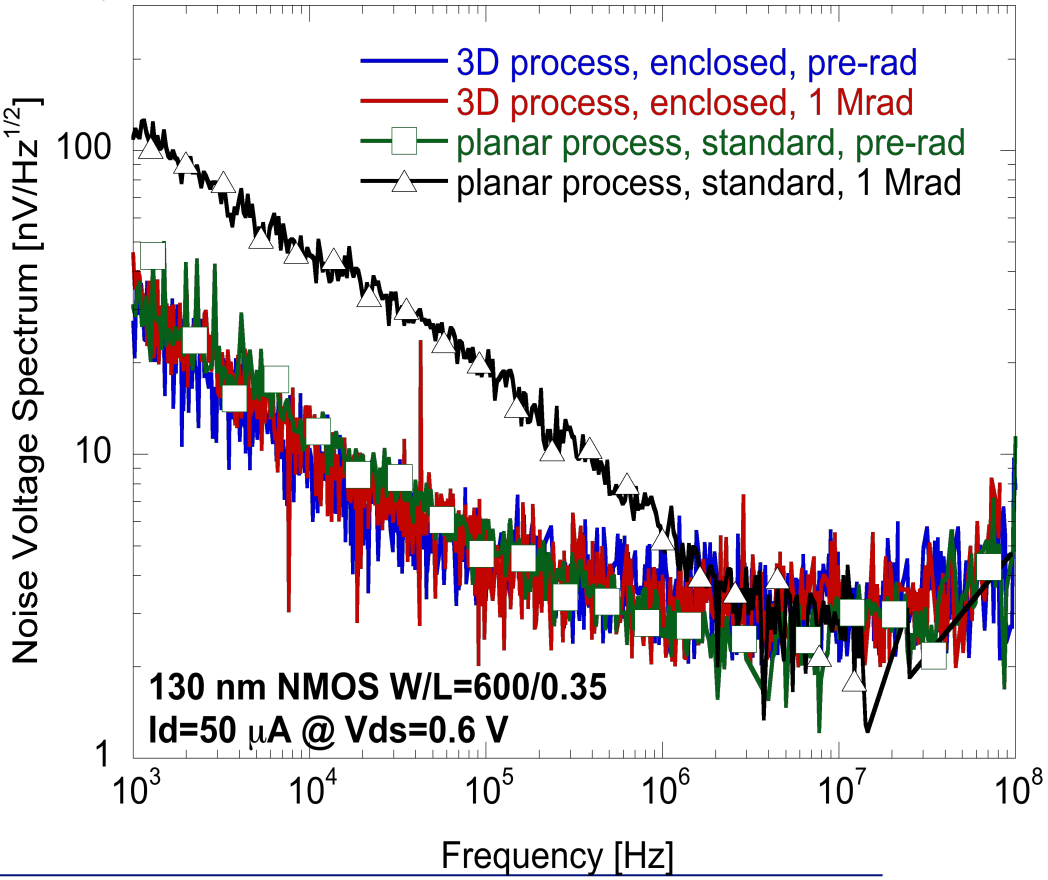




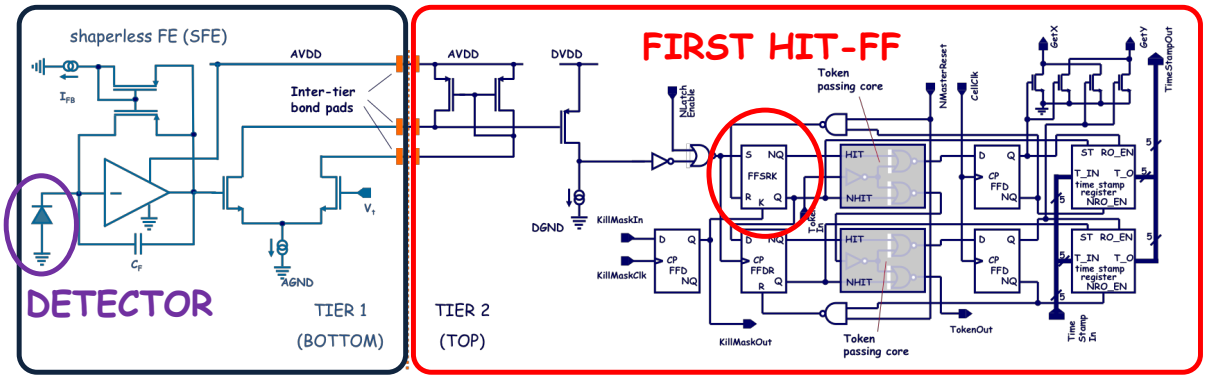
3D enclosed NMOSFETs

- The enclosed layout geometry has been successfully used since the 250 nm node to achieve a large tolerance to very high total doses of ionizing radiation, by **removing lateral leakage paths along lateral thick oxides**. As expected, this technique works also in 3D-IC 130 nm MOSFETs in the Tezzaron/GlobalFoundries process.

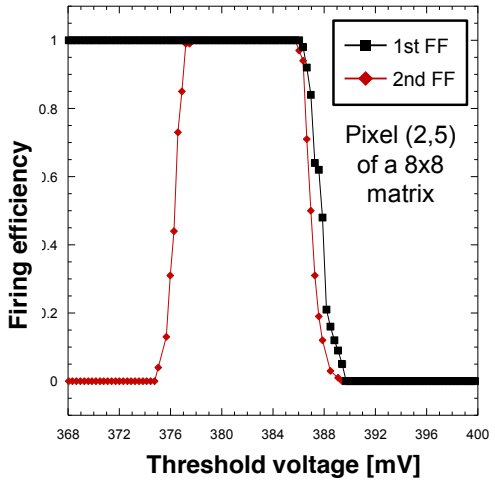


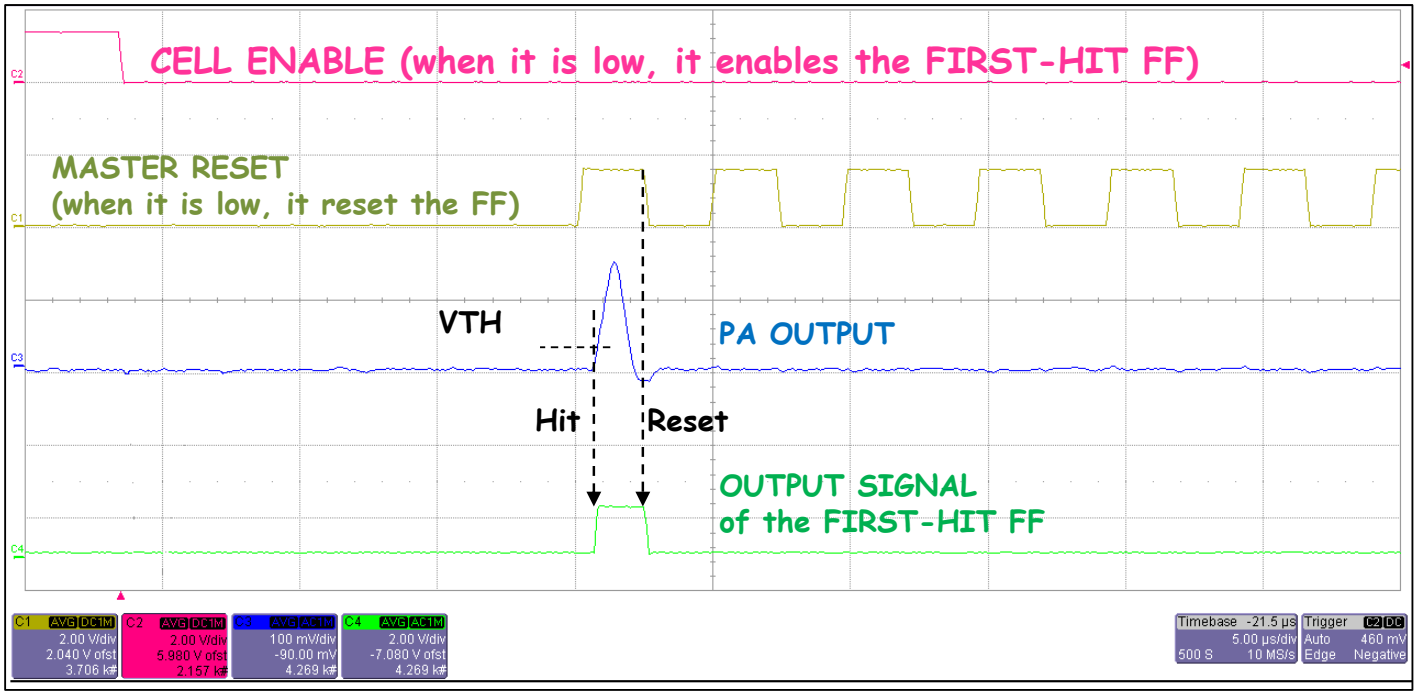


Tests on digital and analog section of 3D DNW sensors

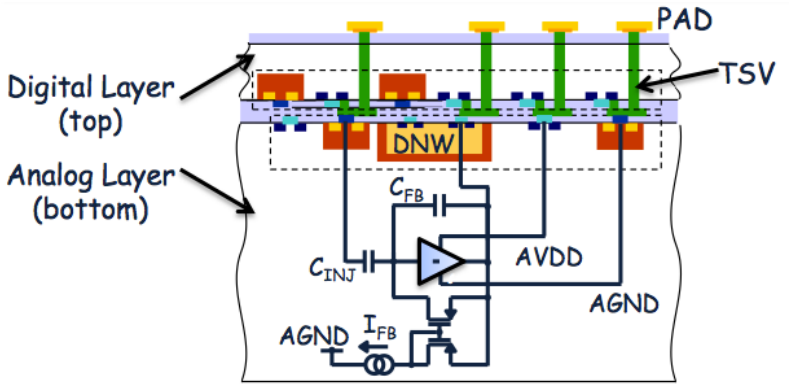


- Tests on SDR1 digital circuits show the full functionality of vertically integrated chips

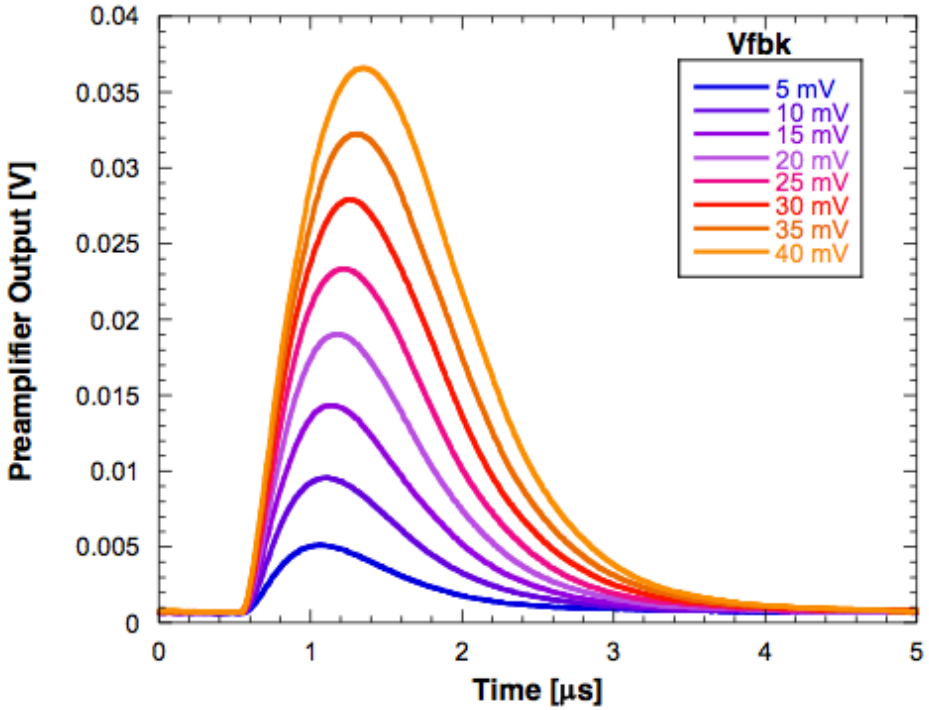


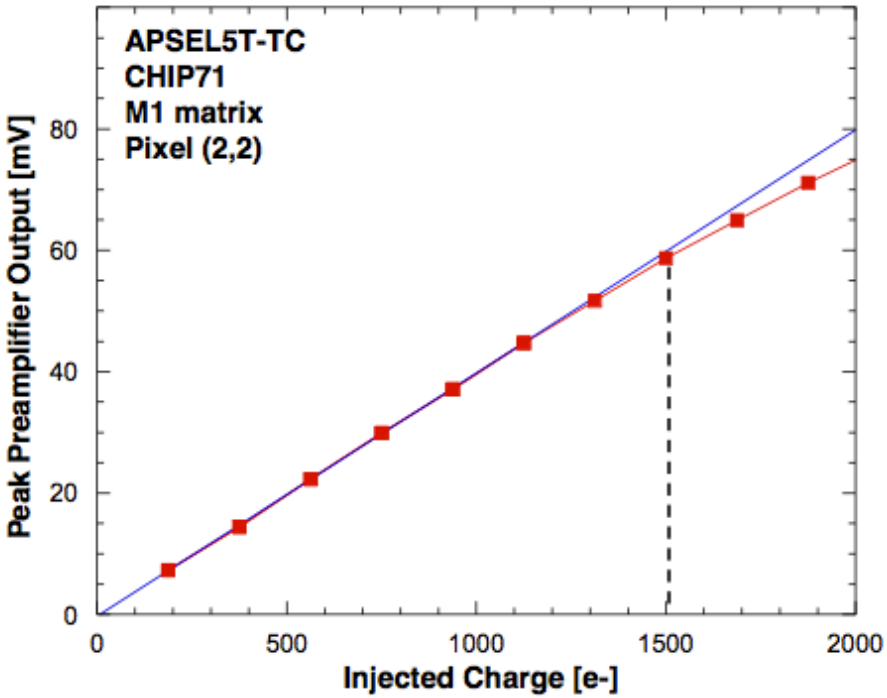


3D DNW MAPS: analog front-end characterization



- Charge sensitivity: 250 mV/fC
- Input dynamic range: 1500 electrons
- ENC: 40 electrons rms
- Power dissipation: 5 μW/pixel



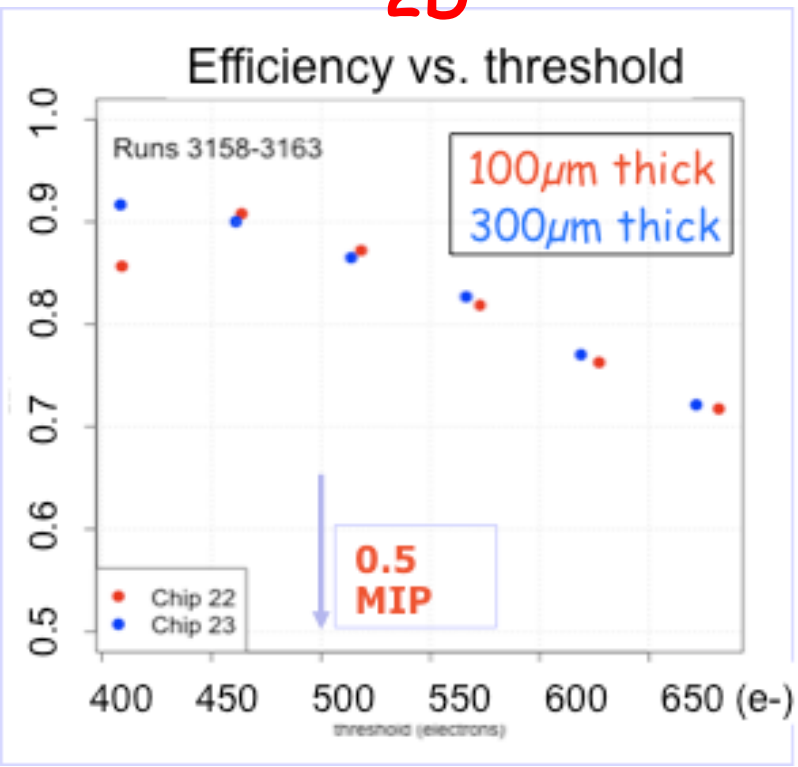


3D integration improves efficiency of DNW CMOS sensors

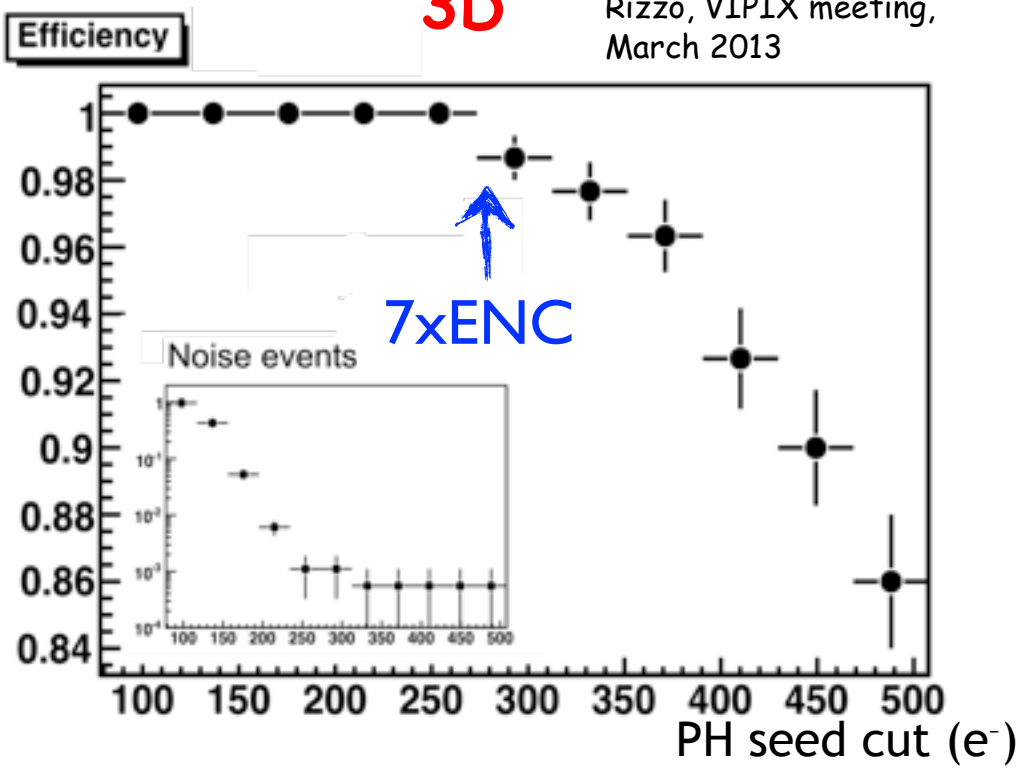
- In the first 3D-IC run, besides "ILC-like" devices, we had also DNW CMOS sensors with continuous sparsified readout (originally developed for SuperB, which was then cancelled), called APSEL.
- Beam test results on these 3D APSEL prototypes confirm the advantage in charge collection efficiency with respect to previous 2D versions, because of the reduction of the area of competitive PMOS N-wells.

S. Bettarini, G. Casarosa, F. Morsani, A. Perez, G. Rizzo, VIPIX meeting, March 2013

2D



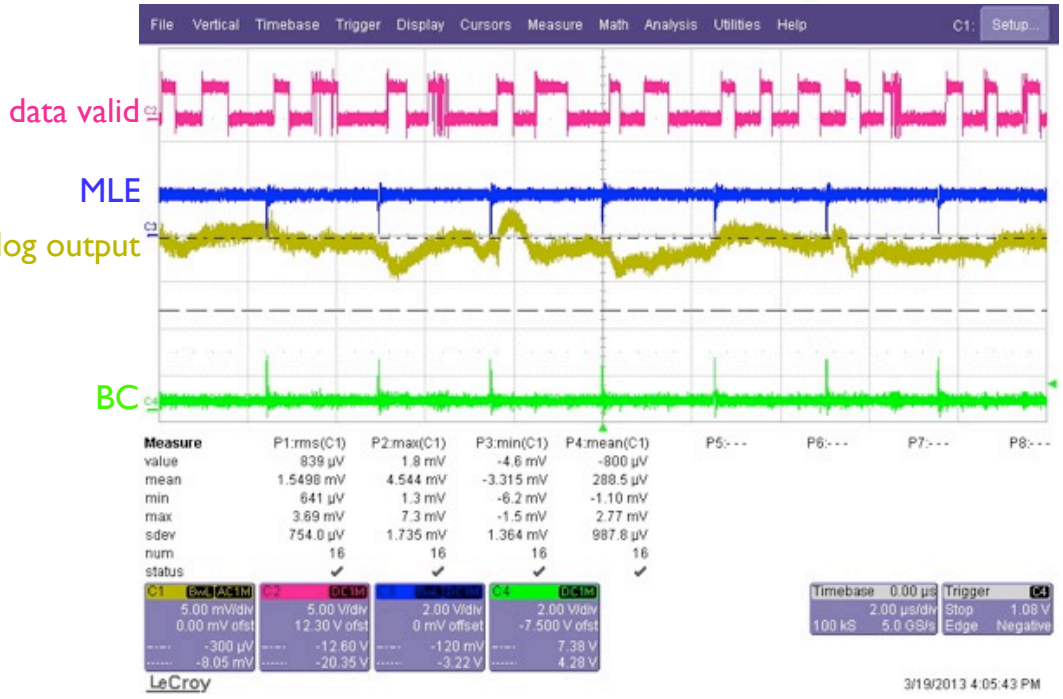
3D



3D integration reduces digital-to-analog interferences

- In the APSEL chips, the digital readout is always up and running (50 MHz clock), sending out data from hit pixels. In 2D versions, coupling of digital signals to the analog front-end was not negligible.
- In the 3D version, thanks to the separation of the analog and digital substrates, digital-to-analog interferences are drowned in the electronic noise and do not give spurious signals.

readout running:



S. Bettarini, G. Casarosa, F. Morsani, A. Perez, G. Rizzo, VIPIX meeting, March 2013

A new generation of 3D chips

- The yield, reliability and turnaround time of the aggressive 3D process we used so far still seem to be an issue.

- Since an experimental proof of 3D-related performance advantages was provided by the first 3D-IC run, there are plans for submitting two new 3D chips, whenever a viable access is provided to the technology.

Main analog features	3D APSEL	SUPERPIX1
Charge sensitivity [mV/fC] @ DAC out	700	50
peaking time [ns]	300	250
ENC [e rms]	40 @ C_D=300 fF	180 @ C_D=150 fF
Threshold dispersion before/after correction [e rms]	106/15	560/65
Pitch [μm]	50	50
Matrix size	128x100	128x32
Power/pixel [μW]	36	13.5

1) Large-scale 3D deep N-well MAPS (3D APSEL)

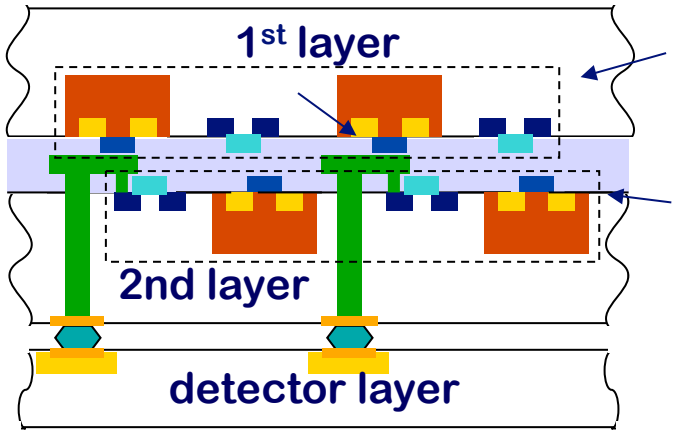
2) 3D readout chip for high resistivity pixel sensors (SUPERPIX1)

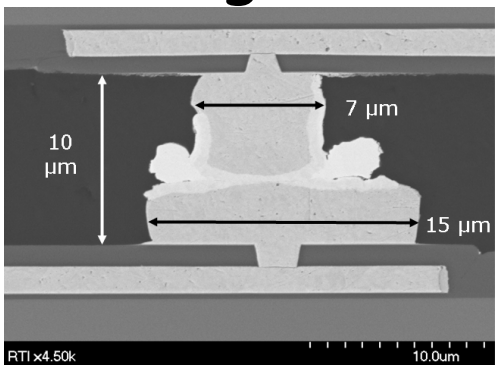
Both chips share a new flexible readout architecture: data push & triggered version

3D readout integrated circuits interconnected to high resistivity sensors:

standard bump bonding vs vertical integration

Bump bonding

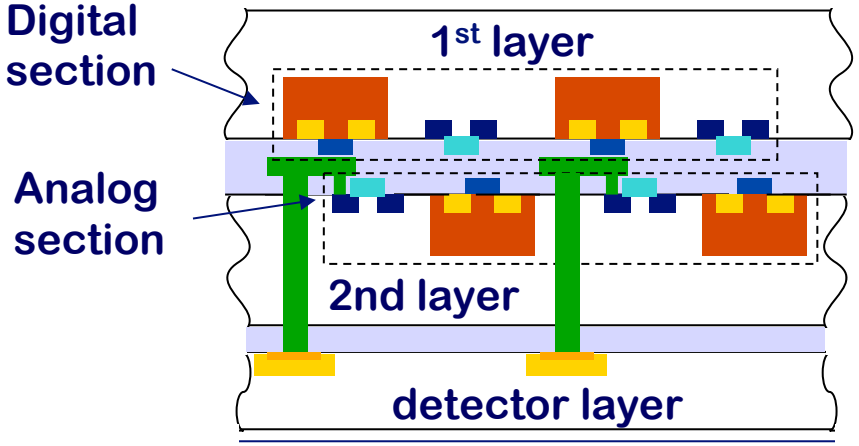




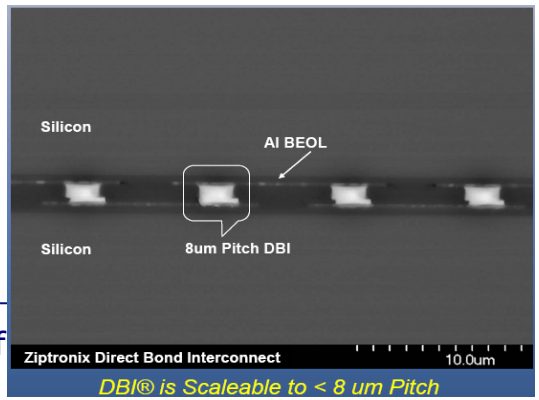
CuSn bond cross section

Conventional solder bumps or more advanced, low pitch CuSn bonding may still pose a problem for low mass assemblies

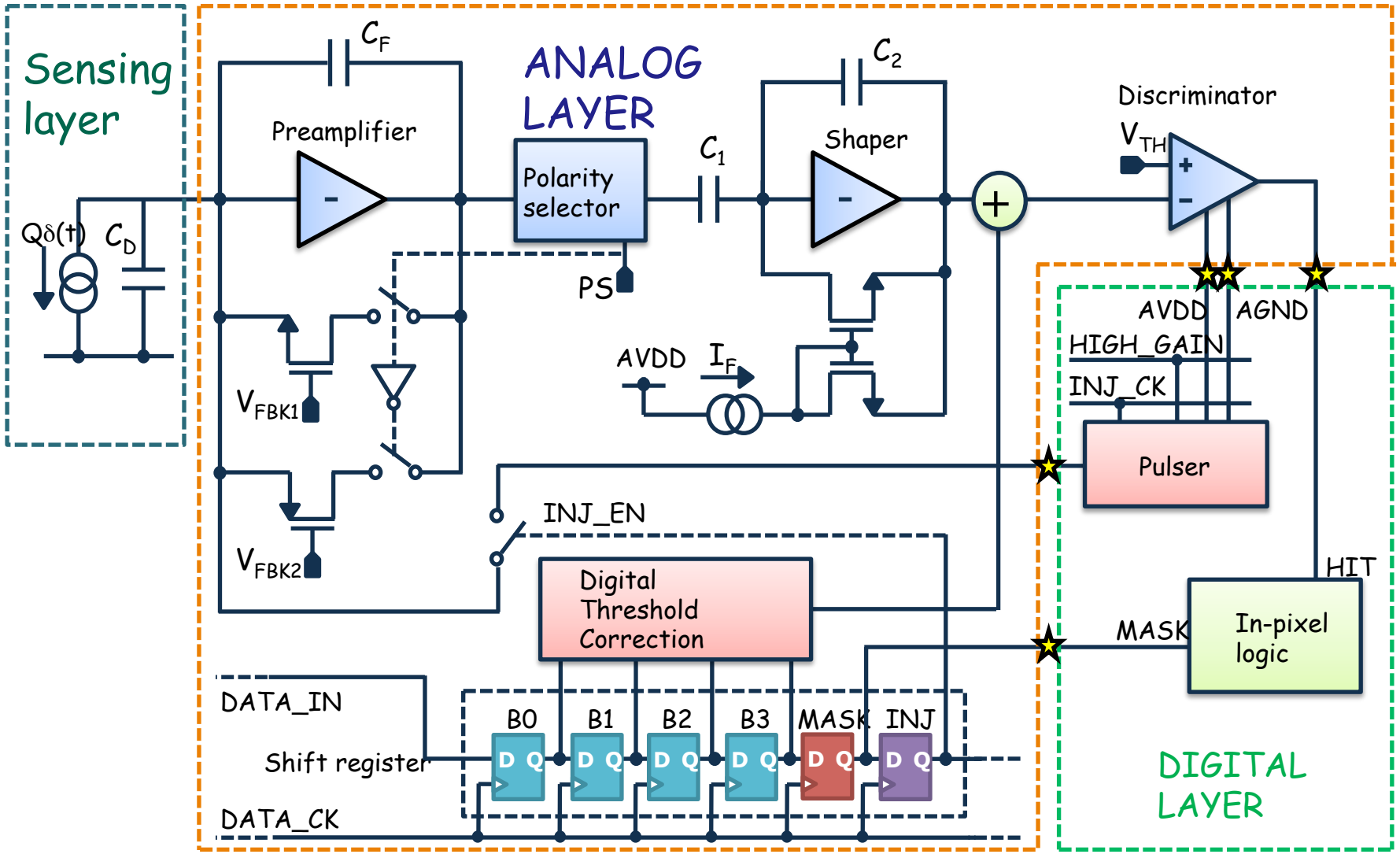
Low-mass bonding of sensors to readout circuits is possible with advanced high-density interconnection technologies



Wafer bonding

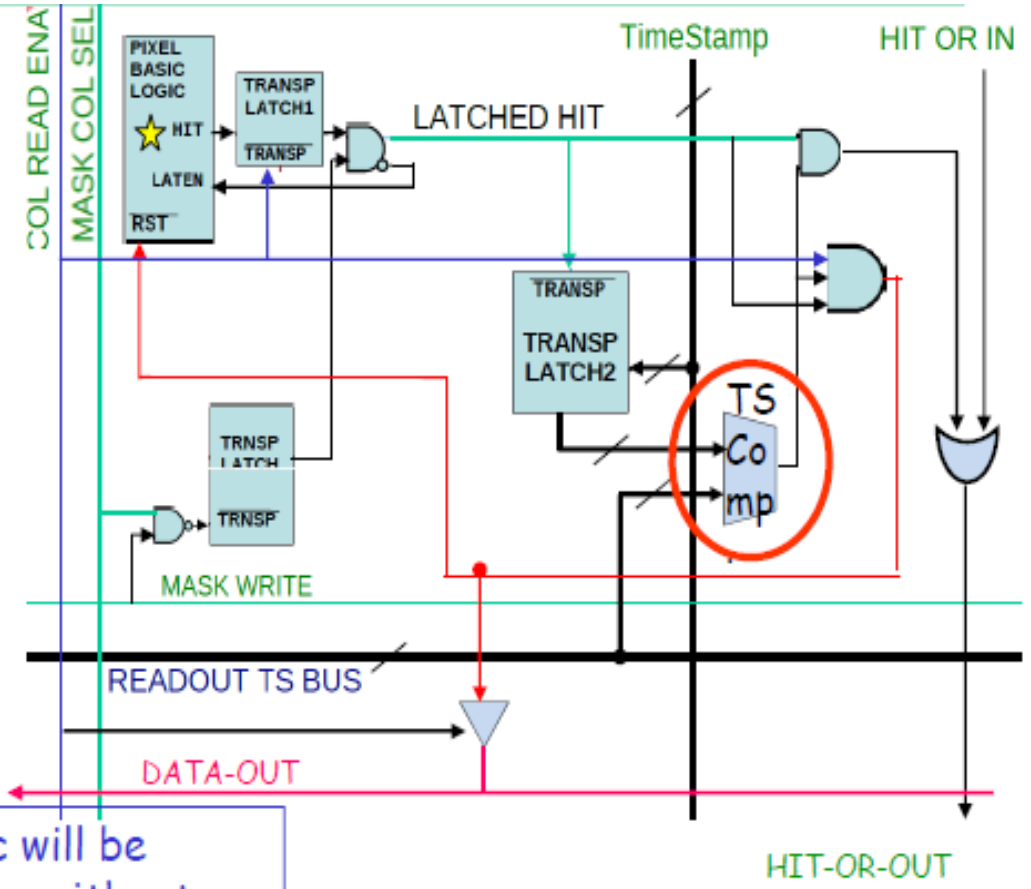


Exploiting 3D integration: the analog section of a 3D readout chip for high resistivity pixels (50 μm pitch)



Exploiting 3D integration: pixel-level logic with time-stamp latch and comparator for a time-ordered readout

- No Macropixel
- Timestamp (TS) is broadcast to pixels & pixel latches the current TS when is fired.
- Matrix readout is timestamp ordered
  - A readout TS enters the pixel, and a HIT-OR-OUT is generated for columns with hits associated to that TS.
  - A column is read only if HIT-OR-OUT=1
  - DATA-OUT (1 bit) is generated for pixels in the active column with hits associated to that TS



- This more complex in pixel logic will be implemented with 3D integration without reducing the pixel collection efficiency ever improving the readout performance (*readout could be data push or triggered*)

VHDL simulation of the data push chip (100MHz/cm^2 input hit rate)

- Readout Effi > 99 % @ 50 MHz clock with timestamp of 200 ns.

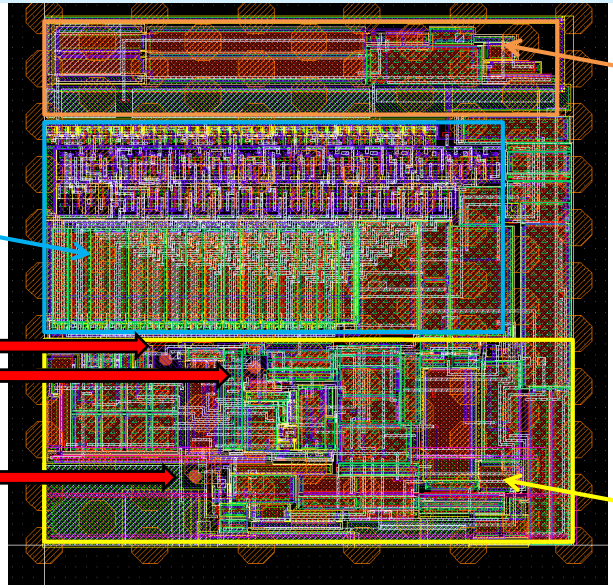
Layout and electronic functions in a 2-tier pixel readout cell (50 x 50 μm²)

Analog tier

DRC
LVS
Routing

DAC, decoder and shift register

3 connections PA input – bump bond pad (Supercontact)



Discriminator

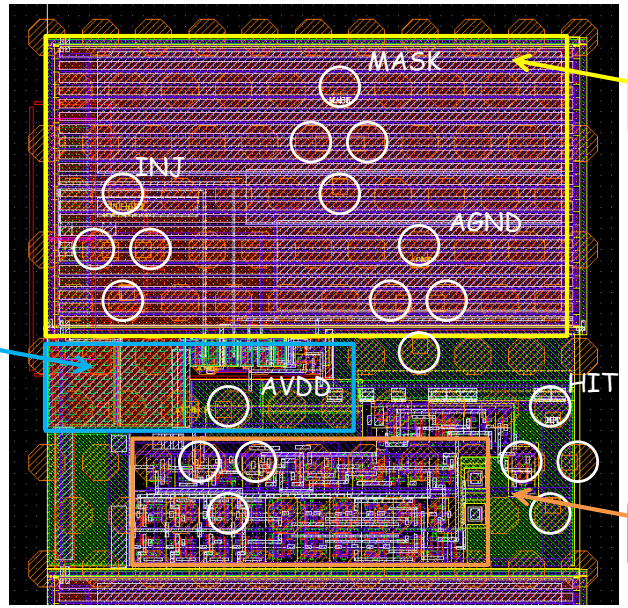
Preamplifier, polarity selector and shaper blocks

Digital tier

(includes a pulser for an accurate calibration of the pixel cell)

DRC
LVS
Routing
Integration with digital front-end (Fabio)

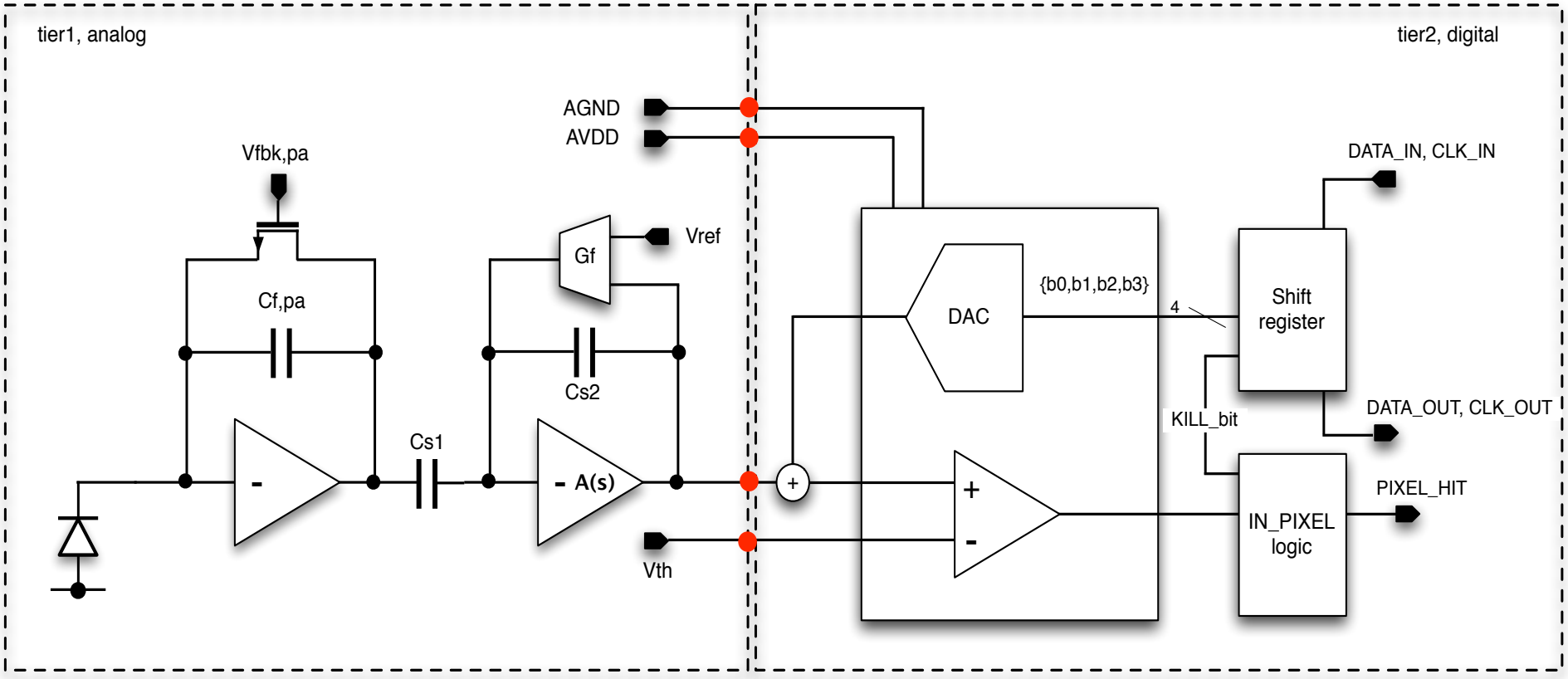
Pulser circuit



poly resistors

In-pixel logic

ApselVI front-end architecture

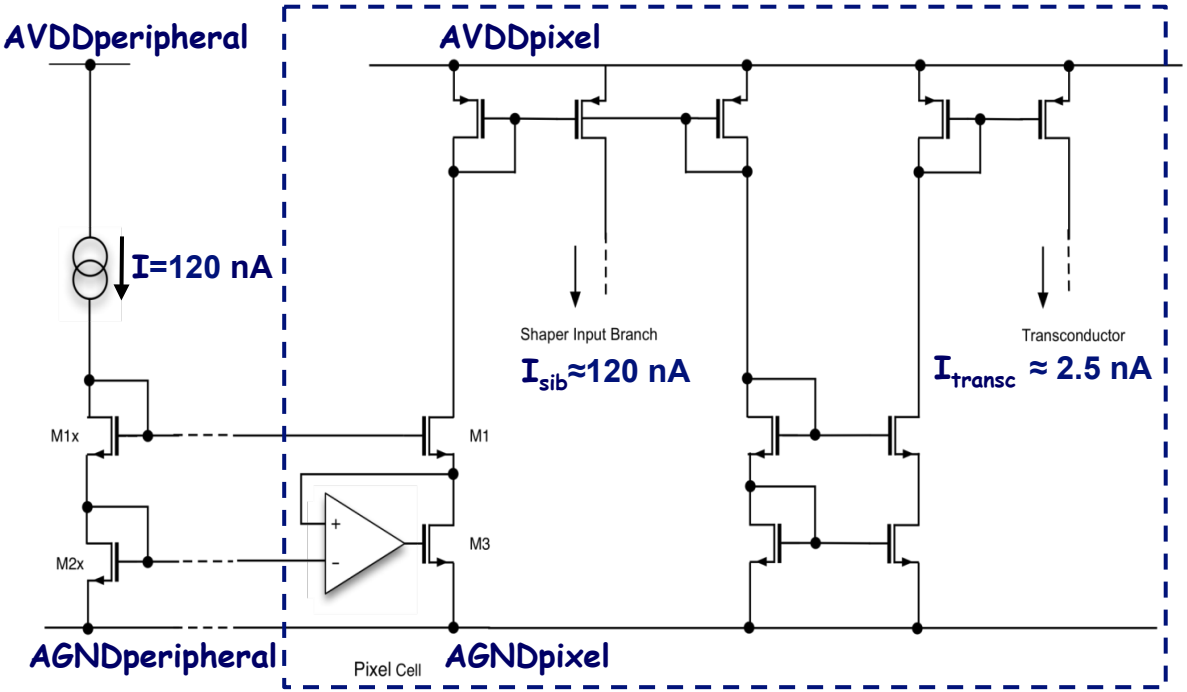


Thanks to 3D integration, the addition of a shaping stage in the analog tier makes it possible to independently optimize noise and threshold dispersion (also with a DAC for local threshold adjustment), achieving a high charge sensitivity in a reliable way

Compensation of power supply voltage drops in a large matrix

- 3D Apsel features:
  - I_{analog_cell}=25 μA
  - 128x100 pixels matrix for the next run
  - Considering the case of a larger matrix, supplied from both sides, we obtain the following voltage drop on AVDD and AGND:

ΔV_d=15/20 mV (typ/max)

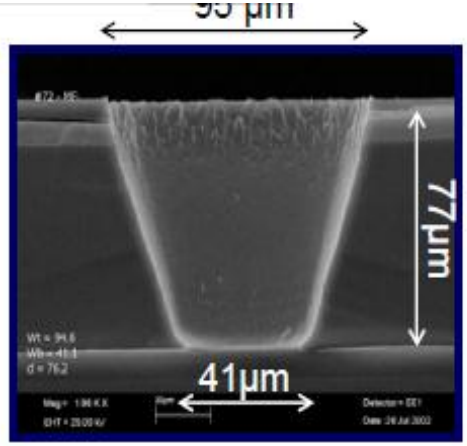


M. Manghisoni, E. Quartieri et al.,"High Accuracy Injection Circuit for Pixel-Level Calibration of Readout Electronics" presented at the *2010 IEEE Nuclear Science Symposium Conference*, Knoxville, USA, October 30 - November 6 2010.

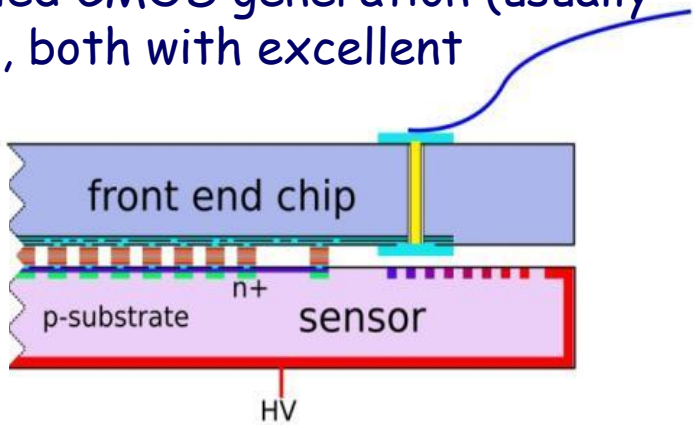
- Voltage drop on the AVDD and AGND lines causes changes in some pixel current sources, in particular in the **shaper input branch** and in the **transconductor**. These current changes lead to a degradation of the front-end performance (i.e. charge sensitivity and peaking time).
- **This problem is overcome by distributing a reference voltage to each pixel according to the schematic above.**

Perspectives and support to 3D integration in the semiconductor detector community

- 3D integrated circuits based on homogeneous layers (same CMOS technology) and high density TSVs and interconnections are a very promising approach to advanced pixel detector readout and other applications.
- The **AIDA WP3** project is supporting the less aggressive **"via last"** variant of 3D integration, where **low-density TSVs are etched in fully processed CMOS wafers**. It is a mature technology, presently available at various vendors.



- This technique makes it possible to **use heterogeneous layers** (different technologies) for sensors and front-end electronics and to fabricate four-side buttable devices with minimal dead area.
- A high-resistivity, fully depleted sensor can be combined in a low-mass assembly with a readout chip designed in an aggressively scaled CMOS generation (usually not available in the typical MAPS "Opto"processes), both with excellent radiation hardness (among other properties).
- Low-density peripheral TSVs can be used to reach backside bonding pads for external connection. The interconnection technology can be chosen according to the pixel pitch.



The diversity of 3D integration approaches: "via first" vs "via last"

- Different approaches to 3D integration differ in terms of the minimum allowed pitch of bonding pads between different layers and of vertical Through-Silicon Vias (TSVs) across the silicon substrate.
- Even with not so aggressive 3D technologies (the so-called "via last" ones, where TSVs are fabricated on fully processed CMOS wafers), a significant advantage can be gained by designing a 2-tier readout chip (for example, analog layer + digital layer)
- In most cases, only one or two connections are needed between the analog and digital blocks of a single pixel cell, and the digital layer can use low-density peripheral TSVs (pitch > 50 μm) to reach backside bonding pads for external connection.
- The "via last" approach was successfully tested by AIDA groups, both for HEP and imaging applications, and may open the way to new design ideas.

New ideas for 3D integration in photon science

At INFN, we are developing plans for a new project, with the goal of developing new detector systems for X-ray imaging applications.

> Potential benefits from 3D vertical integration

- Reduction of pixel size (presently limited by the need of complex electronic functions in the pixel cell)
- Larger memory capacity (store more images)
- Advanced pixel-level processing
- 4-side buttable tiles

Conclusions

- The first 3D-IC run provided demonstrators of 3D CMOS chips, and confirmed potential advantages of 3D integration. The problems associated with this run do not have to prevent us to continue pursuing 3D as a way of devising advanced pixel detectors.
- 3D integration is progressing in the microelectronic industry, and we have to be ready to exploit it. Ultimately, it may allow designers to avoid using sub-50 nm processes for analog and digital circuits in very small pixel readout cells.
- R&D activities in these technologies have to be supported by our community, since they enable new concepts for detector systems. AIDA WP3 is doing this job of testing diverse approaches to 3D.
- Technology watch for novel devices and processes (including 3D integration) has to continue, since the evolution of microelectronics is not going to end soon.

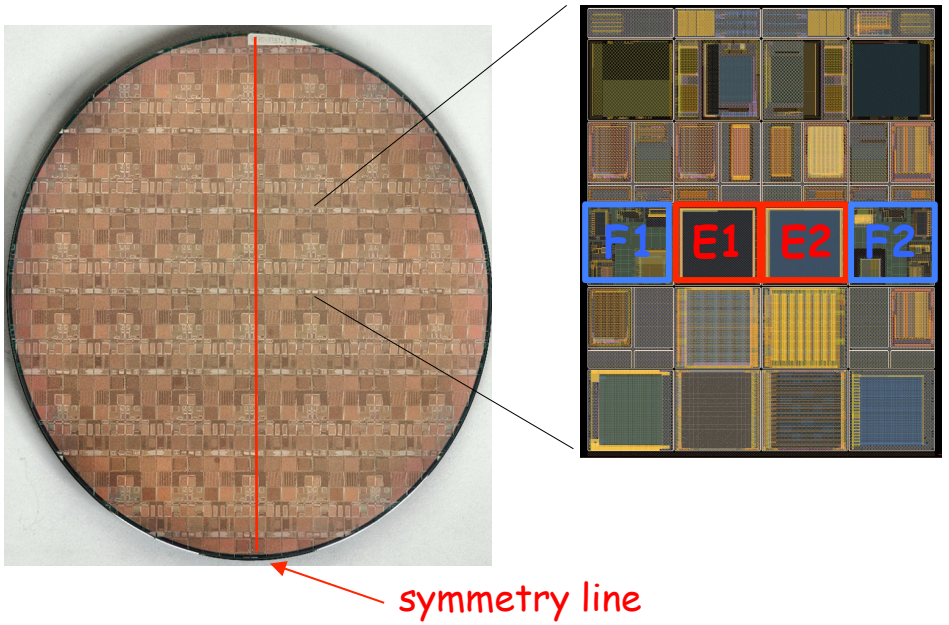
Backup slides

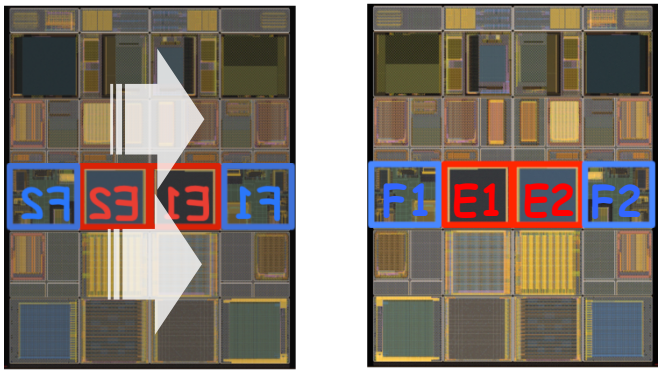
3D Technology Advantages for pixel sensors

- Aggressive thinning leads to low mass circuits resulting in low particle scattering applications.
- New bonding technologies for 3D lead to alternatives to conventional bump bonding that can provide lower mass, finer pitch, and enhanced mechanical robustness for additional mechanical processing (thinning without destroying the connections)
- Via formation allows for increased circuit density with multiple tiers, and/or allows for 4 side buttable circuits.
- 3D via formation allows for mixed circuit technology design and independent analog and digital substrates.

First MPW run of the 3D-IC consortium

- ✓ Several groups from US and Europe have been involved in the first 3D MPW for HEP (pixel and strip readout chips for ATLAS, CMS, B-factory, ILC) and photon science applications (X-ray imaging)
- ✓ Single set of masks used for both tiers to save money
  - ✓ identical wafers produced by Chartered (now GlobalFoundries) and face-to-face bonded by Tezzaron
  - ✓ backside metallization by Tezzaron

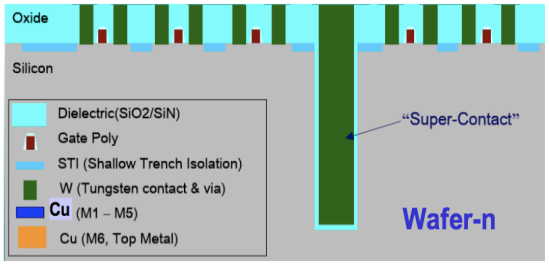




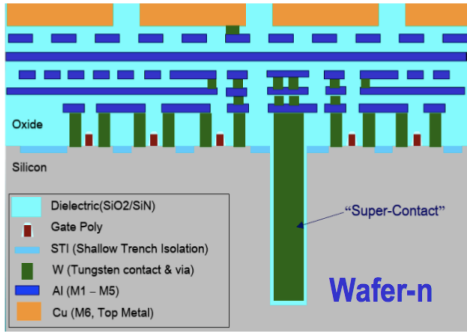
Top layer flipped over Bottom layer

Tezzaron vertical integration (3D) process

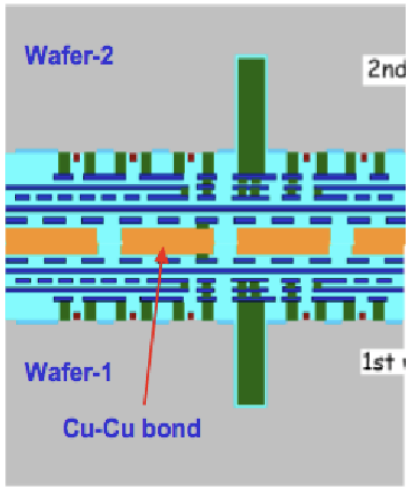
Tezzaron uses a "via middle" approach for the fabrication of 3D chip



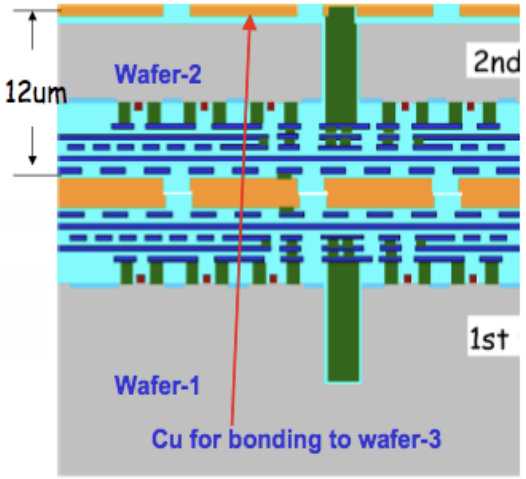
Step 1: On all wafer to be stacked complete transistor fabrication, form TSV, passivation and fill TSV at same time connections are made to transistors



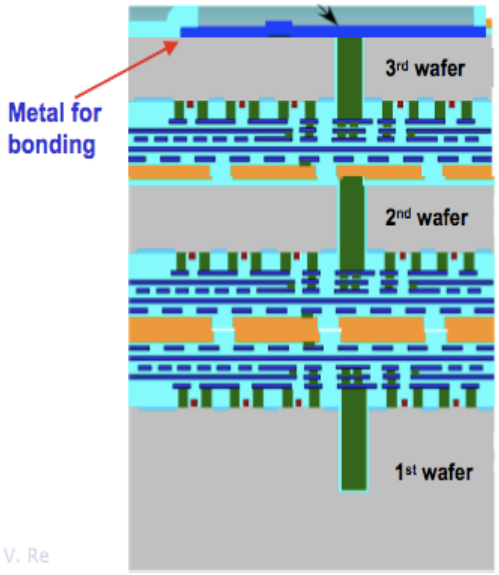
Step 2: Complete back end of line (BEOL) process by adding Al metal layers and top Cu metal (0.7um)



Step 3: bond wafer 2 to wafer 1 (Cu-Cu thermo-compression bond)



Step 4: thin the wafer 2 to about 12um to expose TSV. Add Cu to back of wafer 2 to bond wafer 2 to wafer 3 OR add metallization on back of wafer 2 for bump bonding or wire bonding

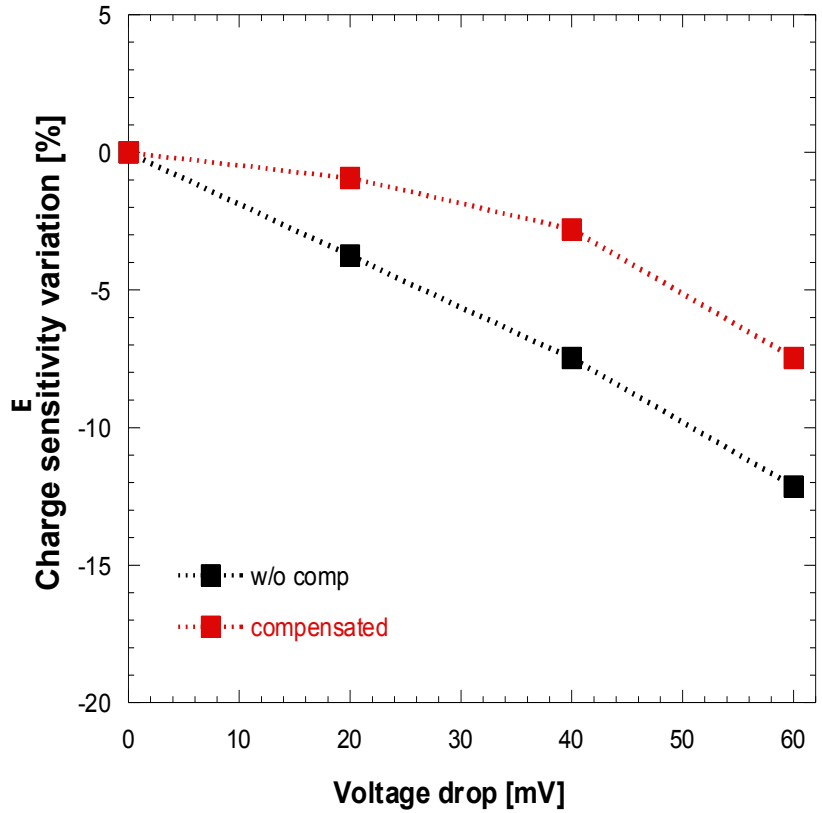


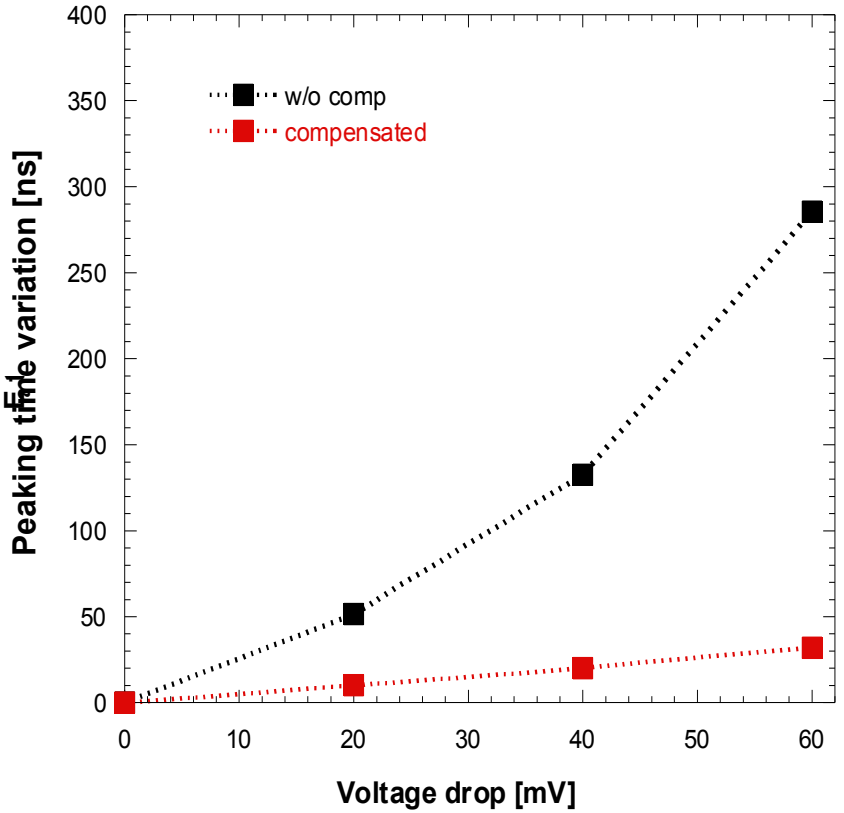
Step 5: stack wafer 3, thin wafer 3 to expose TSV, add final passivation and metal for bond pads

Effect of compensation of power supply voltage drops on peaking time and charge sensitivity

- Voltage drop is simulated as a symmetrical voltage variation in the analog power (AVDD) and ground (AGND) lines.

$$AVDD=1.5\ V-\Delta V_d,\ AGND=\Delta V_d$$





Requirements of pixel sensors in future High Energy Physics experiments

Depending on the application, some (or all!) of the following requirements must be taken into account:

- **Pixel pitch < 20 μm**
- **Timing resolution ~ 25 ns**
- **High radiation tolerance**: total ionizing dose > 100 Mrad, 10^{16} neutrons/cm^2
- **Sensor thickness < 50 μm** (0.1% X_0 per layer at ILC)
- **Noise: 10 – 100 electrons rms**

  S/N adequate to detection of small signals (few hundreds – few thousands electrons); signal ÷ thickness of active sensing layer; depends also on radiation-induced damage
- **Low power dissipation** (~ 100 μW/cm^2 average, may require power cycling)
- **Processing of events with very high rate**

  even with zero suppression, chip architectures with output data rates of 320 MHz;

  detector modules require data links with rate capability ~ 5 Gbps