Towards edgeless detector tiles, using 3D-Integration

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HELMHOLTZ ASSOCIATION

DESY

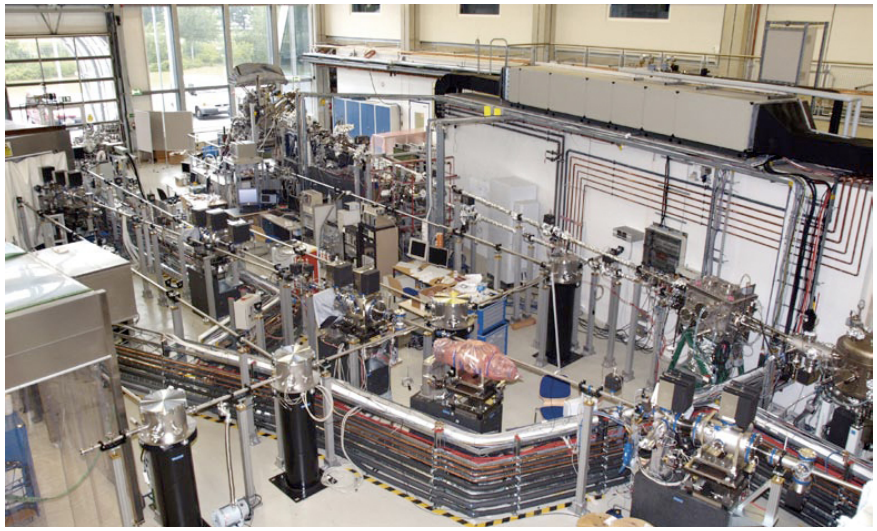
Layout

- What is X-ray Photon-Science about and why do we want edgeless tiles ?
- What is our current state-of-the-art and what are the steps to take ?
- What would we really like to have ?

Large scale X-ray facilities

PETRA III

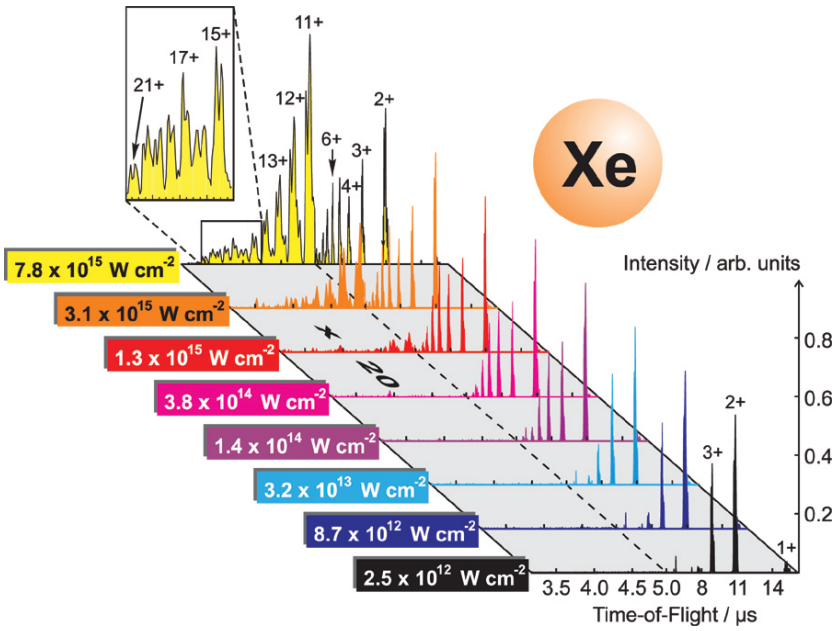
FLASH I



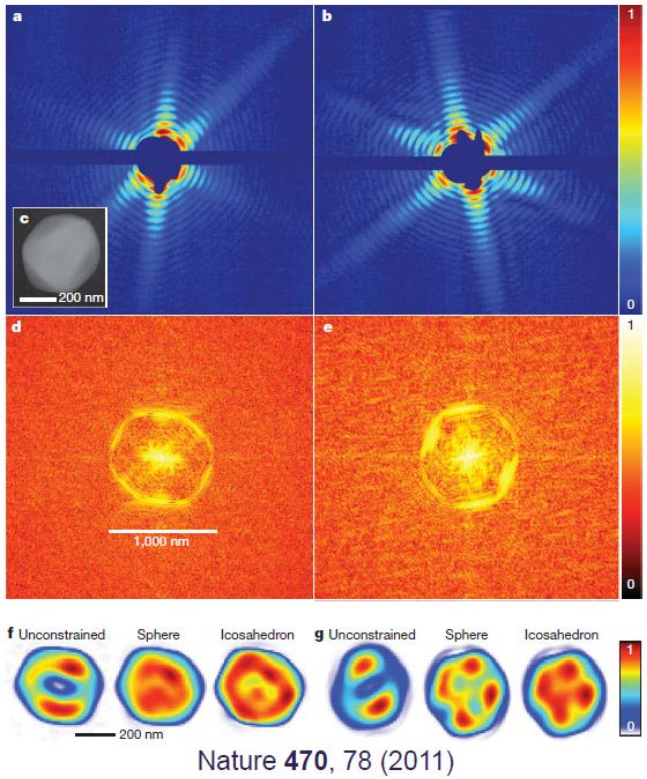
European XFEL

From fundamental to applied science

Study of extremely charged ions



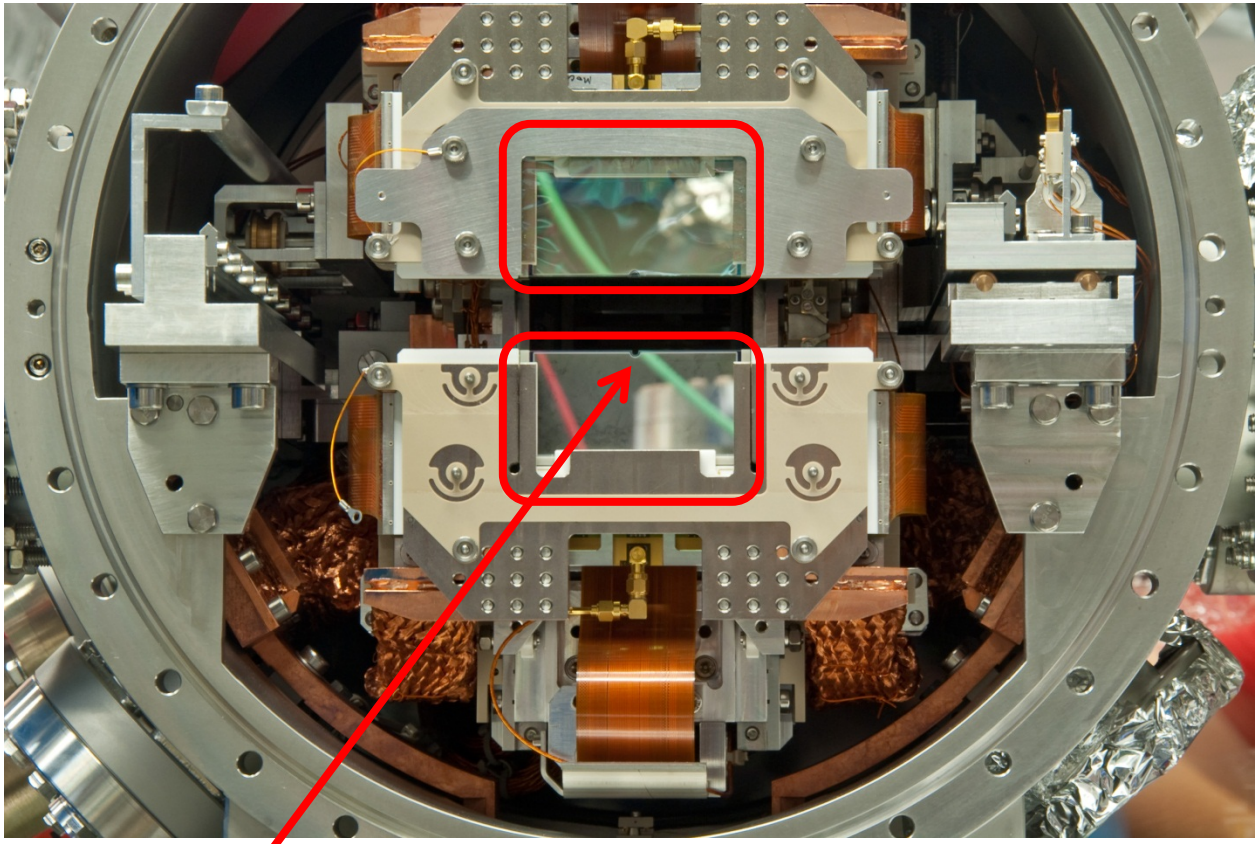
Structure of viruses



Authentication of paintings

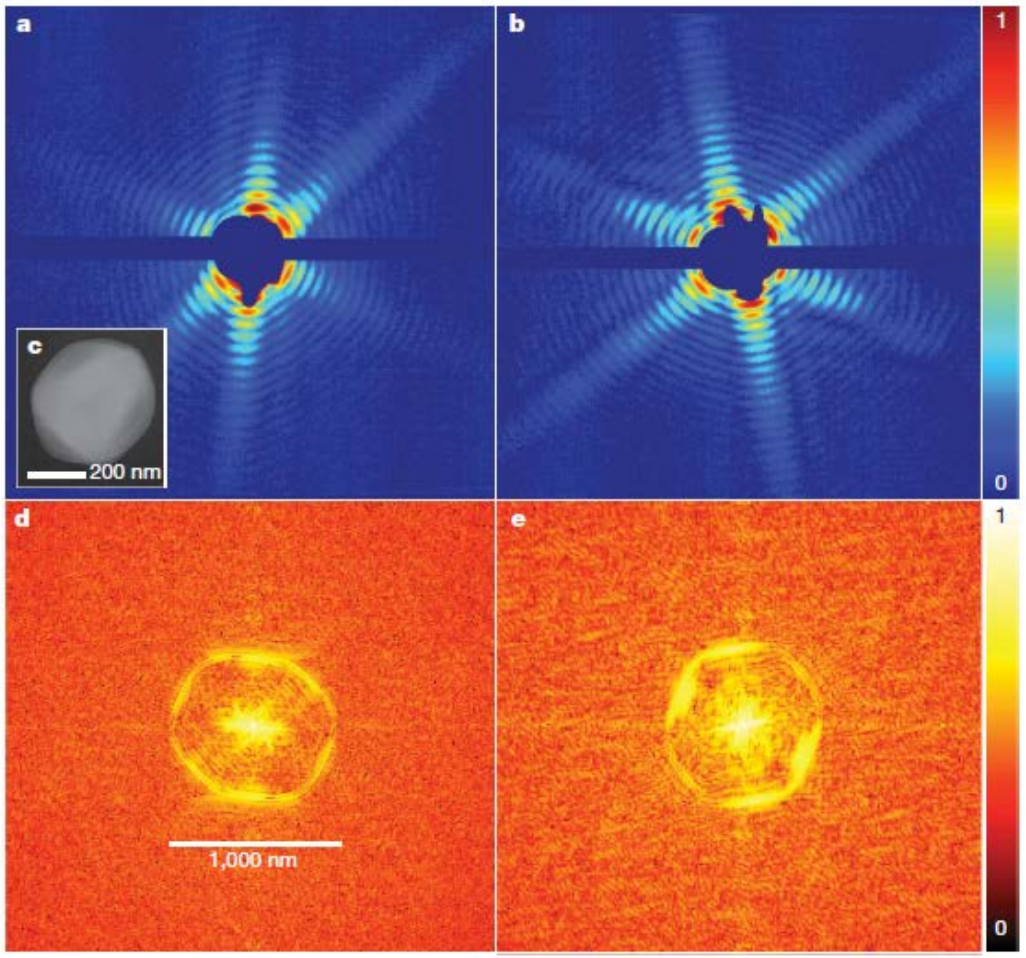
The problem of missing data, an example:

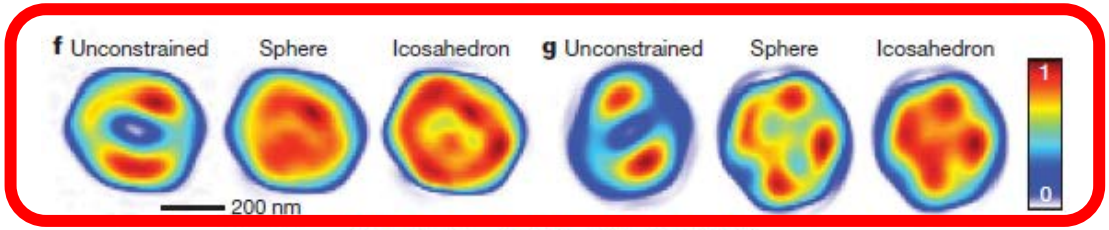
2 pnCCD at LCLS (CAMP-Chamber)



Hole for the direct beam

The problem of missing data, an example:



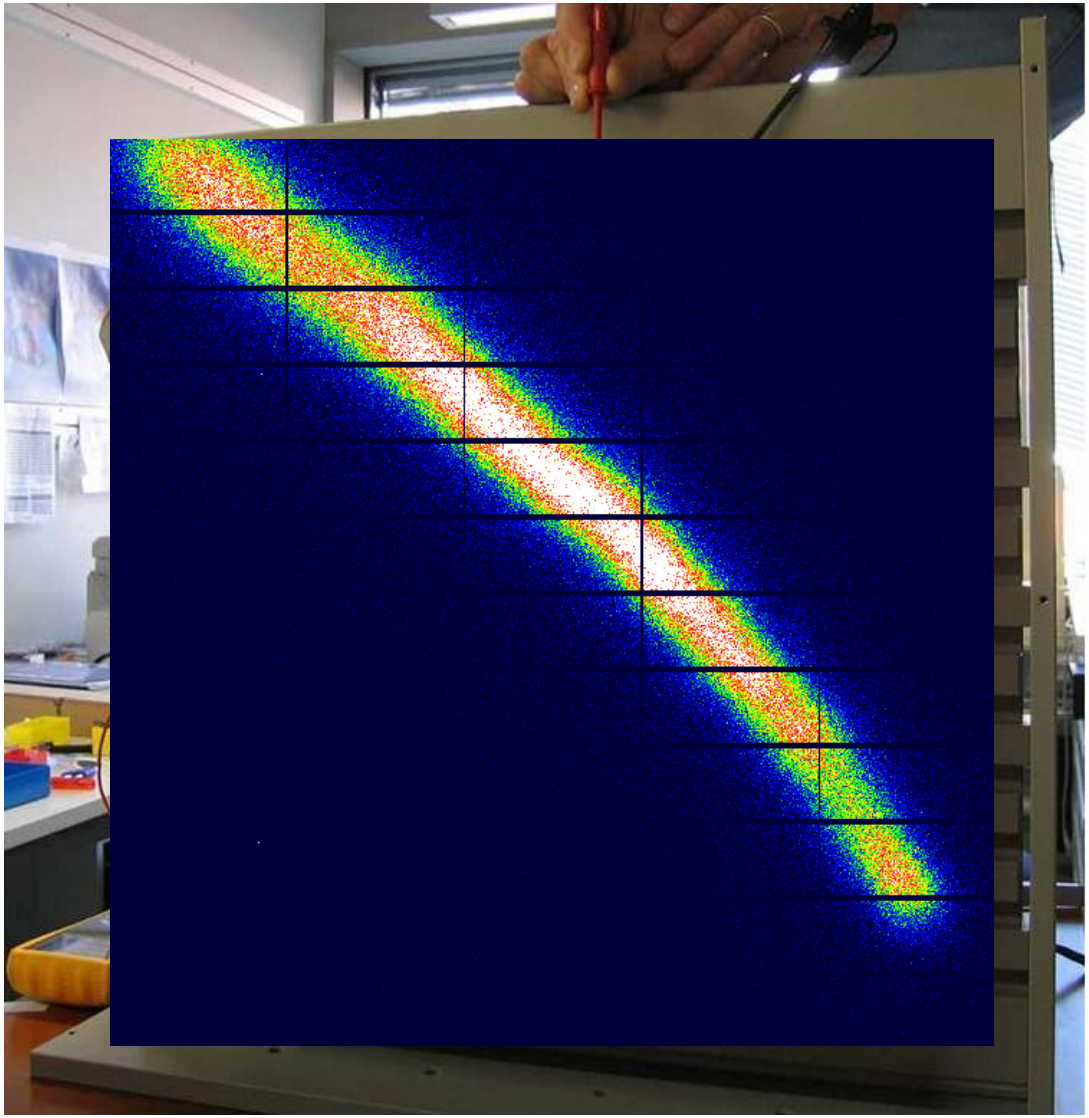


Nature **470**, 78 (2011)

What happens, if central speckle (or more) is not measured?

- The reconstruction becomes ambiguous …
- Quantitative character of the method is lost
- High resolution diffraction signal does NOT help here

Our current state of the art



Hybrid Pixel Array Detectors

- **Modules of limited size**
- **Gap between modules**

➔ **Lots of missing data**

Hybrid Pixel Array Detector (HPAD) Principle

Diode Detection Layer

- **Fully depleted, high resistivity**
- **Direct x-ray conversion**
- **Silicon, GaAs, CdTe, etc.**

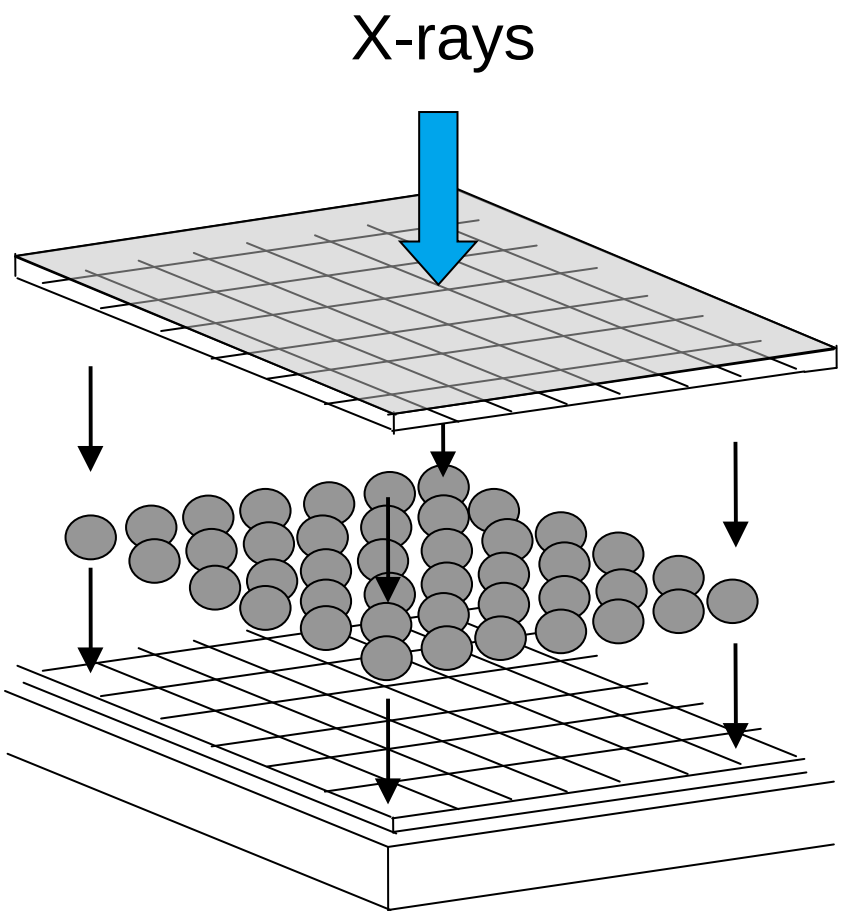
Connecting Bumps

- **Solder or indium**
- **1 per pixel**

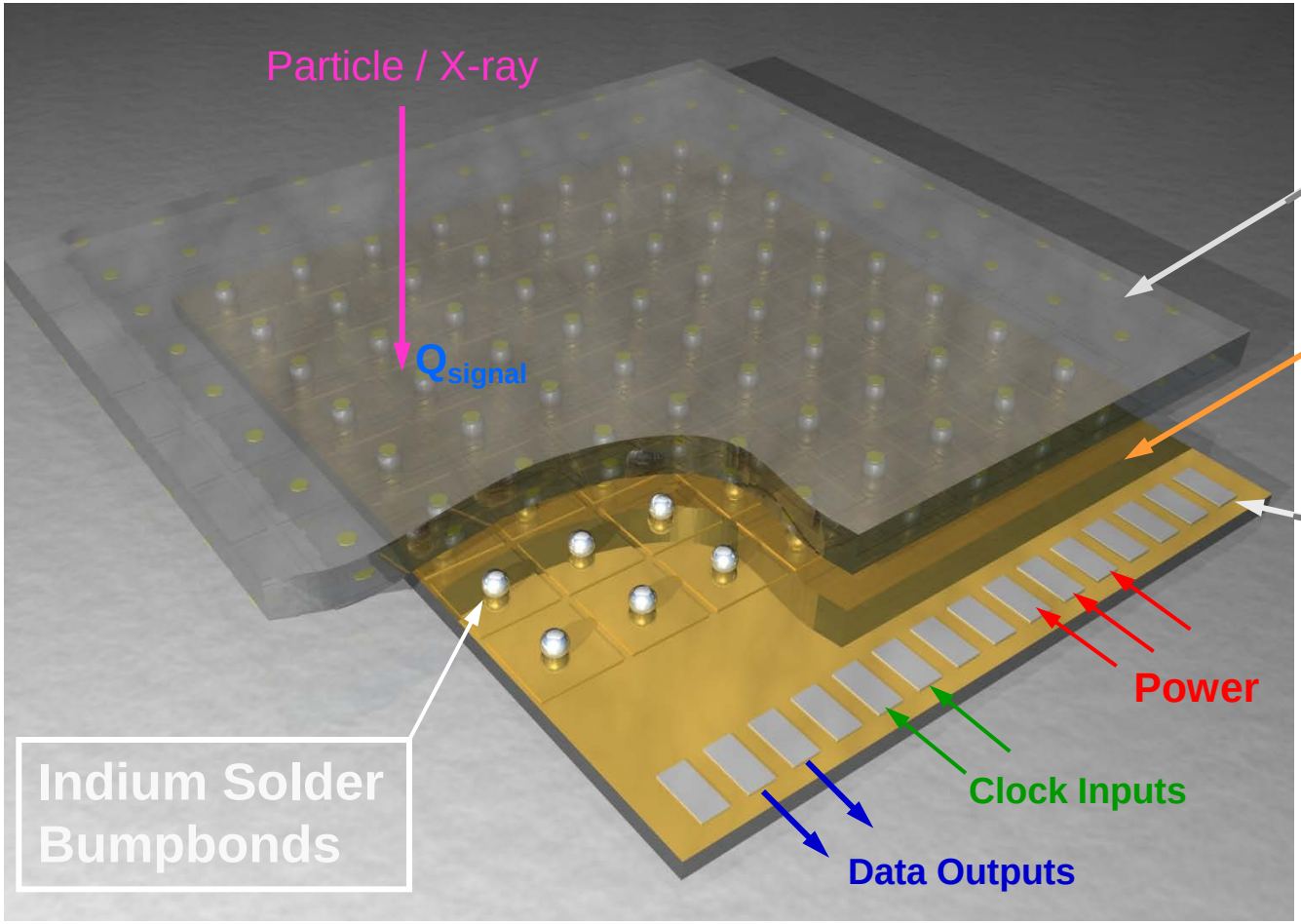
CMOS Layer

- **Signal processing**
- **Signal storage & output**

Gives enormous flexibility!



Hybrid Pixel Array Detector (HPAD) layout



Pixelated Particle Sensor

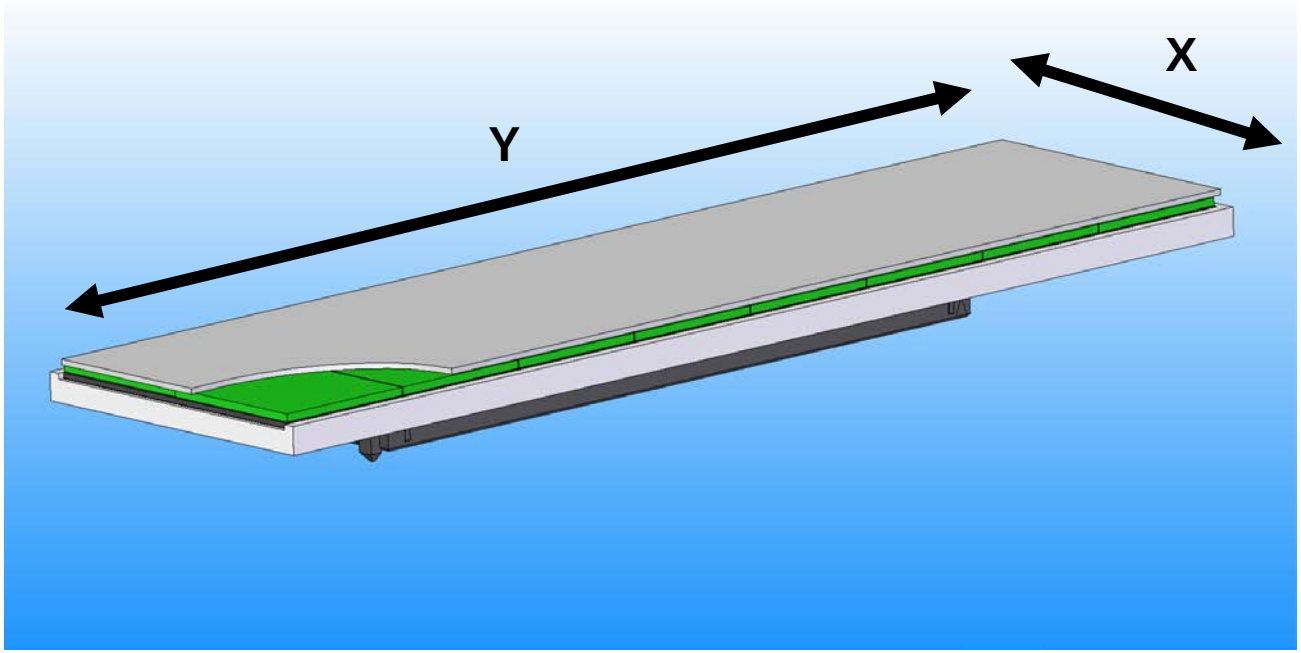
Amplifier & Readout Chip CMOS

Connection wire pads
Power
Inputs
Outputs

Indium Solder Bumpbonds

Particle / X-ray → Signal Charge → Electr. Amplifier → Readout → Digital Data

Detector tile



Cannot make it larger in X:

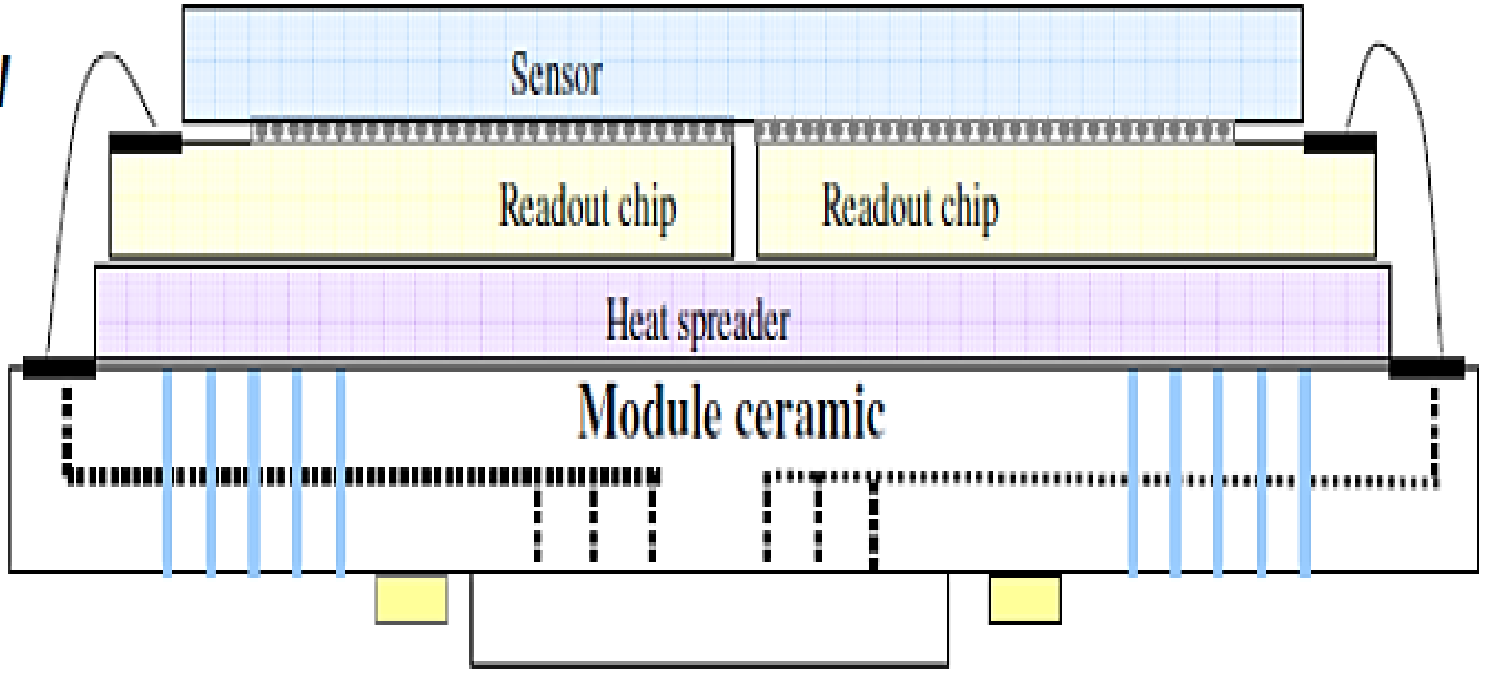
- Limited readout chip size
- Wire bonds on one side

Don’t want to make it larger in Y:

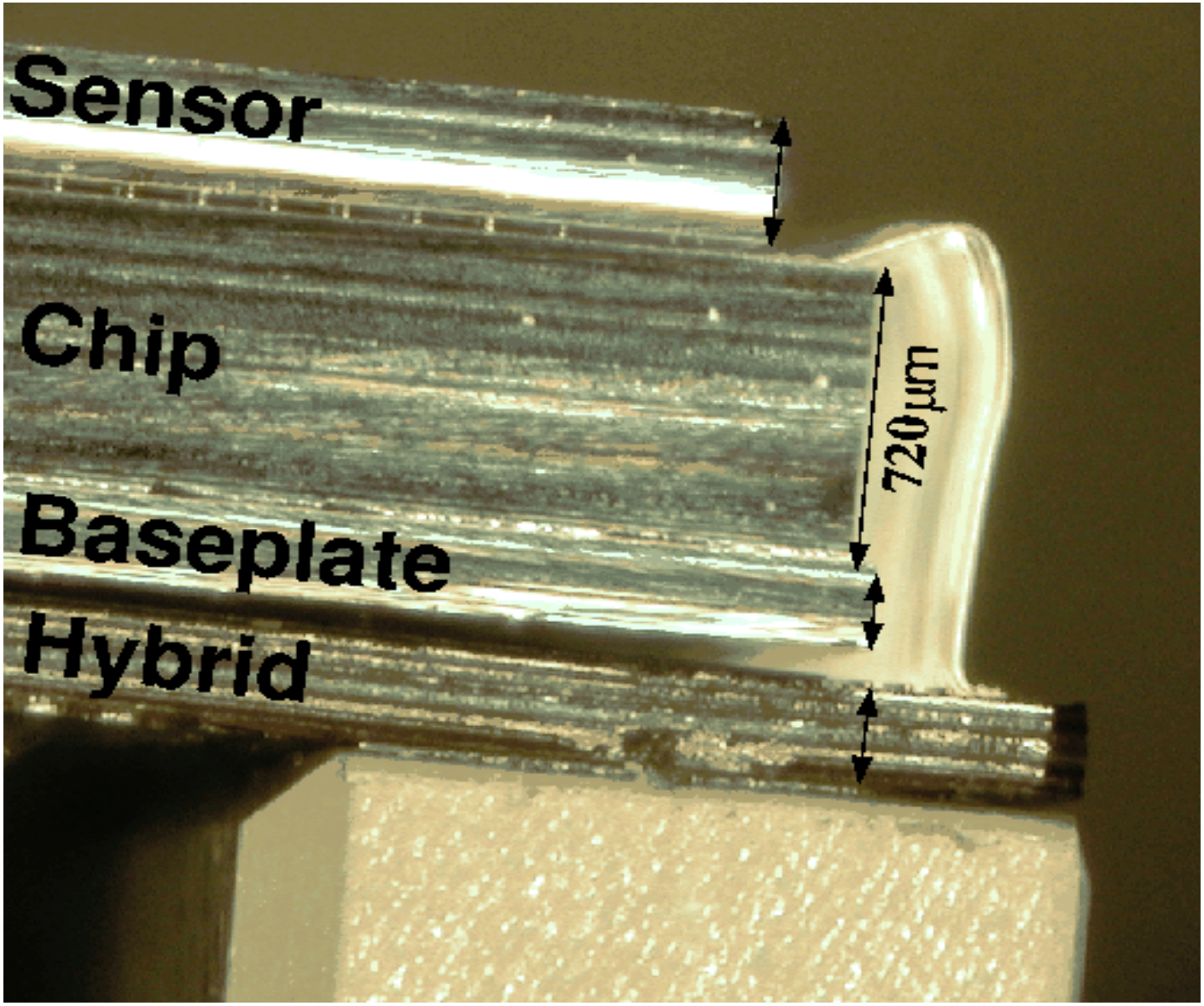
- Limited sensor chip size
- Yield issues

Detector tile in detail

Side view

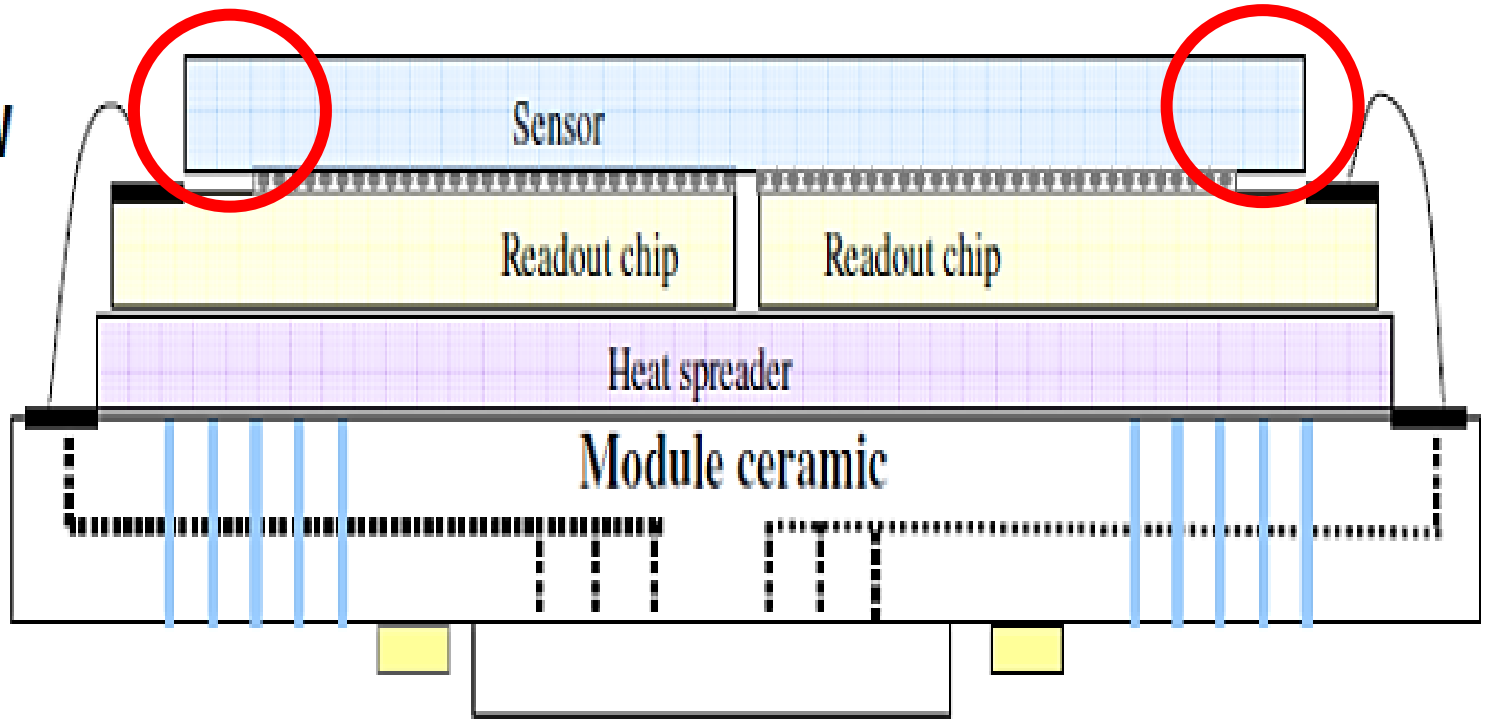


Detector tile the real thing



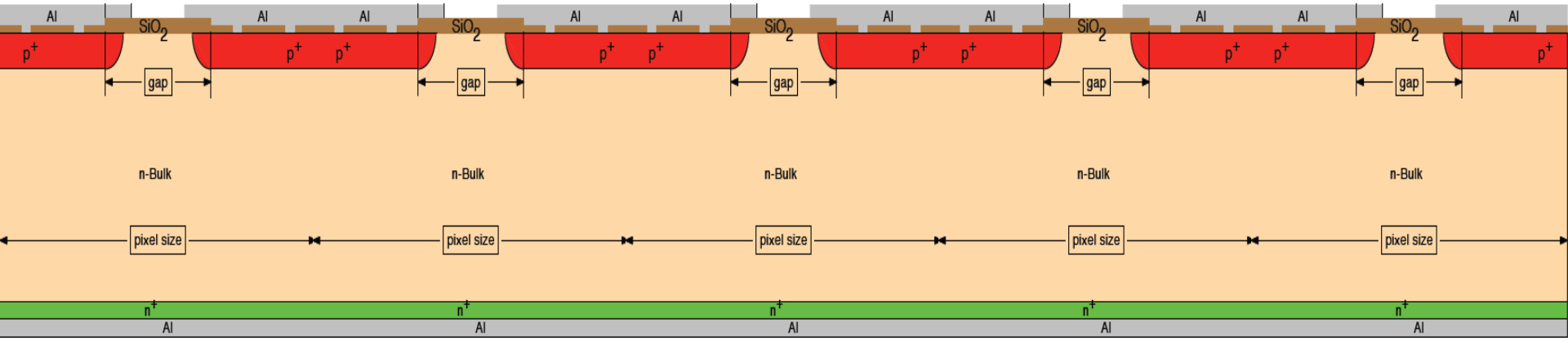
Step 1: remove dead-edge of sensor

Side view



Sensor layout

The pixels: pn-junctions

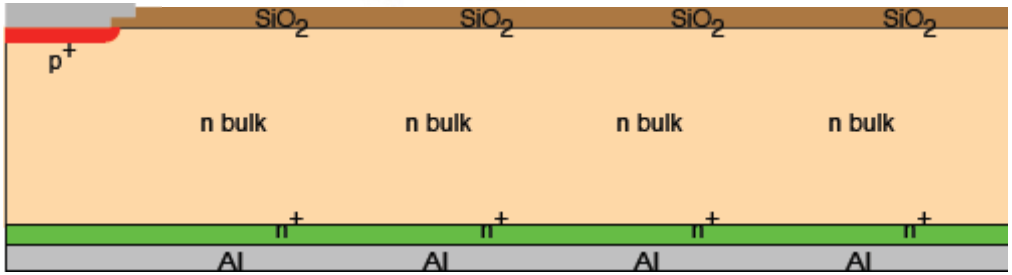


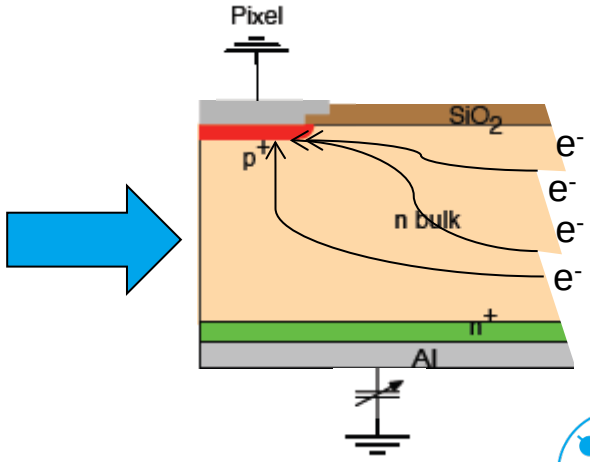
The edge

Diamond saw

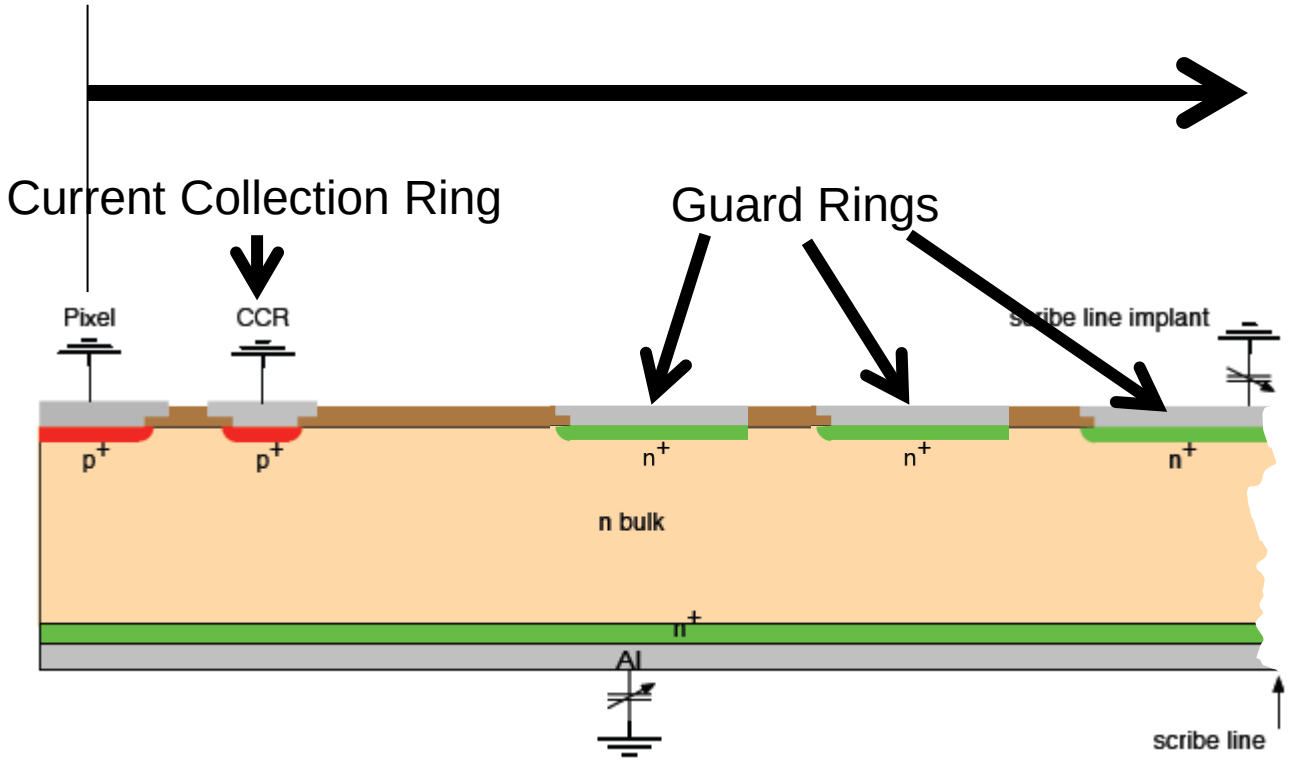
Damaged edge

....



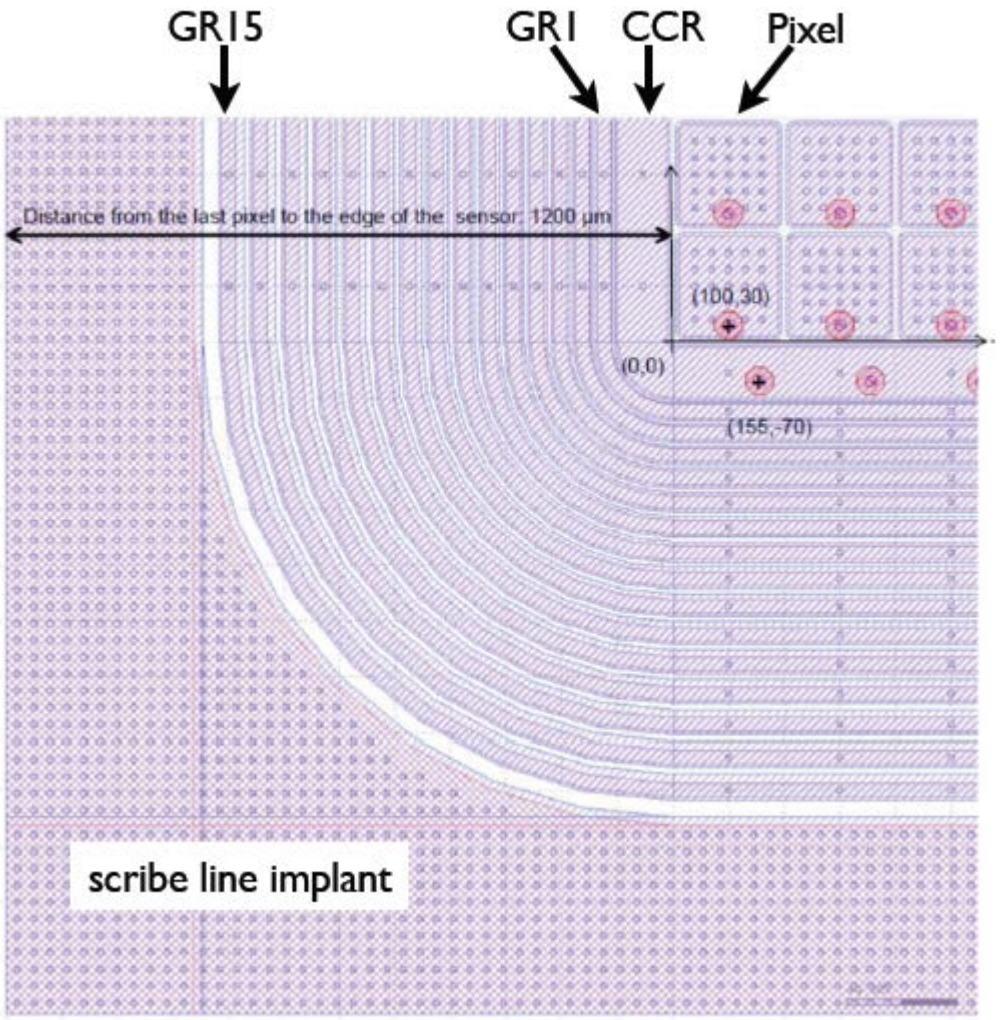


Sensor layout with current collection and guard rings



1) Large distance to the edge
2) Current Collection ring
3) Guard rings to step down voltage

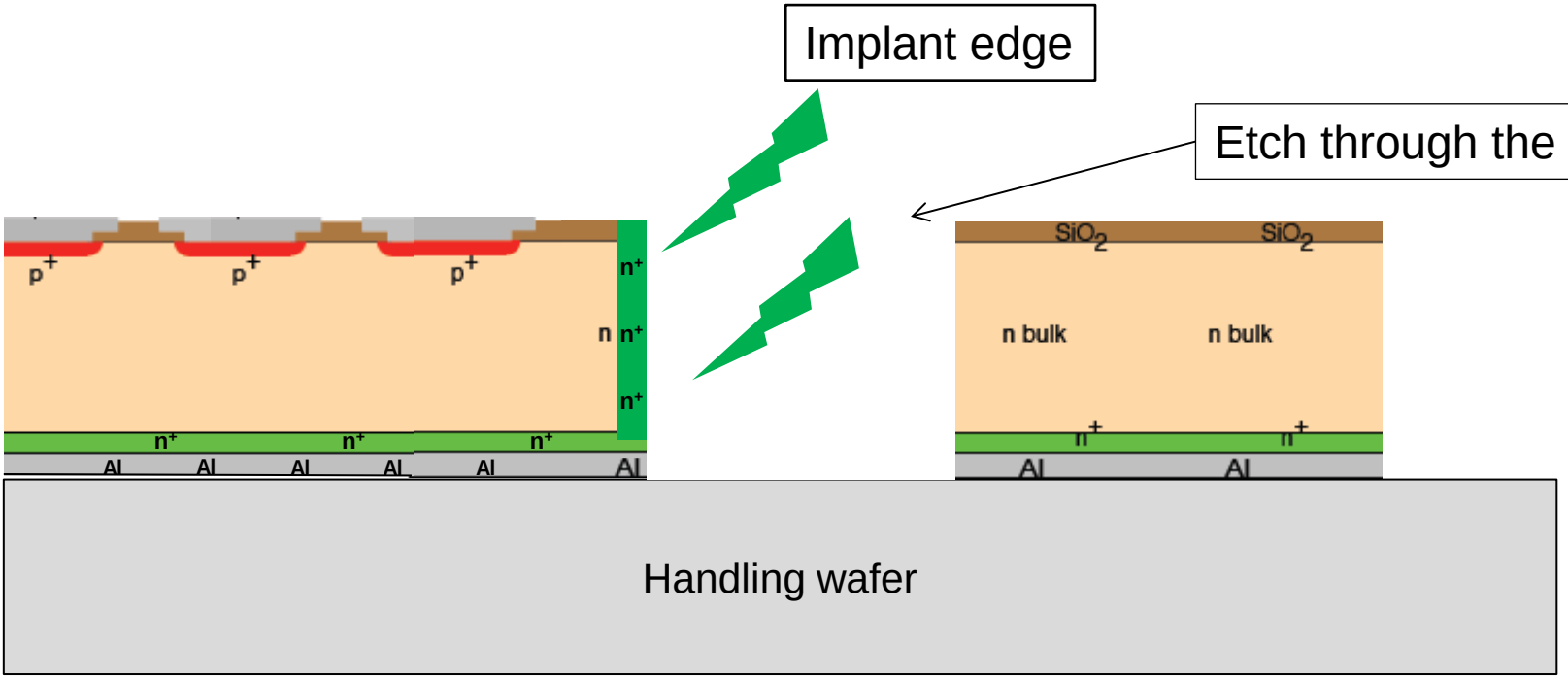
The AGIPD sensor



The AGIPD sensor for the European XFEL.
High Voltage design (900 V):

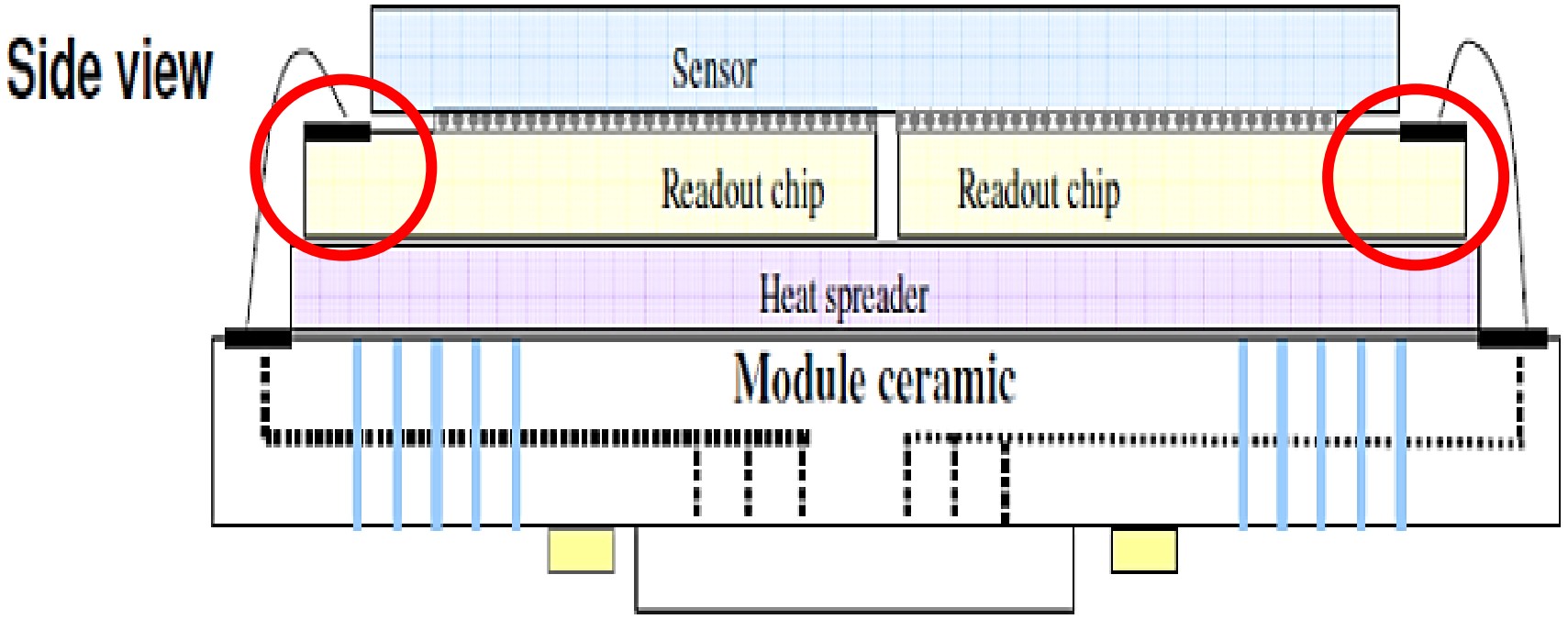
➔ needs 15 guard rings
➔ Large insensitive area

Sensor processing: a better way of doing it

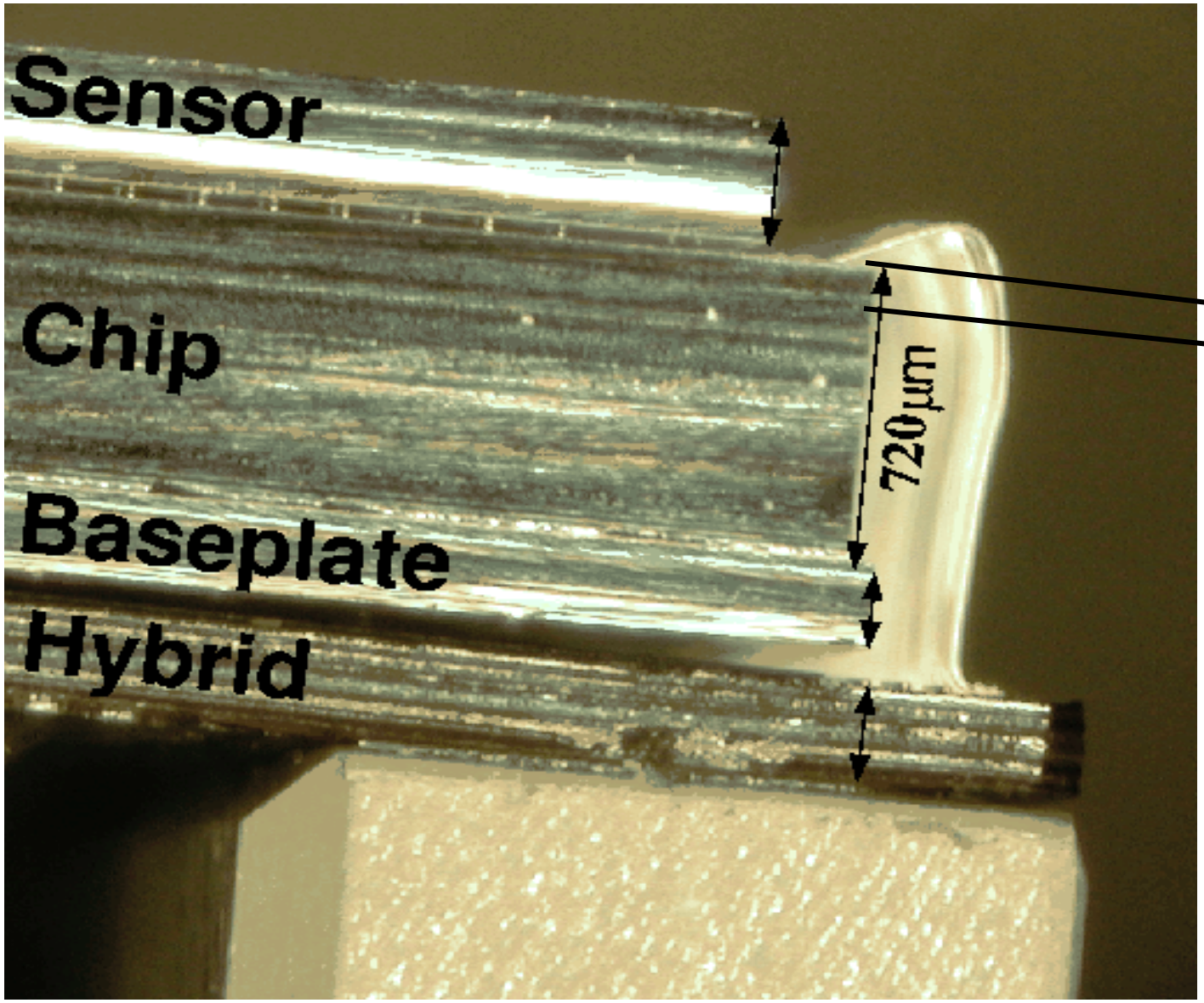


➔ Result: Sensors that are active till the edge (active edge)

Step 2: remove wire-bond region of ASIC



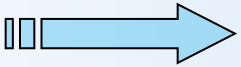
Detector tile the real thing

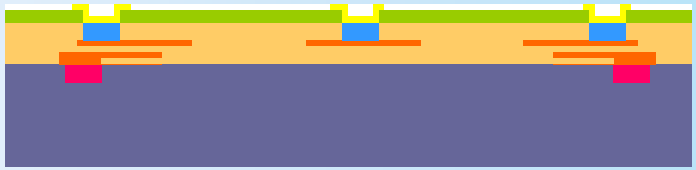


Only ~20 microns
contain circuitry
Rest is support

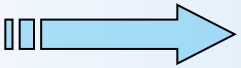
TSV Process (CEA-LETI with Medipix-3)

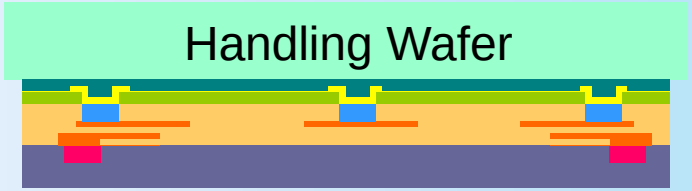
- **Front Side UBM**
  - UBM
    - TiNiAu Deposition
    - Litho UBM
    - UBM etch



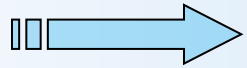


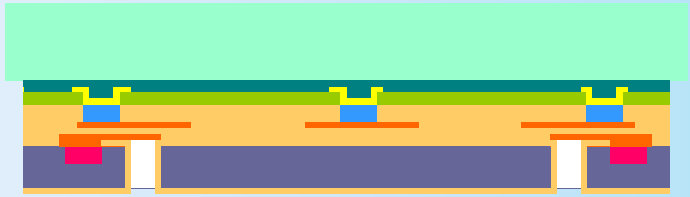
- **Bonding / Thinning**
  - Bonding
  - Grinding/edge dicing
  - CMP Si

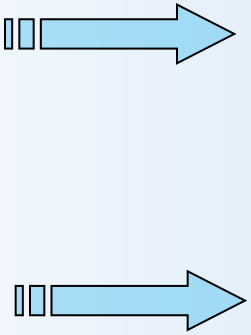


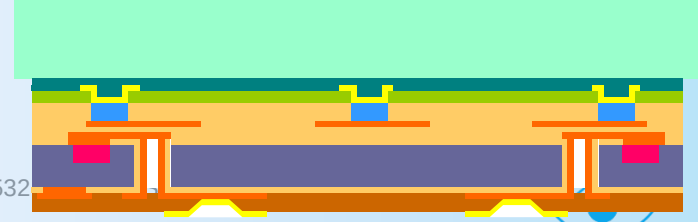


- **Back Side: TSV Last + RDL + Passivation + UBM**
  - TSV
    - Litho TSV
    - TSV AR2 etch
    - SiON conf deposition
    - Etch back
  - RDL
    - SEED TiCu
    - Litho RDL
    - ECD Cu
    - Litho PASSIV
  - UBM
    - TiNiAu deposition
    - Litho UBM
    - UBM etch
    - Debonding / Dicing

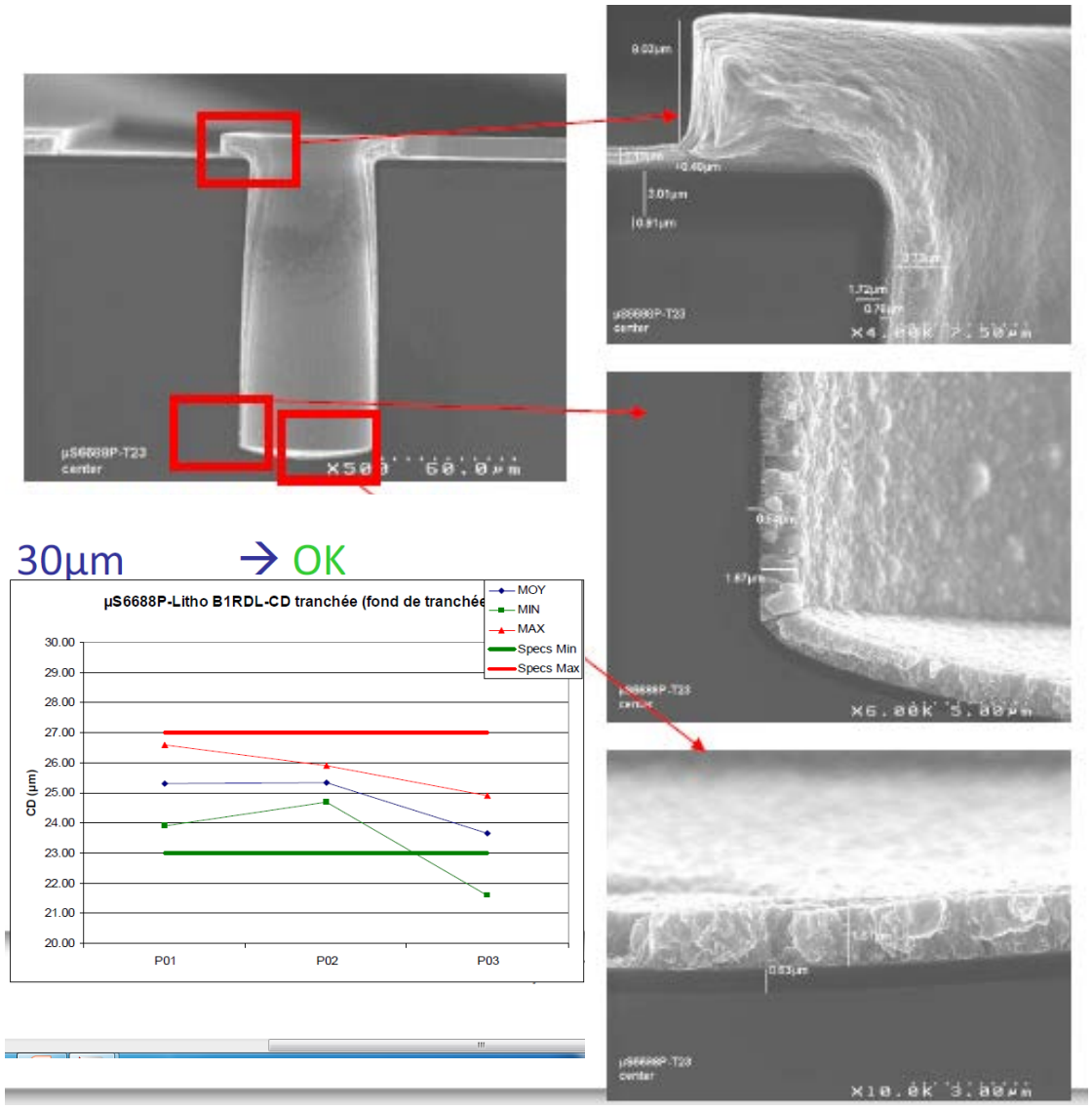




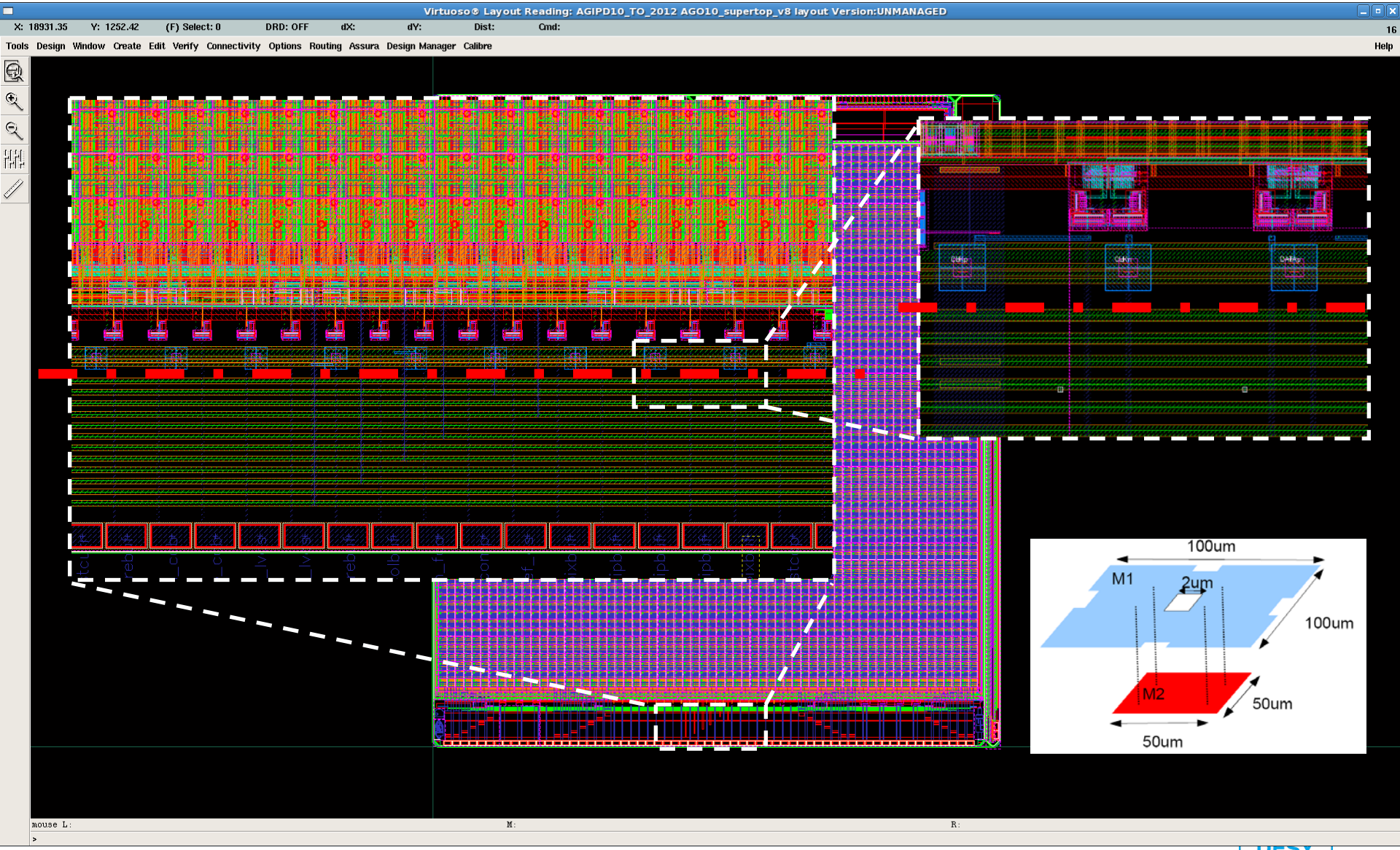




TSV Process (CEA-LETI with Medipix-3)

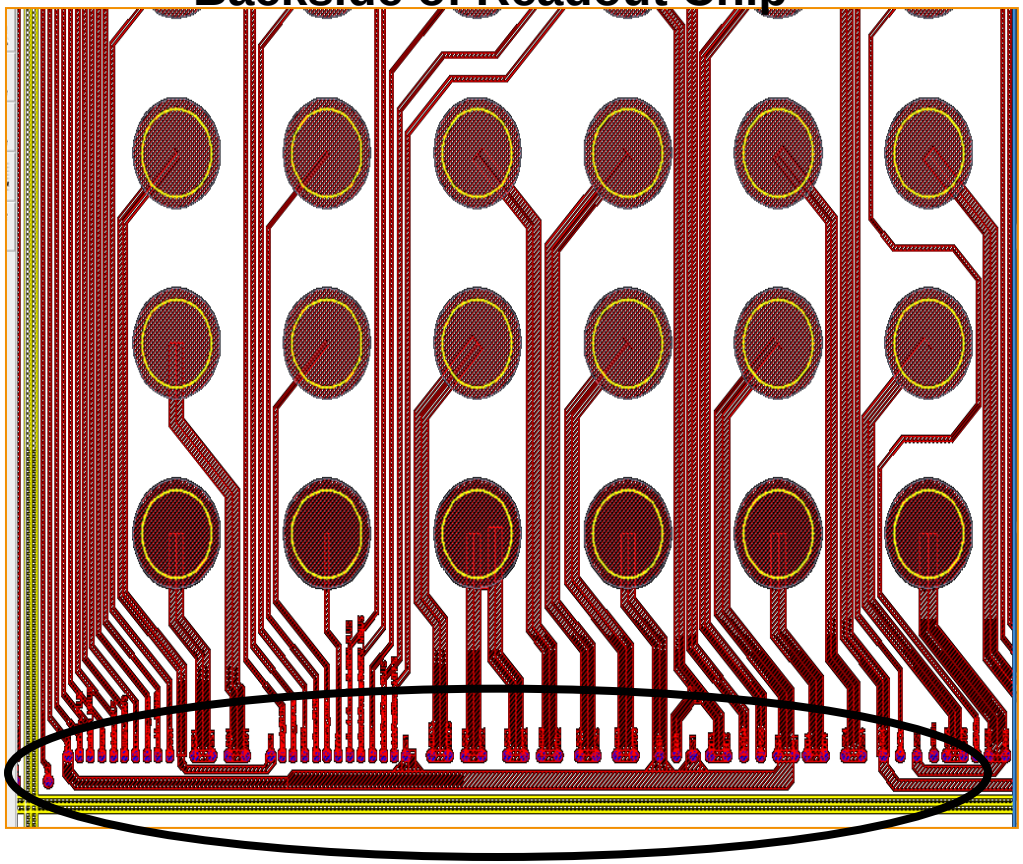


Through Silicon Vias (TSVs): AGIPD



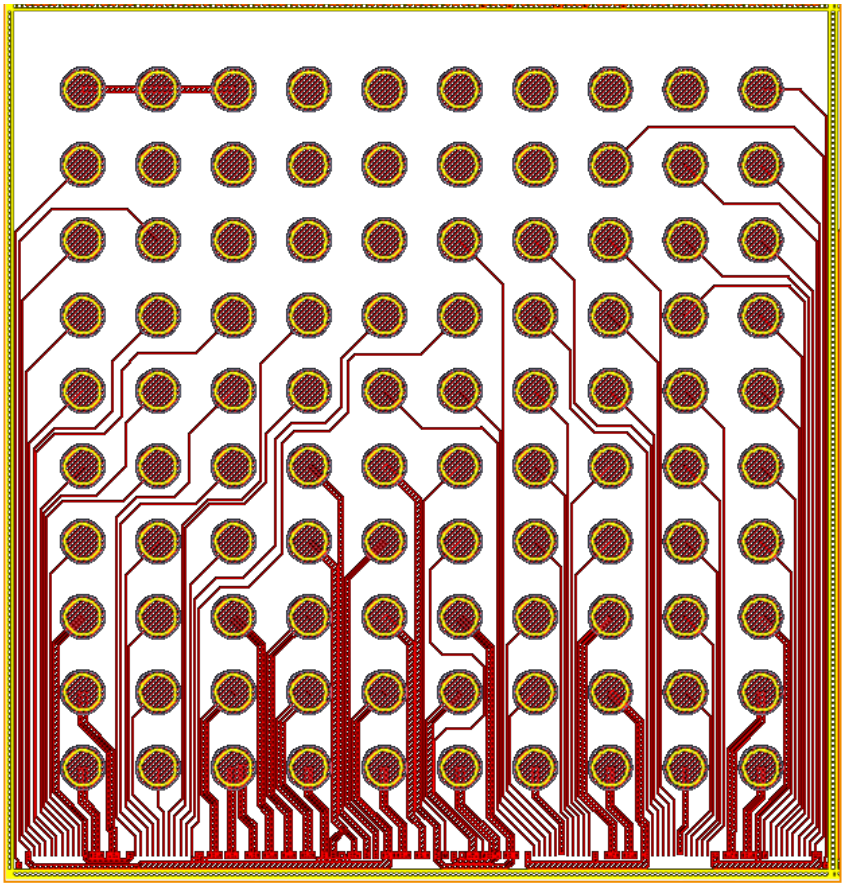
Redistribution layer ➔ Ball Grid Array (like FPGA's)

Backside of Readout Chip

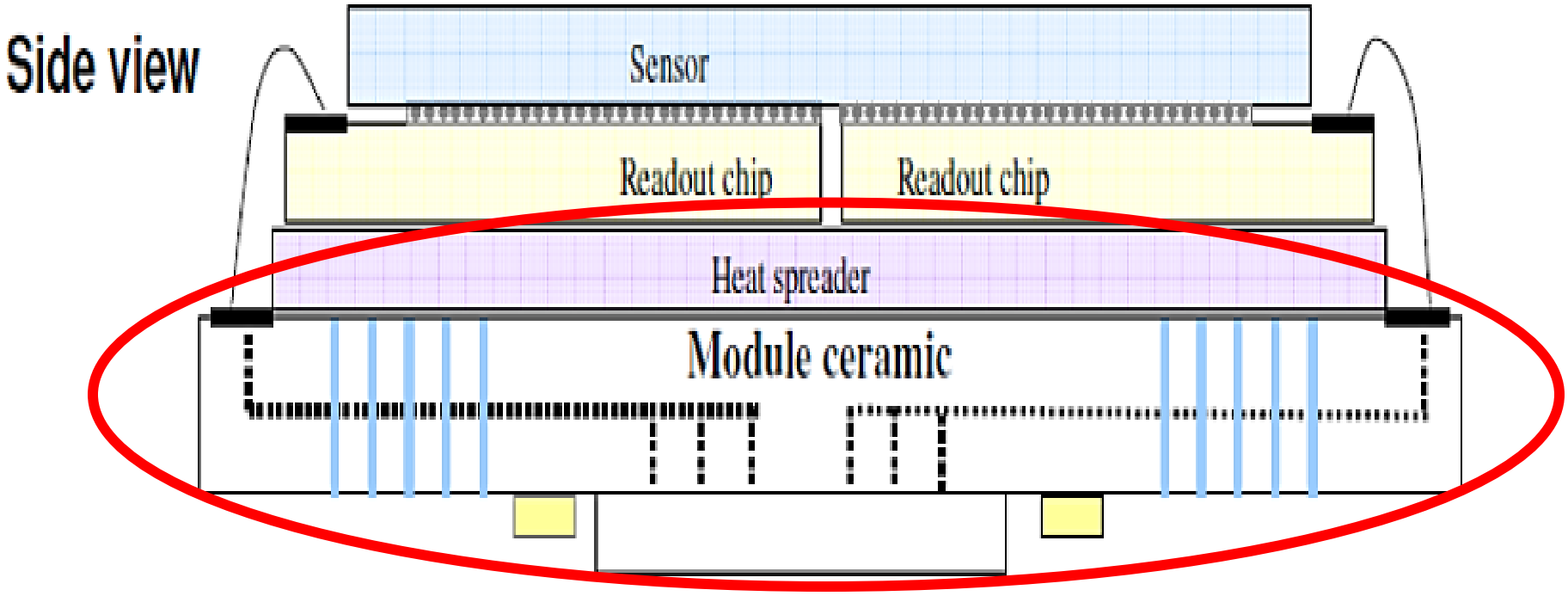


TSVs

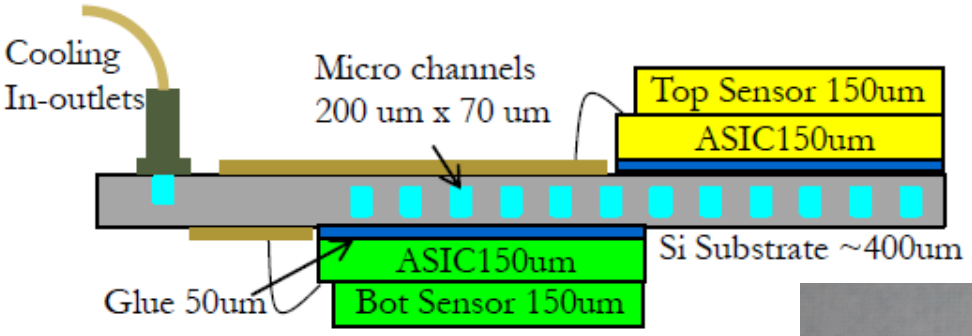
Medipix-3 chip with CEA-LETI TSVs and 10 x 10 BGA

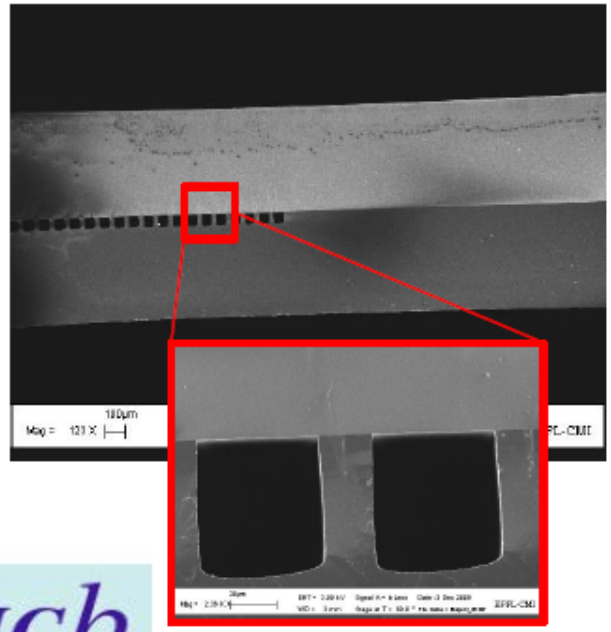


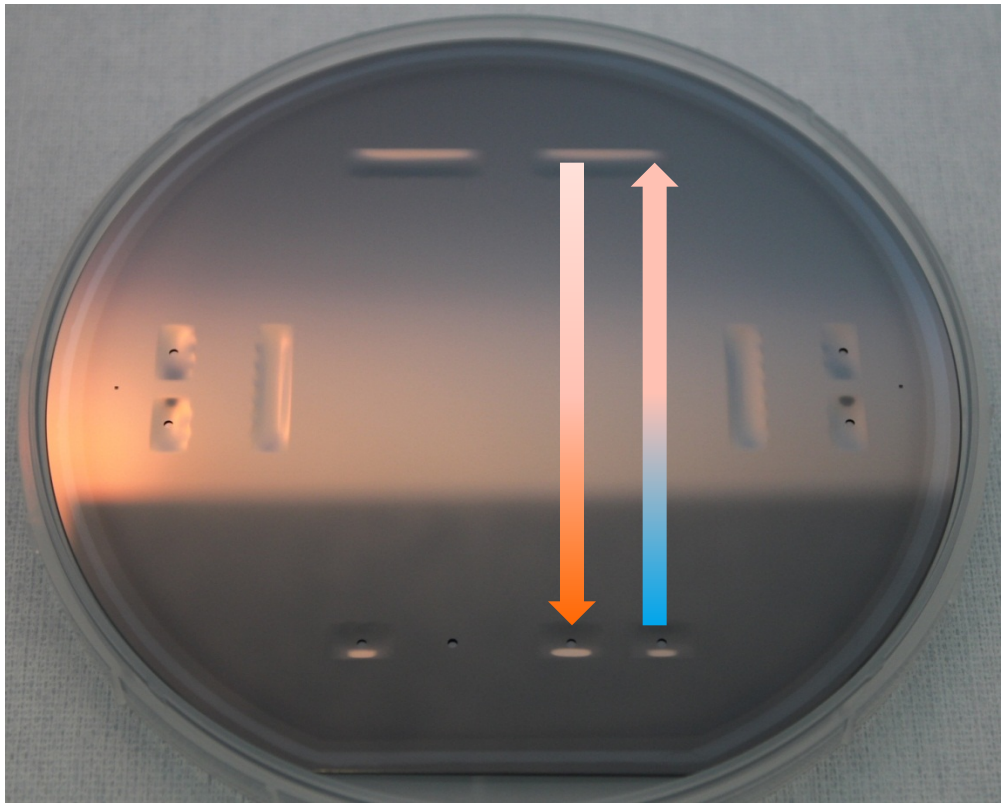
Step 3: redesign module ceramic and heat spreader



Micro-Channel cooling







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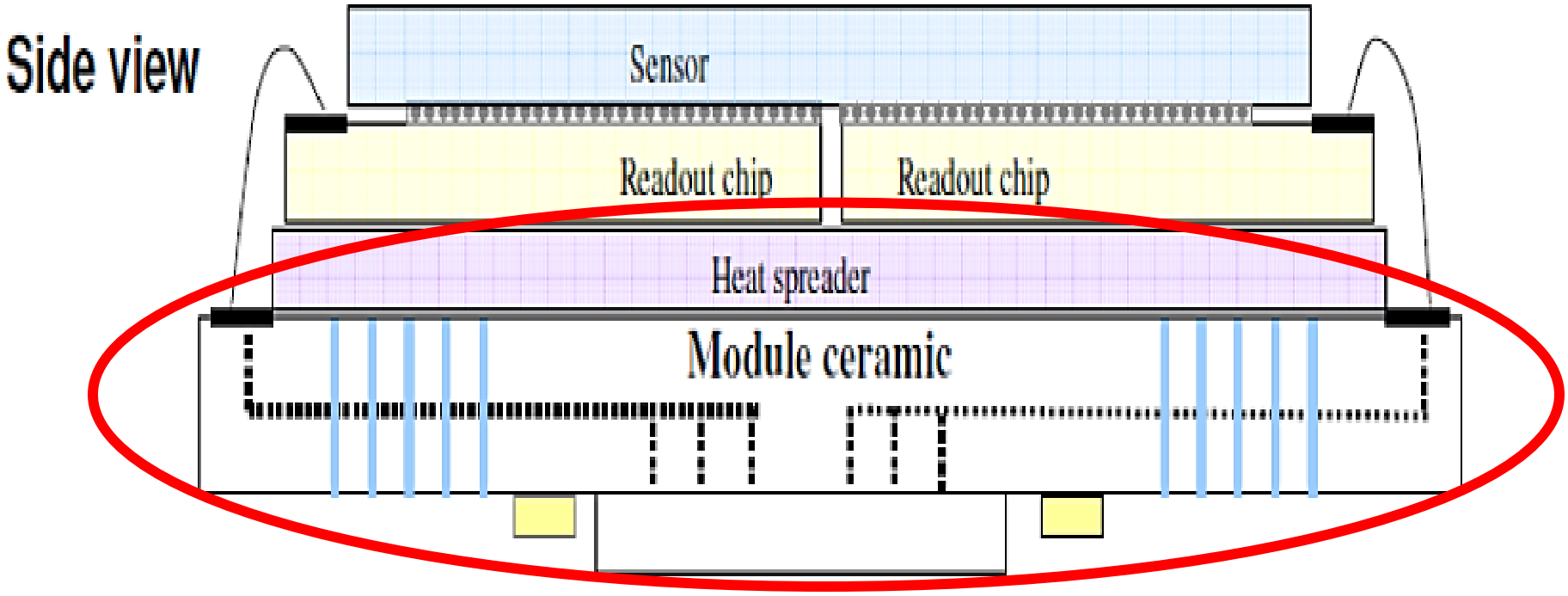
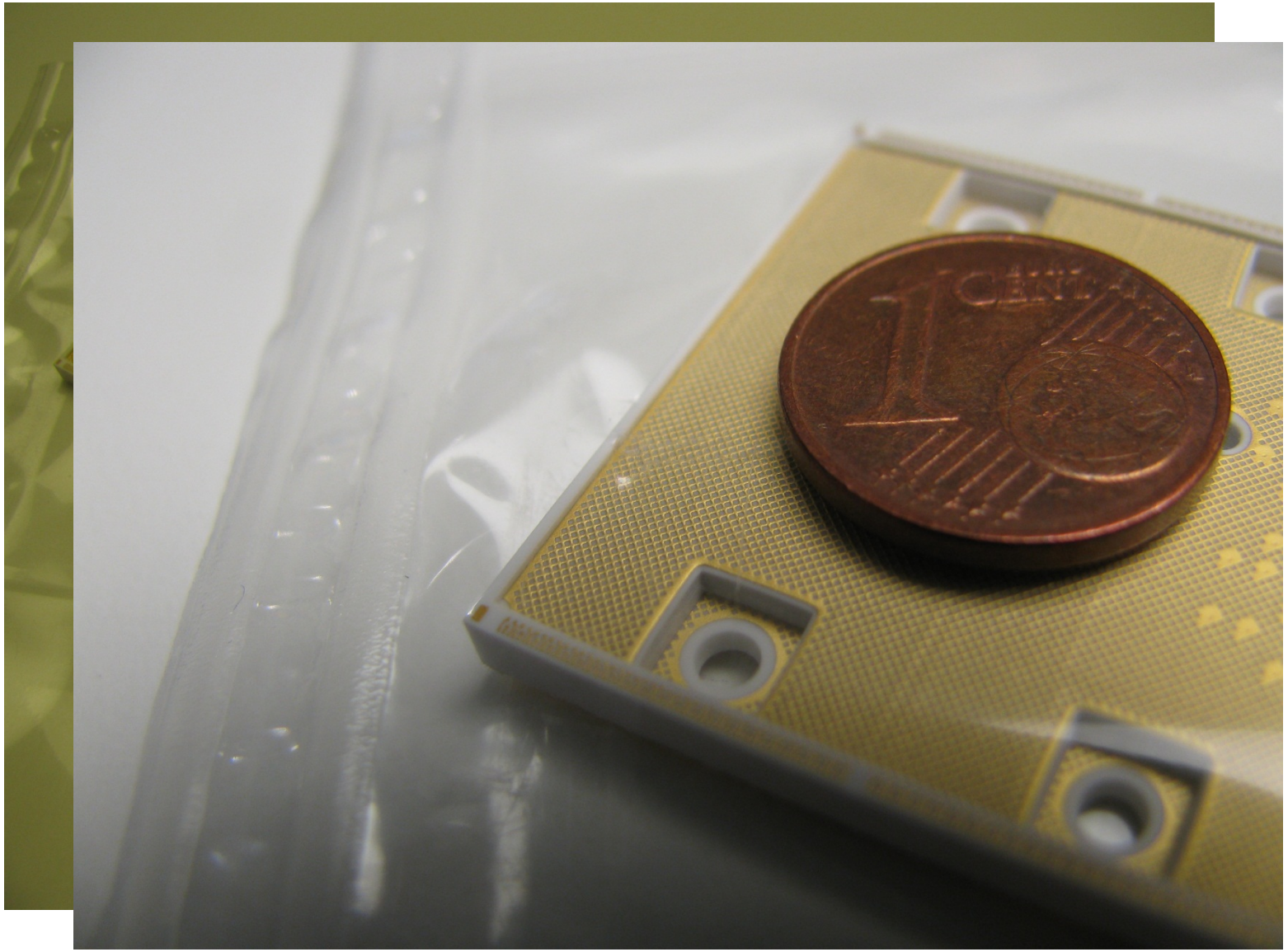
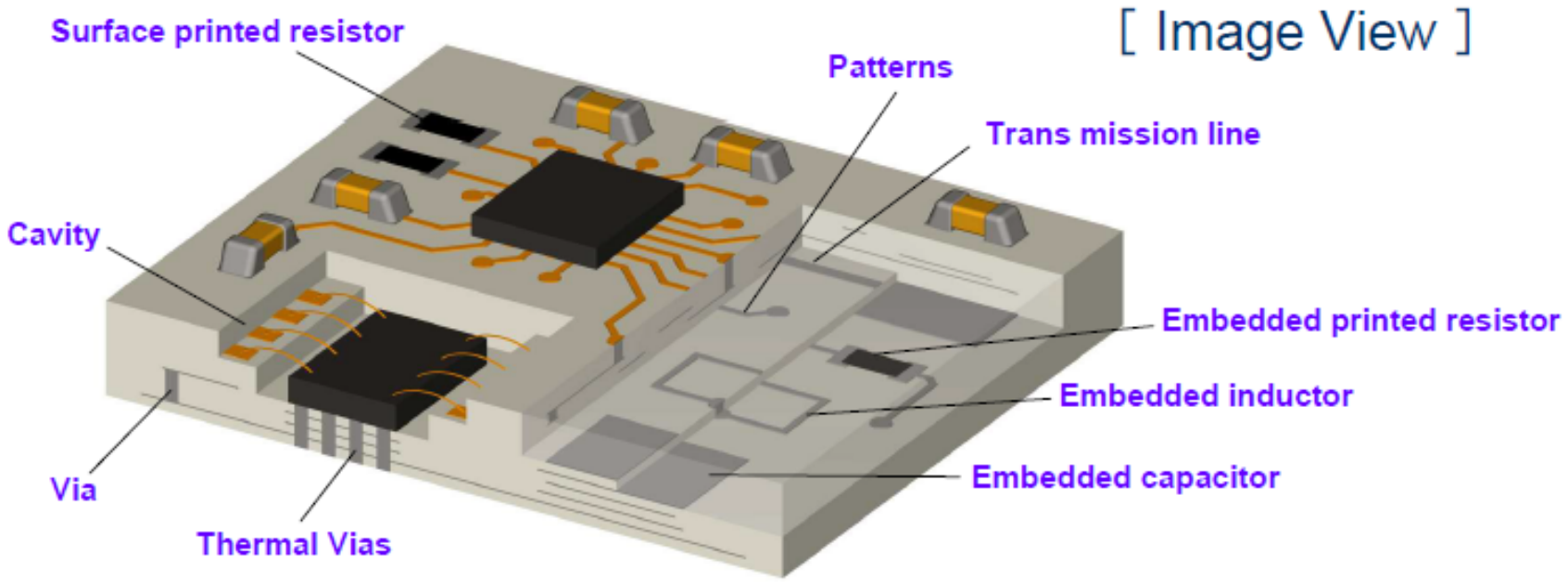


Advanced Chip-Carrier Boards (LTCC); KOA-Japan



Advanced Chip-Carrier Boards (LTCC); KOA-Japan

Structure of LTCC module



Advanced Chip-Carrier Boards (LTCC); KOA-Japan

Features of KOA LTCC 4

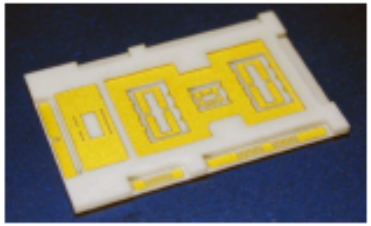
Variety of specially-shaped substrate

Variety of specially-shaped substrate is available

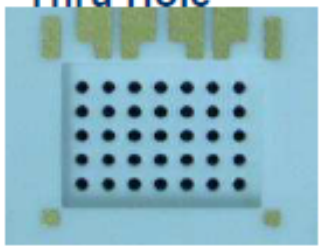
- Complicated cavity
- Thru Hole
- Flow channel structure
- Hollow structure

etc,

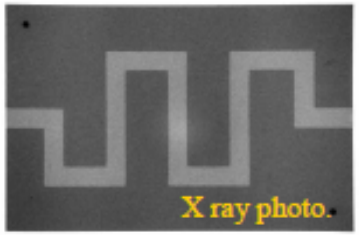
Complicated cavities



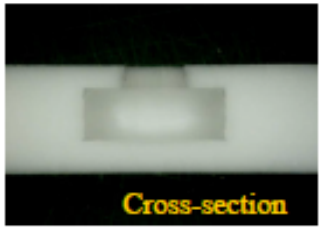
Thru Hole



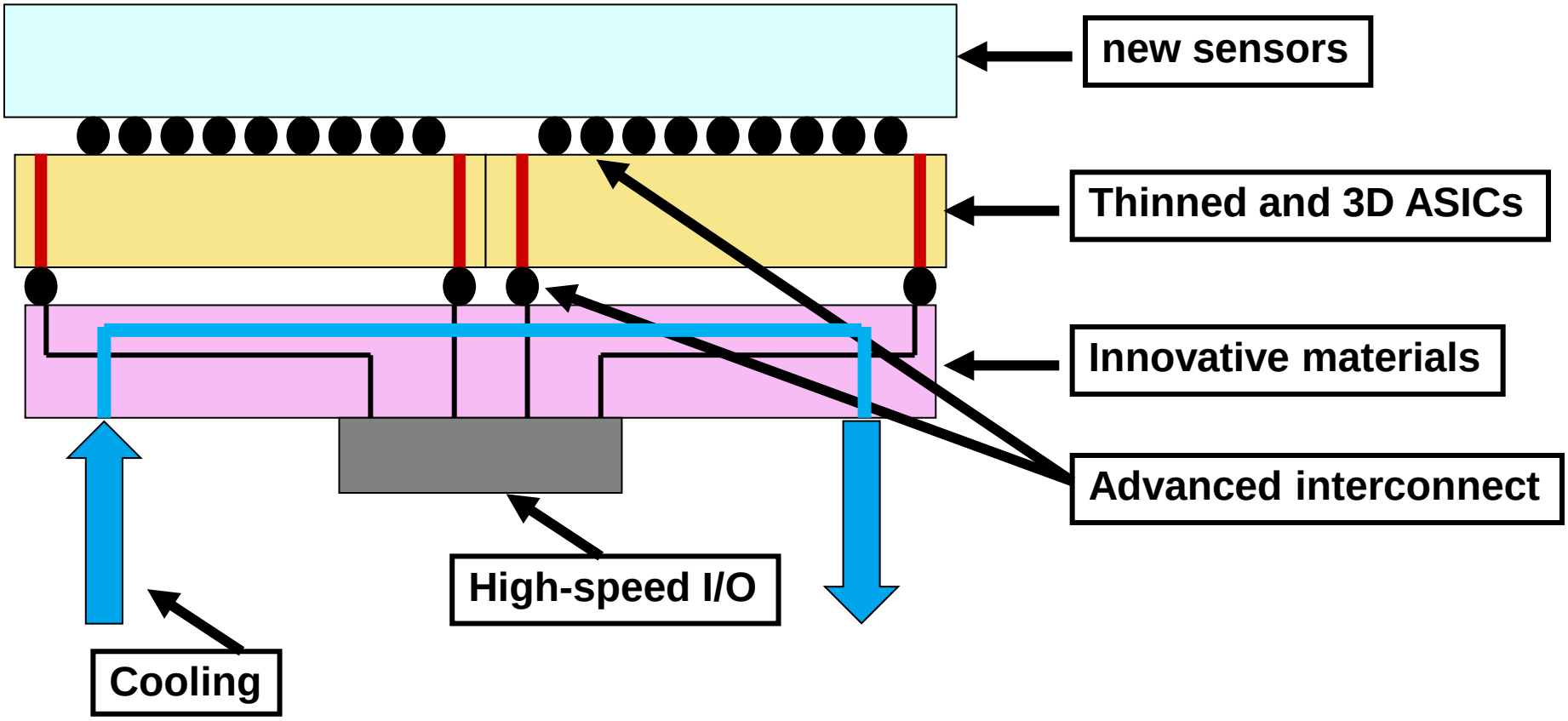
Flow channel



Hollow structure

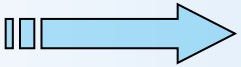


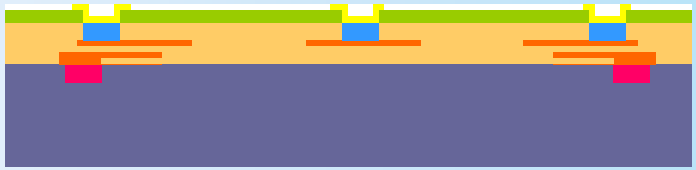
The goal: an “edgeless” building block



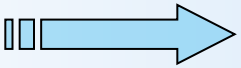
What we really want

- **Front Side UBM**
  - UBM
    - TiNiAu Deposition
    - Litho UBM
    - UBM etch

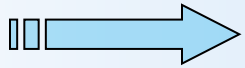


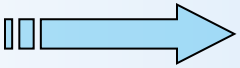


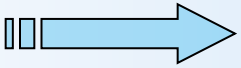
- **Bonding / Thinning**
  - Bonding
  - Grinding/edge dicing
  - CMP Si

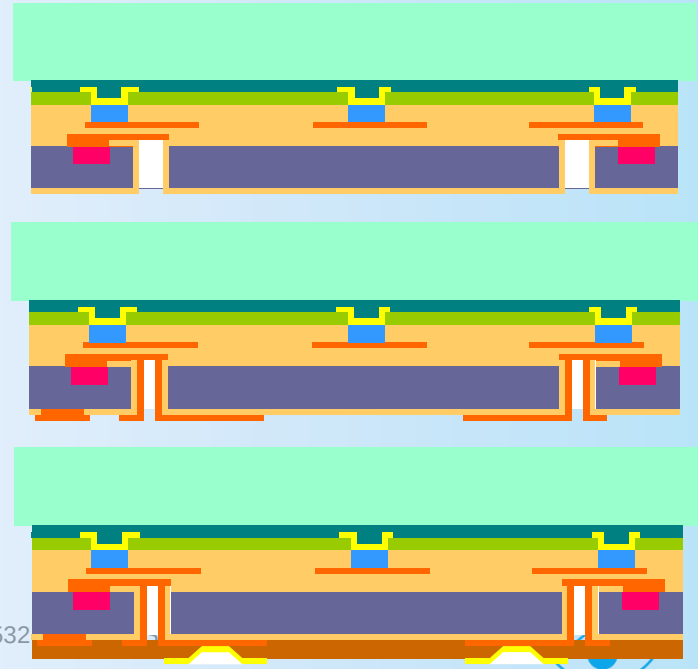


- **Back Side: TSV Last + RDL + Passivation + UBM**
  - TSV
    - Litho TSV
    - TSV AR2 etch
    - SiON conf deposition
    - Etch back
  - RDL
    - SEED TiCu
    - Litho RDL
    - ECD Cu
    - Litho PASSIV
  - UBM
    - TiNiAu deposition
    - Litho UBM
    - UBM etch
    - Debonding / Dicing





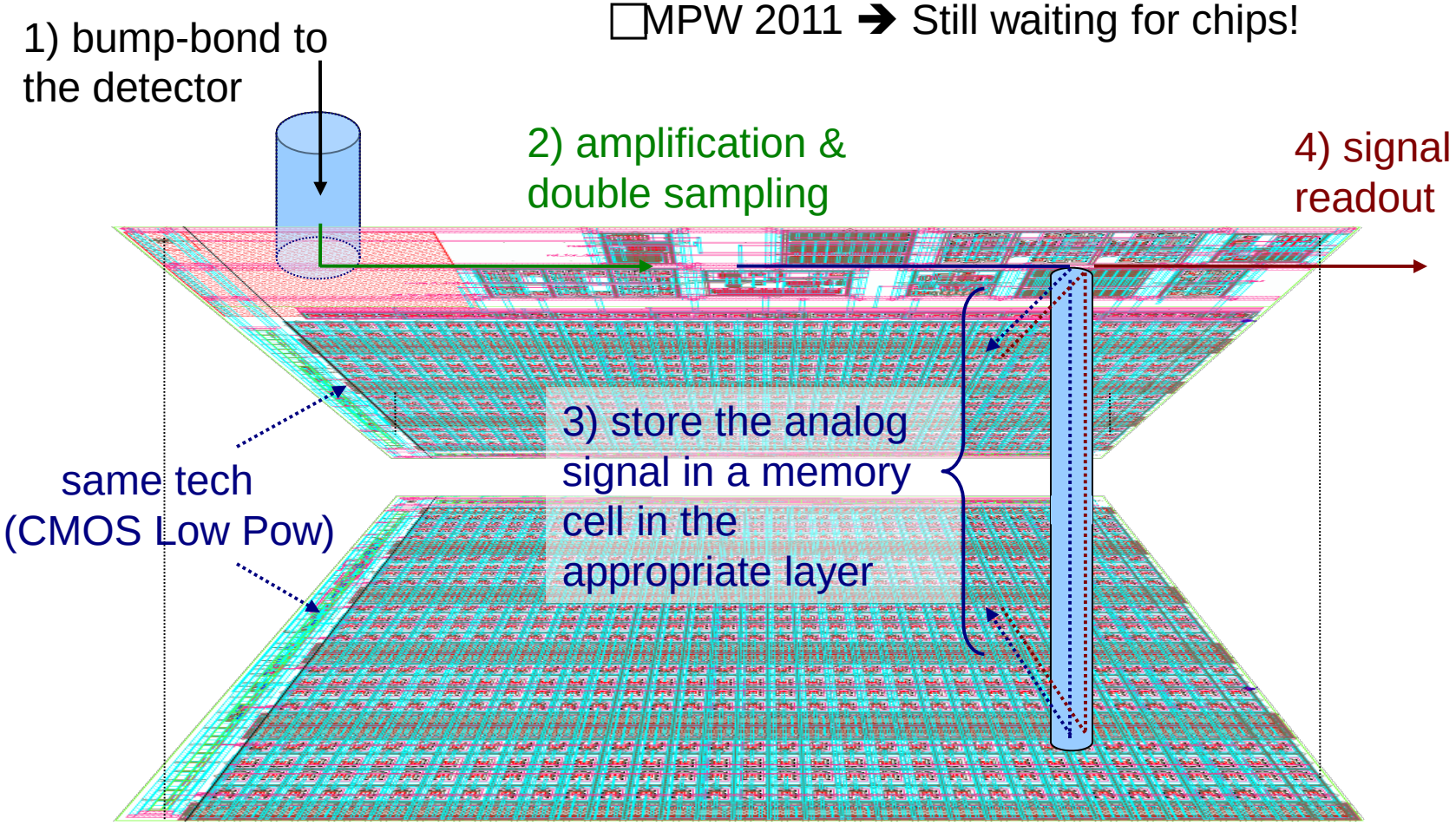




What we really want: AGIPD 2-tier ASICs

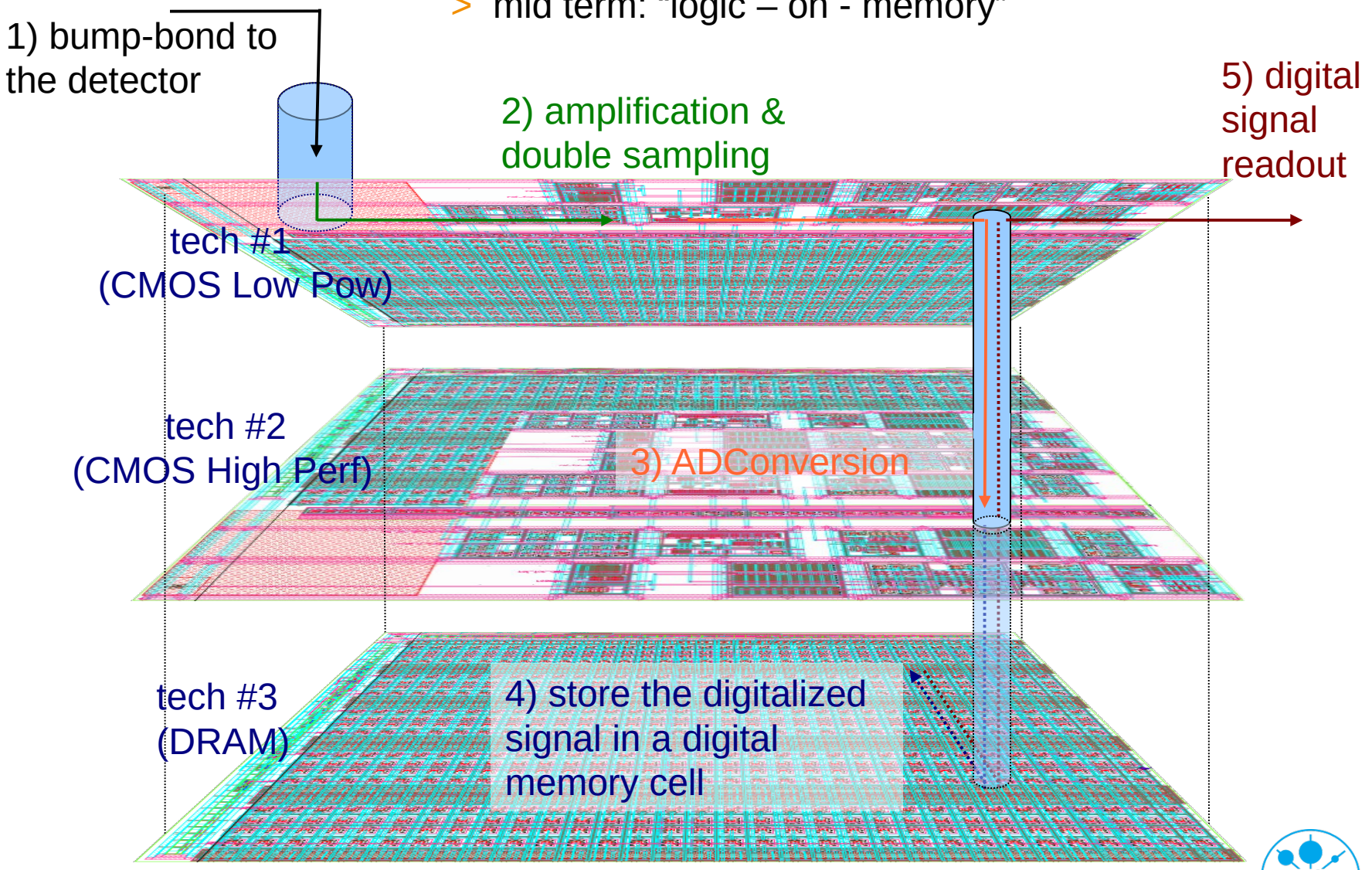
> near future: “logic – on – logic”

- MPW 2011 ➔ Still waiting for chips!

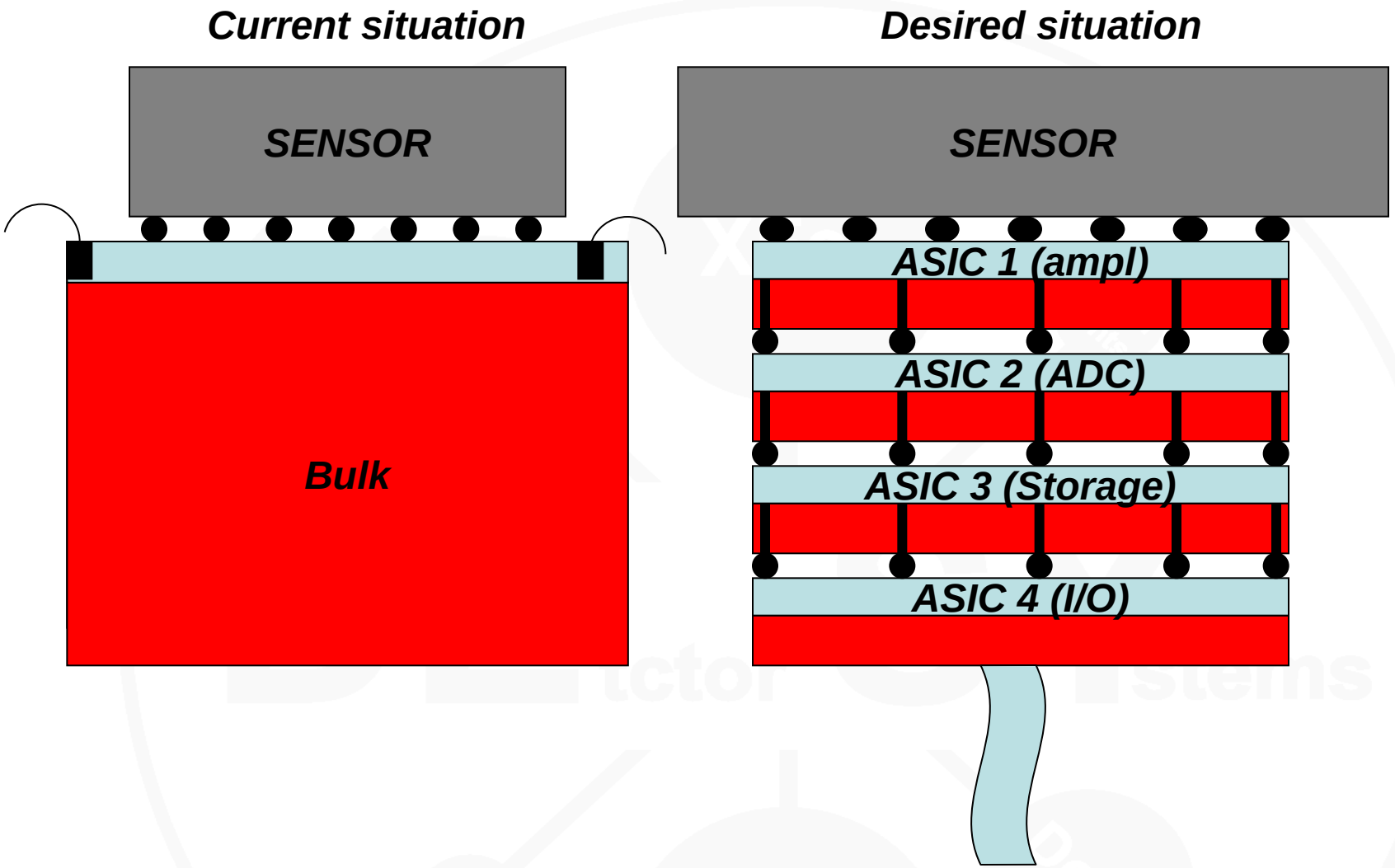


What we really want: AGIPD 3-tier ASICs

> mid term: “logic – on - memory”



Some Dreams


Current situation
SENSOR
Bulk
Desired situation
SENSOR
ASIC 1 (ampl)
ASIC 2 (ADC)
ASIC 3 (Storage)
ASIC 4 (I/O)

Conclusion

- 3D-integration of Hybrid Pixel Array Detectors is happening
- Multi-tier ASICs are still a (non-fulfilled) promise
- Dreaming is mandatory
- Dreams sometimes come through
- ….and then….we make new dreams…