# Potential & Achievements of CMOS Pixel Sensors for Charged Particle Tracking & Vertexing

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## *Outline*

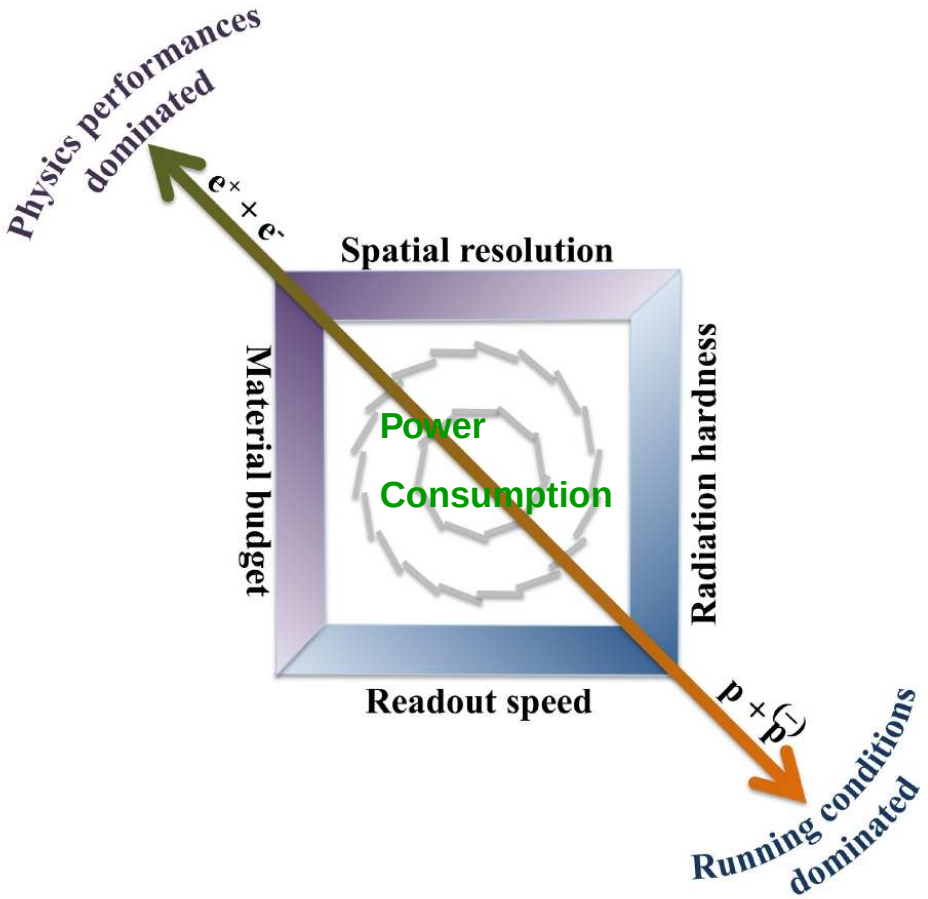
- *General introduction to CMOS Pixel Sensors (CPS)*
  - motivations
  - CMOS technology
  - principle: sensing & read-out
  - limits
- *State-of-the-Art :*
  - MIMOSA-26 : EUDET-BT
  - MIMOSA-28 : STAR-PXL
- *New Generation of Subatomic Physics Applications*
  - ALICE-ITS & CBM-MVD $\longmapsto$ ILC $\Rrightarrow$ new CMOS process : first test results
- *Outlook :*
  - 2D sensors
  - 3D sensors
- *Summary*

# The Quest for very high Precision Pixel Sensors

- **CMOS pixel sensors offer the perspective of**
  **”combining the extremes” (ultimately !)**

- **Several labs develop CMOS pixel sensors :**
  Italy (Univ., INFN), UK (RAL), CERN,
  Germany (Heidelberg, Bonn, ...), USA,
  France (IPHC, Saclay), ...

- **CMOS Pixel Sensors chosen/envisaged by growing number of subatomic physics experiments :**
  - STAR at RHIC/BNL : commissionning
  - ALICE at LHC/CERN : under development
  - CBM at FAIR/GSI : under development
  - ILC : option
  - BESS-3 Inner tracker at BEPC : option
  - ATLAS Tracker upgrade ?
  - Etc.



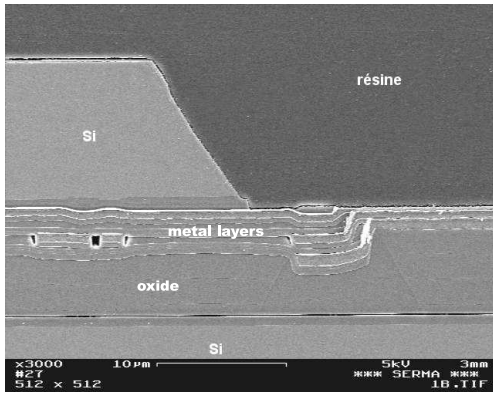

- **Variety of applications besides subatomic physics :**
  dosimetry, hadrontherapy, $\gamma$ & $\beta$ counting, ..., X-Ray imaging (emerging), ...

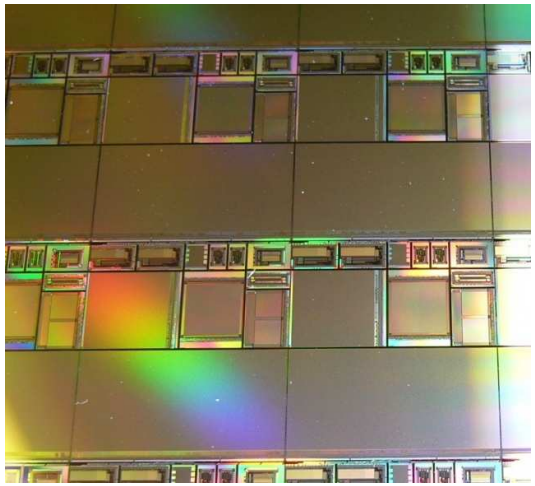
# CMOS Technology

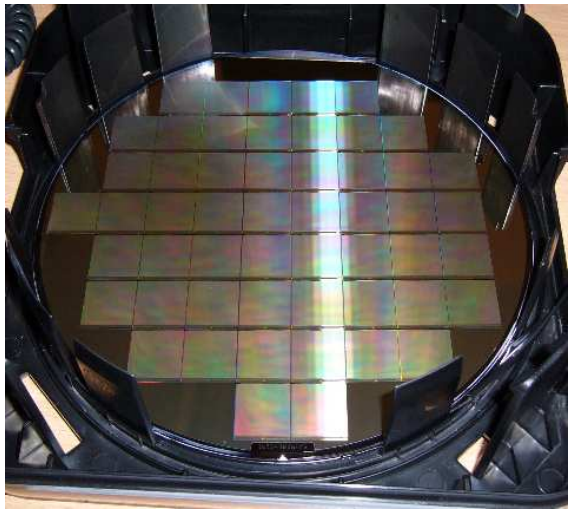
- **C.M.O.S. $\equiv$ Complementary Metal-Oxide-Semiconductor**

- **CMOS pixel sensors exploit the fabrication processes used in industry for mass production of integrated circuits :**
  - micro-processors, micro-controler, RAM, ...
  - cell phones & cameras, lap tops, cars, ...

- **CMOS fabrication mode :**
  - $\mu$circuit lithography on a substrate
  - proceeds through reticules ($\sim$ 2x2 $\longmapsto$ 2x3 cm$^2$) organised in wafers (typically 8")

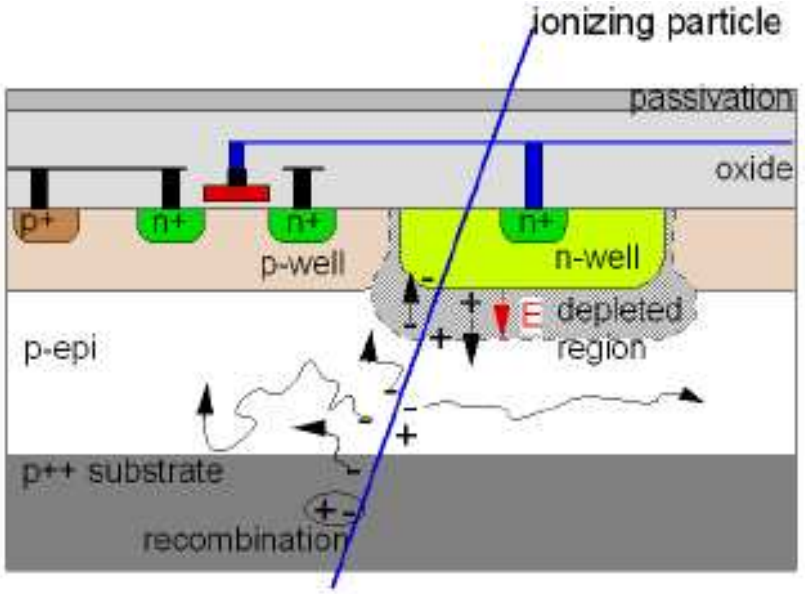




# Main Features of CMOS Sensors

- P-type low-resistivity (O(10)$\Omega \cdot cm$) Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    Q $\sim$ 70–80 e-h / $\mu m \mapsto$ signal $\lesssim$ 1000 $e^-$
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode
    with help of reflection on boundaries
    with p-wells and substrate (high doping)
    $\Rightarrow$ continuous signal sensing (no dead time)




- Prominent advantages of CMOS sensors :
  - ◇ **granularity :** pixels of $\lesssim 10 \times 10\ \mu m^2 \Rightarrow$ high spatial resolution (e.g. $\lesssim 1\ \mu m$ if needed)
  - ◇ **low material budget :** sensitive volume $\gtrsim$ 10 - 20 $\mu m \Rightarrow$ total thickness $\lesssim 50\ \mu m$
  - ◇ **signal processing $\mu$circuits integrated in the sensors** $\Rightarrow$ compacity, high data throughput, flexibility, etc.
  - ◇ **industrial mass production** $\Rightarrow$ cost, industrial reliability, fabrication duration, multi-project run frequency, technology evolution, ...
  - ◇ **operating conditions :** from $\ll 0^\circ$C to $\gtrsim$ 30-40$^\circ$C

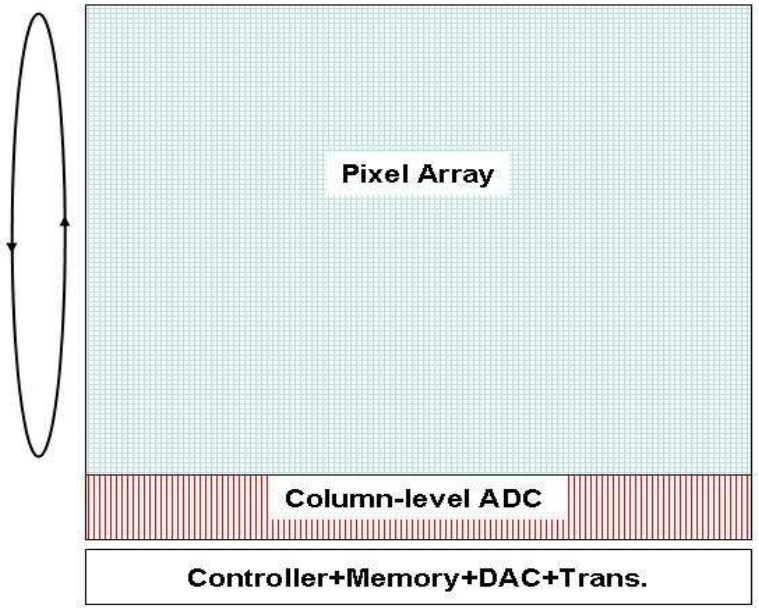
$\triangleright \triangleright \triangleright$ Thinning down to $\sim$ 30–50 $\mu m$ permitted

# Overview of Rolling Shutter Architecture

- **Sensor organisation :**
  - ✳ Signal sensing and analog processing in pixel array
  - ✳ Mixed and Digital circuitry integrated in chip periphery
  - ✳ Read-out in rolling shutter mode

    (pixels grouped in columns read-out in //)

  ⇛ trend : increase functionnalities inside pixels




- **Main consequences :**
  - ✳ **Read-out speed :**

    ≡ integration time

    ≡ nb of pixels × pixel read-out time (O(100 ns))
  - ✳ **Power consumption :**

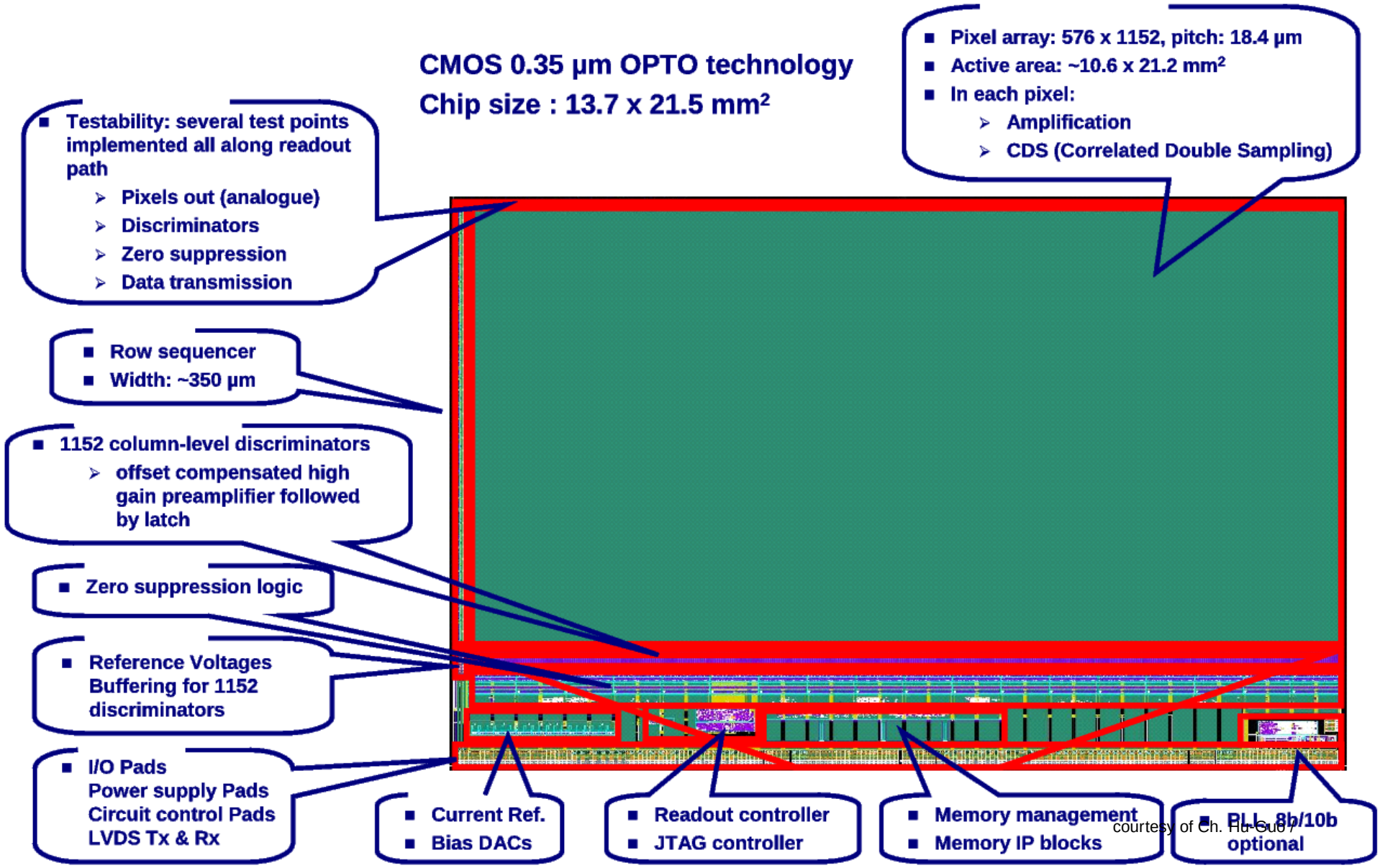
    limited inside the pixel array to the row(s) being read c
  - ✳ **Material budget :**

    peripheral band(s) for mixed+digital circuitry, insensitive to impinging particles

    ↪ ∼ 10 % of chip surface
  - ✳ **Time stamp :**

    each row encompasses a specific time intervalle ⇛ adapt (≡ exploit with) track reconstruction code

# State of the Art : MIMOSA-26 for EUDET-BT




courtesy of Ch. Hu-Guo

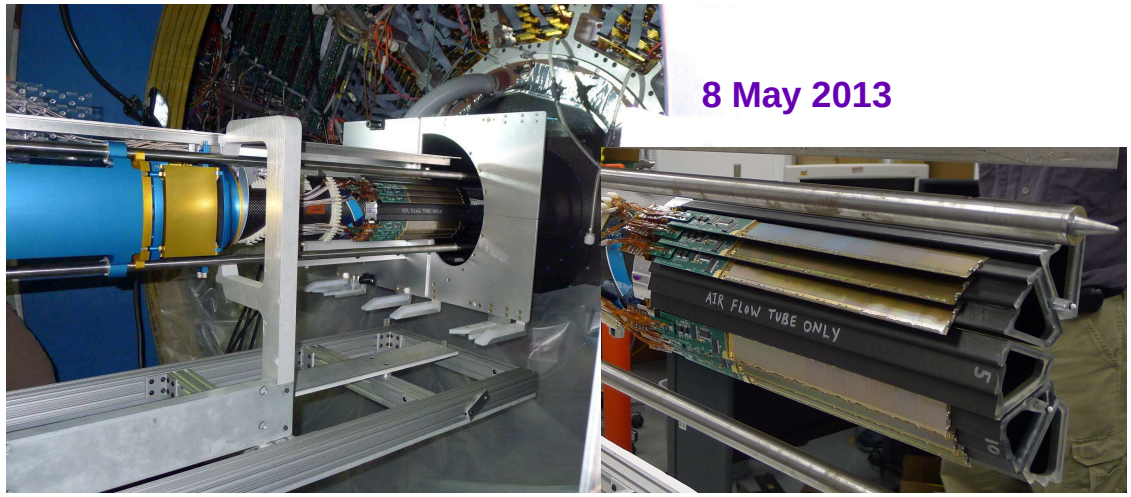
# State-of-the-Art: MIMOSA-28 for the STAR-PXL

- **Main characteristics of ULTIMATE ($\equiv$ MIMOSA-28):**
  - ⁕ 0.35 $\mu m$ process with high-resistivity epitaxial layer
  - ⁕ column // architecture with in-pixel cDS & amplification
  - ⁕ end-of-column discrimination & binary charge encoding
  - ⁕ on-chip zero-suppression
  - ⁕ **active area: 960 colums of 928 pixels (19.9$\times$19.2 mm$^2$)**
  - ⁕ **pitch: 20.7 $\mu m \rightarrowtail \sim$ 0.9 million pixels**
    - ↪ **charge sharing $\Rightarrow$ $\sigma_{sp} \gtrsim$ 3.5 $\mu m$**
  - ⁕ JTAG programmable
  - ⁕ **t$_{r.o.}$ $\lesssim$ 200 $\mu s$ ($\sim$ 5$\times$10$^3$ frames/s) $\Rightarrow$ suited to $>$10$^6$ part./cm$^2$/s**
  - ⁕ 2 outputs at 160 MHz
  - ⁕ **$\lesssim$ 150 mW/cm$^2$ power consumption**

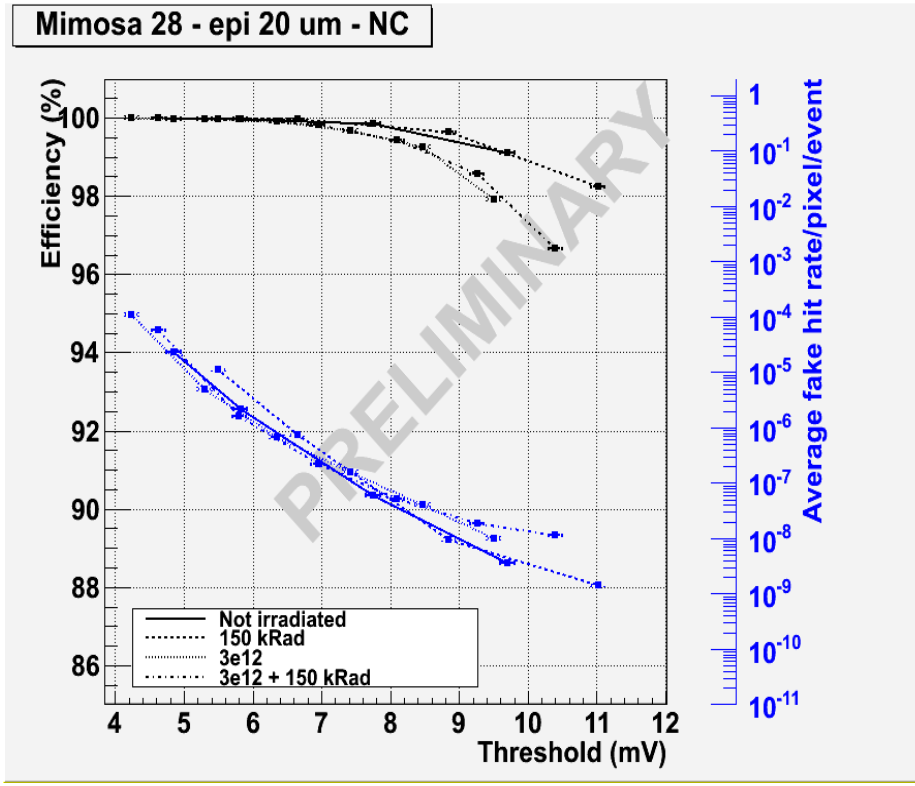
▷▷▷ **Sensors fully validated :** (50 $\mu m$ thin)

- ⁕ N $\lesssim$ 15 e$^-$ ENC at 30-35°C
- ⁕ $\epsilon_{det}$, fake & $\sigma_{sp}$ as expected
- —○ **Rad. tol. validated (3·10$^{12}$ n$_{eq}$/cm$^2$ & 150 kRad at 30°C)**
- —○ All specifications are met $\Rightarrow$ detector construction under way (40 ladders)

▷▷▷ **1st step: Commissioning of 3/10 of detector started at RHIC with pp collisions on May 9th, 2013**




**8 May 2013**



# Technology Limitations and Industrial Trends

- **Thin sensitive volume**
  - $\Rrightarrow$ impact on signal magnitude (mV !) $\Rrightarrow$ very low noise FEE required
    - ▷ **tendency :** $\gtrsim$ 40 $\mu m$ thick epitaxy or low doping substrate

- **Sensitive volume only partly depleted**
  - $\Rrightarrow$ negative impact on radiation tolerance & speed but positive on $\sigma_{sp}$ (charge spread)
    - ▷ **tendency :** high-resistivity epitaxial layer $\Rrightarrow$ improved radiation tolerance (SNR)

- **Commercial fabrication**
  - $\Rrightarrow$ fabrication parametres (doping profile $\longmapsto$ epitaxial layer, number of metal layers, etc.)
    not optimal for charged particle detection *(optimised for markets)* :
    - ✳ real potential of CMOS pixel sensors not exploited (yet !)
    - ✳ choice of process for HEP often driven by epitaxial layer characteristics (governs signal),
      at the expense of the FEE circuitry parametres (feature size, nb of Metal Layers)
    - ▷ **tendency :** CMOS process with feature size $\leq 0.18 \mu m$ on high-res., up to 50 $\mu m$ thick, epitaxy

- **Use of P-MOS transistors inside pixel array restricted in most processes**
  - $\Rrightarrow$ limited signal processing functionnalities inside (small) pixels (most performed on sensor periphery)
    - ▷ **tendency :** buried P-well techno. $\Rrightarrow$ allows use of P-MOS transistors (watch charge coll. eff. !)

# Towards Higher Read-Out Speed and Radiation Tolerance

- **Next generation of experiments calls for improved sensor performances :**

| Expt-System | $\sigma_t$ | $\sigma_{sp}$ | TID | Fluence |
|---|---|---|---|---|
| STAR-PXL (30°C) | $\lesssim$ 200 $\mu s$ | $\sim$ 5 $\mu m$ | 150 kRad | 3·$10^{12}$ $n_{eq}$/cm$^2$ |
| | $\Downarrow$ ? | | $\Downarrow$ ? | $\Downarrow$ ? |
| 30°C $\rightarrow$ $\ll$ 0°C | 10-30 $\mu s$ | $\sim$ 3-5 $\mu m$ | 1 $\rightarrow$ 10 MRad | $10^{13}$ $\rightarrow$ $10^{14}$ $n_{eq}$/cm$^2$ |

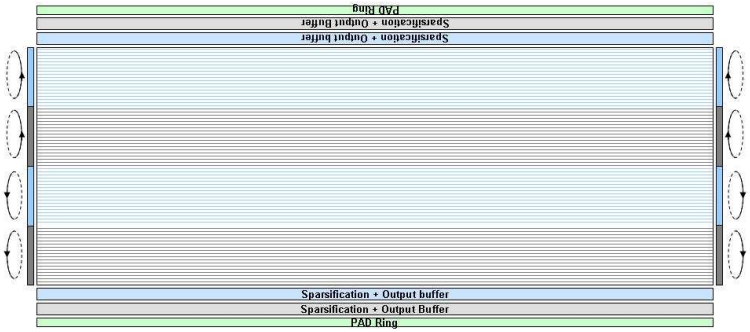
✓

- **Main improvements required to comply with forthcoming experiments' specifications :**
  - **aim for higher epitaxial layer resistivity**
  - **reduce nb(pixels) / read-out unit (column)**
  - **aim for smaller feature size process & more parallelised read-out**

- **How to accelerate the pixel read-out :**
  - elongated pixels $\Rightarrow$ less pixels /col. & in-pixel discri. $\Rightarrow$ 3-8 faster r.o.
  - read out simultaneously 2 or 4 rows $\Rightarrow$ 2-4 faster r.o./side
  - subdivide pixel area in 4-8 sub-arrays read out in // $\Rightarrow$ 2-4 faster r.o./side
  - conservative step: 2 discri./col. **end** (22 $\mu m$ wide) $\Rightarrow$ simult. 2 row r.o.

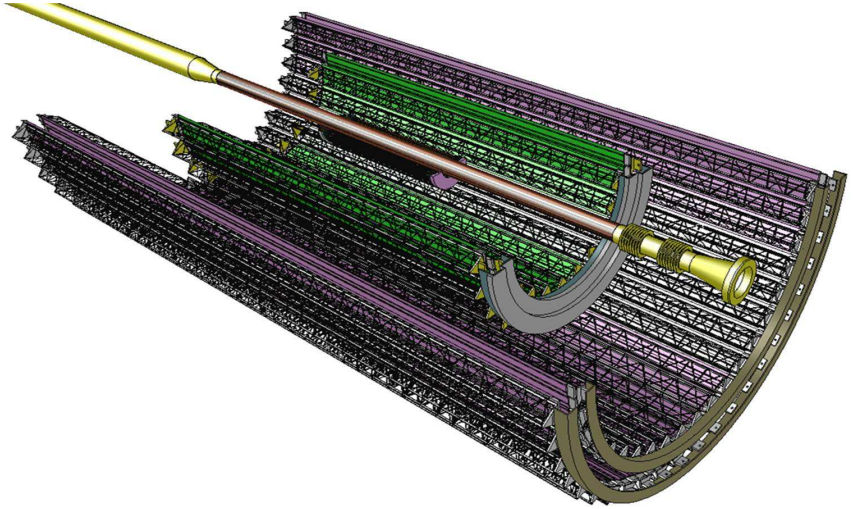
  ↻ remain inside virtuous circle: spatial resol., power, flex mat. budget, ...

  $\Rightarrow$ 0.18 $\mu m$ process needed instead of currently used 0.35 $\mu m$ process

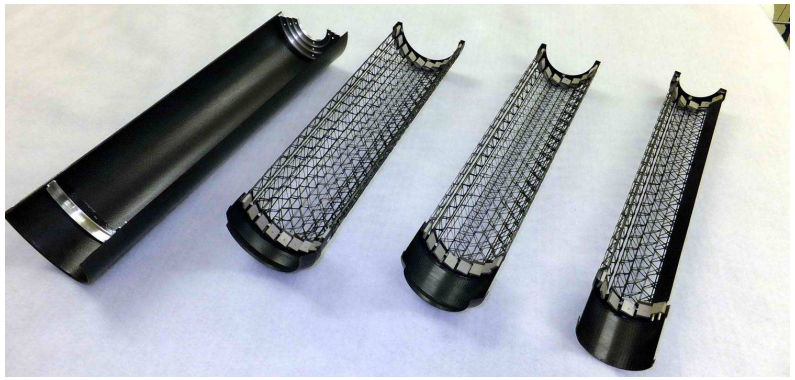


# Applications of CPS : ALICE-ITS Upgrade

- **ITS upgrade :** scheduled for ”2017-18” LHC long shutdown
  - ⁕ exploits space left by replacement of beam pipe with small radius (19 mm) section
  - ⁕ addition of L0 at $\sim$ 22 mm radius to present ITS & replacement of (at least) inner part of present ITS
  - ⁕ 2 geometry options considered (CDR) :
    - ◇ 7 layers with pixels ($\gtrsim$ 9 m$^2$, O($10^{10}$) pixels !)
    - ◇ 3 inner layers with pixels & 4 outer layers with $\mu$strips

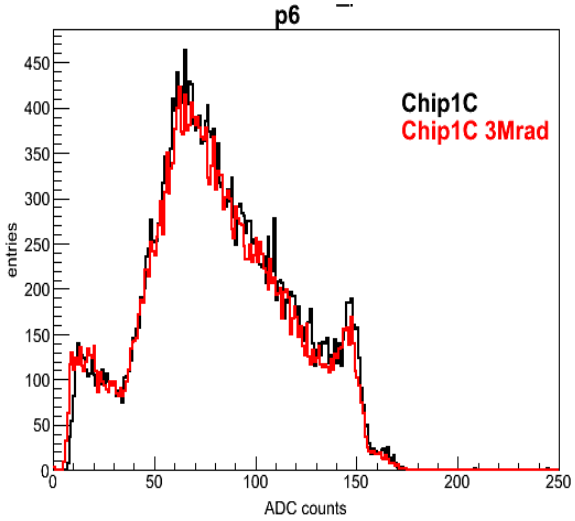


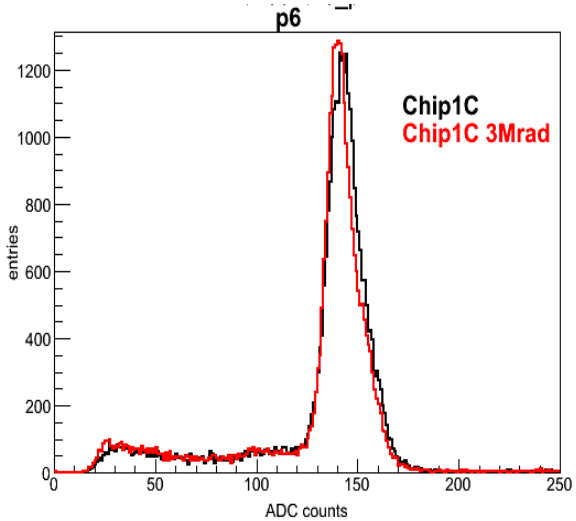
- **Differences w.r.t. ULTIMATE/MIMOSA-28 :**
  - ⁕ $\sim$ 1 MRad & $10^{13}$ $n_{eq}$/cm$^2$ at T = 30°C (target values)
  - ↪ **0.18 $\mu m$ 4-well HR-epi techno. (instead of 0.35 $\mu m$ 2-well hR-epi)**
  - ⁕ $\sim 1 \times 3$ cm$^2$ large sensitive area (instead of $2 \times 2$ cm$^2$)
  - ⁕ parallelised rolling-shutter (pot. in-pixel discri.) $\rightarrowtail$ $\sim$ 10–30 $\mu s$
  - ⁕ 1 or 2 output pairs at $\gtrsim$ 300 MHz (instead of 1 output pair at 160 MHz)
  - ⁕ $\sigma_{sp} \sim 4\ \mu m$; ladders $\sim$ 0.3 % $X_0$
  - ▷▷▷ **Conceptual Design Report $\rightarrowtail$ approved by LHCC in Sept. 2012**
    - ↪ **may include Muon Forward Tracker (MFT) using CPS**
  - ▷▷▷ **Technical Design Report to be delivered in Q3/2013**



# Charge Sensing Properties of 0.18 $\mu m$ Process

- **MIMOSA-32 lab tests ($^{55}$Fe source) of pixel matrix with analog output**
  - ⁂ Read-out time of each sub-matrix = 32 $\mu s$
  - ⁂ Observed CCE (20×20 $\mu m^2$ pixels) :
    - seed pixel : ∼ 40–50 % ▷ ▷ ▷ ▷
    - 2×2 pixel cluster : nearly 100 % ▷ ▷ ▷
      - ⇛ confirms Epi. layer 1-5 $k\Omega \cdot cm$
    - No parasitic charge coll. seen with Deep P-well
    - CCE of 20×40 $\mu m^2$ pixels
      - ↪ seed ∼ 30 %; with 1st crown ∼ 70-80 %
  - ⁂ Noise $\lesssim$ 20 e$^-$ ENC at 20°C, unchanged at 35°C
  - ⁂ Irradiation: 0.4/1/3 MRad ⟼ ∼ no effect up to 35°C **(tbc !)**

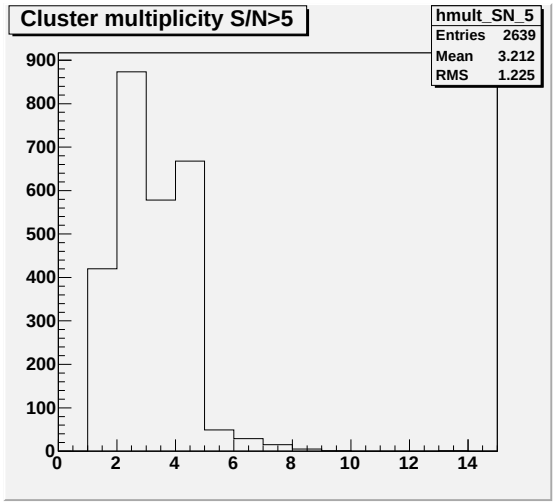


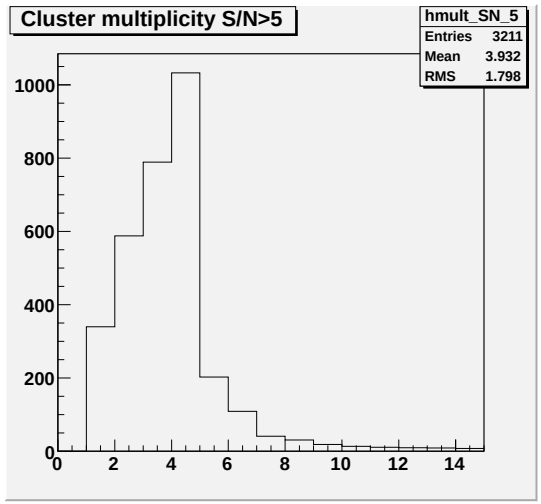

- **Beam tests :**
  - ⁂ Cluster multiplicity for 60 & 120 GeV charged particles

| Radiation Load | 20×20$\mu m^2$ 2T | 3T | Deep P | 20×40$\mu m^2$ 1D-3T | 2D-3T |
|---|---|---|---|---|---|
| **0** | 3.7 | 3.3 | 3.2 | 4.0 | 2.8 |
| | (1.4) | (1.3) | (1.2) | (1.9) | (1.2) |
| **1 MRad and** | 3.0 | 2.7 | 2.6 | 2.7 | 2.4 |
| **$10^{13} n_{eq}$/cm$^2$** | (1.2) | (1.1) | (1.1) | (1.5) | (1.2) |

**Deep P-well**




**Rect. 1D**



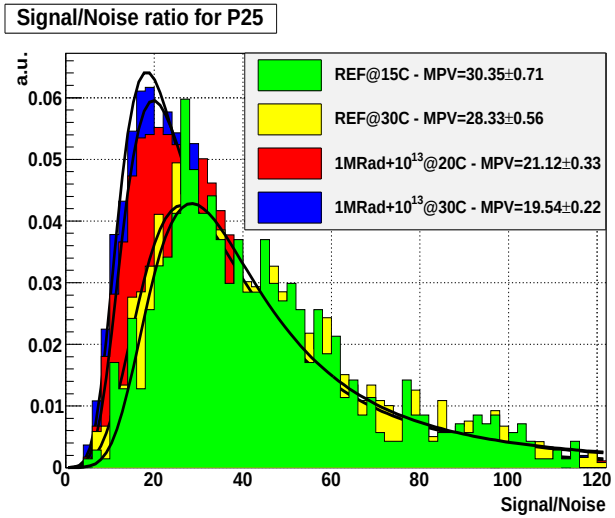

⇛ **High resistivity of epitaxial layer confirmed**

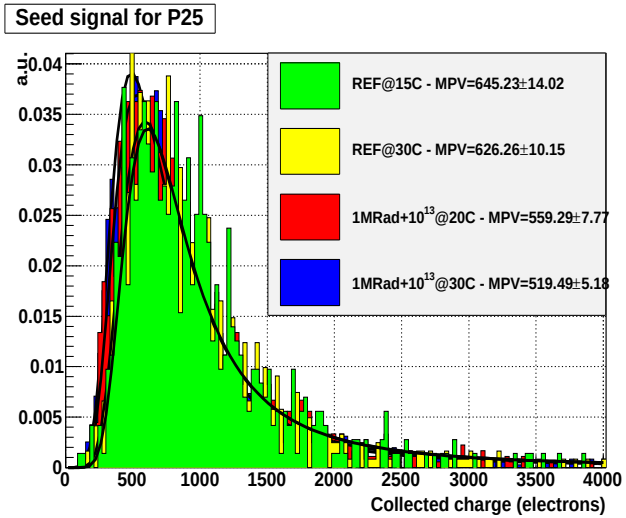
# Beam Test Results of 0.18 $\mu m$ Process Pixels

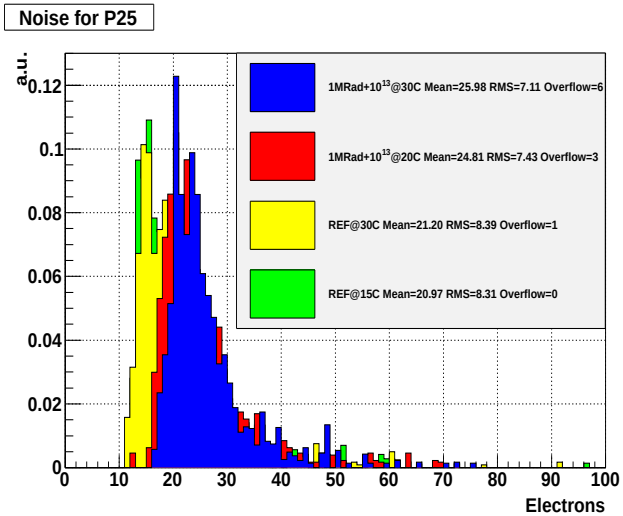
- DATA COLLECTED ON SPS/T4-H6 FROM NOV. 19TH TO 28TH: 80 & 120 GEV PARTICLES (& 20 GEV)
  - $\sim$ 25,000 tracks reconstructed in MIMOSA-32ter prototype $\equiv$ arrays of pixels with in-pixel ampli. & clamping
  - Test results presented at NSS/MIC-12, LCWS-12, RESMDD-12, VCI-13
- $20\times20\mu m^2$ PIXELS WITH N-&P-MOS AMPLI WITH FEEDBACK LOOP ENDED WITH FW BIASED DIODE:

| **Radiation load** | **0 + 0** | | **3·10$^{12}$ n$_{eq}$/cm$^2$ + 300 kRad** | | **10$^{13}$ n$_{eq}$/cm$^2$ + 1 MRad** | |
|---|---|---|---|---|---|---|
| **Coolant temperature** | **15°C** | **30°C** | **20°C** | **30°C** | **20°C** | **30°C** |
| **SNR** | 30.4 $\pm$ 0.7 | 28.3 $\pm$ 0.6 | 22.0 $\pm$ 0.3 | 23.0$\pm$ 0.3 | 21.1 $\pm$ 0.3 | 19.5 $\pm$ 0.2 |
| **Detection Efficiency** | 99.86 $\pm$ 0.14 % | 99.59 $\pm$ 0.14 % | 99.63 $\pm$ 0.13 % | 99.49 $\pm$ 0.16 % | 99.34 $\pm$ 0.19 % | 99.35 $\pm$ 0.13 % |

- SAME PIXEL : SNR(SEED), Q(SEED), N VS T (15–30°C) & RADIATION LOAD (1 MRAD $\oplus$ $10^{13}$N$_{eq}$/CM$^2$)

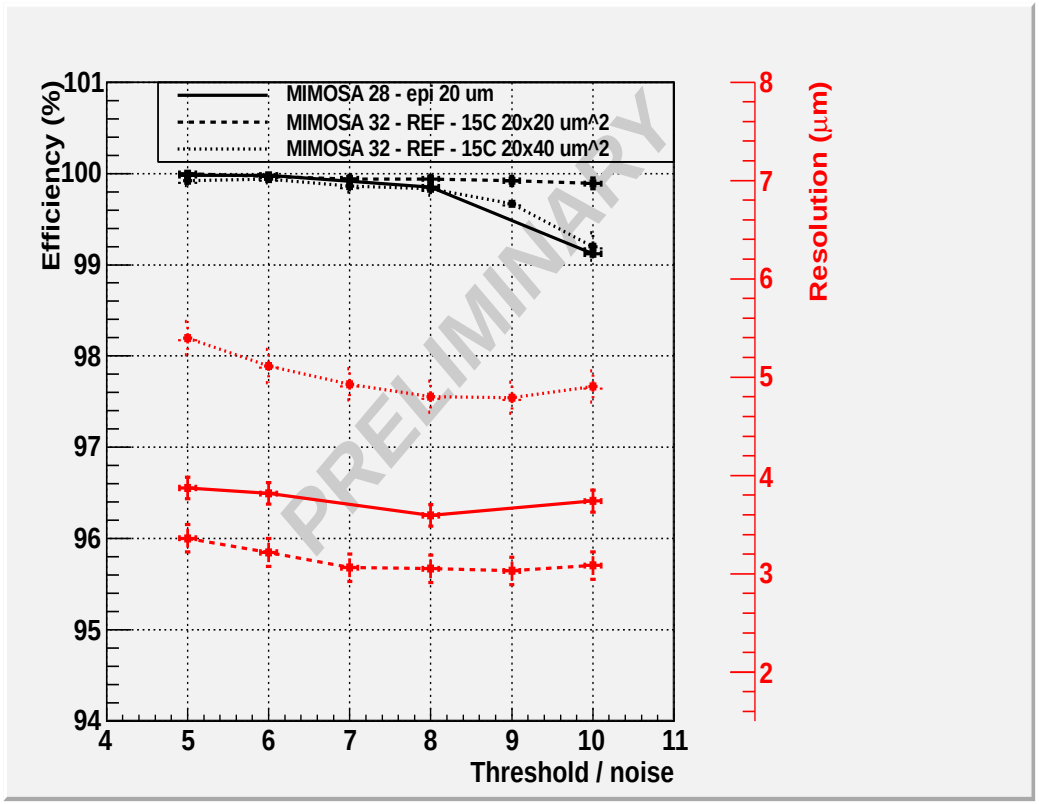


# Spatial Resolution

- **Beam test (analog) data used to simulate binary charge encoding :**
  - ✳ Apply common SNR cut on all pixels using $<$N$>$
    ↪ simulate effect of final sensor discriminators
  - ✳ Evaluate single point resolution (charge sharing) and detection efficiency vs discriminator threshold for 20x20 $\mu m^2$ pixels and 20x40 $\mu m^2$ staggered pixels (1 sensing diode)

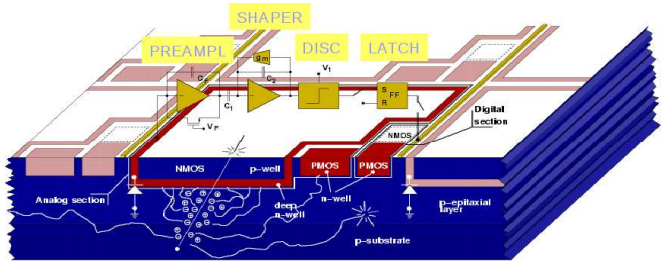


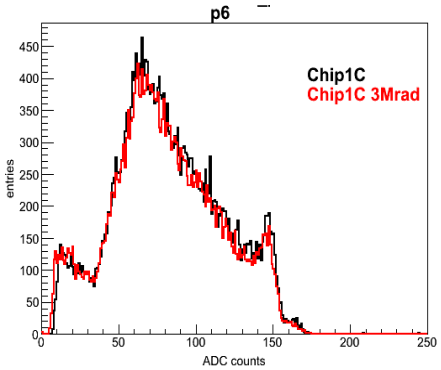

- **Comparison of 0.18 $\mu m$ technology ($>$ 1 $k\Omega \cdot cm$) with 0.35 $\mu m$ technology ($<$ 1 $k\Omega \cdot cm$)**
  (pitch values: 20.0 $\mu m$ and 20.7 $\mu m$)

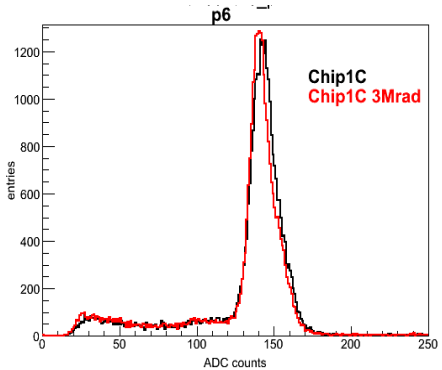
- $\sigma_{sp}^{bin} \simeq 3.2 \pm 0.1\ \mu m$ (20x20 $\mu m^2$)
  AND $\simeq 5.4 \pm 0.1\ \mu m$ (20x40 $\mu m^2$)

# Perspectives: Fast 2D sensors

- **Evolve towards feature size of O(100) nm feature size :**
  - ⁕ $\mu$circuits: smaller transistors, quad-well, more Metal L., ...
  - ⁕ sensing: (fully) depleted 20–40$\mu m$ sensitive vol., ...
- **Benefits :**
  - ⁕ faster read-out $\Rightarrow$ improved time resolution
  - ⁕ higher $\mu$circuit density $\Rightarrow$ higher data reduction capability
  - ⁕ thinner gates, depletion $\Rightarrow$ improved radiation tolerance
  - ⁕ lower $V_T$ $\Rightarrow$ reduced power
- **On-going R&D (examples) :**
  - ⁕ *APSEL* sensor (130 nm) for future Vx Det. :
    - ○ in-pixel pre-amp + shaping + discri. ▷▷▷
    - ○ sensing through buried n-well
    - ○ shallow n-well hosting P-MOS T
  - ⁕ *TJSC* sensors (180 nm) for ALICE-ITS upgrade :
    - ○ high-resistivity, 18-40 $\mu m$ thick, epitaxy ▷▷▷
    - ○ deep n-wells hosting P-MOS T




- **Main limitations :**
  - ⁕ VDSM technologies not optimised for analog $\mu$circuits (low V !) $\Rightarrow$ reliability
  - ⁕ conflict between speed (e.g. 10 ns) and granularity (e.g. 20$\times$20 $\mu m^2$ pixels)

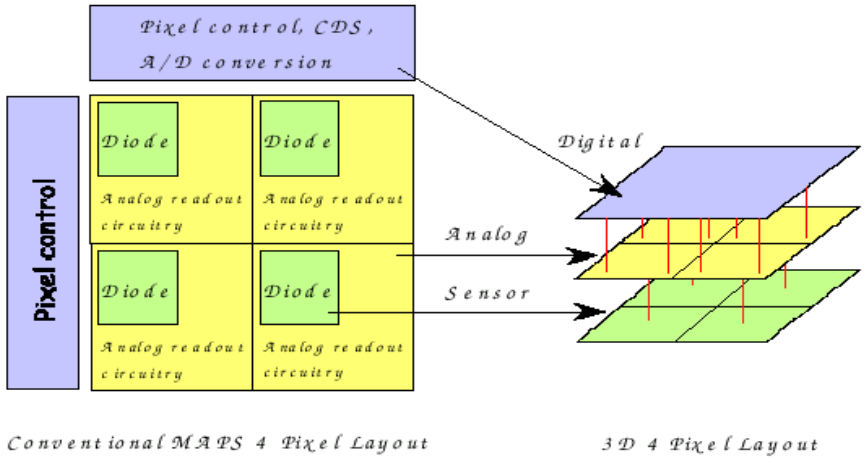
$\Rightarrow$ **Natural trend : chip stacking**

# Using 3DIT to reach Ultimate CMOS Sensor Performances

- 3D Integration Technologies allow integrating high density signal processing $\mu$circuits inside **small** pixels by stacking ($\sim$ 10 $\mu m$) thin tiers interconnected at pixel level

- 3DIT are expected to be particularly beneficial for (small pixel) CMOS sensors :
  - combine different fab. processes $\Rightarrow$ chose best one for each tier/functionnality
  - alleviate constraints on peripheral circuitry and on transistor type inside pixel, etc.

- Split signal collection and processing functionnalities :
  - *Tier-1: charge sensing*
  - *Tier-2: analog-mixed $\mu$circuits*
  - *Tier-3: digital $\mu$circuits*




- **The path to nominal exploitation of CMOS pixel potential :**
  - fully depleted $\sim$ 20–40 $\mu m$ thick epitaxy $\Rightarrow$ $\lesssim$ 5 ns coll. time, rad. hardness $>$ Hybrid Pix. Sensors ???
  - FEE with $\leq$ 10 ns time resolution $\rightarrowtail$ solution for CLIC & HL-LHC specifications ???
  - 2 tiers may be enough in most cases (e.g. 180 nm $\oplus$ 65 nm process)
    $\Rightarrow$ significant connection process simplification (explored in EU project AIDA)

# SUMMARY

- **CMOS sensor technology has become mature for high performance vertexing and tracking**
  - ⁕ most relevant for specifications governed by granularity, material budget, power consumption, cost, ...
  - ⁕ excellent performance record with beam telescopes (e.g. EUDET project)
  - ⁕ 1st vertex detector experience will be gained with STAR-PXL, having started data taking May 9th, 2013
  - ⁕ numerous spin-off applications : hadrontherapy (FIRST exp., p-imager), dosimetry, ...
  - ⁕ new generation of sensors under development for experiments $>$ 2015 (including trackers & calo.)
    $\hookrightarrow$ ALICE-ITS upgrade, CBM-MVD (see talk of M. Deveaux), ..., ILC VD (?), ...

- **Recently accessible technologies tend to allow coming quite close to full potential of CPS :**
  **($>$ 2 k·cm, up to $\sim$ 50$\mu m$ thick, epitaxial layer with 4-well, O(100)$\mu m$ feature size processes)**
  $\hookrightarrow$ **applications to X-Ray imaging, TraCal, ...**

- **Evolution of industry opens the door to 2 "natural" steps towards "ultimate" CPS performances :**
  - ⁕ **fast 2D sensors** fab. in VDSM CMOS techno. may allow $\lesssim$ O(1)$\mu s$, $\gg$ 10 MRad, $>$ $10^{14}$ $n_{eq}/cm^2$
  - ⁕ **3D chips** are expected to "exhaust" the technology potential, but there is still a rather long way to go
    $\hookrightarrow$ 1st step : 2-tier sensors

  $\Rightarrow$ **may lead to fast & rad. hard devices suited to HL-LHC & CLIC**

# Examples of Applications in Subatomic Physics

- Beam telescopes :
  - EUDET (FP-6 / 2006-2010) : 6 planes with $1 \times 2$ cm$^2$ sensors
  - AIDA (FP-7 / 2011-2015) : $\geq$ 3 planes with $4 \times 6$ cm$^2$ sensors
- Vertex detectors :
  - STAR-PXL at RHIC : 2 layers
  - CBM-MVD at FAIR/GSI : 2-3 stations
  - ALICE-ITS at LHC : 3 inner layers
  - FIRST at GSI (p/C PMMA x-sec) : 4 stations
  - option for ILD-VTX at ILC : 3 double-layers
- Trackers (”large pitch”) :
  - BES-III at BEPC
  - ALICE-ITS at LHC : 4 outer layers ($\lesssim$ *10 m$^2$ !*)
  - in general : trackers surrounding vertex detectors
- EM calorimetres : SiW calorimetre
  - generic R&D on **T**RA**C**AL