The 3D integration and SOI pixels

Grzegorz (Gregory) Deptuch
on behalf of ASIC Design Group
PPD/EED Fermilab

532. WE-Heraeus Seminar
Bad Honef, Germany, May 23-25, 2013

U.S. DEPARTMENT OF ENERGY

Fermilab

Outline

- (3D-IC) Introduction:
  - definition
  - flavors
  - *alignment, TSVs, wafer bonding*
  - advantages
- (3D-IC) Status
  - Fermilab organized 3D-IC run - peripeteia
  - Results at Fermilab – *selected VICTR/VIPIC*
  - 3D-IC directions
- (SOI APS) Perspectives
  - Technology
  - Status … at Fermilab
- Conclusions

3D-IC: definition

3D-IC definition

3D-IC revolution

A chip in three-dimensional integrated circuit (3D-IC) technology is composed of two or more layers of active electronic components using horizontal intra-tier and vertical inter-tier connectivity routing

- Through Silicon Vias (TSV): small diameter vertical connectivity *(not only to build electronic chips but also for attaching detectors to readouts)*
- Bonding: Oxide-, polymer-, metal-, or adhesive strengthened- (W-W, C-W or C-C)
- Wafer thinning: aggressive and ultra-precise
- Back-side processing: metallization and patterning

Why 3D-IC?

Real estate analogy

How much time, effort and energy (gasoline) is needed to communicate with your neigbors that live in a 2D assembly?

3D-IC: definition

3D per se

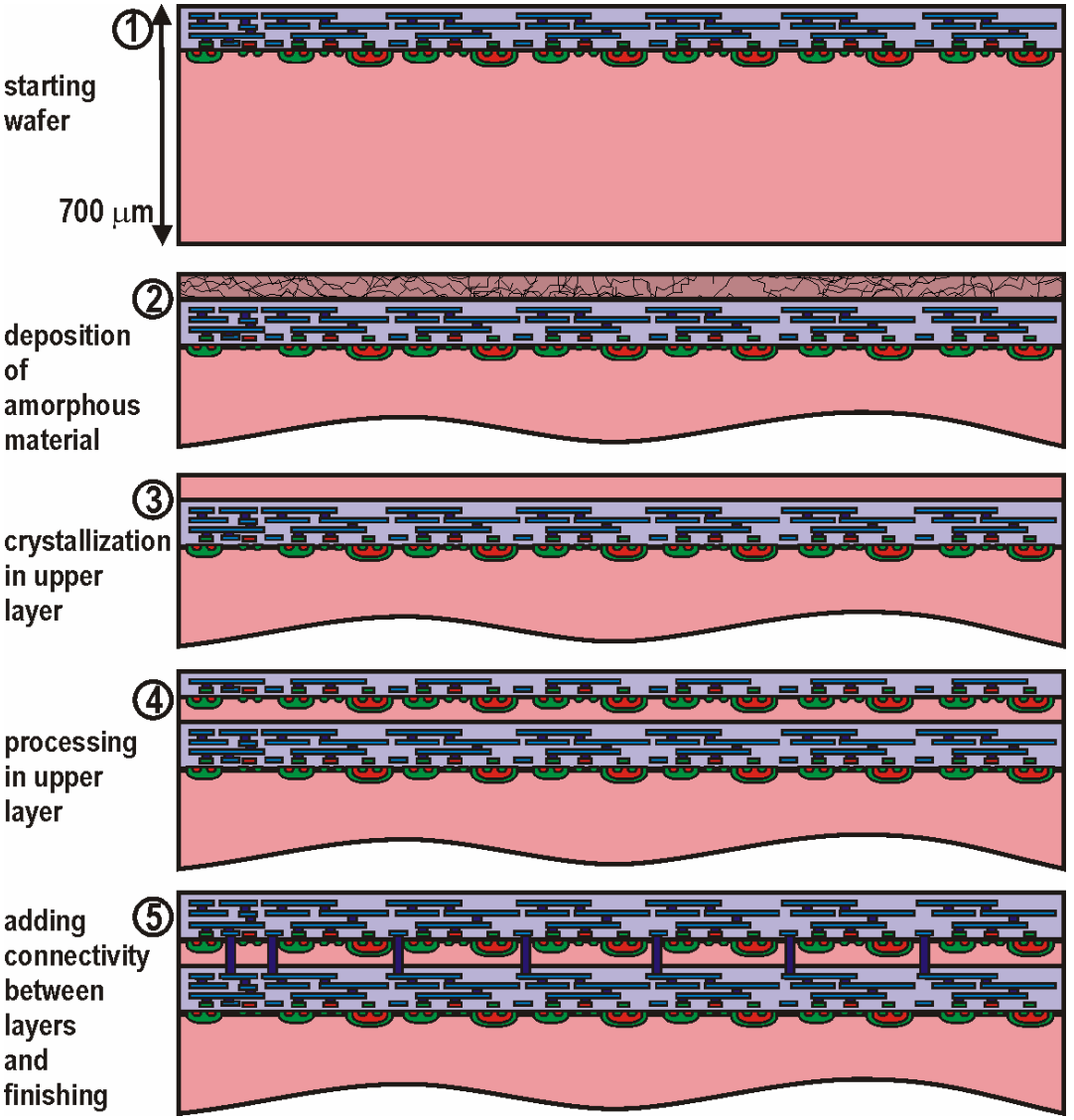
growing

3D circuit

Very difficult

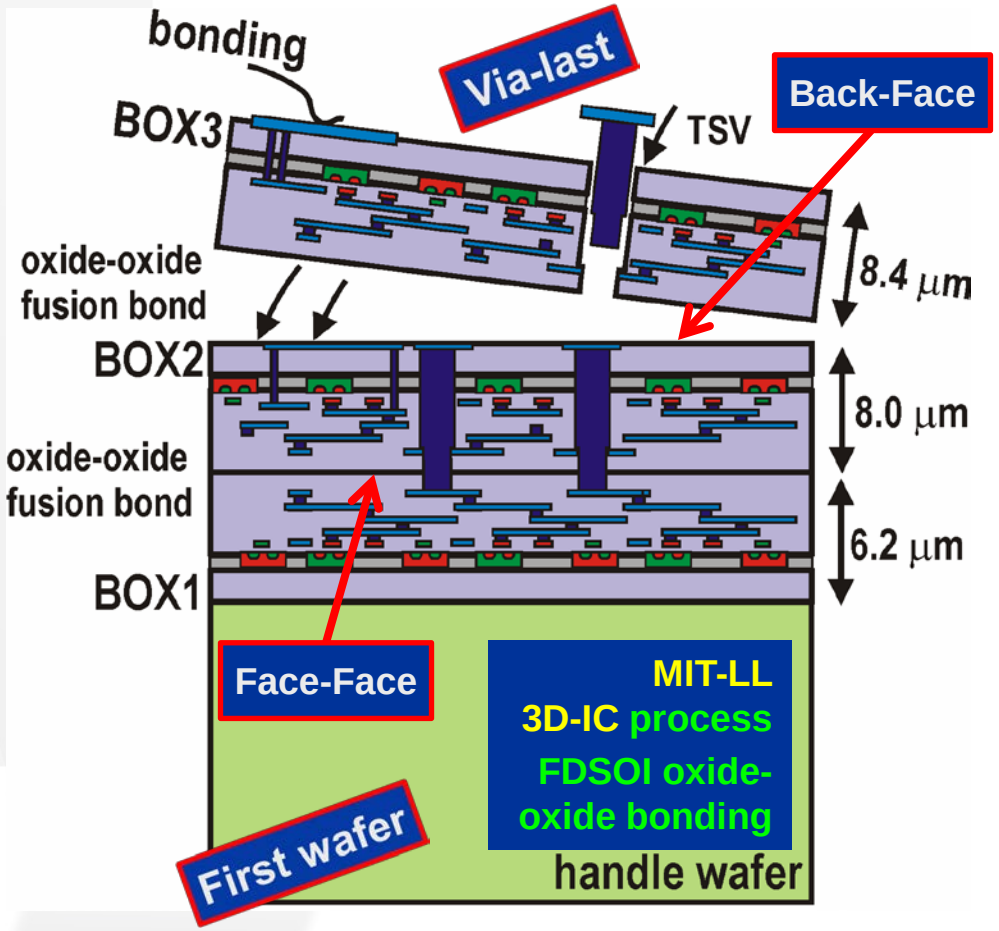
Crystallization and activation of dopants require high temperature that is not compatible with steps already acomplished on underneath layers (e.g. mettalization)

Thus not available ...

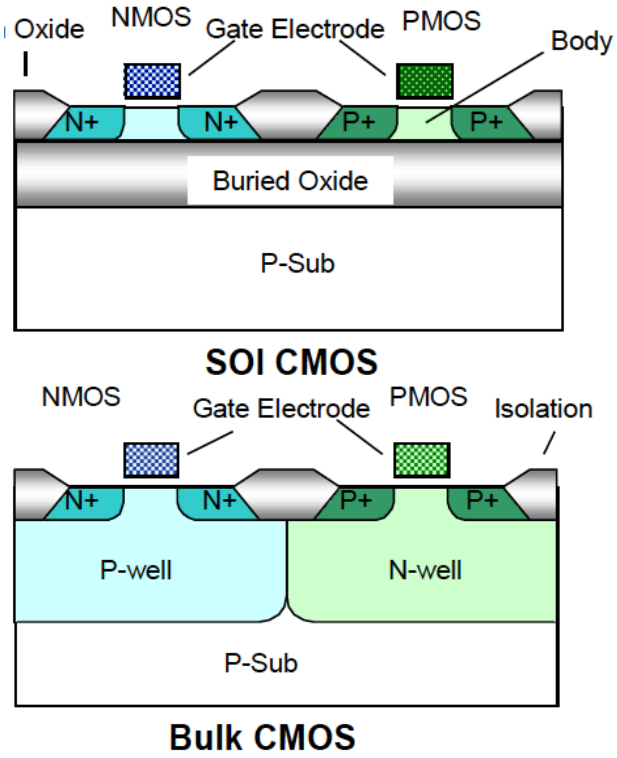


3D-IC: flavors (2006)

VIA LAST (SOI) vias added to wafers after bonding and thinning – excludes large area for local interconnect in TSV locations; based on SOI (oxides = etch stoppers and bonding surfaces) use of heteregenous wafers

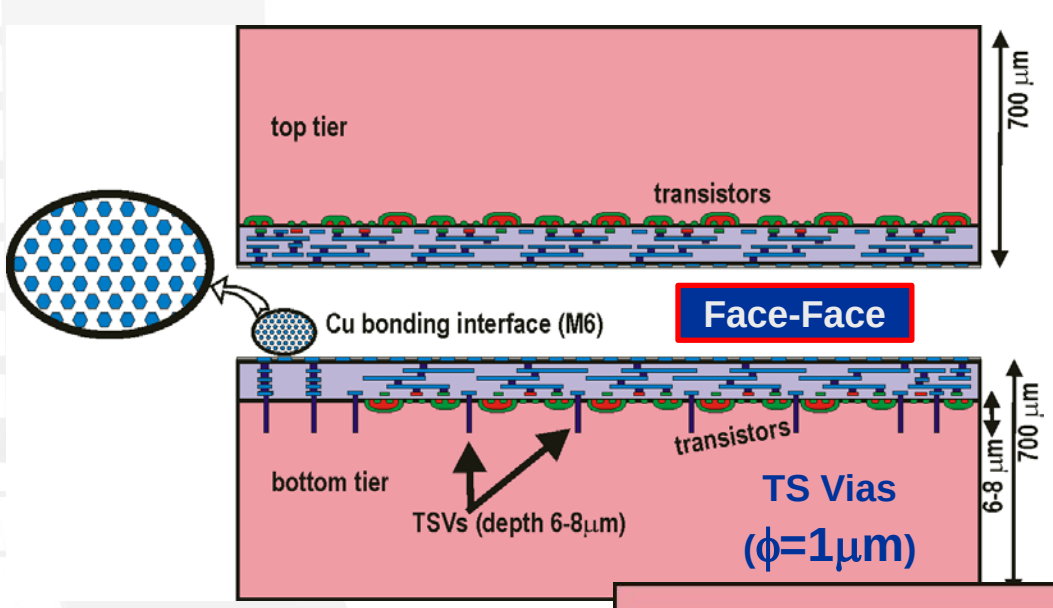


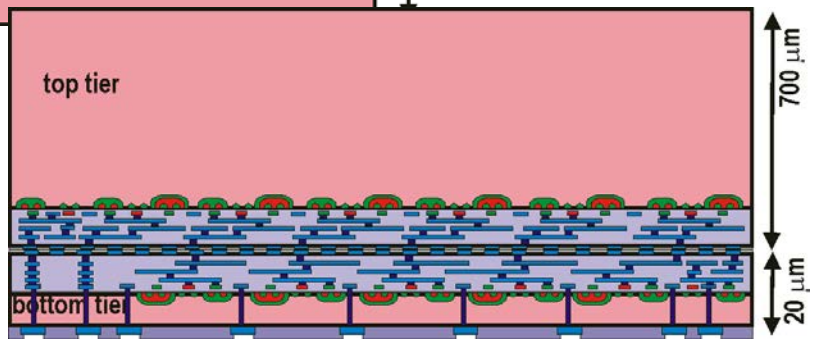
Technology option based on VIA LAST and SOI wafers



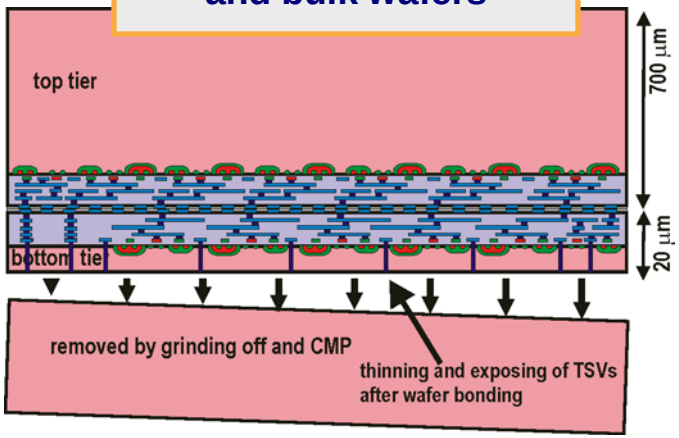
3D-IC: flavors (2009 - …)

VIA FIRST (bulk) vias are part of the wafer processing inserted before or right after forming transistors – metal interconnect lines are not excluded over TSVs; based on bulk wafers, use of wafers from specific foundry





Technology option based on VIA FIRST and bulk wafers

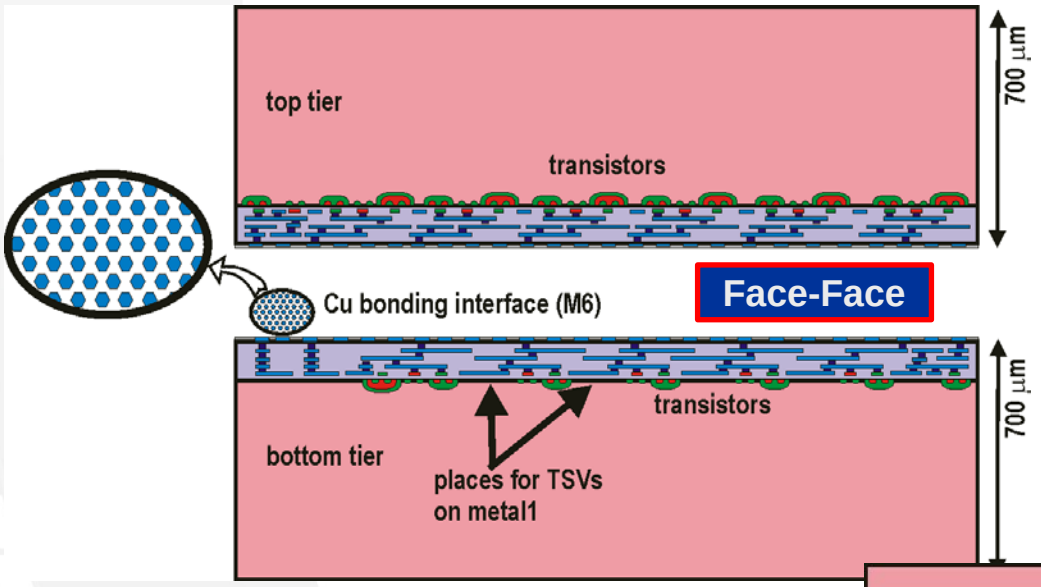


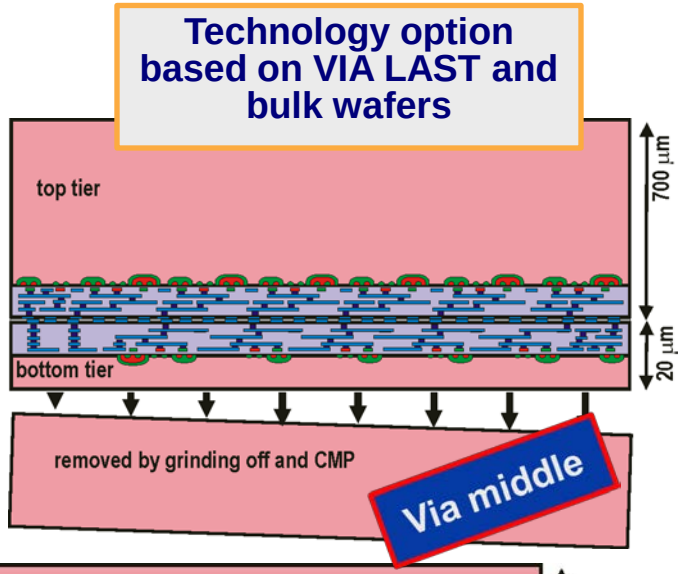
8” wafers, ~26 × 31 mm^2 reticule (GF 130nm), 6th metal = bond interface for face-face Cu-Cu thermo-compression bonding

Tezzaron 3D-IC
bulk CMOS Cu-Cu thermocompression or Cu DBI bonding

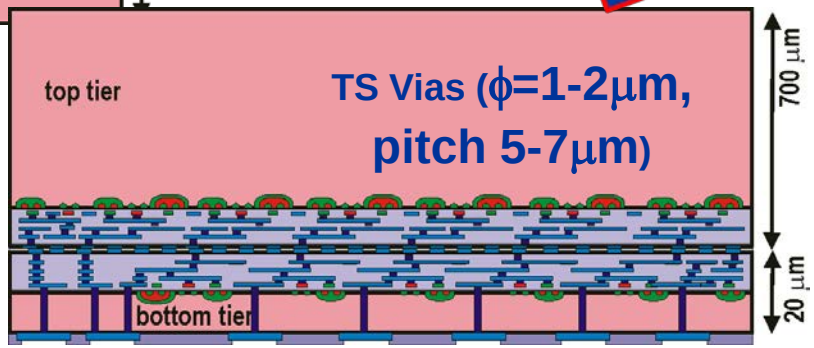
3D-IC: flavors (2013)

VIA LAST (bulk) vias added to wafers after bonding and thinning – requires larger pads for TSVs & excludes some routing in TSV locations; based on bulk wafers (make independent 3D stacking from specific foundry, but …)





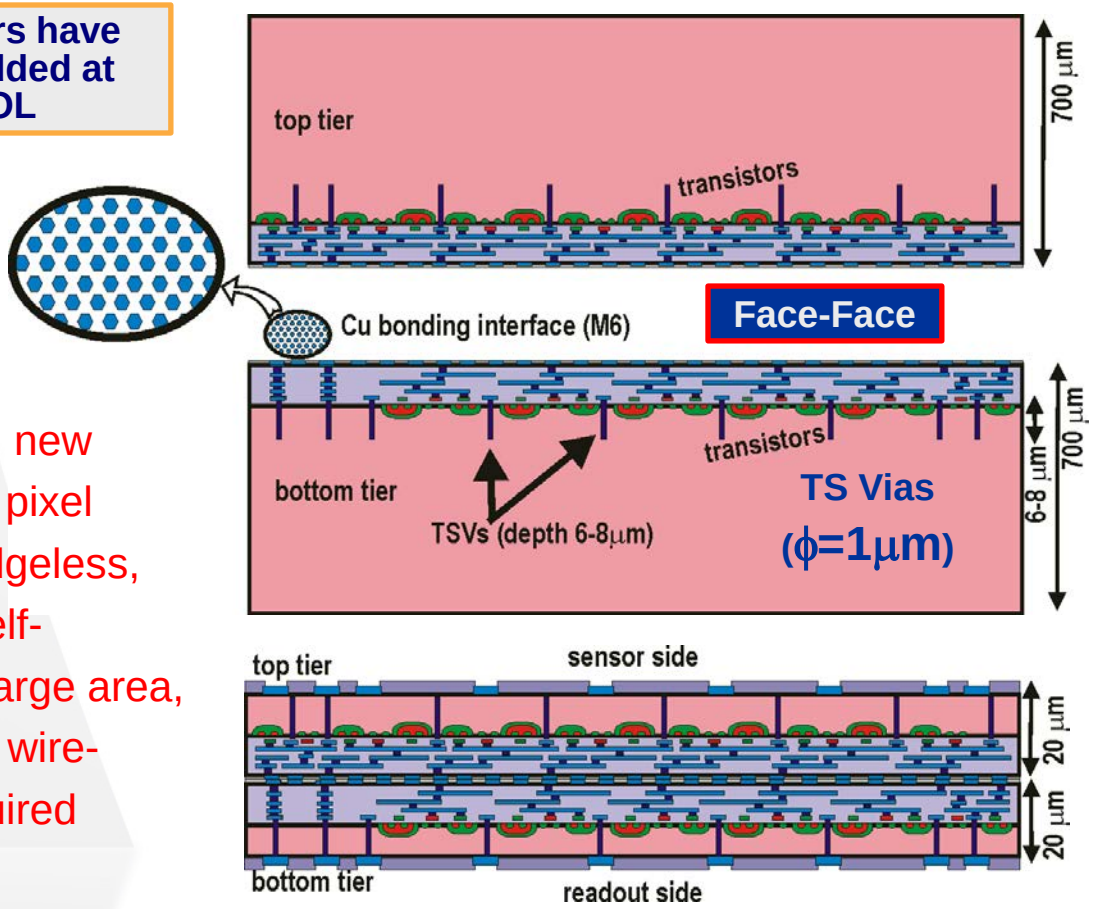
Relying on addition of TSVs by the mainstream foundry is a significant risk factor - instead leave out in-foundry TSVs and add them after bulk CMOS Cu-Cu thermocompression or Cu DBI bonding abd wafer thinning



3D-IC: flavors (most appealing)

VIA FIRST in both tiers vias added to both tiers at FEOL stage - using handle wafer makes possible processing of both sides of a 3D stack and attaching of one side to a sensor, while the other is to be mounted on PCB

Both tiers have TSVs added at FEOL



Vias present in both tiers

Opens up on new structures of pixel detectors: edgeless, seamless, self-supporting, large area, etc. no more wire-bonding required

Achieved on the 1st HEP 3D MPW run organized by Fermilab based on Tezzaron 3D-IC process

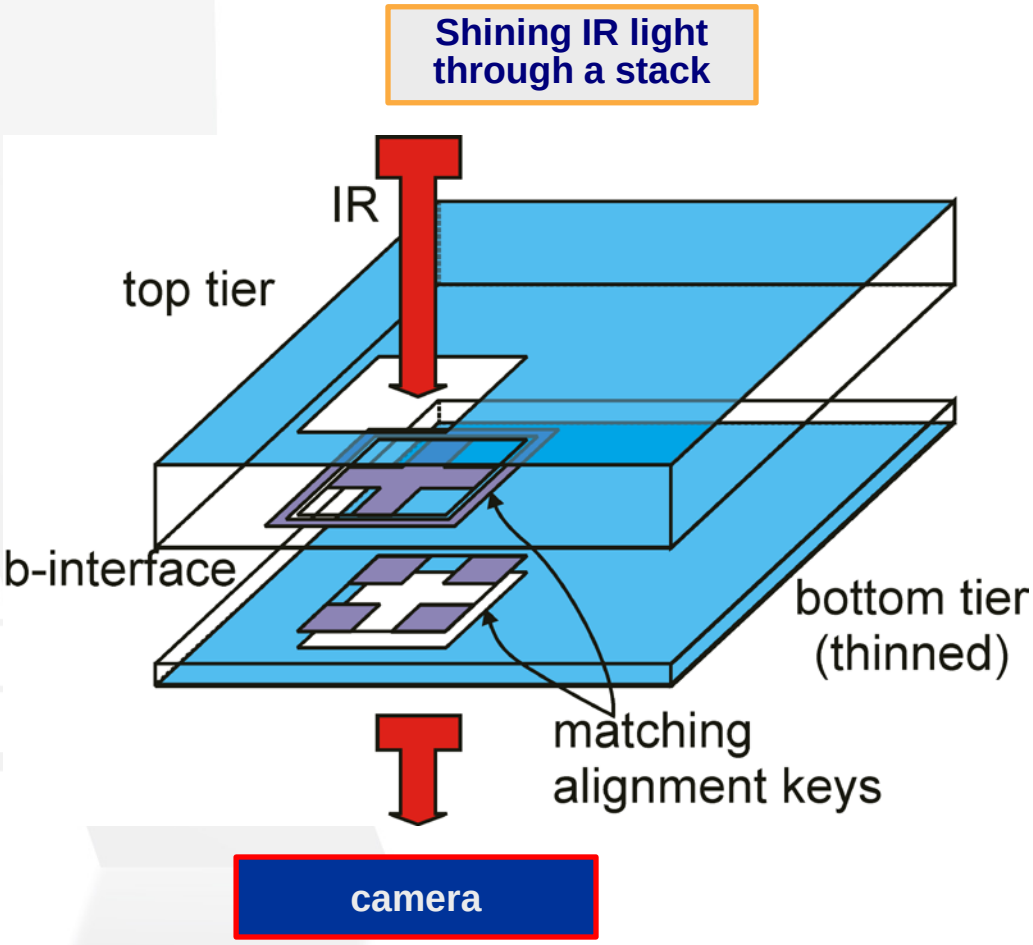
bulk CMOS Cu-Cu thermocompression or DBI bonding

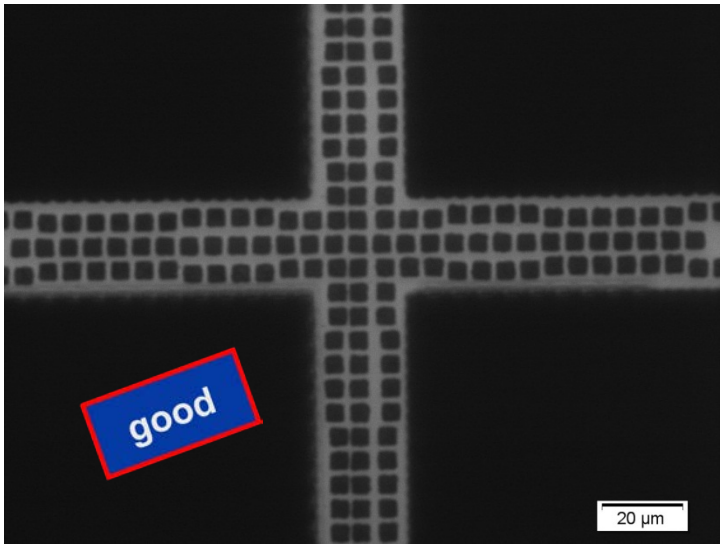
Using GF 130nm wafers

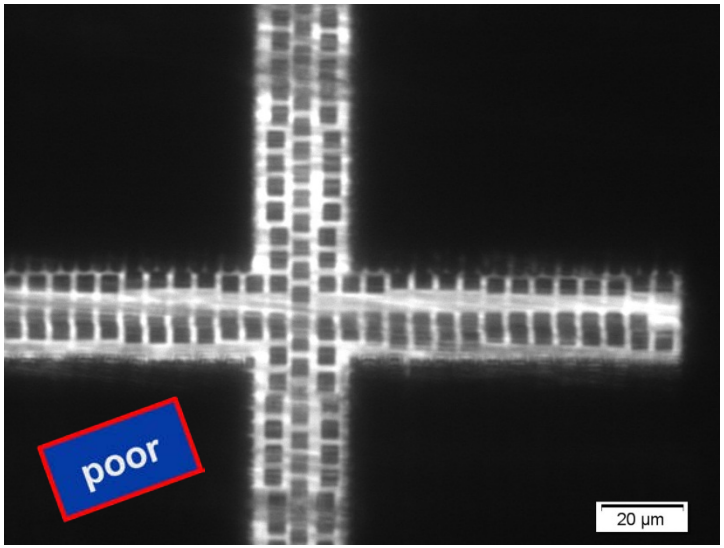
3D-IC: alignment of wafers

alignment keys

Keys placed on both wafers, imaging of achieved in infra-red light,







3D-IC: TSVs

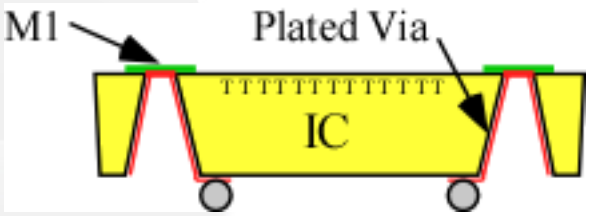
- **dry etching (RIE or Bosch) for "drilling" TSVs' cavities; typically 1:5-1:10 ϕ/d; (laser drilling used too)**
- **could be extensions of STI process in ICs**
- **cylindrical vias, ϕ>3 μm filled with electro-plated Cu; W doesn't work well for ϕ>2μm**
- **Cu serious issues with thermal stress in Si interface; W used in high density TSVs**
- **Annular TSV geometries are popular, especially with W filling**

Material	Thermal conductivity (W/m/K)	Thermal coefficient (ppm/K)
Si	149	2.6
SiO_2	1.4	0.5
Al	235	23.1
W	170	4.5
Cu	410	16.5

contrary to popular belief, TSVs are not effective in assisting the transport of heat

low density TSV:

- **Through unthinned or partially thinned wafers to bring connectivity at the pad level (3D-SOC),**
  - Large cavity diameter >50μm
  - Cavity completely filled or cavity walls plated (poly-Si, Copper)

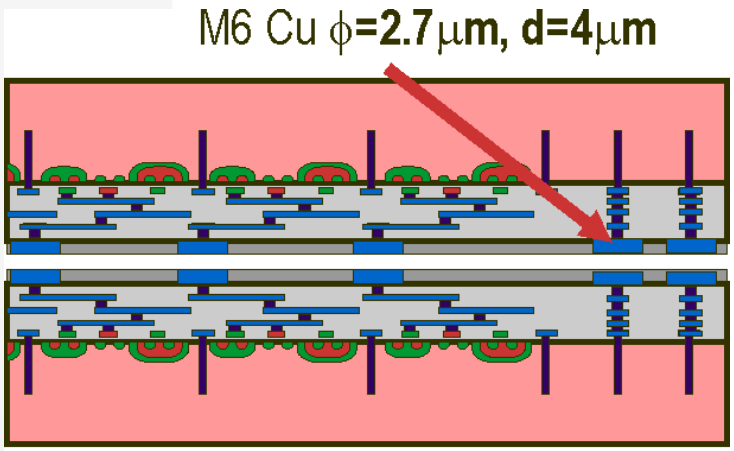


high density TSV:

- **Through thinned wafers to bring connectivity to local connections between transistor layers (groups of transistors in 3D-IC) or individual devices (3D-SIC)**
  - Ultra small cavity diameter ~1μm
  - Cavity completely filled with W
  - Liner obtained with SiO_2

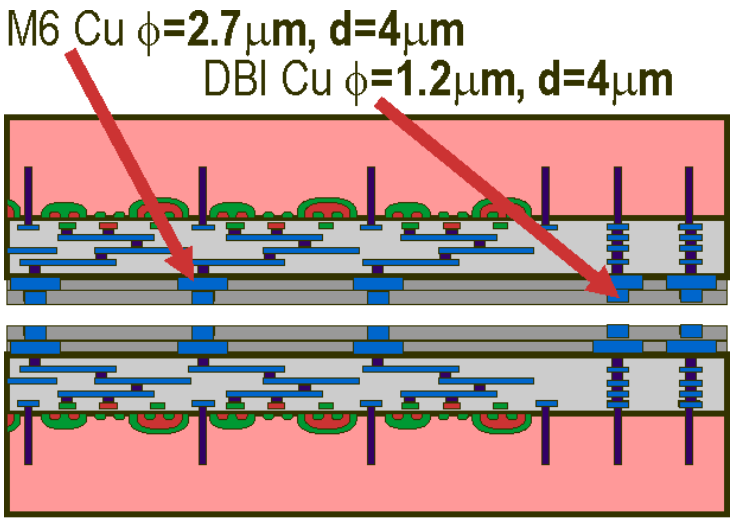
3D-IC: bonding of wafers

Tezzaron / Novati



Cu-Cu Thermocompression

Ziptronix / licensed to Novati

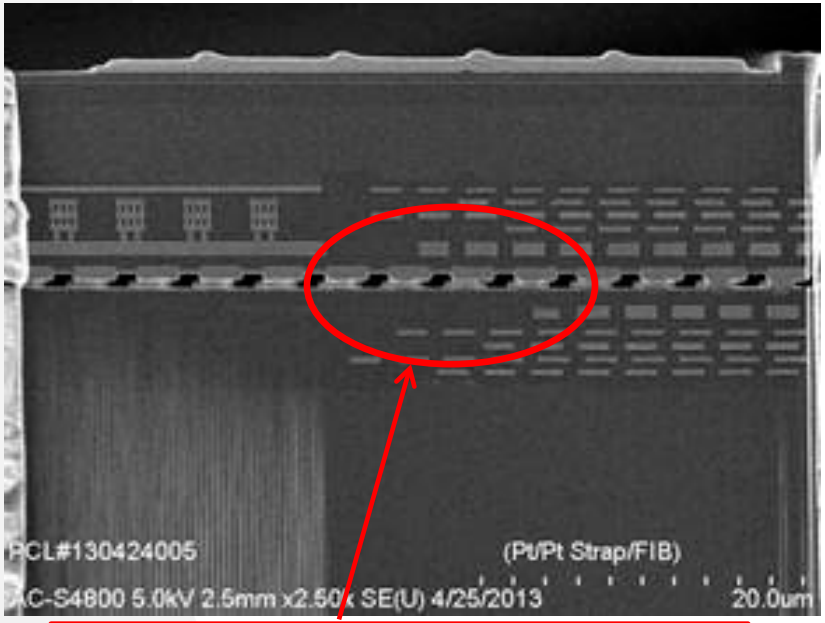


Cu DBI

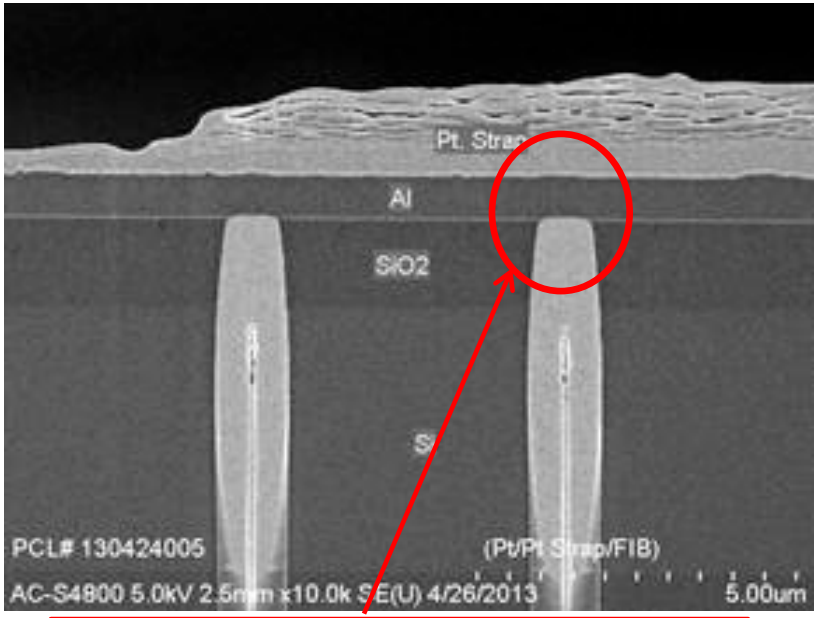
- Difference between Cu-Cu thermocompression and Cu DBI wafer bonding methods:
  - Cu-Cu not reworkable, bonding established by fusing metal pads, forgiving on surface planarity
  - Cu DBI reworkable shortly after bonding, bonding established by chemically fusing oxide surfaces, must be ultra planar

3D-IC: bonding of wafers

Tezzaron wafers



SEM image of Cu-Cu TC bonding interface on VIPIC1 acceptable alignment tolerance $3\sigma<1.2\mu m$



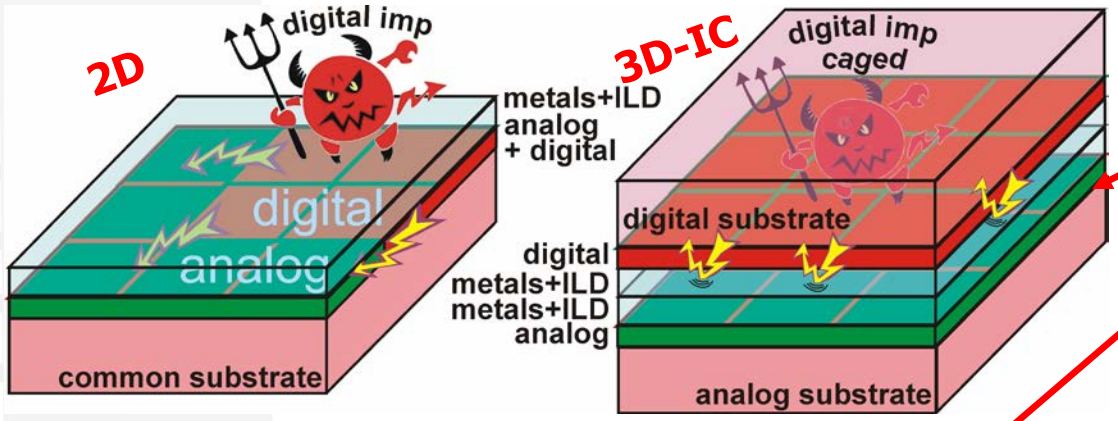
SEM image of W TSVs providing contact to back-side Al pad on VIPIC1

Not all wafer lots, not all chips look so perfect, nevertheless goo quality bonding and back-side processing is achievable

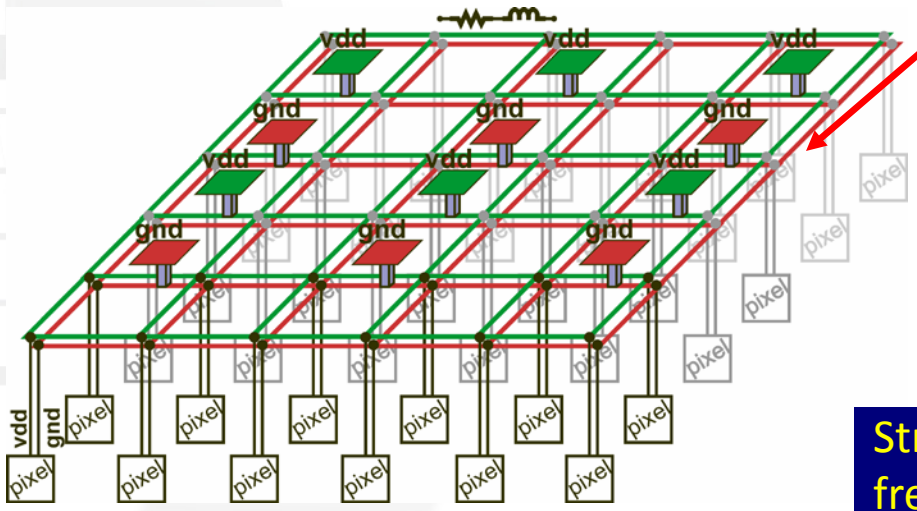
3D-IC: advantages

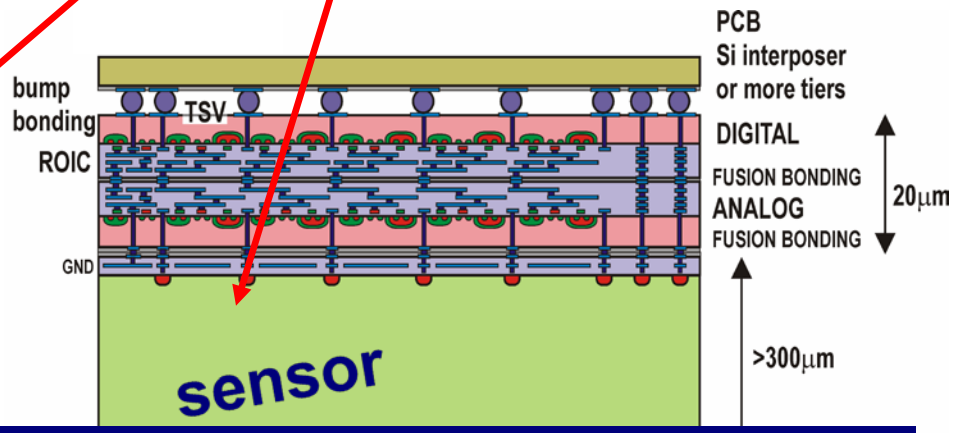
Why?

- 3D-IC offers a transformational change to address current roadblocks in advancing fine-grained detector, and with in-situ processing.



- 3D ROICs - complete separation of digital activity from low-noise analog parts
- 3D ROICs - uniform distribution of power supply and I/O pads on the back side
- ROICs can be integrated with sensors without bump-bonds

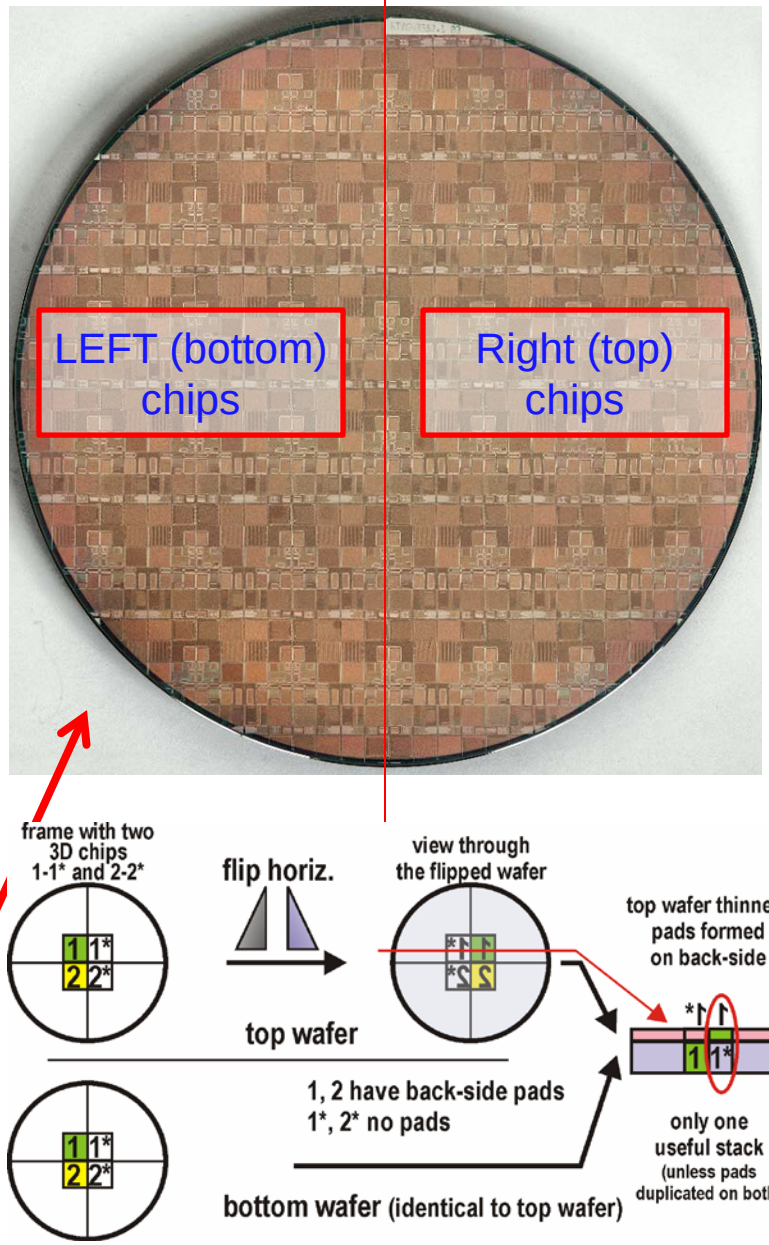




Strategic direction: 4 side buttable, dead-area-free detectors

‘Fermilab’ 3D-IC run

- **Initial (small) efforts started with MIT-LL 3D process in 2006 (DARPA 3-tier 3D run):**
  - **stimulated great interest among the detector community worldwide and move to Tezzaron/GF**
- **3D-IC Consortium established in late 2008, now 17 members; 6 countries: USA, Italy, France, Germany, Poland, Canada) + Tezzaron – *various goals among members, activities going at slower pace but progressing***
- **Fermilab organized first 3D-IC MPW run for HEP**
- **Designs in: 05/2009; Chartered (GF) 130nm**
  - **Fermilab had a role of silicon broker**
  - **Many challenges in working with cutting edge technology; to name some: design mistakes, incompatibility of software tools (Tezzaron not Cadence), lack of 3D oriented verification, handling of databases >10GB, shifting GF requirements (DRC), changing personnel at GF, etc.**
- **MPW frame accepted for fab in 03/2010**



130nm GF/Tezzaron wafer - FNAL MPW before 3D bonding; single mask set used to fabricate top and bottom tier chips on the same wafer;
Bonding by flipping wafers over symmetry line

‘Fermilab’ 3D-IC run

- **3D bonding did not yield for initial lot of wafer,**
  - **Fermilab MPW in fab in parallel with 2 other runs (DARPA and SNL) – they were successful**
  - **A) 3D bonding not successful on almost all wafer pairs from 1st lot 10/2011 (30 wafers, *2 recycled pairs bonded yielded some chips that were tested operational*)**
  - **B) 2nd lot is in bonding now (resubmission of 18 wafers)**
- **1st working chips obtained from 2 bonded pairs of wafers (A) in 06/2012**
  - **Fermilab tested VICTR (CMS track trigger) and VIPIC (X-ray imaging)**
  - **CPPM Marseilles tested FE-TC4 (ATLAS pixels)**
  - **Univ. of Bergamo / INFN tested MAPS chips**
- **2 new 3D wafers in 03/2013; 1wafer diced (a few TC bonded chips tested but misalignment found)**
  - **2 wafers are Cu-Cu TC bonded coming in May 2013**
  - **4 wafers are coming from Cu DBI bonding in June 2013 -> bonding to sensors using DBI with Ziptronix asap**
- **3D-IC MPWs in MOSIS portfolio**
  - **1st run offered in Nov 2011 –> in fab March 2012**
  - **No chips yet;**
  - **possible strategy change (not relying on GF and using via-middle after M4 or via-last after thinning (Tezzaron subsidiary: Novati)**

chips with pads on front side to a sensor DBI or stud bonding

chips with pads distributed on whole back surface

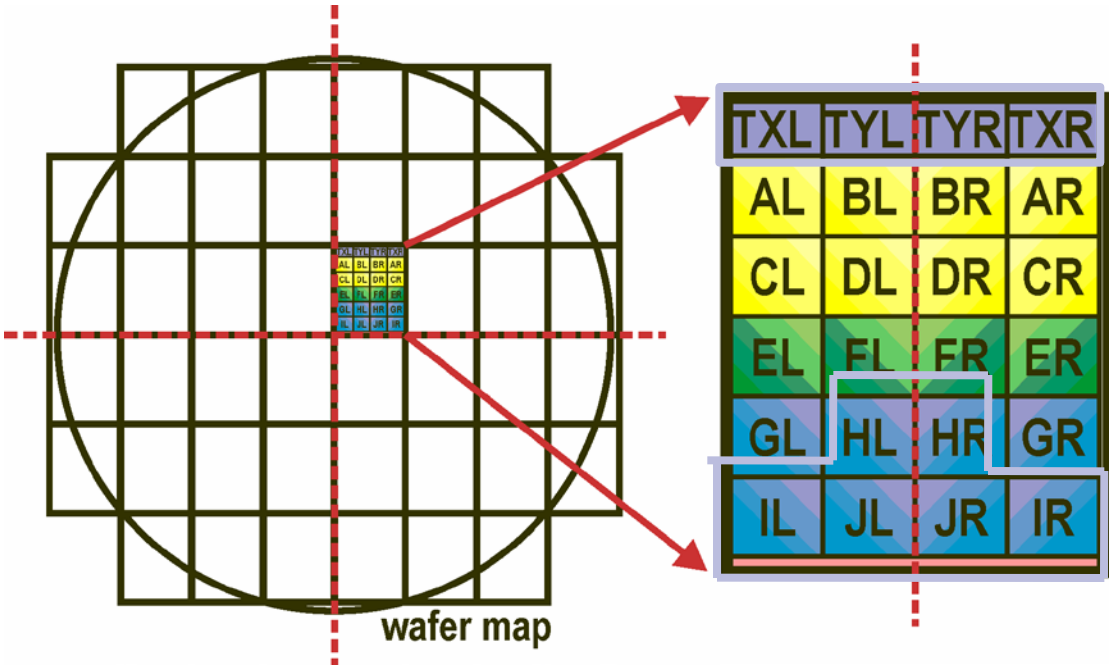
CMP CNRS-INPG-UIF CMC MICROSYSTEMS

ANNOUNCEMENT

CMP/CMC/MOSIS partner to introduce a 3D-IC process

Grenoble, France, 22 June 2010, CMP/CMC/MOSIS are partnering to offer a 3D-IC MPW service based on Tezzaron's SuperContact technology and GLOBALFOUNDRIES 130nm CMOS.

‘Fermilab’ 3D-IC run

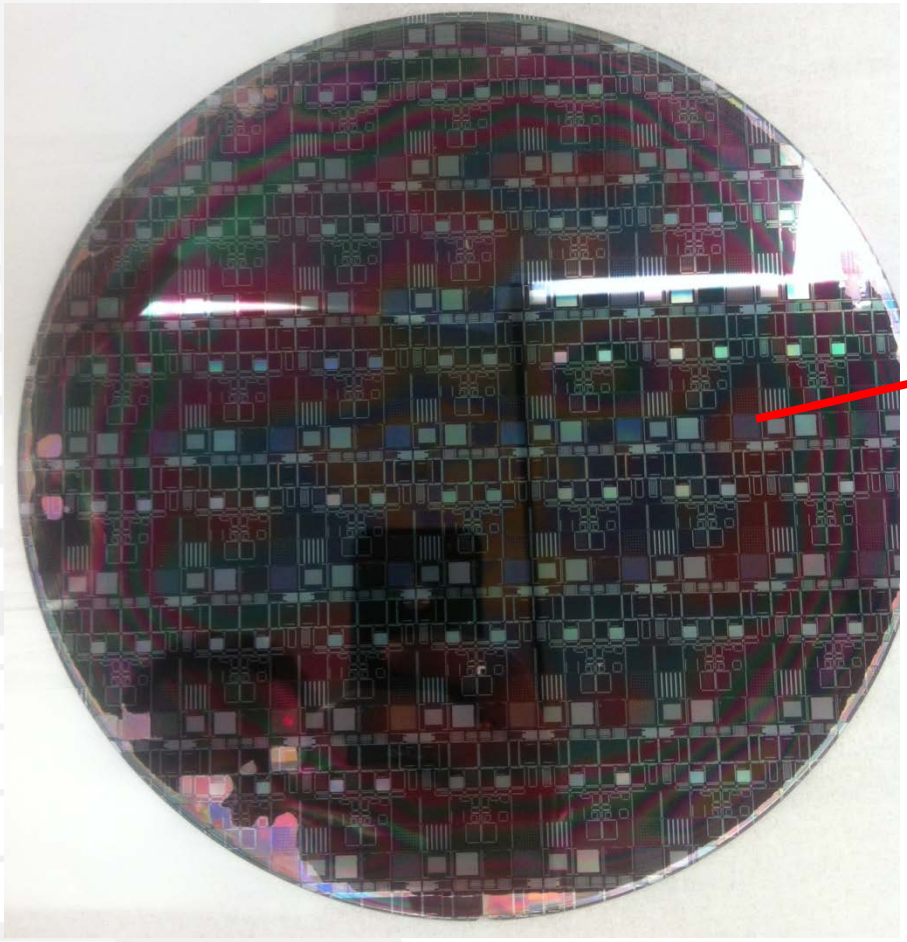


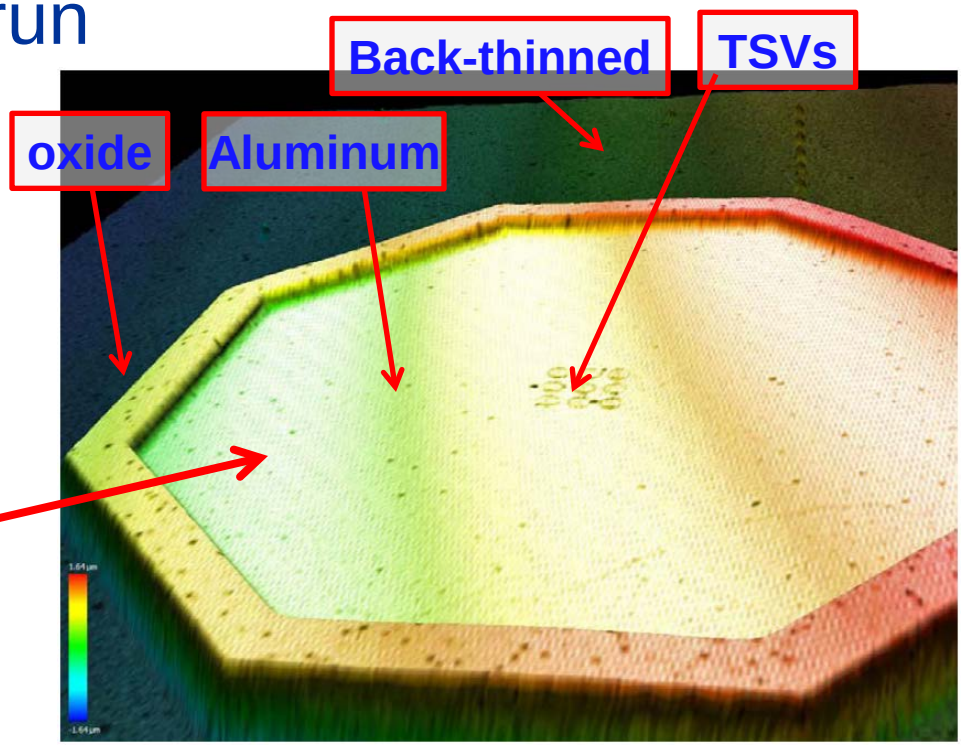
Division of the frame into 12 subreticule pairs: left-right.

Fermilab’s designs:

- **H = VICTR; short pixel realizing p_T cut for L1 trigger embedded in tracker for CMS @ HL-LHC (*particle physics*)**
- **I = VIP2b; time stamping pixel for vertex detector @ ILC (*particle physics*)**
- **J = VIPIC; very high frame rate with sparsification pixel for X-ray Photon Correlation Spectroscopy @ light source (*photon science*)**
- **TX, TY; test structures (single transistors and subcircuits)**

‘Fermilab’ 3D-IC run





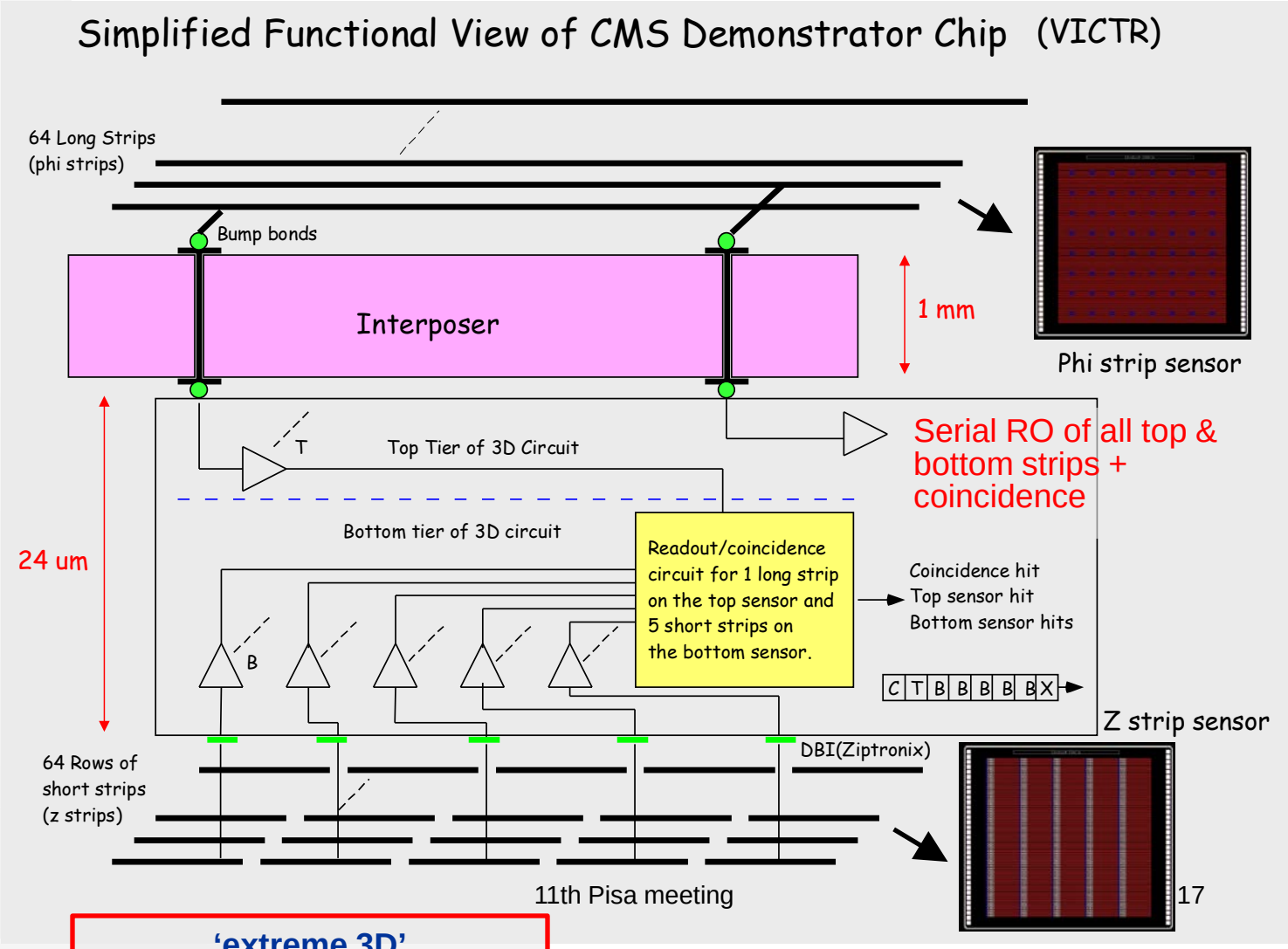
Main objectives of demonstration of 3D program - achieved
(Cu-Cu TC and Cu-Cu DBI bonding), but:

- **limited number of available 3D dies**
- **need to make a connection to sensors**

Fully finished 3D wafer (March 2013) Cu-Cu TC 130nm GF/Tezzaron wafer;

- **Important**
  - **Back-grinding down to TSVs’ tips and full back side processing up to Al pads!**

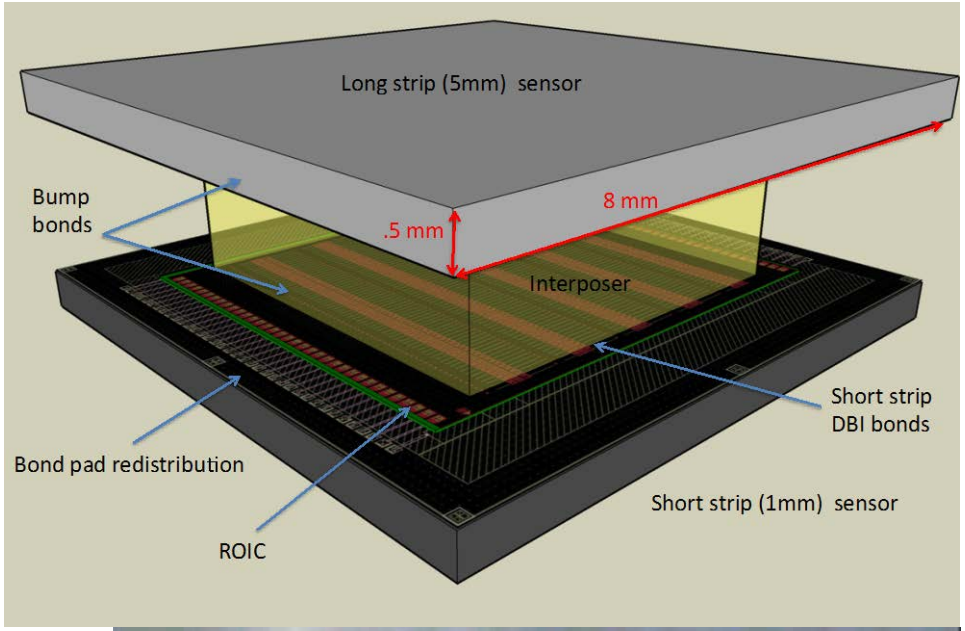
Selected results – VICTR

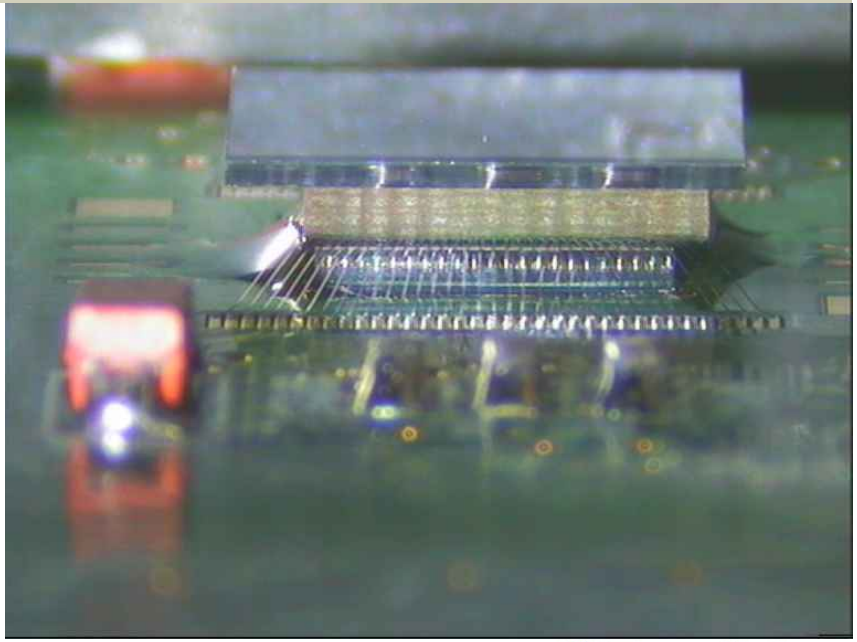


Selected results - VICTR

Interposer-based Demonstration Stack

- We have been working on bonding of the interposer and long strip sensor to the VICTR 3D chip.
  - Gold studs or solder bumps placed on individual chips
- Initial attempt with gold studs to silicon interposer did not result in good adhesion – temperature budget issues
- Gold studded VICTR was bonded to a sensor with a PCB interposer – this worked.
- Initial test showed expected noise increase, but the chip may now be damaged – loss of daisy chain connection

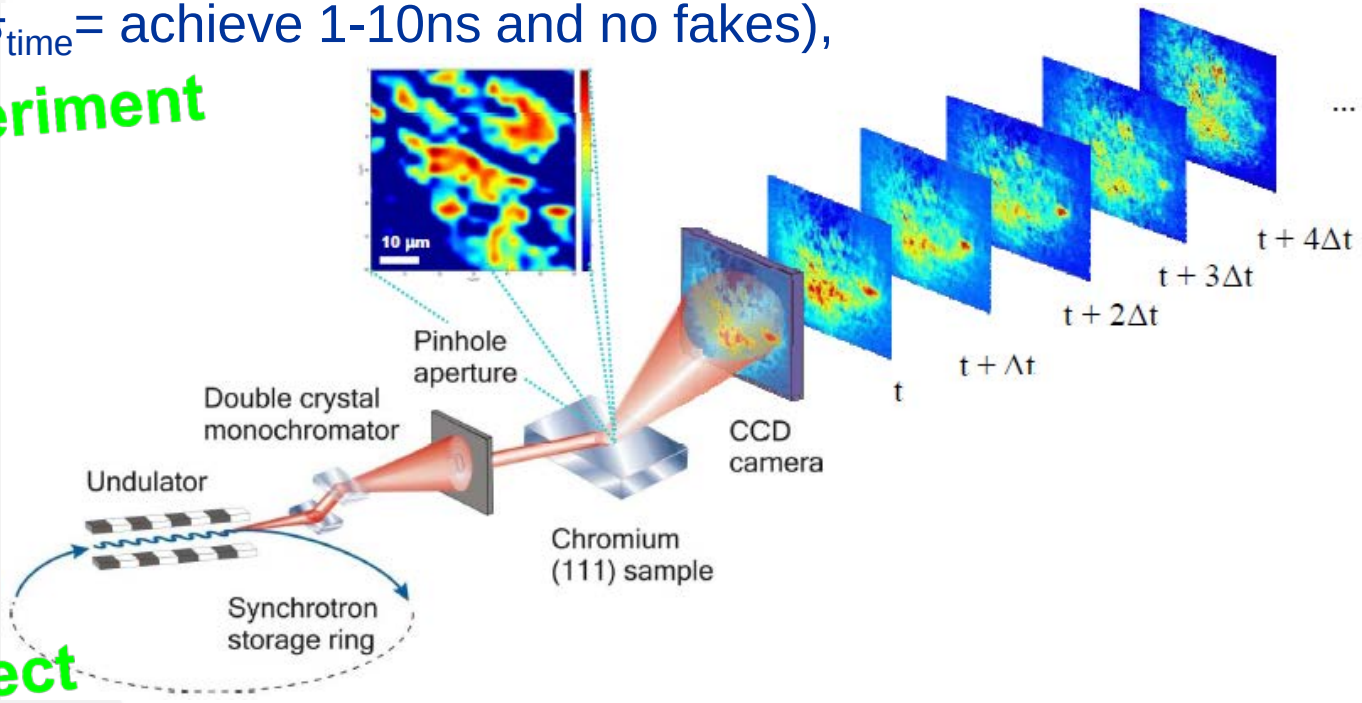




Selected results - VIPIC

Develop pixel ROIC for XPCS (*X-Ray Photon Correlation Spectroscopy*) – essentialy from functionality stand: it is timing spectroscopy (large area detector, dead-time-less readout, σ_{time}= achieve 1-10ns and no fakes),

experiment



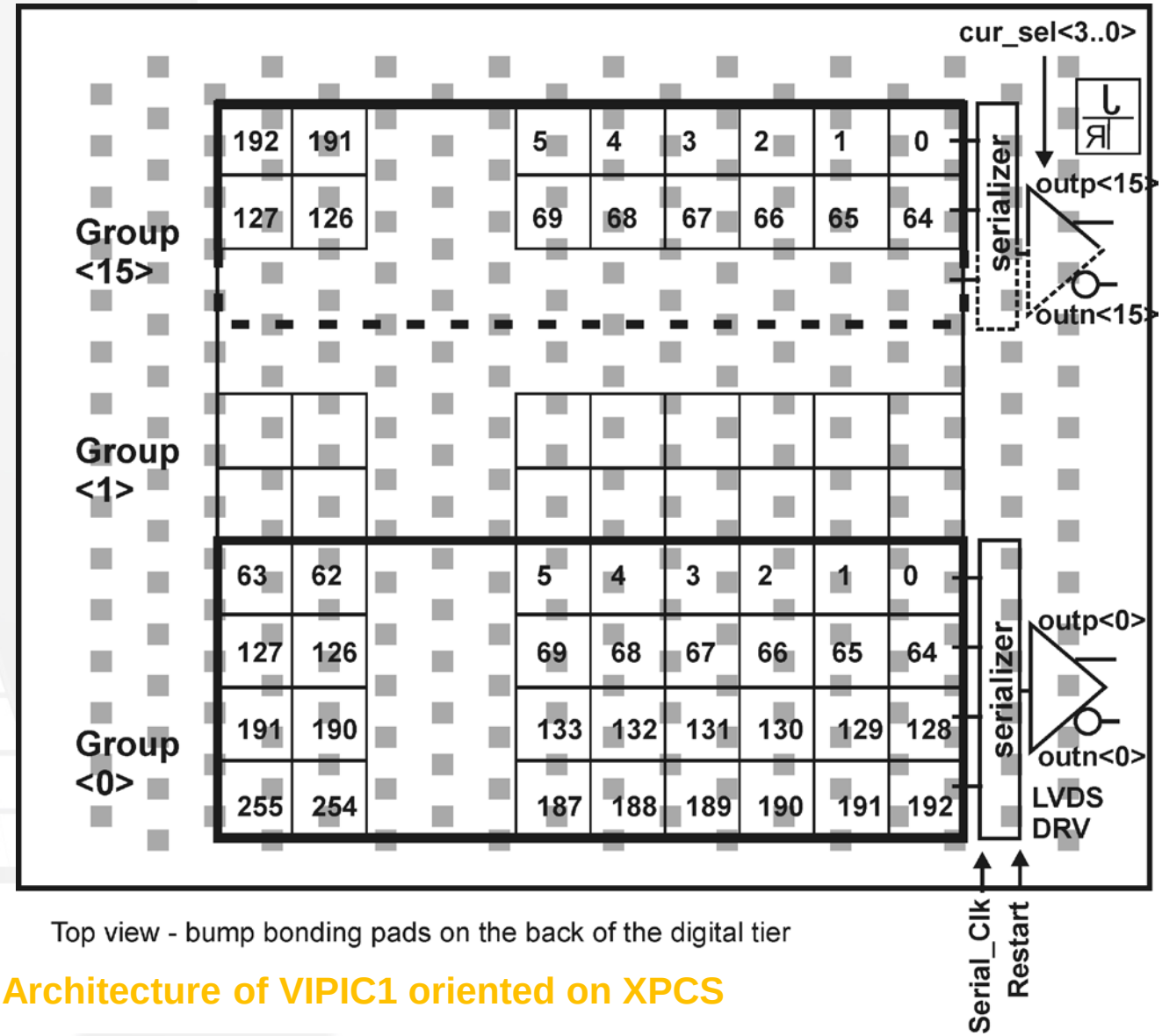
project

Vertically Integrated Photon Imaging Chip (VIPIC)

detector: Si d=500 µm, pitch 80 × 80 - 100 × 100µm^2, soft 8keV X-rays

Collaborating institutions: Fermilab, AGH-UST, BNL

Selected results - VIPIC



Top view - bump bonding pads on the back of the digital tier

How it works:

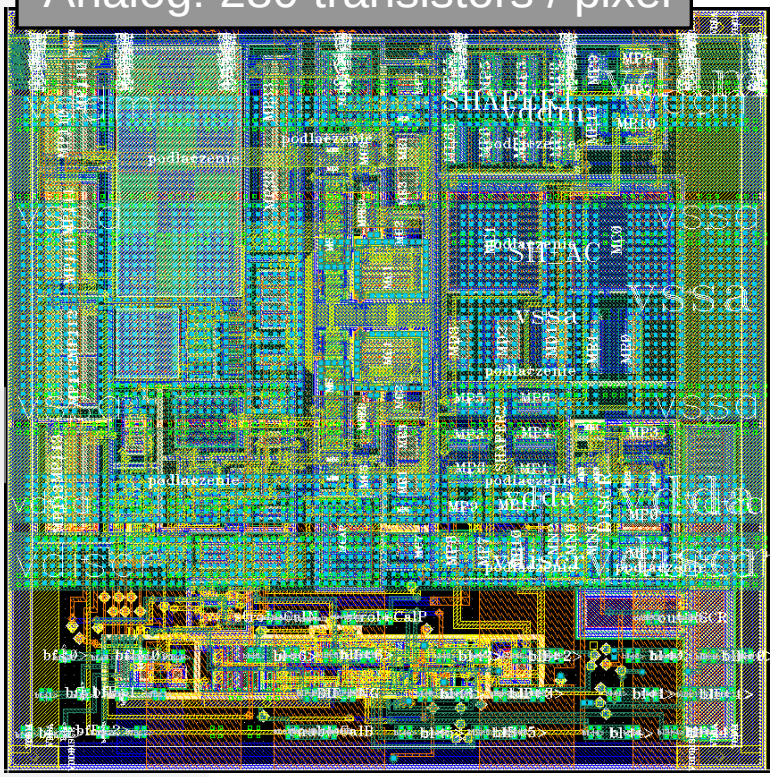
- Continuously, in dead-time-less way outputs hits on 16 parallel outputs from 64 × 64 matrix of pixels using priority encoder based sparsification method
- 5 bit long content of pixel counters followed by 8 bit long address of hit pixel
- Die size: $5.5 \times 6.3 mm^2$

Architecture of VIPIC1 oriented on XPCS

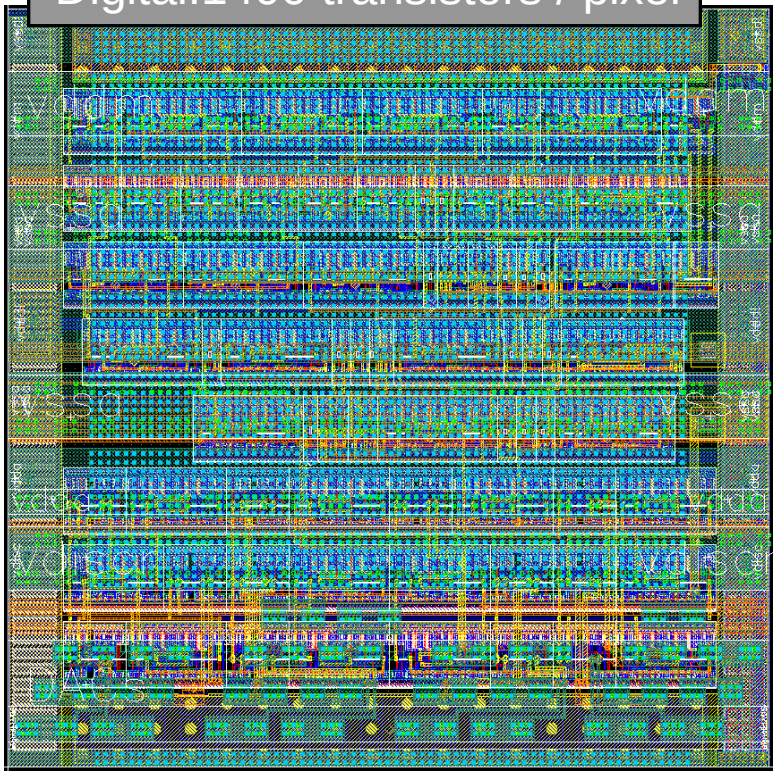
Selected results - VIPIC

Pixel 80x80 μm²

Analog: 280 transistors / pixel



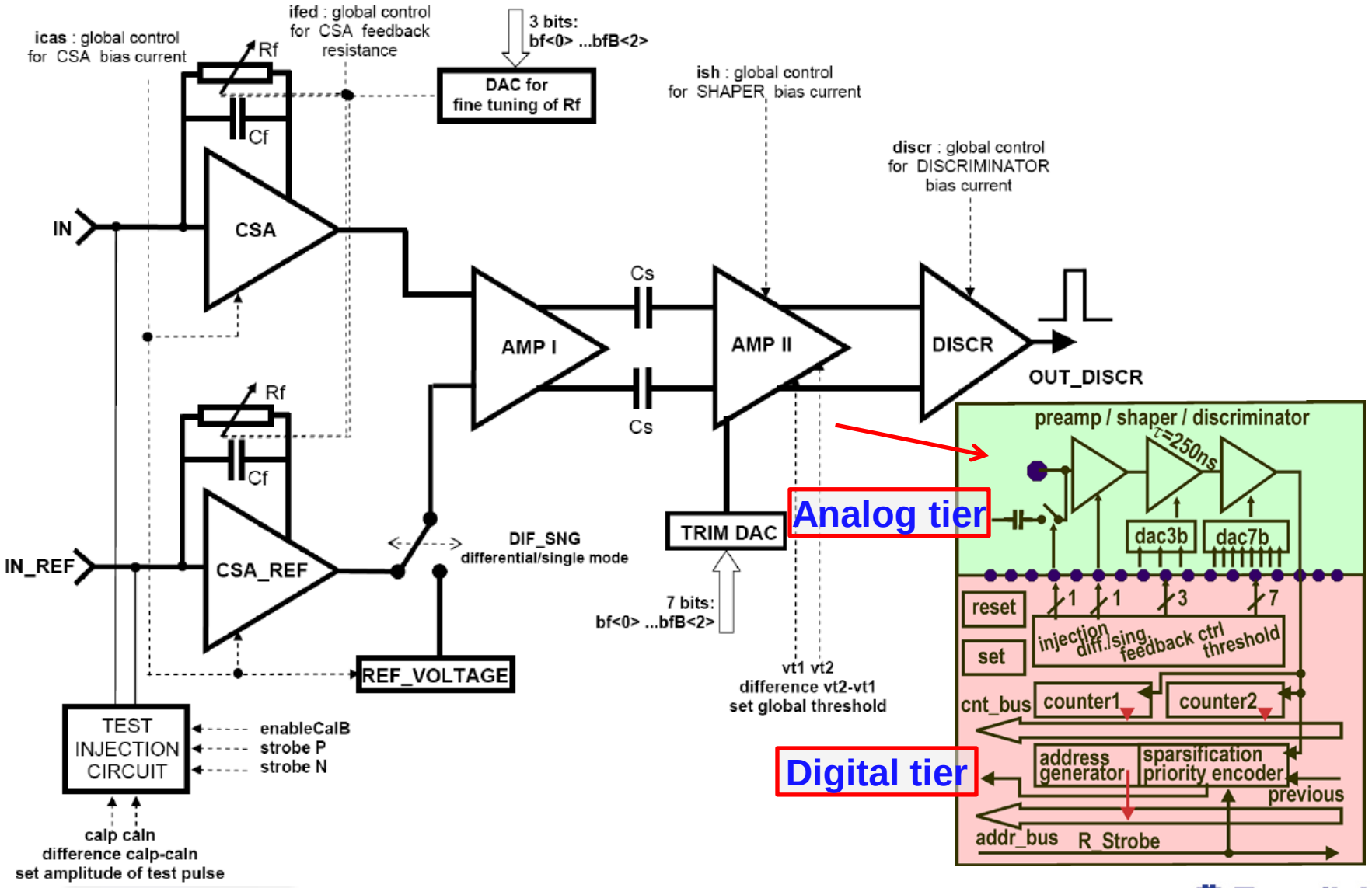
Digital:1400 transistors / pixel



- Pseudo-differential CSA-shaping filter-discriminator
- shaping time τ_p=250 ns, power ~25 μW / analog pixel, noise <150 e^- ENC, optimized for 8 keV
- 12 bit/pixel DAC adjustments
-

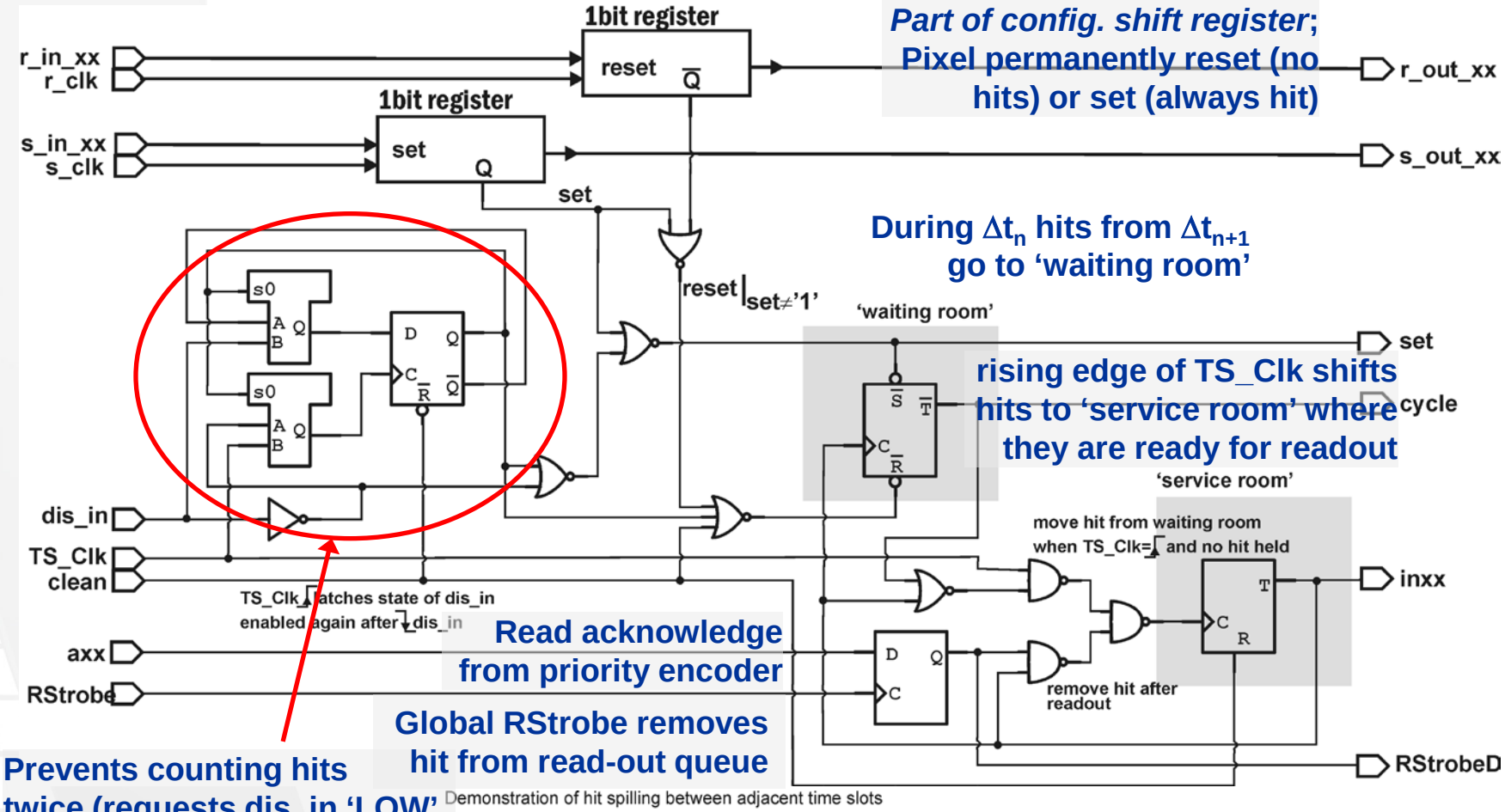
- 2 dead-time-less modes:
  - timed readout address and hit count σ_t=~ 10μs
  - imaging – counting of events
- 2 5 bit-long counters / pixel *(counting limited by duration of analog signals)*, RO with sparsification but clamping addresses: $t_{read}= (f_{clk})^{-1} \times (3+5)$ bits $\times 4 \times 64 < 20\mu s$
- 'Set' + 'Kill' bits/pixel

Selected results - VIPIC



Fermilab

Selected results - VIPIC



Part of config. shift register; Pixel permanently reset (no hits) or set (always hit)

During Δt_n hits from Δt_{n+1} go to 'waiting room'

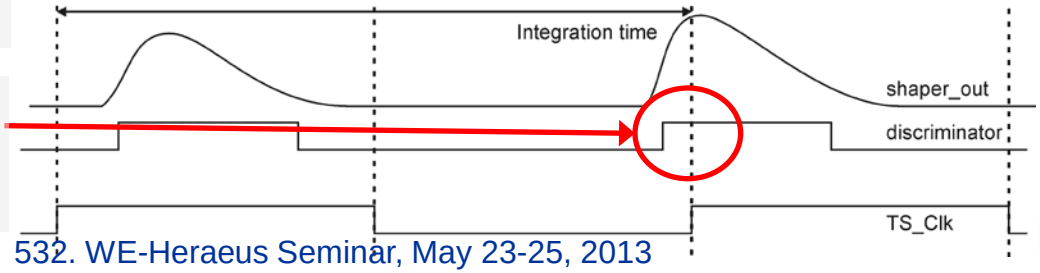
rising edge of TS_Clk shifts hits to 'service room' where they are ready for readout

Read acknowledge from priority encoder

Global RStrobe removes hit from read-out queue

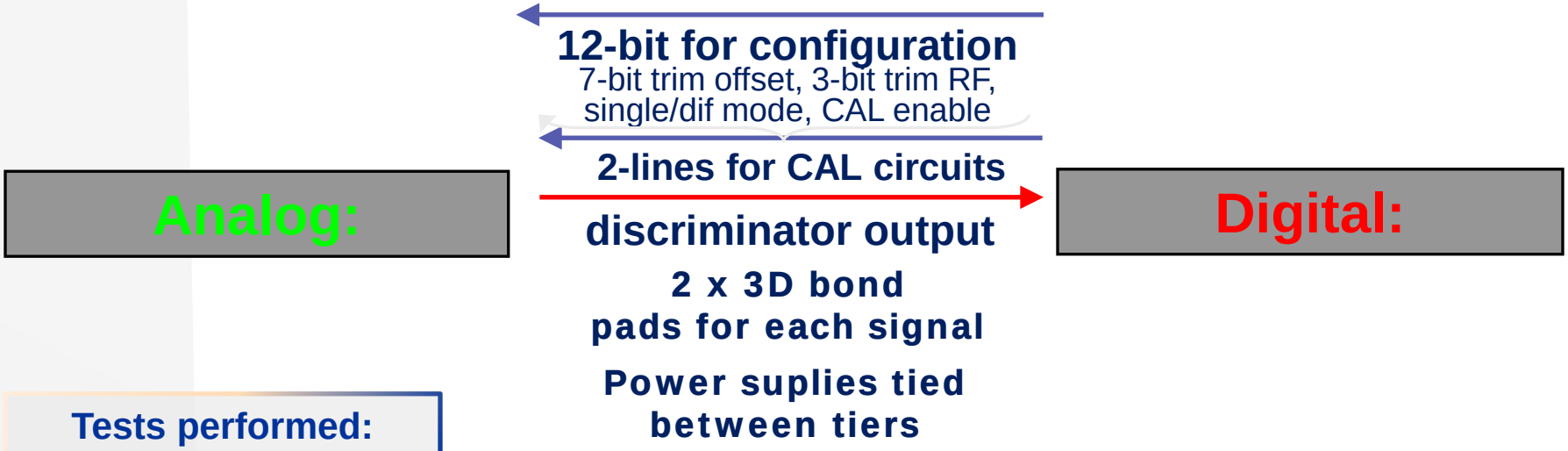
Prevents counting hits twice (requests dis_in 'LOW' after rising edge of TS_Clk)

Demonstration of hit spilling between adjacent time slots



Ambiguous: discriminator being high at the boundary of adjacent time slices

Selected results - VIPIC



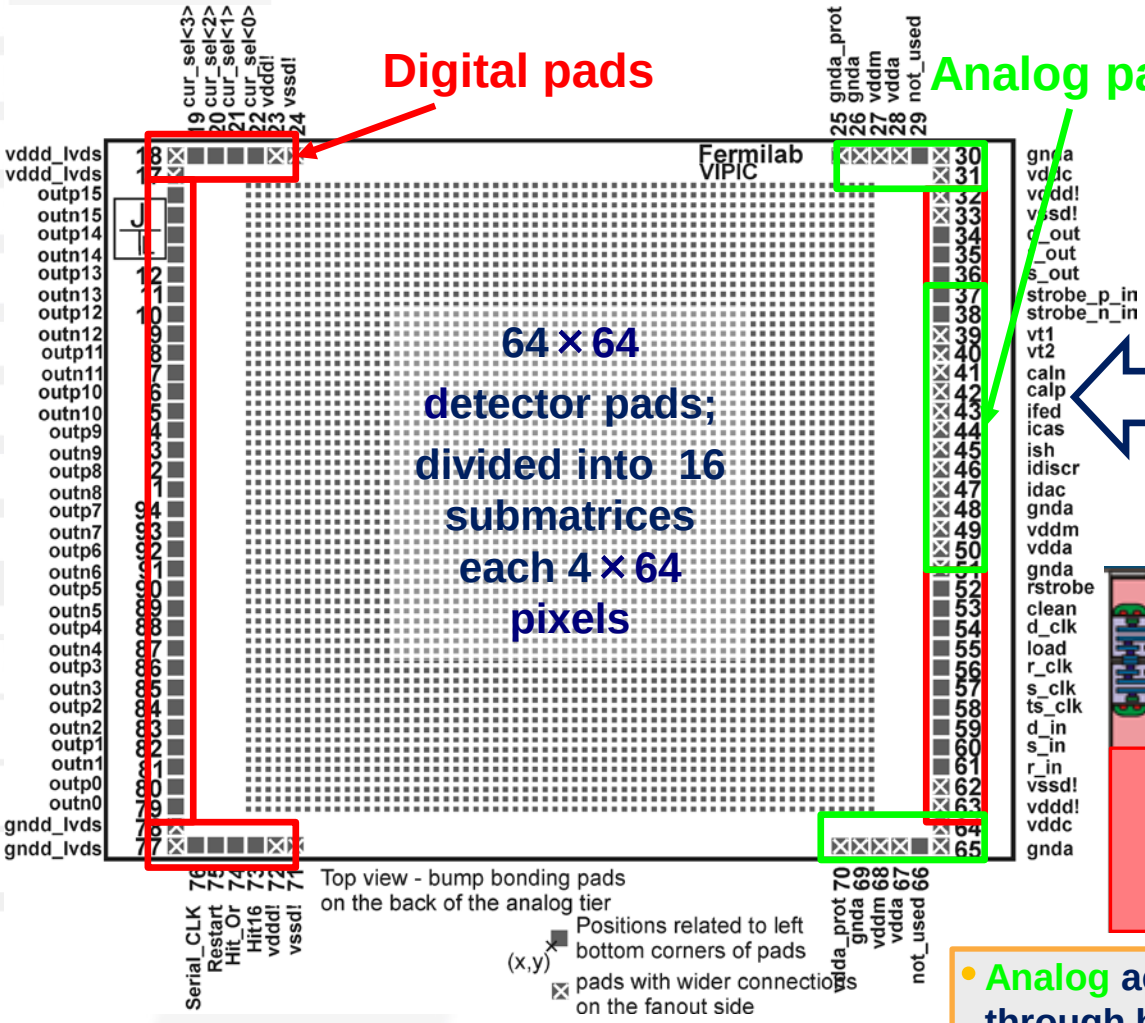
Tests performed:

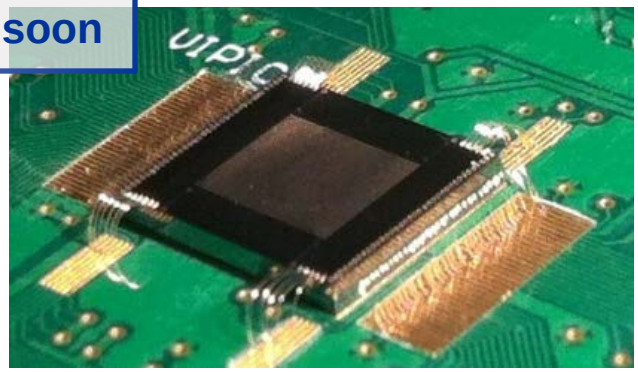
- **Measured:**
  - all bias currents for CSA, shaper, discr. and reference for trimming DACs
  - overall power consumption in static and in operation
  - Noise of FE and offsests of discriminators

- **Tested:**
  - digital shift registers defining configuration of a pixel (pixel SET, pixel RESET, reset, pixel SETTINGs
  - digital readout (pixel 1-stage pipe-line logic, sparsifier: 8 bit priority encoder, pixel readout selector, serializer, level adapters, LVDS)
  - readout chain including analog in acquisition of noise hits (with alternating counters)
  - discriminator threshold scan with noise counts (full readout)
  - readout with internal calibration

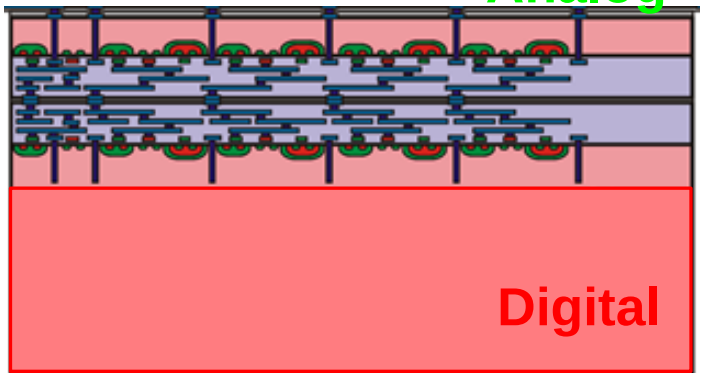
Selected results - VIPIC

VIPIC1 in 1st version of pads tested so far; 2nd to be done soon





VIPIC1 on test PCB



- **Analog accessed directly, Digital must pass through bonding interface between tiers**

Selected results - VIPIC

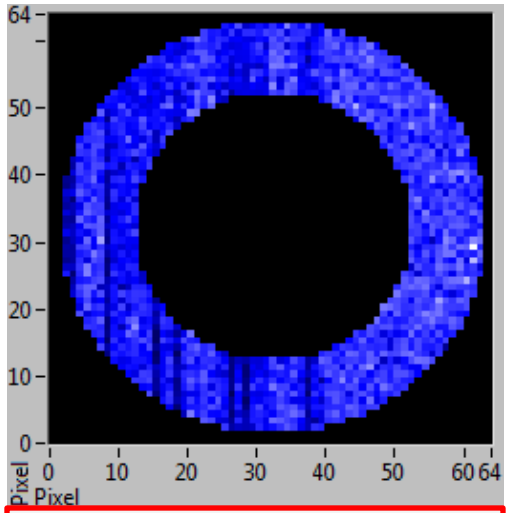
pixel SET - pixels hit permanently and feeding into the readout (RESET, to make pixel never fed into sparsifier, works too)

pixel #01 with hit

Address 00001

Priority encoder, sparsified hit readout

equivalent of giant OR; 32 pixels shown

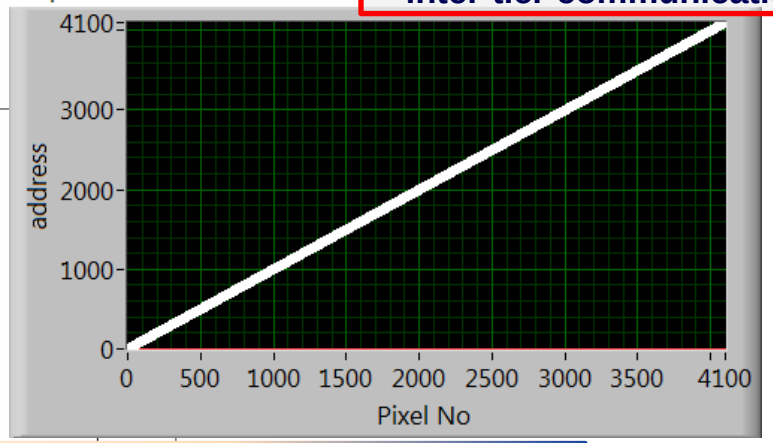


sparsified readout inter-tier communication

Logic (with tri-state capability) for generation of binary addresses

Both work:

Responsive Pixels Addresses



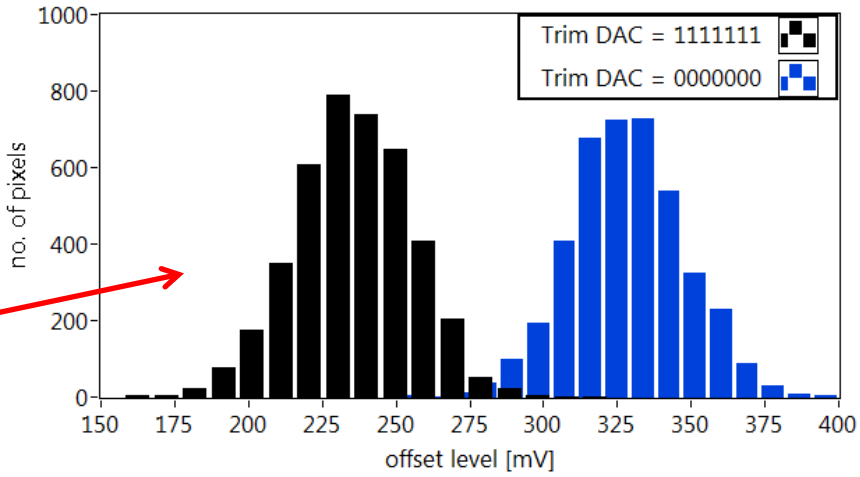
based on: P. Fischer, NIM A461, 2001, 499-504

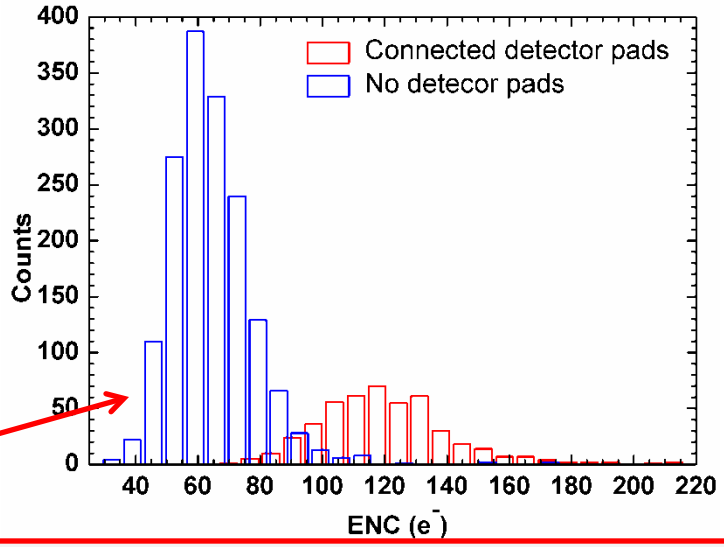
lowering discr. threshold - all pixels feed to sparsifier their noise hits! 256 addresses

Selected results - VIPIC

Threshold scans:

- **All pixels respond ! All readouts through whole sparsifier!**
- **Scans performed at two extreme DAC's setting `0000000` → `1111111`**
- **Two unambiguously self-resolving groups resulted from noise hits!**
- **Communication between tiers does not show any misses:**
  1) all DAC settings
  2) discriminator outputs sent to sparsifier
  3) calibration injection
- **Gain ~ 40μV/e$^-$ (C_{inj}=1.7fF)**
  ENCrms ~75e$^-$ (close to expected)





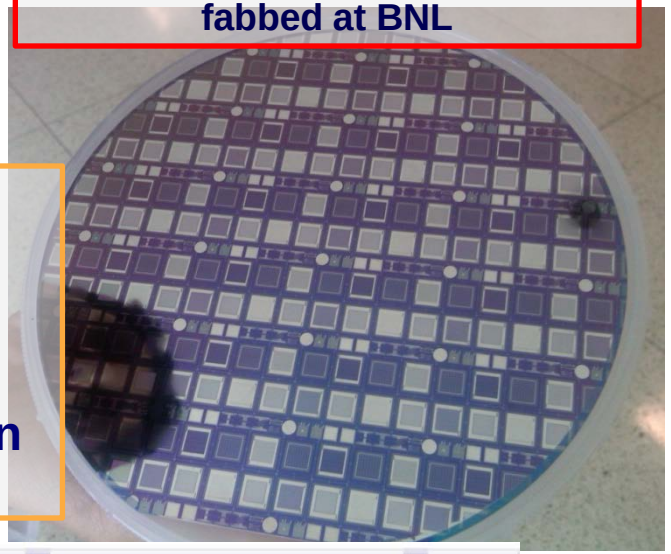
noise @ nominal bias in input transistor and with CSA replica off for gain from measurements

Fermilab

Directions of efforts

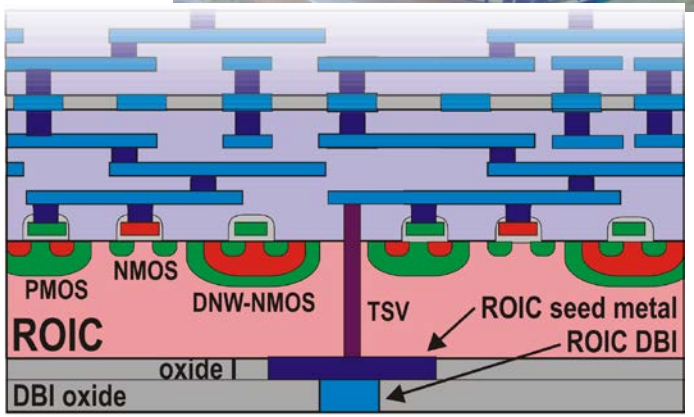
- **Explore possibilities of building V-stacked ROICs**
- **Explore high-density and minimum dead area bonding of ROICs to sensors**
- **Explore multi-tier assemblies with communication for in situ processing**

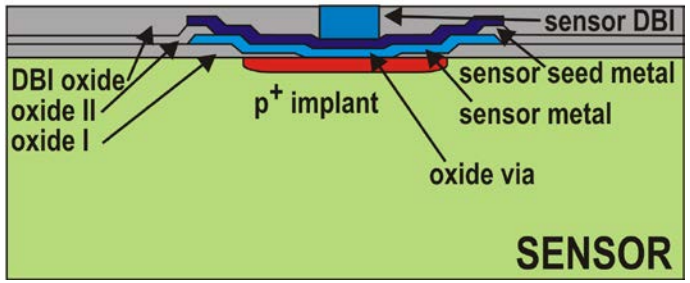
Sensor wafer for all 3D pixel chips fabbed at BNL



Direct Bonding Interconnect (DBI®) by Ziptronix oxide-oxide W-W bonding

Small Ni or Cu seeds embedded in ultra-planarized oxide establish contacts when oxide surfaces chemically fuse

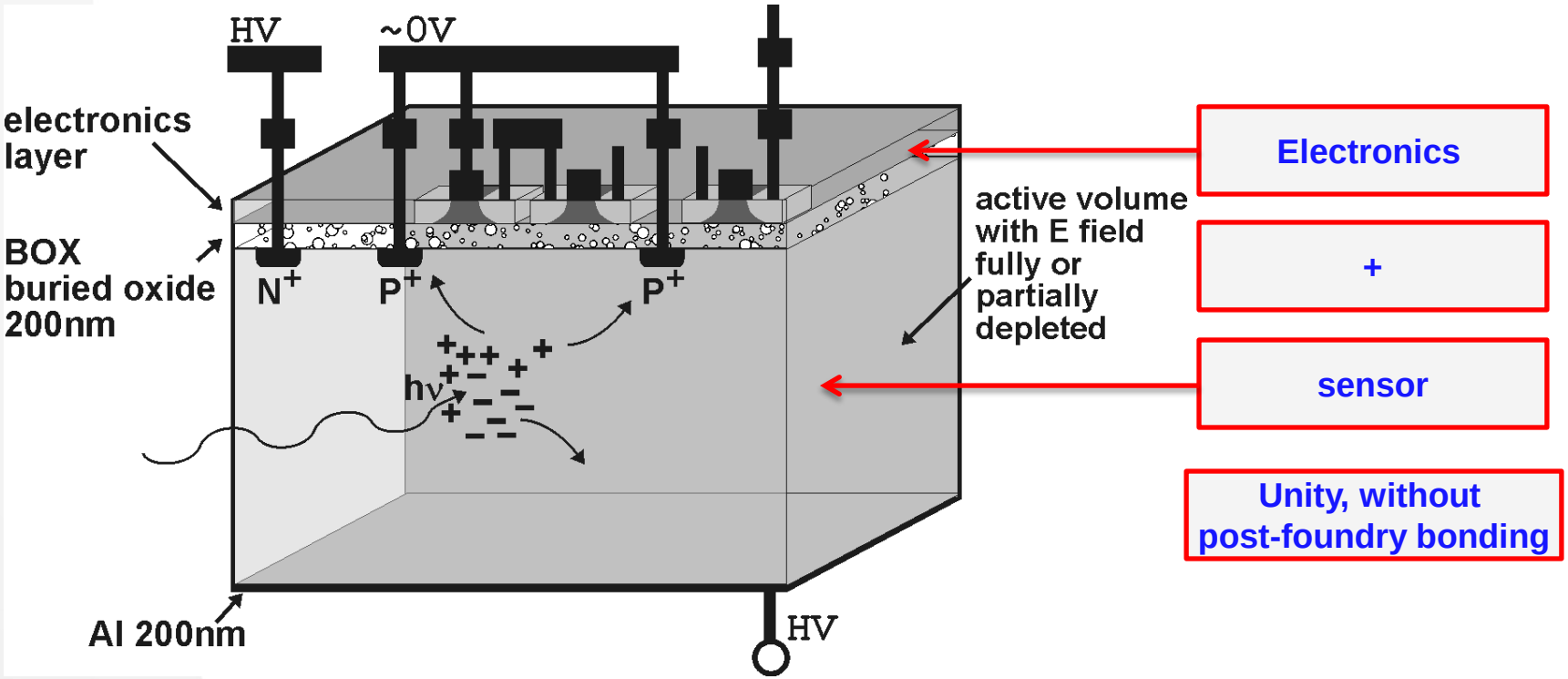




- **3D technologies can also be used to integrate sensors to ROICs**
- **Pitches as small as 3μm, devices thinned to 25μm**
- **Fully active sensors as large as 6" (or 8" wafer) based on tiled ROICs**

Silicon On Insulator (SOI) pixels

- Collaboration established with KEK and under a Japan-US agreement (MoU 2007) on monolithic SOI devices + OKI/LAPIS (industrial partner).
- SOI pixels are a kind of naturally 3D integrated, ready for further stacking



process was a slightly modified version of a commercial FD SOI process at the beginning

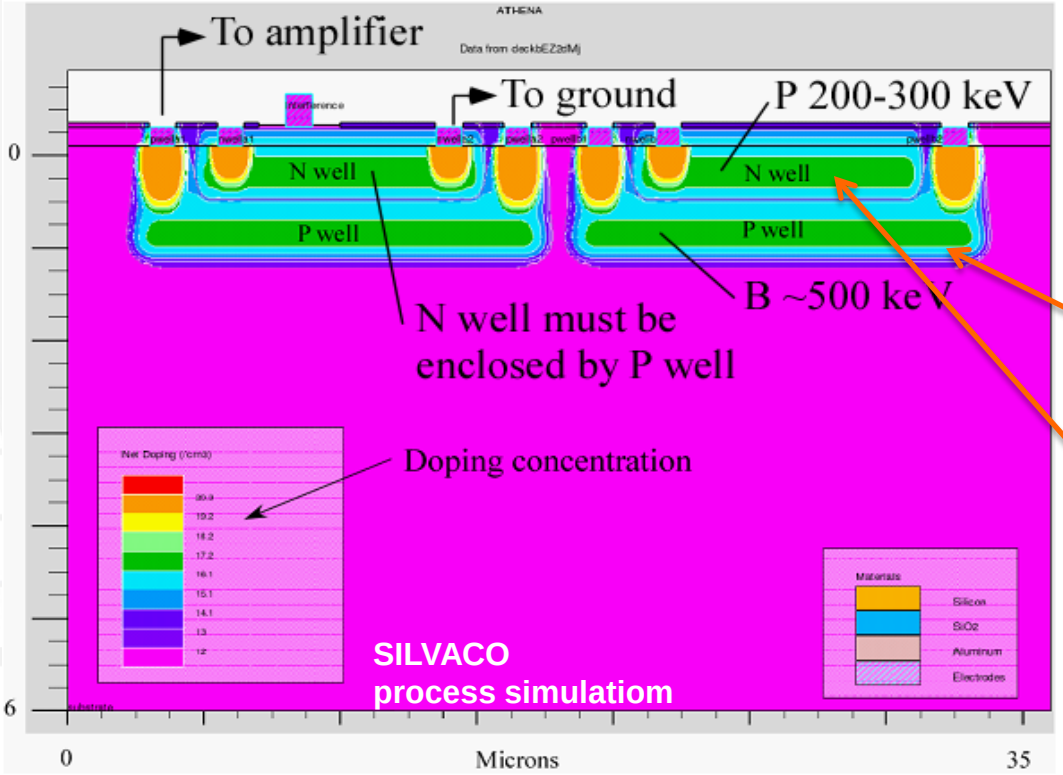
Suffering from strong back-gating and generally coupling between sensor and electronics

SOI pixels: shielding

– **Triple role of shielding between the SOI electronics and detector layer:**

- **to avoid back-gating in transistors** (DC potential underneath the BOX shifts threshold of transistors),
- **to avoid injection of parasitic charges** (from the SOI electronics to detector),
- **to avoid strong electric field in BOX** (that results in accelerated radiation damage).

improvement proposed by Fermilab (nested wells)



- Simulation with Silvaco
- Feature introduced in the design kit together with scientist from KEK and engineers from OKI/LAPIS

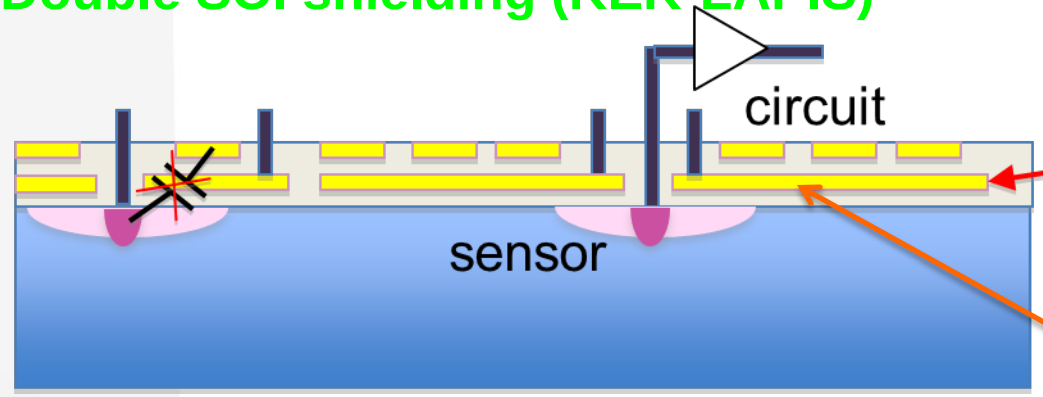
This well collects the charge carriers

This well separates digital circuits from sensor substrate and prevents back gating effects

Another improvement proposed by KEK (double SOI)

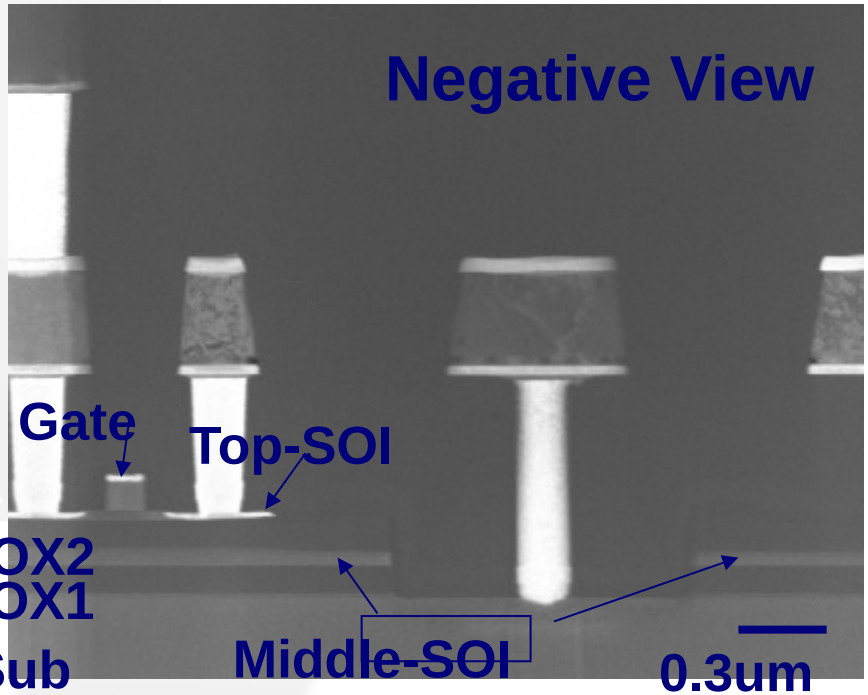
SOI pixels: shielding

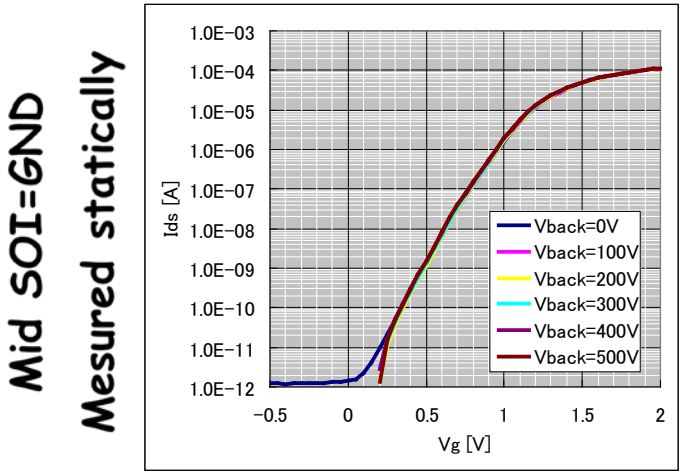
Double SOI shielding (KEK-LAPIS)



additional conduction layer

- It is very thin, but it must be low resistivity to be effective



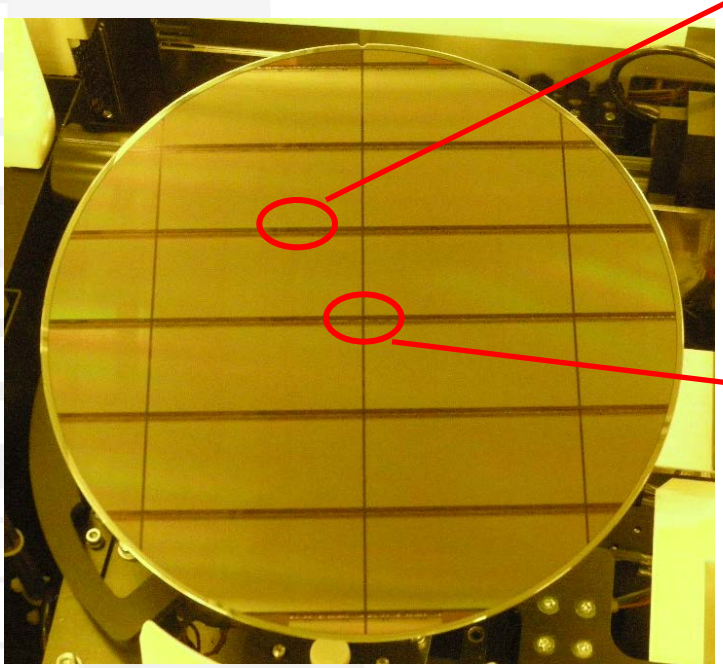


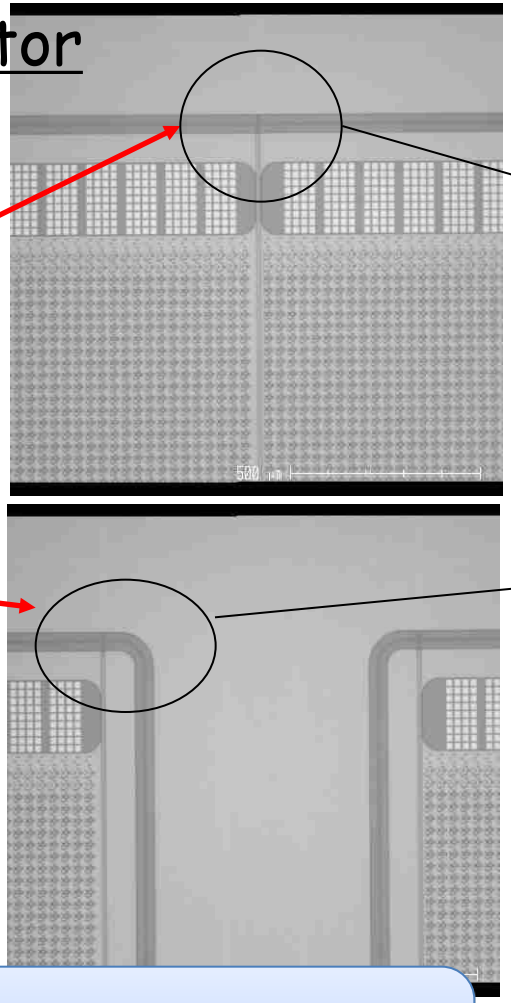
Courtesy of Yasuo Arai (KEK)

SOI pixels: stitching

Riken SOPHIAS detector

Stitching Exposure



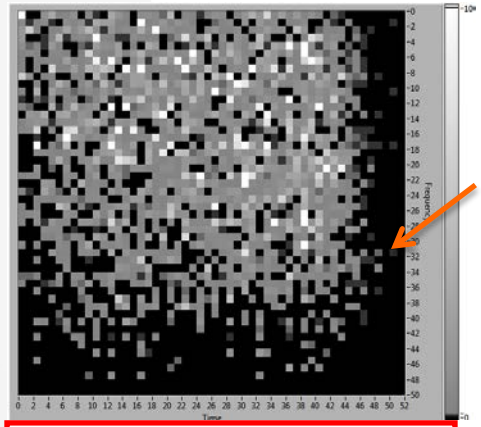


- **Width of the Buffer Region can be less than 10um.**
- **Accuracy of Overwrap is better than 0.025um.**

Courtesy of Yasuo Arai (KEK)

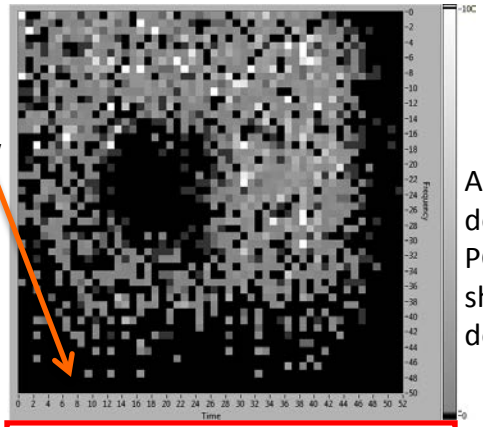
SOI pixels results with MAMBO

Images obtained with MAMBO V using W object and ^{109}Cd source



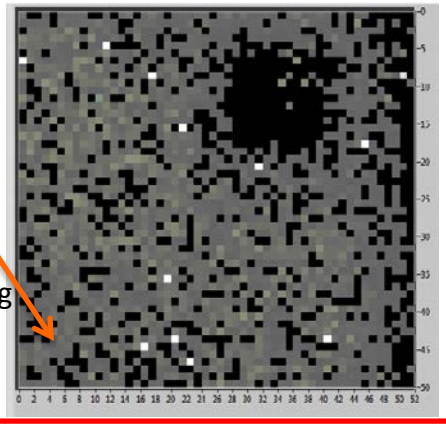
Flat field - no mask

Shadow of PCB



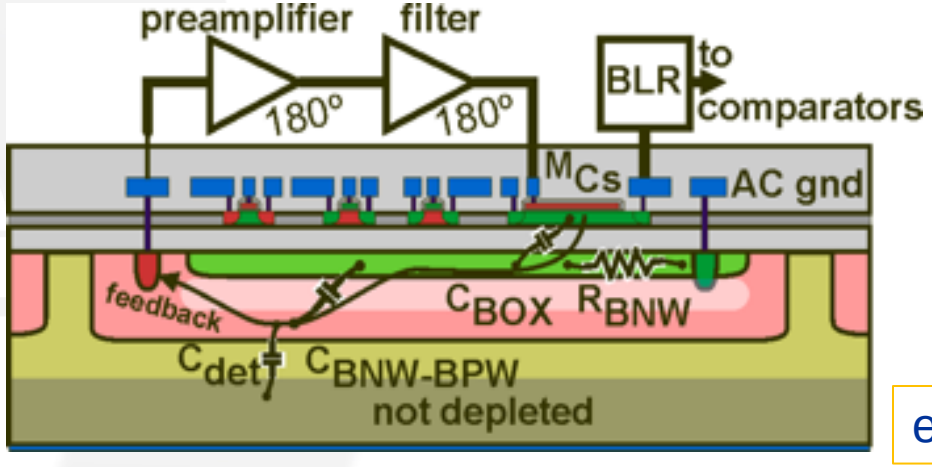
W mask - no det. bias

Another device; PCB not shadowing detector



W mask - det. reverse bias

Probably first images of counting X-rays pixels in the SOIPIX community with depleted detector



- Why low resistivity is important?
- experienced instabilities although statically no shifts

- Shallow and lower concentration of BNW produces higher resistance across the N well contacts
- The resistance is independent of the Die pad voltage

efforts by Farah Fahim and Scott Holm

Perspectives

- **3D work accomplished so far - dip a toe in the water**
- **Opened strategies for new forms of detectors *(but many flavors of how to achieve almost the same thing)***
- **Results obtained on a limited number of chips are positive;**
  - observed problems are not 3D bonding related, are mostly circuit design related
  - 3D is THE solution for certain types of detectors, e.g. processing in-situ
- **Analysis of potential further direction for 3D-ICs**
  - **business model of GF not interested by low volume and working with research institutes (good side of GF is competitive price)**
  - **MOSIS: either improve reliability of GF (to keep schedules, provide customer service, and access to run information) – keep via-first and GF130 as a base option for next runs, or fabricate wafers at another foundry and do via last of via middle**
- **3D components very useful for building assemblies even with conventional ICs**
- **SOI pixels are appealing as part of 3D assemblies or standalone**
  - **technology needs to be viable**
- **All that to make the dream happen!**