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## GPU Accelerators for the usage in the cosmic ray simulation CORSIKA

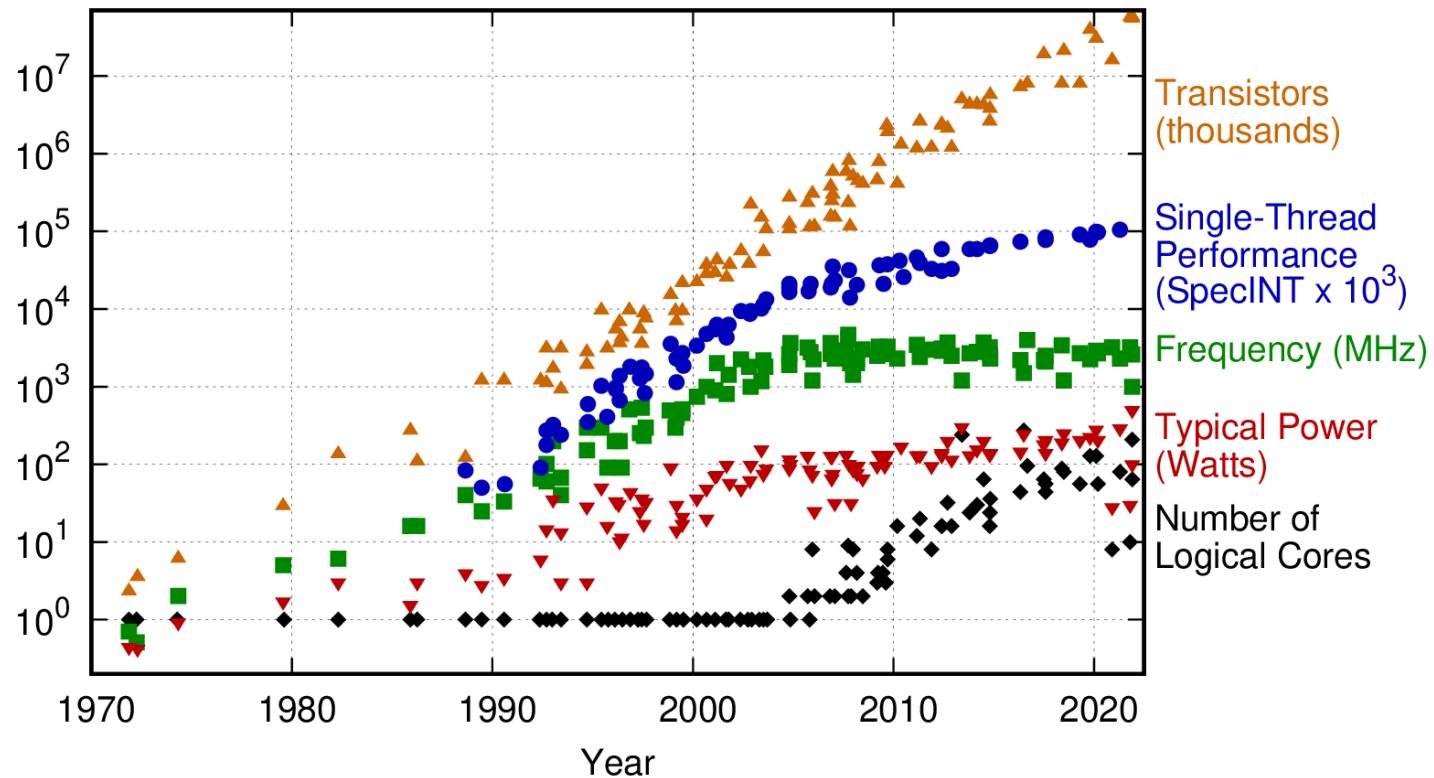
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Dominik Baack  
Corsika Workshop  
Heidelberg - 2022  
13. 07. 2022

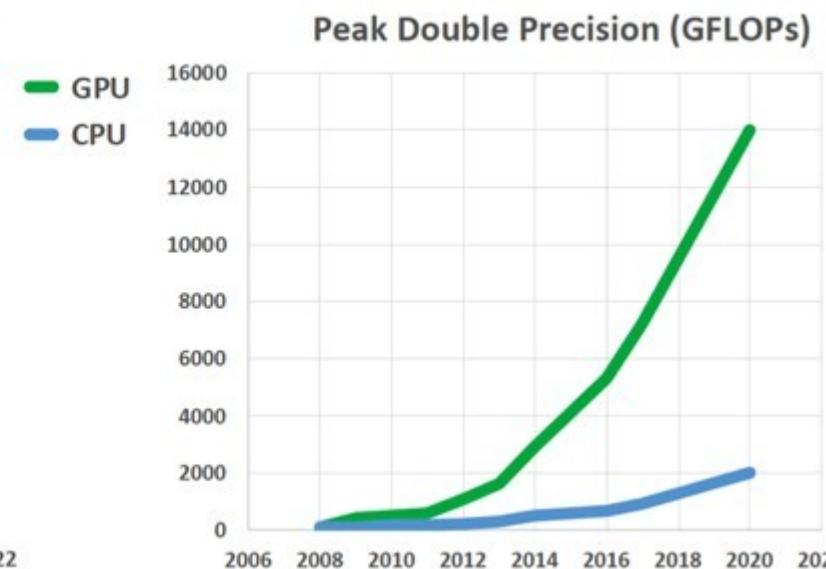
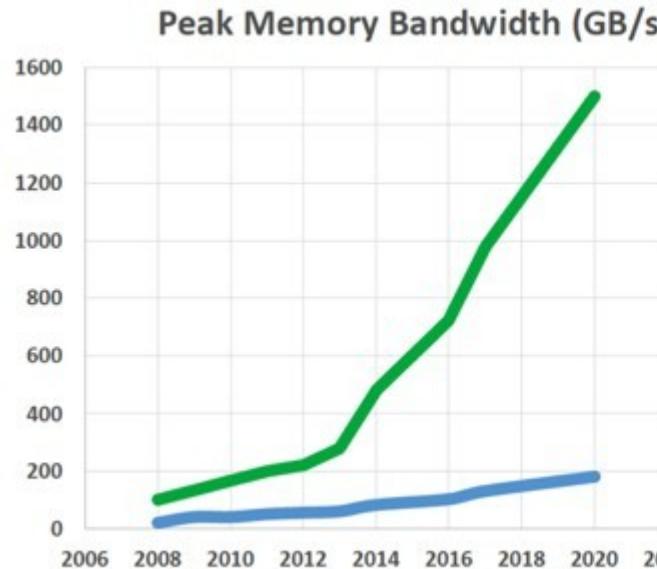
# CPU Development

## 50 Years of Microprocessor Trend Data



Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten  
New plot and data collected for 2010-2021 by K. Rupp

# GPU Development



<https://www.nextplatform.com/2019/07/10/a-decade-of-accelerated-computing-augurs-well-for-gpus/>

# Acceleration Hardware

Formfaktor	H100 SXM	H100 PCIe
<b>FP64</b>	30 teraFLOPS	24 teraFLOPS
<b>FP64-Tensor-Core</b>	60 teraFLOPS	48 teraFLOPS
<b>FP32</b>	60 teraFLOPS	48 teraFLOPS
<b>TF32-Tensor-Core</b>	1.000 teraFLOPS*	800 teraFLOPS*
<b>BFLOAT16-Tensor-Core</b>	2.000 teraFLOPS*	1.600 teraFLOPS*
<b>FP16-Tensor-Core</b>	2.000 teraFLOPS*	1.600 teraFLOPS*
<b>FP8-Tensor-Core</b>	4.000 teraFLOPS*	3.200 teraFLOPS*
<b>INT8-Tensor-Core</b>	4.000 TOPS*	3.200 TOPS*
<b>GPU-Speicher</b>	80 GB	80 GB
<b>GPU-Speicherbandbreite</b>	3 TB/s	2 TB/s
<b>Decoder</b>	7 NVDEC 7 JPEG	7 NVDEC 7 JPEG
<b>Max. Thermal Design Power (TDP)</b>	700 W	350 W
<b>Mehr-Instanzen-Grafikprozessoren</b>	Bis zu 7 MIGs mit je 10 GB	
<b>Formfaktor</b>	SXM	PCIe Zwei Steckplätze mit Luftkühlung
<b>Konnektivität</b>	NVLink: 900 GB/s PCIe Gen5; 128 GB/s	NVLINK: 600 GB/s PCIe Gen5; 128 GB/s
<b>Serveroptionen</b>	NVIDIA HGX® H100-Partner und NVIDIA-Certified Systems™ mit 4 oder 8 GPUs, NVIDIA DGX® H100 mit 8 GPUs	

\* Mit geringer Dichte dargestellt. Die Spezifikationen sind ohne geringe Dichte um die Hälfte niedriger. Vorläufige Spezifikationen. Änderungen vorbehalten.

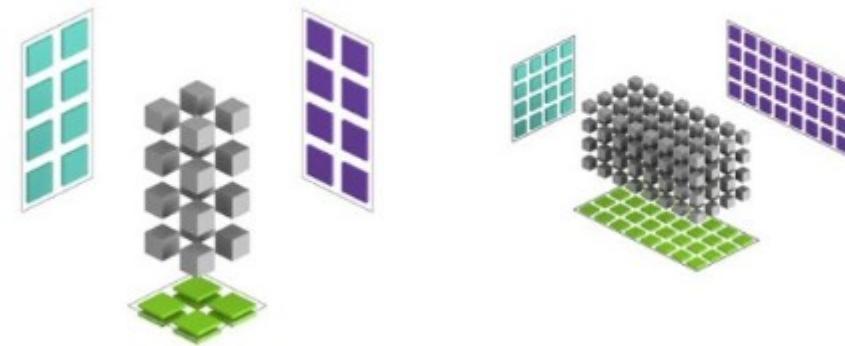
GPU Features	NVIDIA Tesla P100	NVIDIA Tesla V100	NVIDIA A100
GPU Codename	GP100	GV100	GA100
GPU Architecture	NVIDIA Pascal	NVIDIA Volta	NVIDIA Ampere
GPU Board Form Factor	SXM	SXM2	SXM4
SMs	56	80	108
TPCs	28	40	54
FP32 Cores/SM	64	64	64
FP32 Cores/GPU	3584	5120	6912
FP64 Cores/SM (excl. Tensor)	32	32	32
FP64 Cores/GPU (excl. Tensor)	1792	2560	3456
INT32 Cores / SM	NA	64	64
INT32 Cores / GPU	NA	5120	6912
Tensor Cores / SM	NA	8	4 <sup>2</sup>
Tensor Cores / GPU	NA	640	432
GPU Boost Clock	1480 MHz	1530 MHz	1410 MHz
Peak FP16 Tensor TFLOPS with FP16 Accumulate <sup>1</sup>	NA	125	312/ <del>624</del> <sup>43</sup>
Peak FP16 Tensor TFLOPS with FP32 Accumulate <sup>1</sup>	NA	125	312/ <del>624</del> <sup>44</sup>
Peak BF16 Tensor TFLOPS with FP32 Accumulate <sup>1</sup>	NA	NA	312/ <del>624</del> <sup>43</sup>
Peak TF32 Tensor TFLOPS <sup>1</sup>	NA	NA	156/ <del>312</del> <sup>22</sup>
Peak FP64 Tensor TFLOPS <sup>1</sup>	NA	NA	19.5
Peak INT8 Tensor TOPS <sup>1</sup>	NA	NA	624/1248 <sup>3</sup>
Peak INT4 Tensor TOPS <sup>1</sup>	NA	NA	1248/2496 <sup>3</sup>
Peak FP16 TFLOPS <sup>1</sup> (non-Tensor)	21.2	31.4	78
Peak BF16 TFLOPS <sup>1</sup> (non-Tensor)	NA	NA	39
Peak FP32 TFLOPS <sup>1</sup> (non-Tensor)	10.6	15.7	19.5
Peak FP64 TFLOPS <sup>1</sup> (non-Tensor)	5.3	7.8	9.7
Peak INT32 TOPS <sup>1,4</sup>	NA	15.7	19.5
Texture Units	224	320	432
Memory Interface	4096-bit HBM2	4096-bit HBM2	5120-bit HBM2
Memory Size	16 GB	32 GB / 16 GB	40 GB
Memory Data Rate	703 MHz DDR	877.5 MHz DDR	1215 MHz DDR

# Acceleration Hardware

- Tensor Cores A100

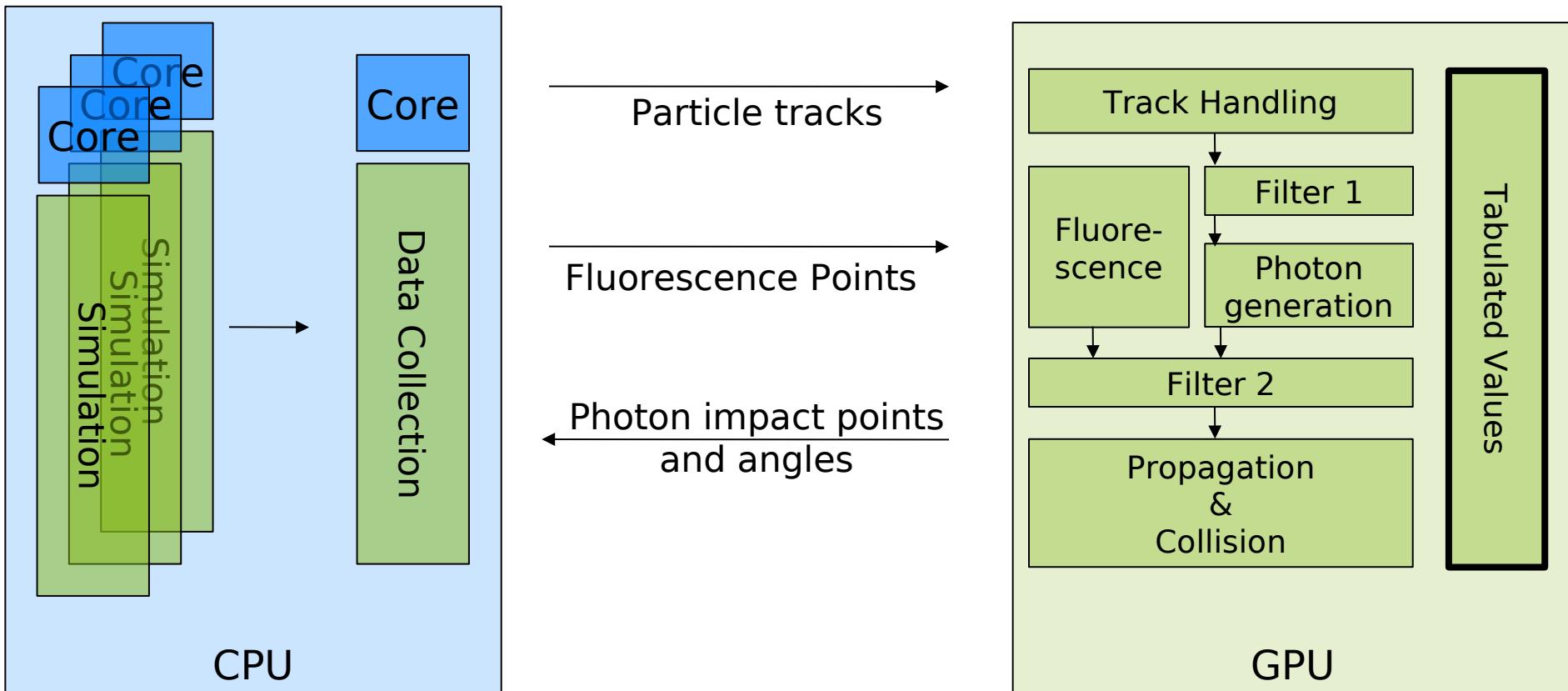
FP64

FP32



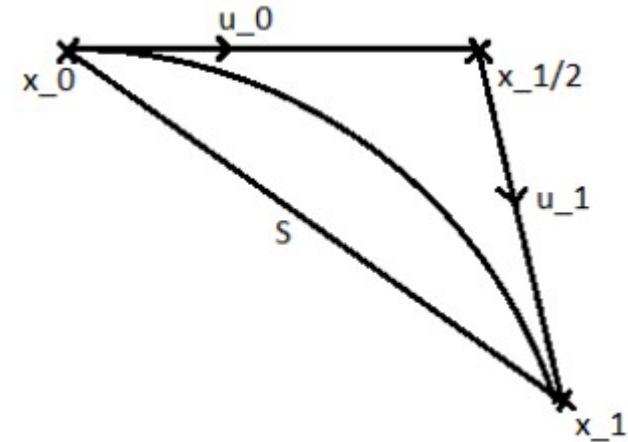
$$D = \left( \begin{array}{cccc} A_{0,0} & A_{0,1} & A_{0,2} & A_{0,3} \\ A_{1,0} & A_{1,1} & A_{1,2} & A_{1,3} \\ A_{2,0} & A_{2,1} & A_{2,2} & A_{2,3} \\ A_{3,0} & A_{3,1} & A_{3,2} & A_{3,3} \end{array} \right) \left( \begin{array}{cccc} B_{0,0} & B_{0,1} & B_{0,2} & B_{0,3} \\ B_{1,0} & B_{1,1} & B_{1,2} & B_{1,3} \\ B_{2,0} & B_{2,1} & B_{2,2} & B_{2,3} \\ B_{3,0} & B_{3,1} & B_{3,2} & B_{3,3} \end{array} \right) + \left( \begin{array}{cccc} C_{0,0} & C_{0,1} & C_{0,2} & C_{0,3} \\ C_{1,0} & C_{1,1} & C_{1,2} & C_{1,3} \\ C_{2,0} & C_{2,1} & C_{2,2} & C_{2,3} \\ C_{3,0} & C_{3,1} & C_{3,2} & C_{3,3} \end{array} \right)$$

# Computing Structure



## Prerequisite

- Linear particle tracks
- >>1024 track segments accumulated to reach good performance



Andre Schmidt - KIT

## Track Handling

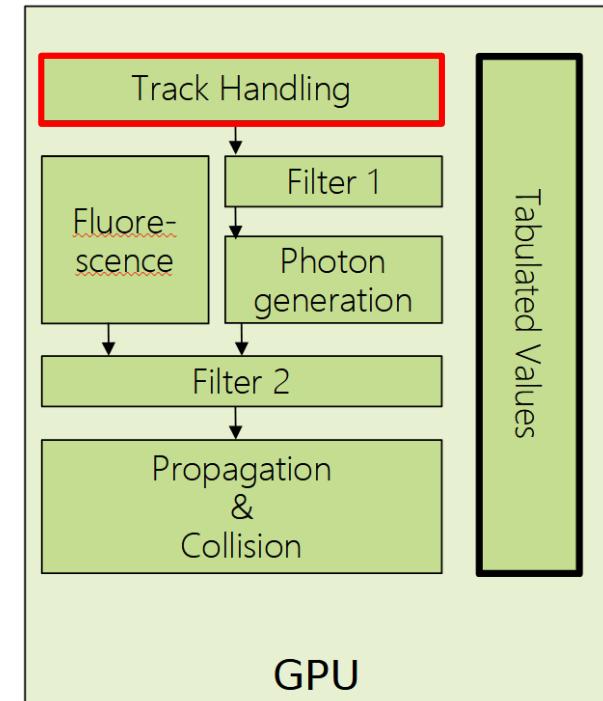
- Photon count:

float64 vs float32

$$\frac{1}{\beta n} \sim \# \text{ Photon}$$

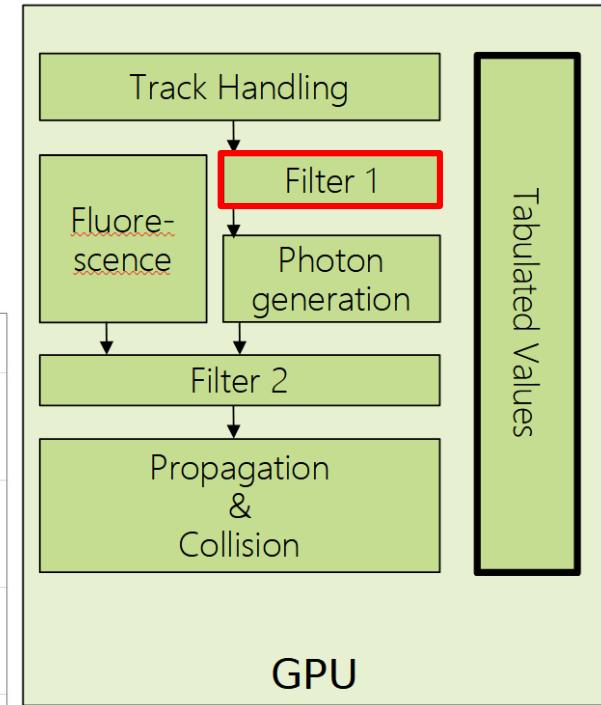
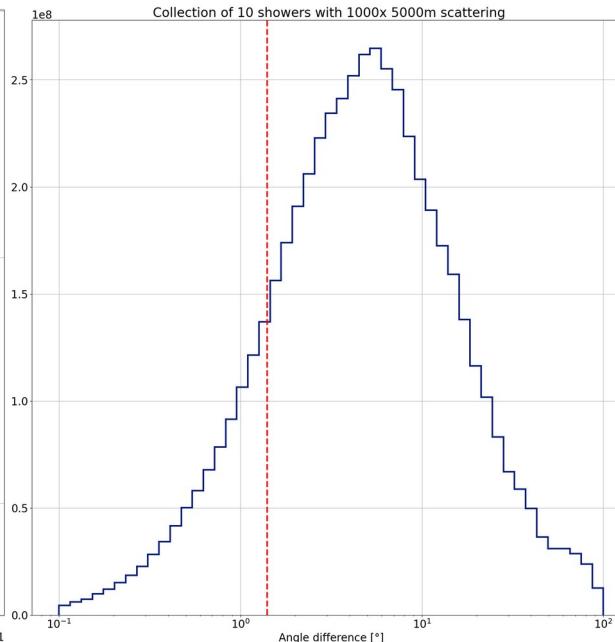
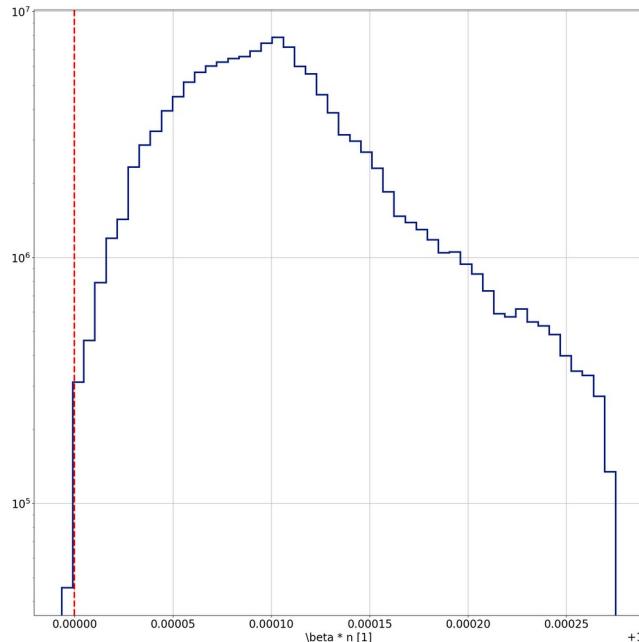
- $\beta, n$  very close to 1  
 $\rightarrow 0.03\%$  difference in photon generation

- Mostly multiplications and memory operations



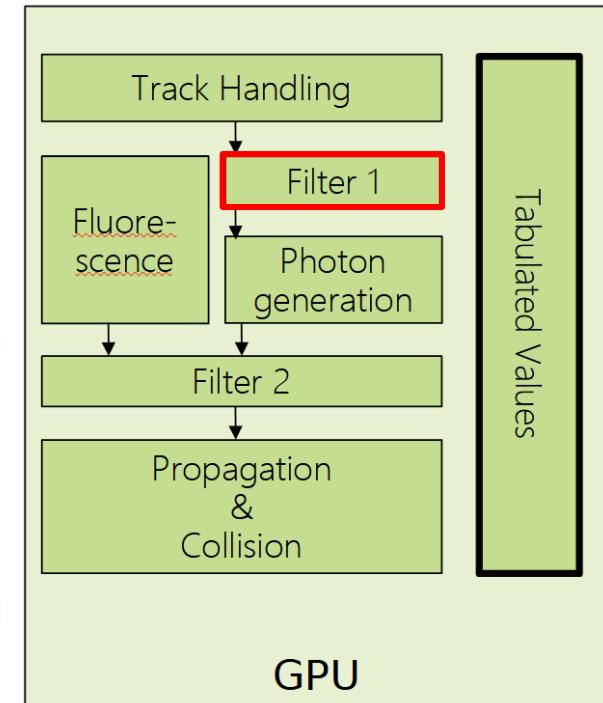
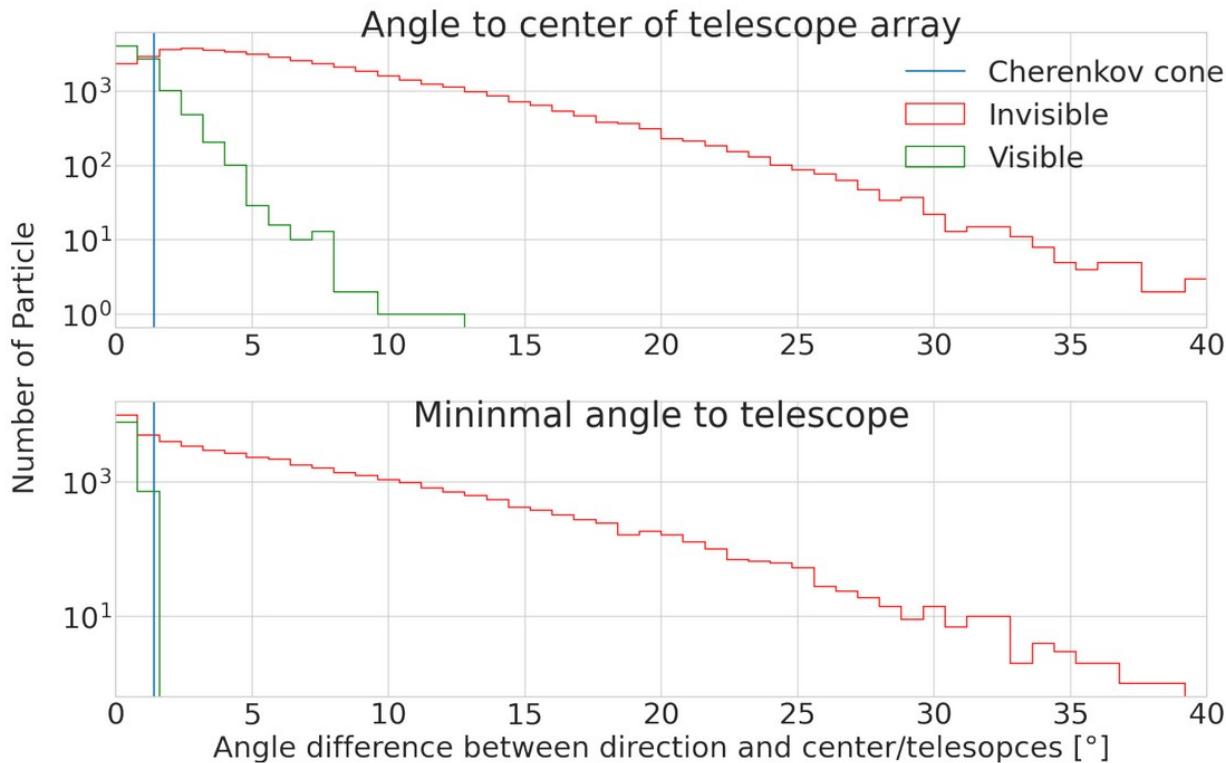
## Filter 1

- Angular cuts
- Dot product → Tensor possible



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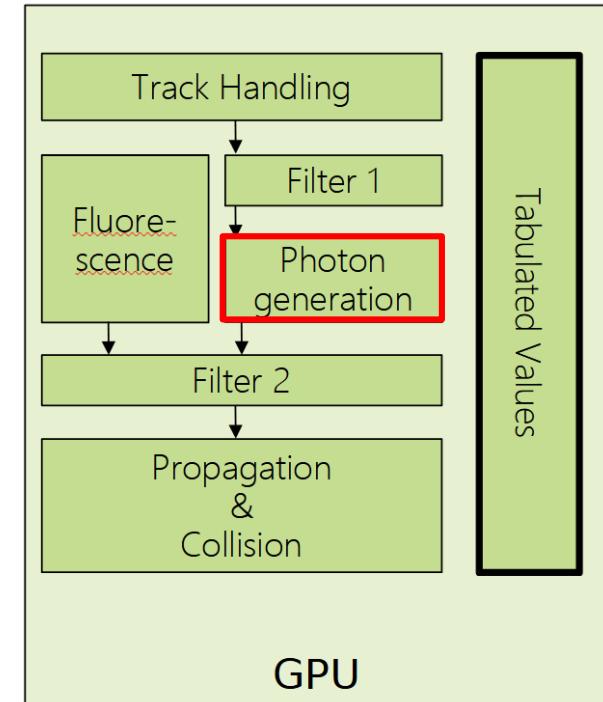


## Photon Generation

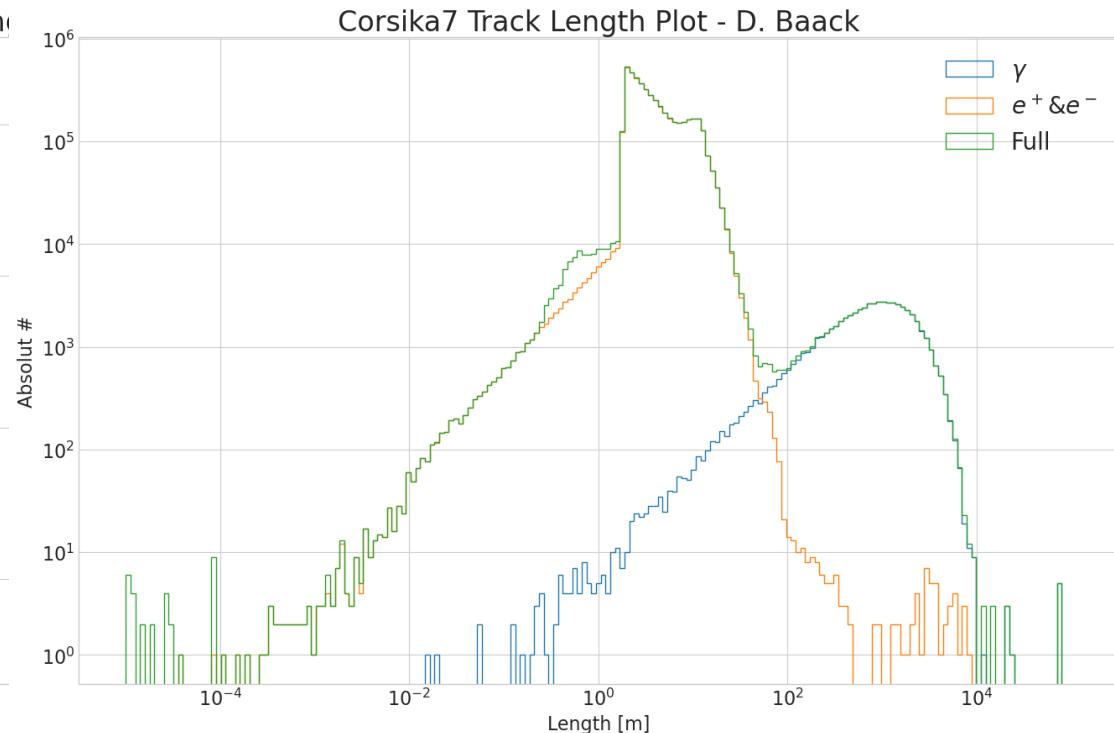
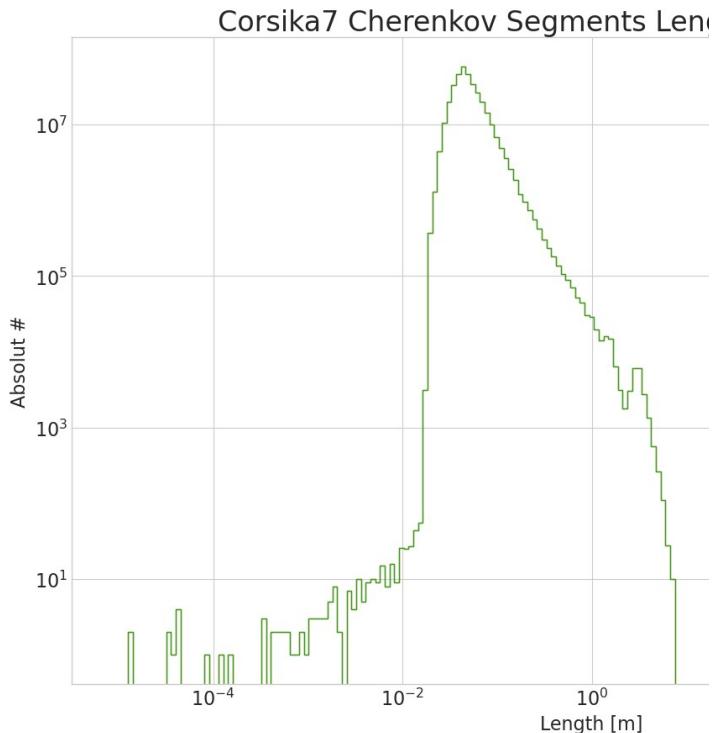
- Generate photons directions → vector
- Rotate and translate into particle system  
Matrix multiplication

$$N_{\text{cher}} = 2\pi\alpha z^2 L \frac{\lambda_1 - \lambda_2}{\lambda_1 \cdot \lambda_2} \cdot (1 - (n\beta)^{-2})$$

- Rotate and Translate to Emission position

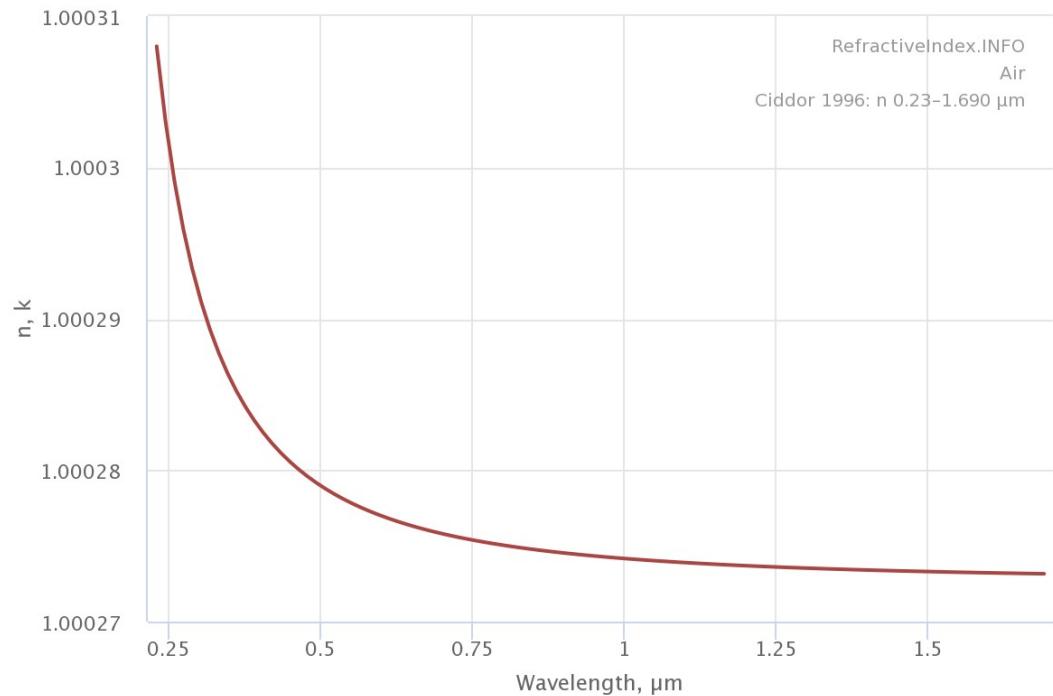


# Photon Generation



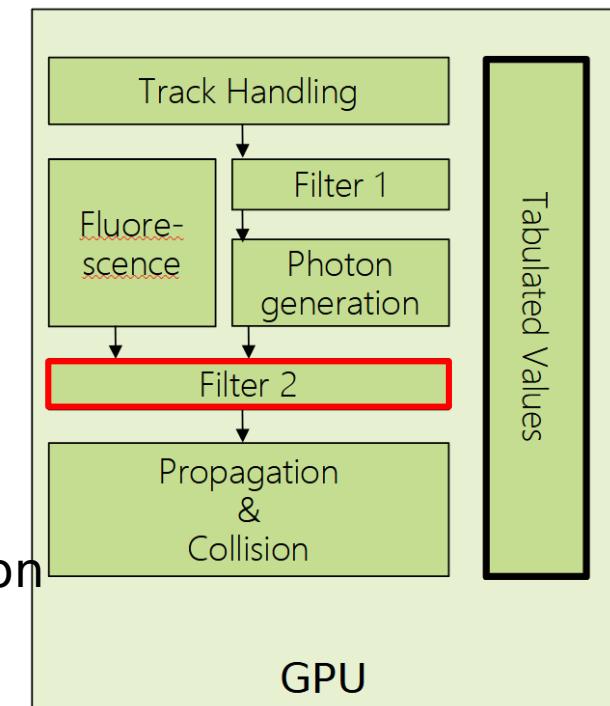
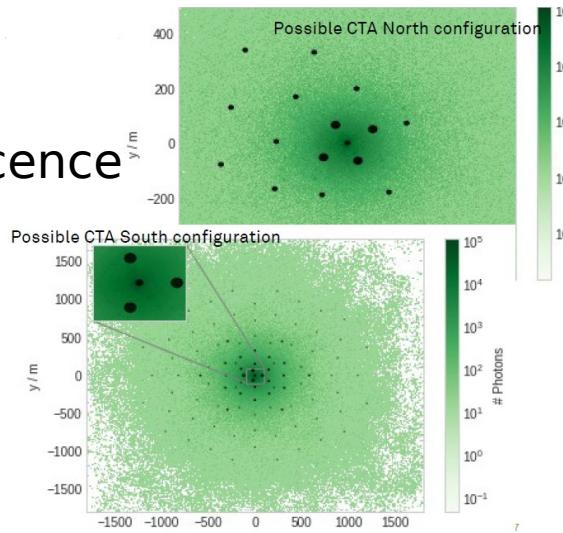
## Chromatic Dispersion

- Emission Wavelength dependent
- Edge cases:
  - Emission only part of specified wavelength possible
- 



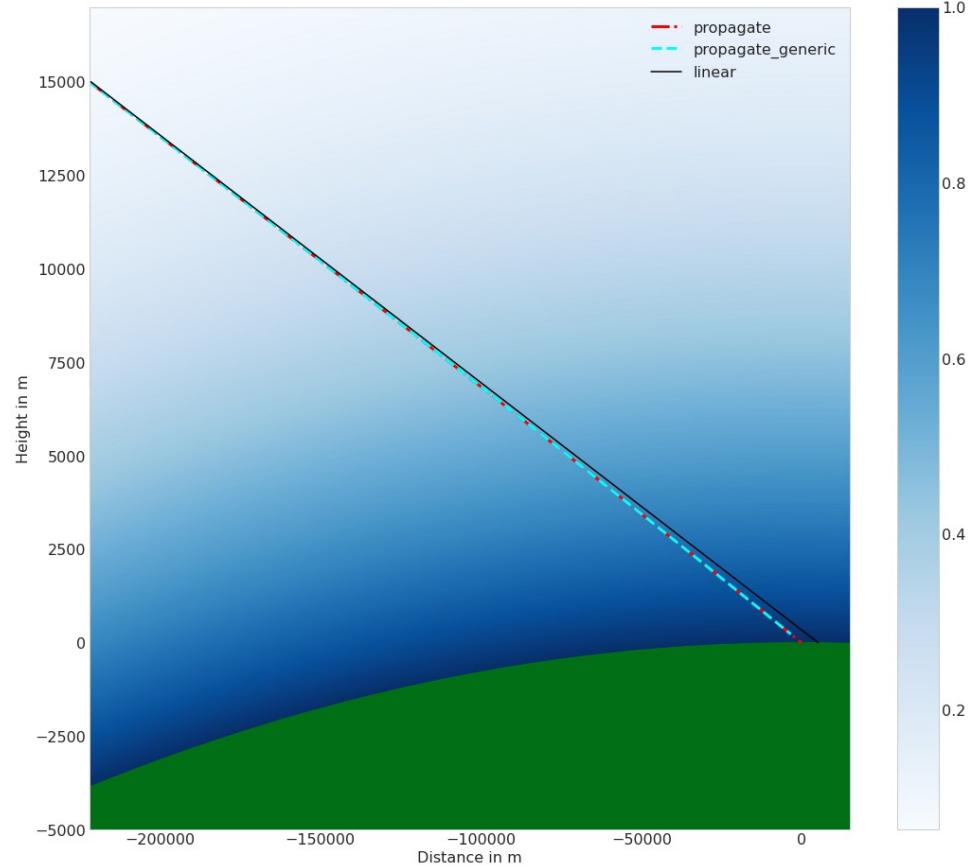
## Filter 2

- Merged with fluorescence generation



- Not feasible for default Cherenkov propagation
  - Cuts cost more than simple propagation

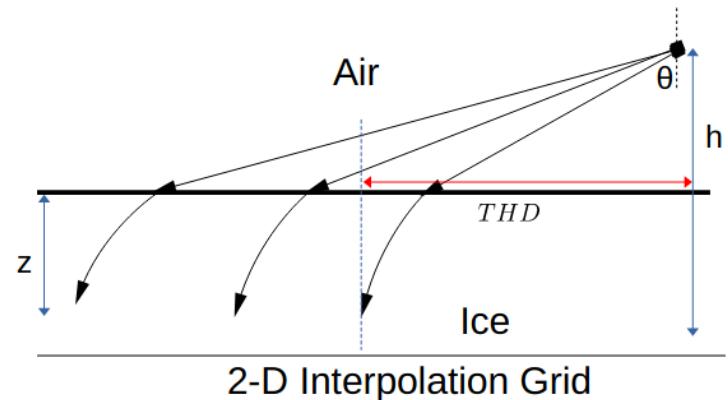
# Propagation



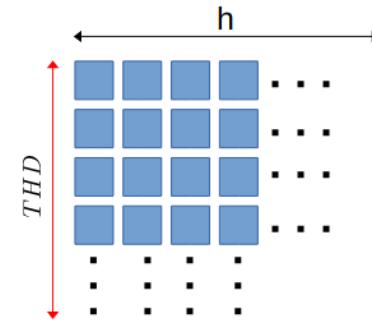
## Propagation

of:

- Yesterday:  
Propagating Air Shower Radio  
Signals to In-ice Antennas



2-D Interpolation Grid

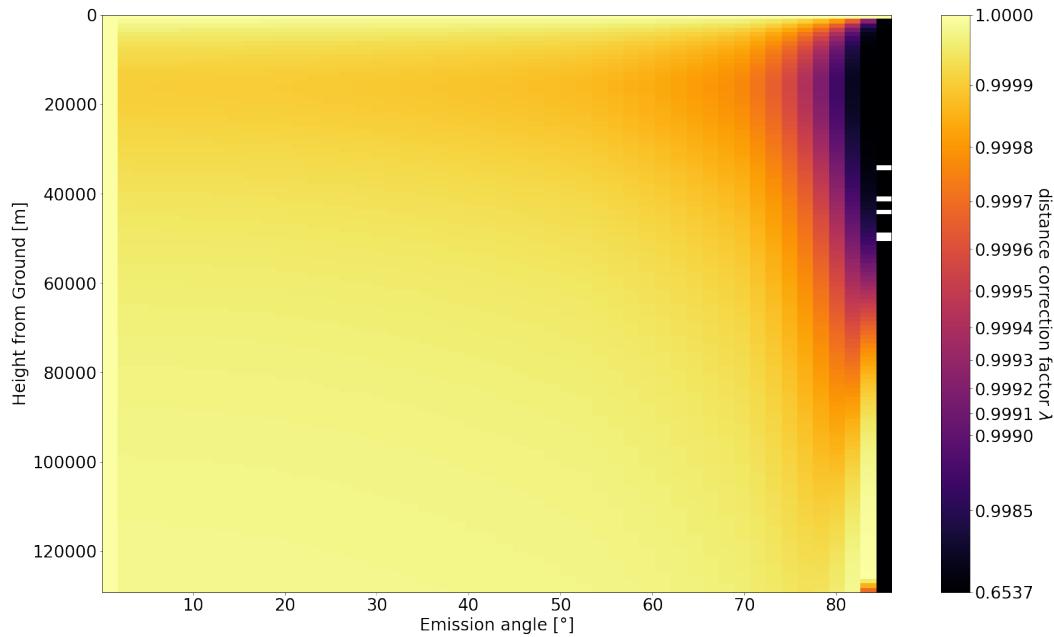
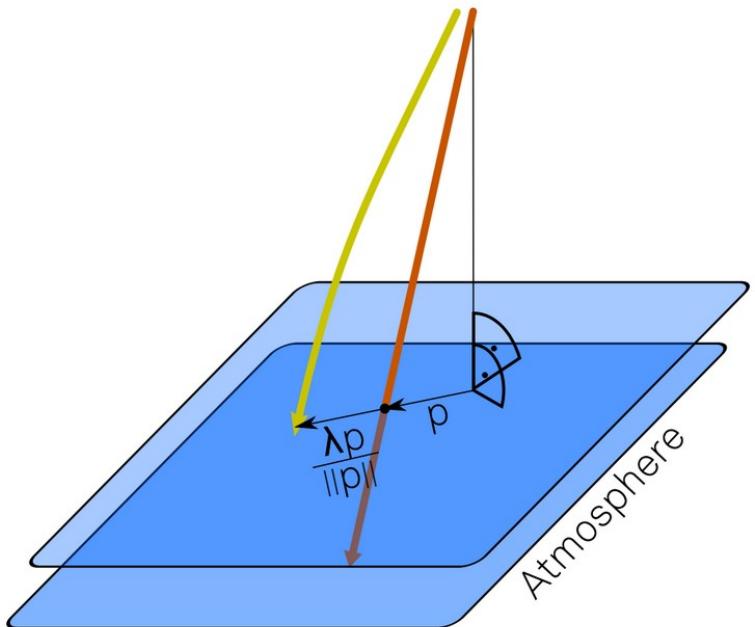


Uzair A. Latif et al

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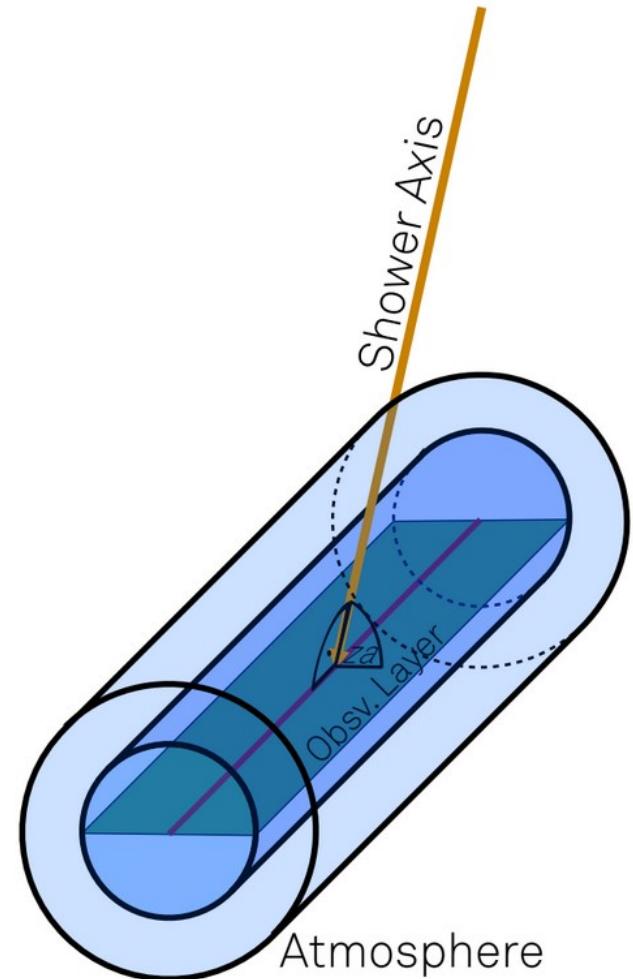
## Propagation

- 2 Parameter: Height and Angle



## Propagation

- Offset/Distance, Height, Angle
- Still possible to interpolate in hardware



## Conclusion

- Cross-Check with Corsika 6.9, 7.4 and real Magic data started.
- Possible cooperation with Mathieu and LST possible

