

Tools/likwid/example_topology_Ice_Lake_cache

Example likwid-topology Cache Topology on Intel Xeon Ice Lake

```
likwid-topology --caches
```

```
...
```

```
*****
```

Cache Topology

```
*****
```

```
Level:                1
Size:                 48 kB
Type:                 Data cache
Associativity:        12
Number of sets:       64
Cache line size:      64
Cache type:           Non Inclusive
Shared by threads:    2
Cache groups:         ( 0 76 ) ( 1 77 ) ( 2 78 ) ( 3 79 ) ( 4 80 ) ( 5 81 ) ( 6 82 ) ( 7 83 )
```

```
-----
Level:                2
Size:                 1.25 MB
Type:                 Unified cache
Associativity:        20
Number of sets:       1024
Cache line size:      64
Cache type:           Non Inclusive
Shared by threads:    2
Cache groups:         ( 0 76 ) ( 1 77 ) ( 2 78 ) ( 3 79 ) ( 4 80 ) ( 5 81 ) ( 6 82 ) ( 7 83 )
```

```
-----
Level:                3
Size:                 57 MB
Type:                 Unified cache
Associativity:        12
```

```

Number of sets:      77824
Cache line size:     64
Cache type:          Non Inclusive
Shared by threads:   76
Cache groups:        ( 0 76 1 77 2 78 3 79 4 80 5 81 6 82 7 83 8 84 9 85 10 86 11 87 12 8
-----

```

```

*****
NUMA Topology
*****

```

```

NUMA domains:        2
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```

```

Domain:              0
Processors:           ( 0 76 1 77 2 78 3 79 4 80 5 81 6 82 7 83 8 84 9 85 10 86 11 87 12 8
Distances:            10 20
Free memory:          241844 MB
Total memory:         256560 MB
-----

```

```

Domain:              1
Processors:           ( 38 114 39 115 40 116 41 117 42 118 43 119 44 120 45 121 46 122 47
Distances:            20 10
Free memory:          244947 MB
Total memory:         258029 MB
-----

```

- Number of cache levels, groups and sizes
- Cache line size -> How many bytes are fetched from memory simultaneously?
- Associativity -> Memory addresses get mapped to cache addresses. How many cache lines from memory mapping to the same cache address can be held simultaneously?