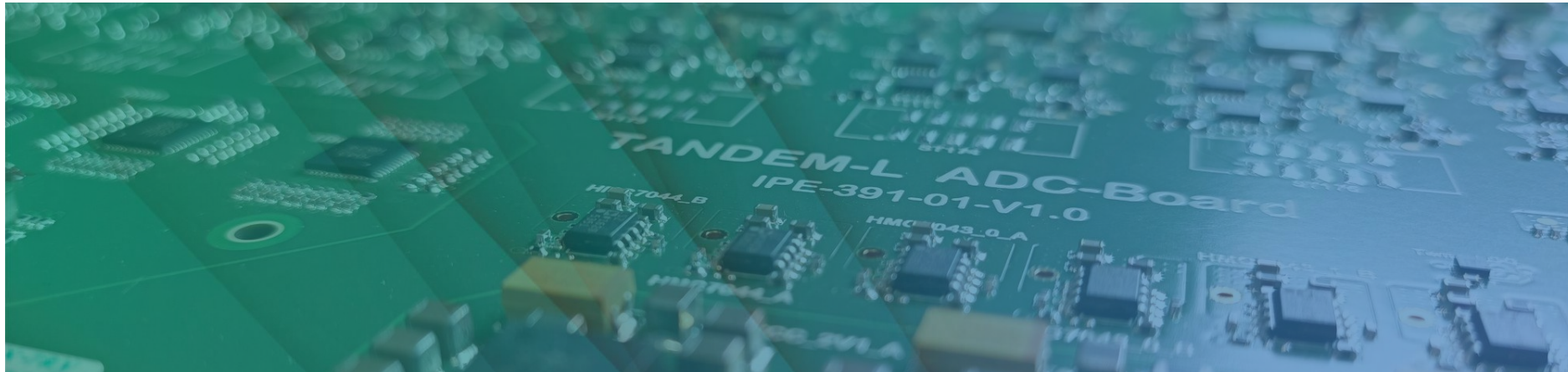
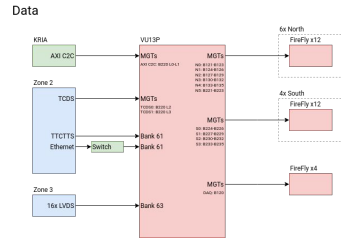


# Altium Designer am IPE

Torben Mehner



# PCB Design Process



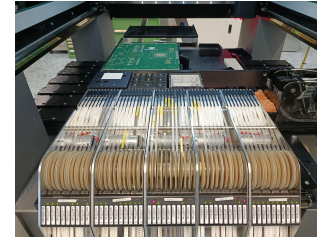
System Design



Schematic Capture  
PCB Layout



PCB Production



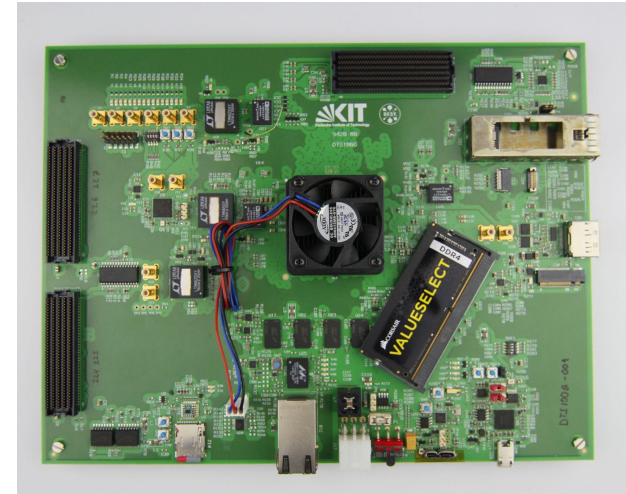
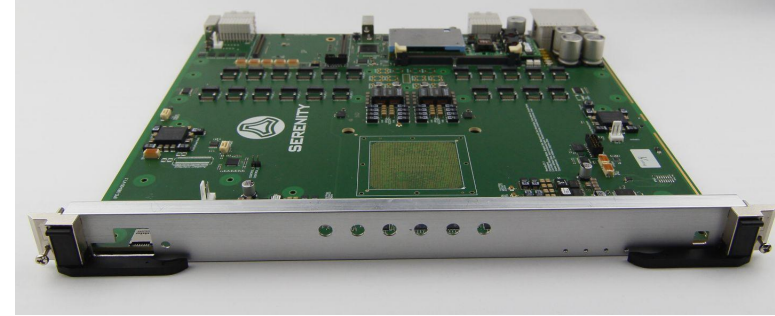
PCB Assembly



PCB Commissioning

# System Design

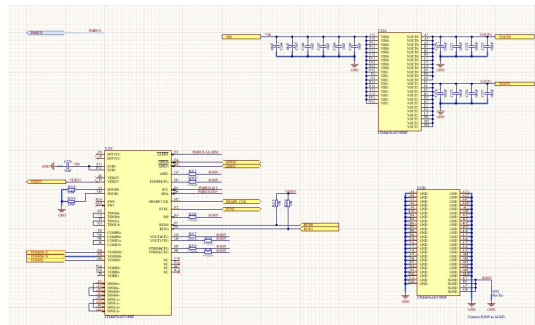
- Off-the-shelf general purpose systems
  - Serenity-S1, DTS-100G, HiFlex
  - Little to no design work
  - Soft-/Firmware prepared once
- Common set of standardized components
  - Present in component library
  - Purchase in bulk (manufacturing/price)
  - Soft-/Firmware prepared once



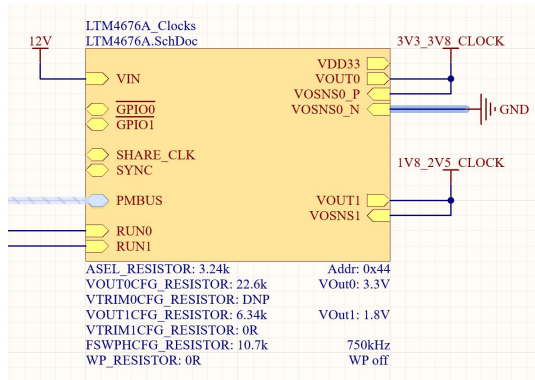
# Schematic Capture and PCB Layout

- Start working in modules now
  - Modules include typical application schematics and recommended layout
  - Modules fulfil a single task (e.g. power supply, clock)
  - Reuse modules from library
- Common set of standardized components
  - Present in component library
  - Purchase in bulk (manufacturing/price)
  - Soft-/Firmware prepared once

Why do this?



When you can do this?



# Guidelines for Modularity in EDA

- Hierarchical Design
- SOLID design principles
  - Single Responsibility
    - Single central part or
    - Single functionality by multiple parts
  - Open for additions - Closed for changes
    - Simple “Placeholder” module for e.g. LDOs, SMPS
    - Extendable with additional connections
  - Interface Segregation Principle
    - Only have absolutely needed functionality in a module
    - Use parameters for potentially changing values
- GIT integration for collaboration

# Guidelines for Modularity in Schematic Modules

- Copy recommended design diagram
- Parametrize your design
  - Through ports
  - Through parameters
- If possible, use 0402 passives
  - Larger resistors only for power
  - Larger caps are necessary

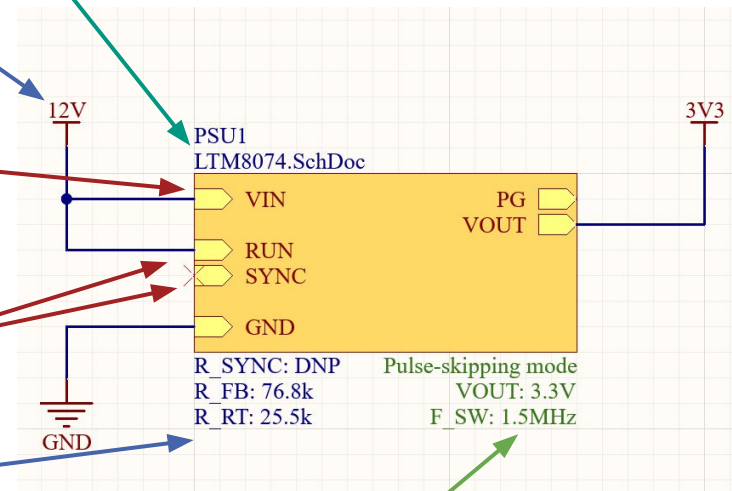
Single Central Part

Parameter  
(through ports)

Common SMPS  
connection

Additional  
connections

Parameters

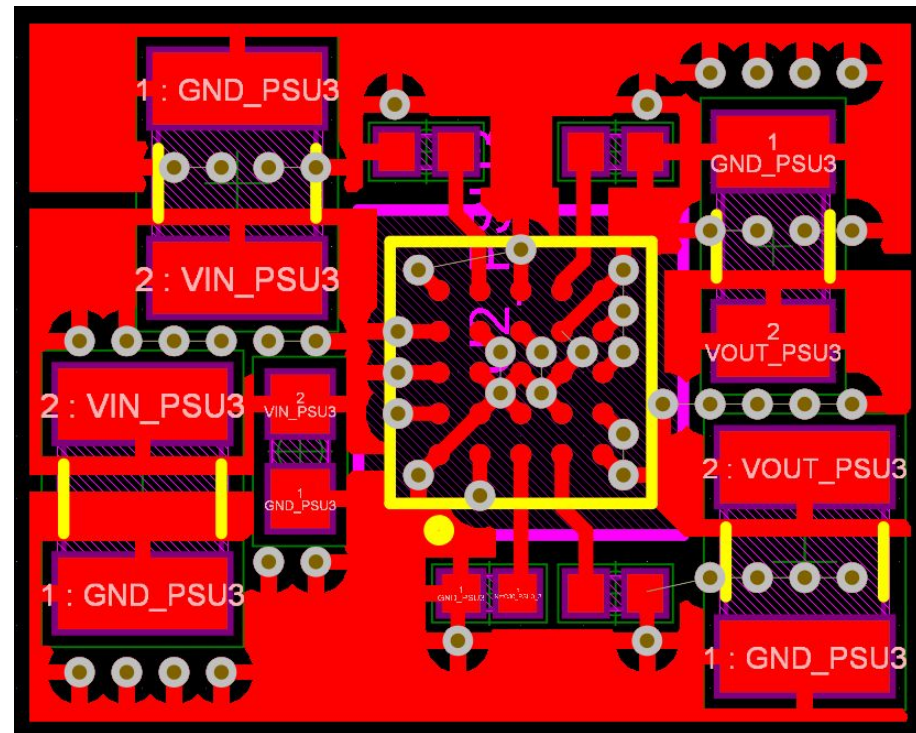


This currently needs to be written manually



# Guidelines for Modularity in PCB Modules

- *If possible*, use low-spec prerequisites
  - Low-spec design rules
  - All components on top
  - All traces on top and bottom
  - No Via-In-Pad
  - Only through-hole vias
- Copy recommended layout
- Fanout signals and terminate with vias



# PCB Production

- Use shared production information
  - Common PCB stack-ups
  - Common design rules
  - Predefined board outlines
- Automatic Gerber/ODB+ generation

Revision ID	Revision	Name	Description	Revision State	Note
ALS-0000	3	2 Layer 0 Plane Isola F...	2 Layer 0 Plane Isola F...	<input type="checkbox"/> Draft	
ALS-0001	3	2 Layer 2 Plane Isola F...	2 Layer 2 Plane Isola F...	<input type="checkbox"/> Draft	
ALS-0002	3	4 Layer 2 Plane Isola F...	4 Layer 2 Plane Isola F...	<input type="checkbox"/> Draft	
ALS-0003	3	4 Layer 4 Plane Isola F...	4 Layer 4 Plane Isola F...	<input type="checkbox"/> Draft	
ALS-0004	3	6 Layer 4 Plane Isola F...	6 Layer 4 Plane Isola F...	<input type="checkbox"/> Draft	
ALS-0005	1	4 Layer MultiCB 4L-01...		<input type="checkbox"/> Draft	Added MultiCB 4L-01...
ALS-0006	2	6 Layer MultiCB 6L-01	6 Layer MultiCB defin...	<input checked="" type="checkbox"/> Approved	Used in ZL30274 clock...
ALS-0008	1	8 Layer MultiCB 8L-01		<input type="checkbox"/> Draft	

Create, Edit, Set Default Templates in one place. [Open Template Settings...](#)

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.4mil	3.5	
1	TOP	CF-004	Signal		1.378mil		
	Dielectric 2	PP-006	Prepreg		9.055mil	4.25	0.02
2	IN2	CF-004	Signal		1.378mil		
	Dielectric 4	PP-006	Core		11.811mil	4.5	0.02
3	IN3	CF-004	Signal		1.378mil		
	Dielectric 1	FR-4	Dielectric		13.386mil	4.25	
4	IN4	CF-004	Signal		1.378mil		
	Dielectric 7	PP-006	Core		11.811mil	4.5	0.02
5	IN5	CF-004	Signal		1.378mil		
	Dielectric 9	PP-006	Prepreg		9.055mil	4.25	0.02
6	BOT	CF-004	Signal		1.378mil		
	Bottom Solder	Solder Resist	Solder Mask		0.4mil	3.5	
	Bottom Overlay		Overlay				

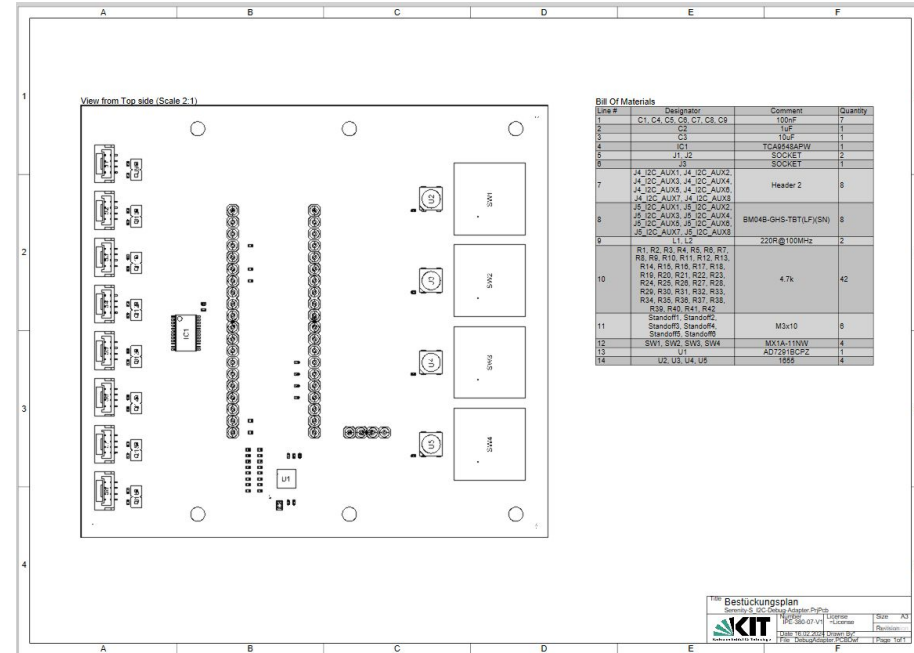
Stackup Impedance Via Types

Preview Details Lifecycle Origin



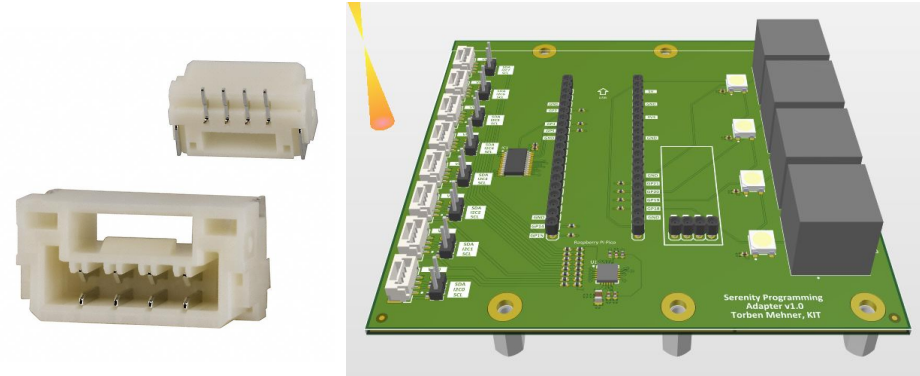
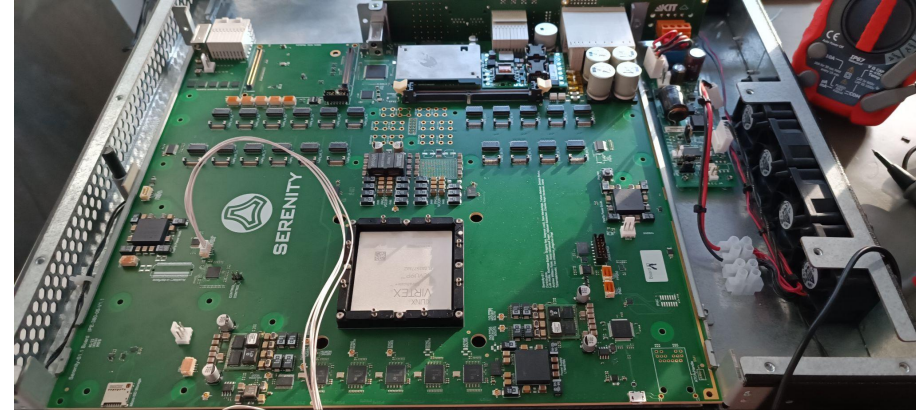
# PCB Assembly

- Templates for assembly file generation
  - Draftsman for assembly plan
  - Pick and place files
  - Bill of materials
- *TODO*: scripts to convert Altium output directly to AVT-usable files
- *TODO*: central AVT parts database (as supplier for Octopart)



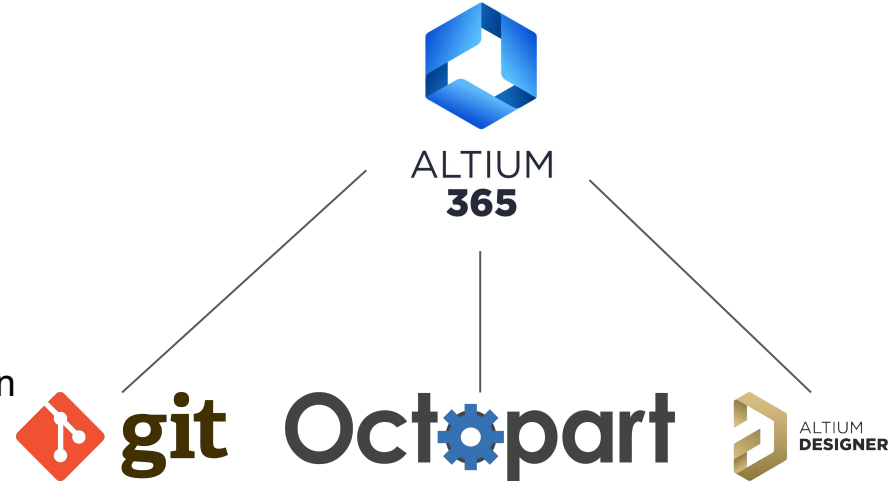
# PCB Commissioning

- Bridging back to system design
  - If reused design is proven to work, no commissioning is necessary
  - Soft- and Firmware can be reused
- Using common PCB commissioning tools
  - Serenity Debug Adapter accesses I2C through very small SMT connectors



# But why Altium?

- Full featured, widely used PCB software
- Altium 365 brings cloud integration
  - Ease of sharing design
  - Unprecedented reuse capabilities
  - Git integration, allows great collaboration
- Octopart integration
  - Better BOM management
  - Manufacturer part search

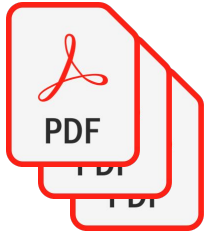
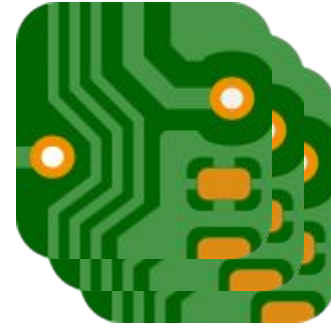
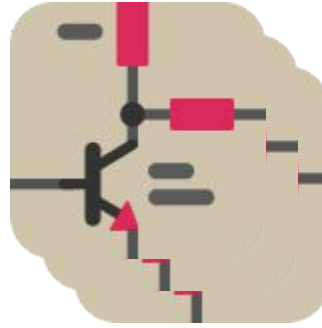
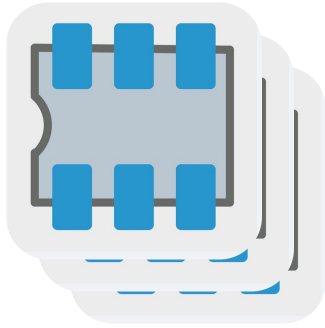


# Current PCB Design Process

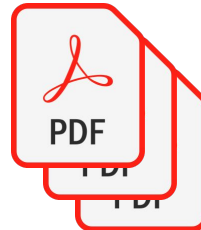
Create all symbols  
and footprints

Draw all schematics

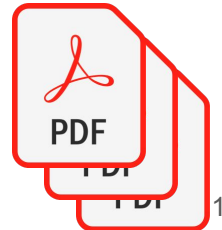
Layout PCB



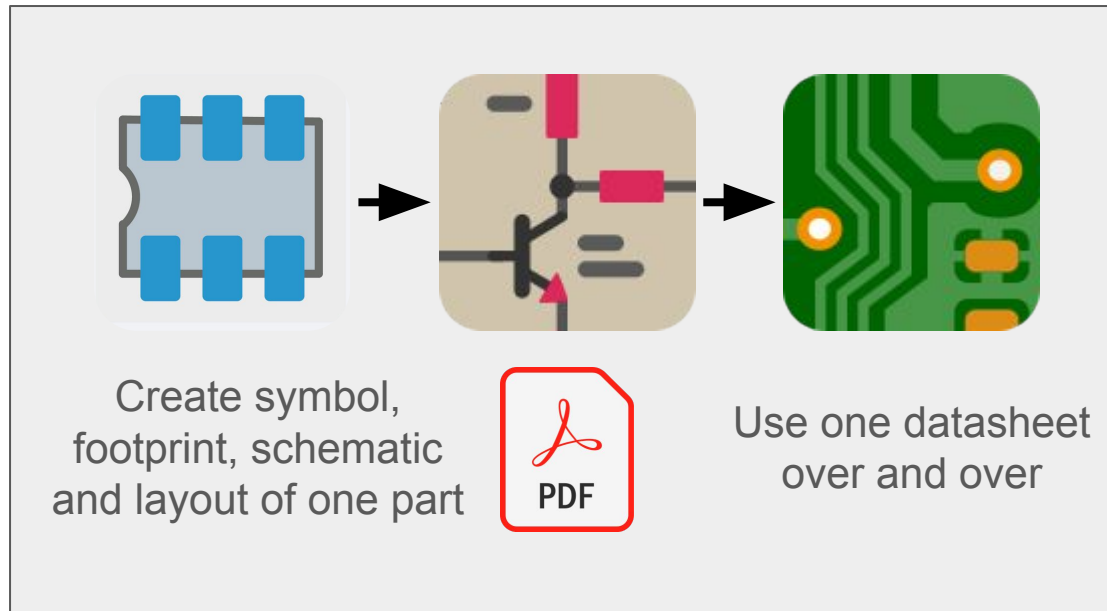
\*Forget datasheet\*



\*Forget datasheet\*



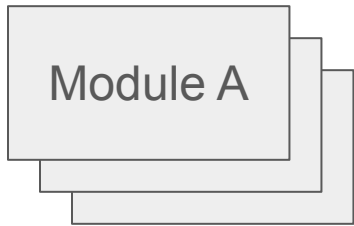
# Proposed PCB Design Process



Module A

# Proposed PCB Design Process

Design all modules



Connect modules  
in schematic



Connect modules  
in layout

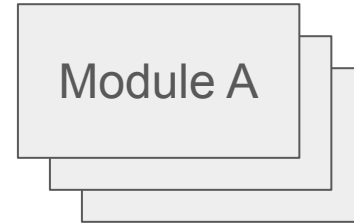


# Proposed *Reverse* PCB Design Process

Finished & Tested  
PCB



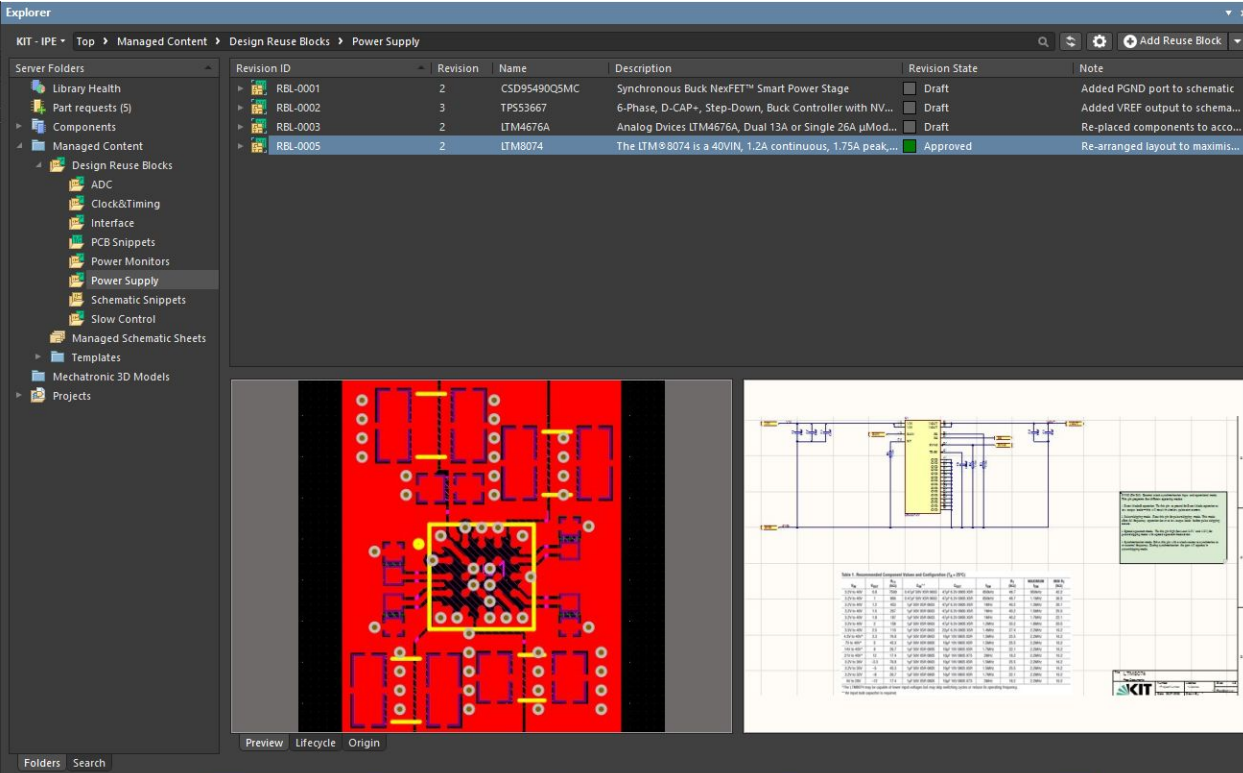
Extract working  
modules





# Module Library

- Library to store modules
- Adaptable categories through sub-folders
- Revisions allow for improving modules
- Revision status shows if module is already tested



The screenshot displays the KIT IPE Explorer interface, showing the Design Reuse Blocks library and a detailed view of the LTM8074 module.

**Design Reuse Blocks Library:**

Revision ID	Revision	Name	Description	Revision State	Note
RBL-0001	2	CSD95490Q5MC	Synchronous Buck NexFET™ Smart Power Stage	Draft	Added PGND port to schematic
RBL-0002	3	TP533667	6-Phase, D-CAP+, Step-Down, Buck Controller with NV...	Draft	Added VREF output to schema...
RBL-0003	2	LTM4676A	Analog Devices LTM4676A, Dual 13A or Single 26A $\mu$ Mod...	Draft	Re-placed components to acco...
RBL-0005	2	LTM8074	The LTM8074 is a 40VIN, 1.2A continuous, 1.75A peak,...	Approved	Re-arranged layout to maximis...

**Module Details (LTM8074):**

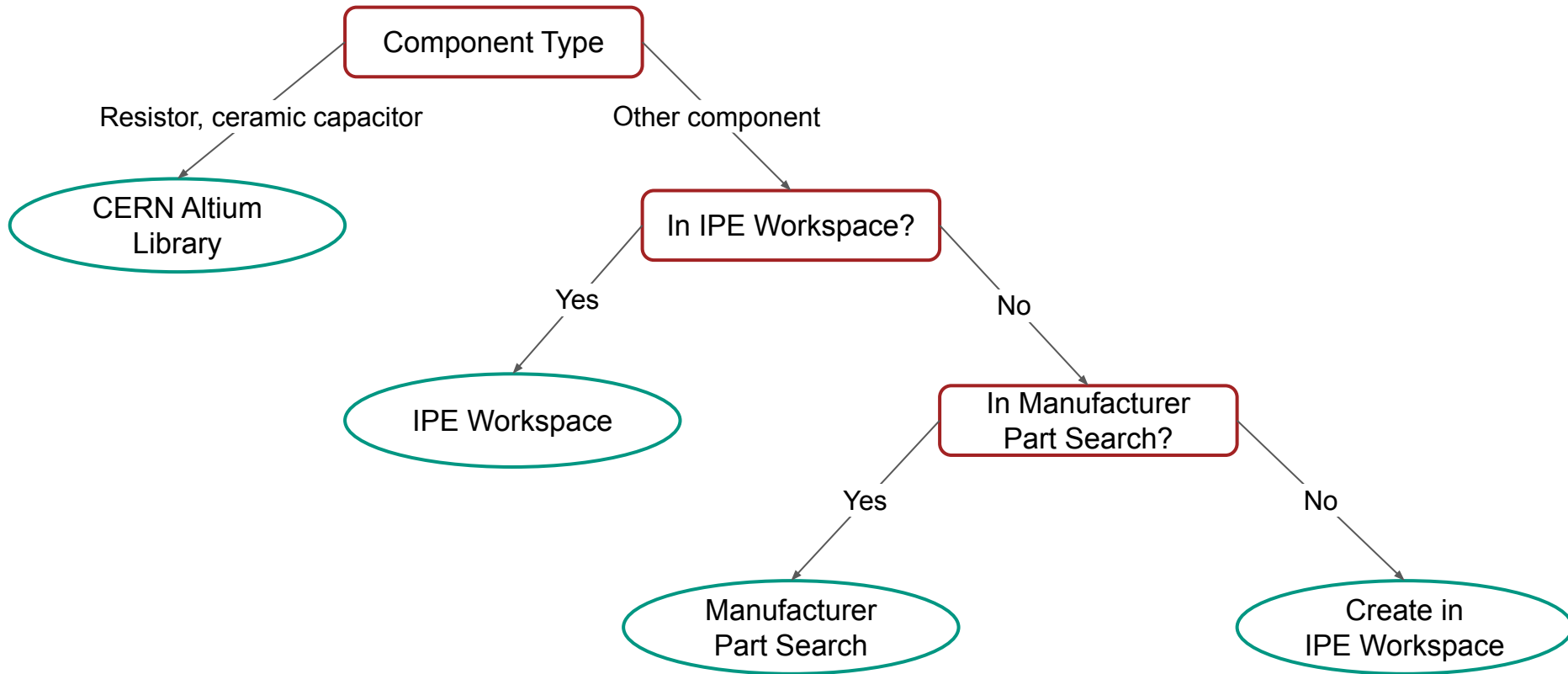
Description	Revision State
Synchronous Buck NexFET™ Smart Power Stage	Draft
6-Phase, D-CAP+, Step-Down, Buck Controller with NV...	Draft
Analog Devices LTM4676A, Dual 13A or Single 26A $\mu$ Mod...	Draft
The LTM8074 is a 40VIN, 1.2A continuous, 1.75A peak,...	Approved

The bottom section of the interface shows a detailed schematic diagram of the LTM8074 module, including a PCB layout view and a detailed schematic diagram with component values and a table of component values.

# Where do I find...?

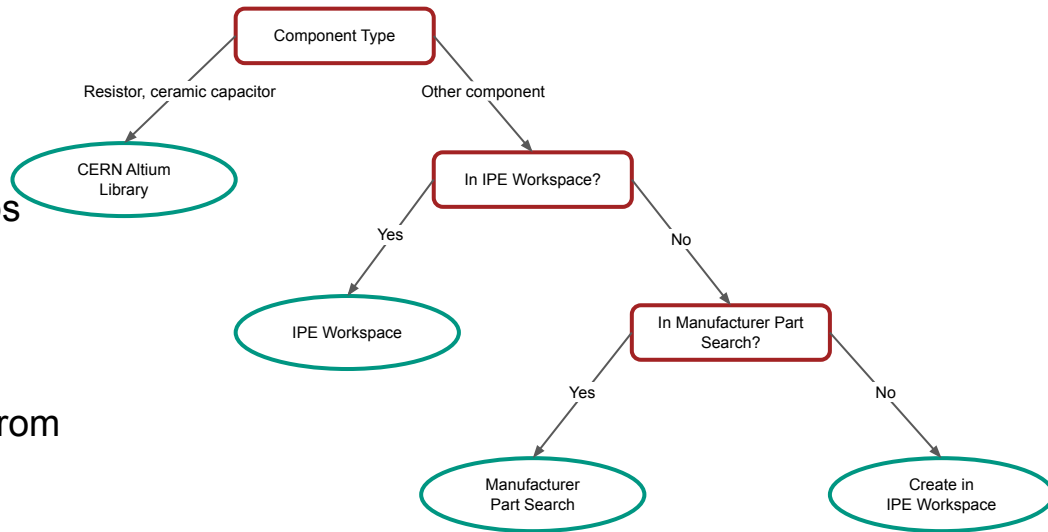
- Components
- PCB Modules
- KIT Project Template
- KIT Schematic Template
- PCB Layer Stacks
- Design rules

# Where do I find components?



# Where do I find components?

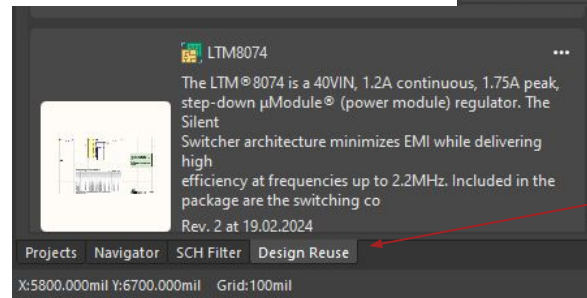
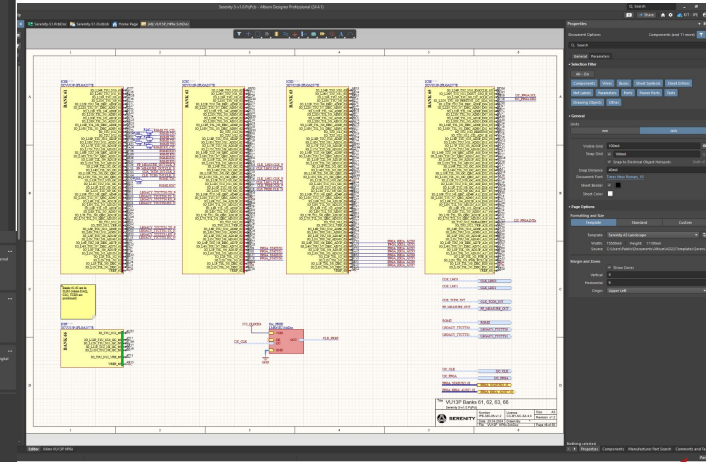
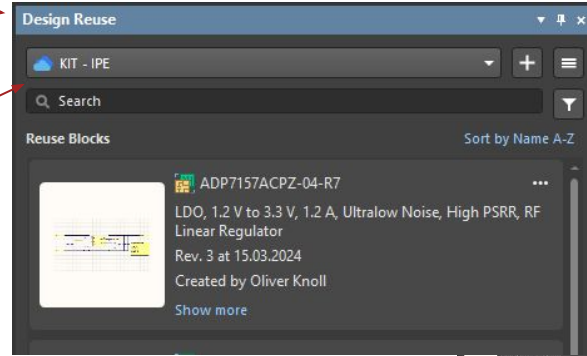
- CERN Altium Library
  - Good passive footprints
  - Use specific types for ceramic caps
  - Use “no-value”-types for resistors
- IPE Workspace
  - Components that were improved from manufacturer part search
  - Specific components
  - [Video on how to create a component](#)
- Manufacturer part search
  - Wide variety of available components



# Where do I find PCB Modules?

Design reuse panel

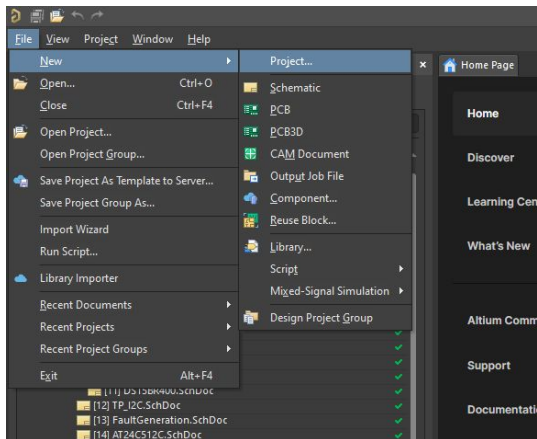
KIT-IPE Workspace



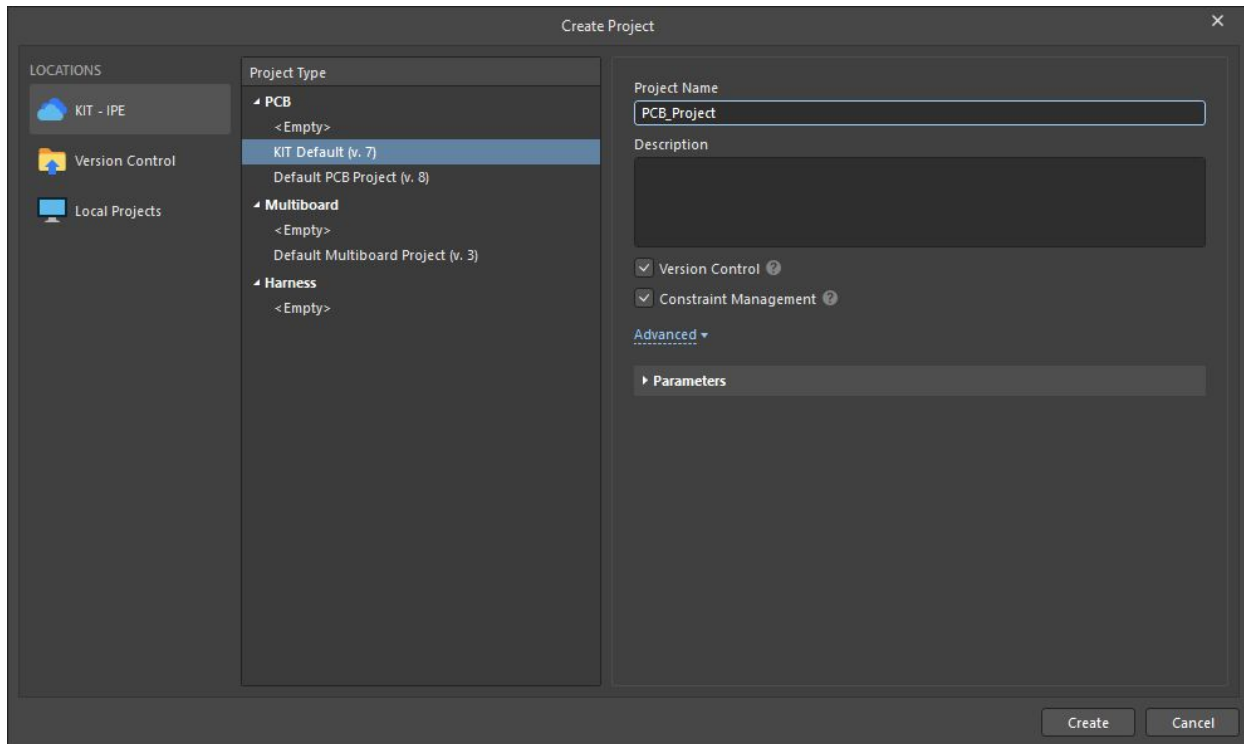
Design reuse panel

If not found, you must enable it in the bottom right

# Where do I find the KIT Project Template?

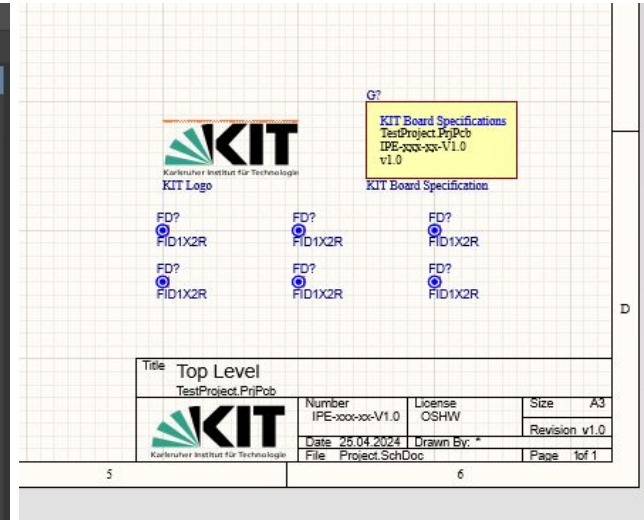
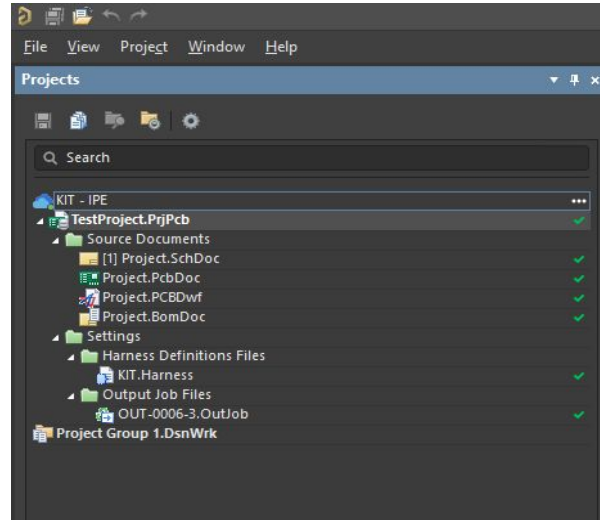


- New - Project...
- Select KIT Default



# What does the KIT Project Template include?

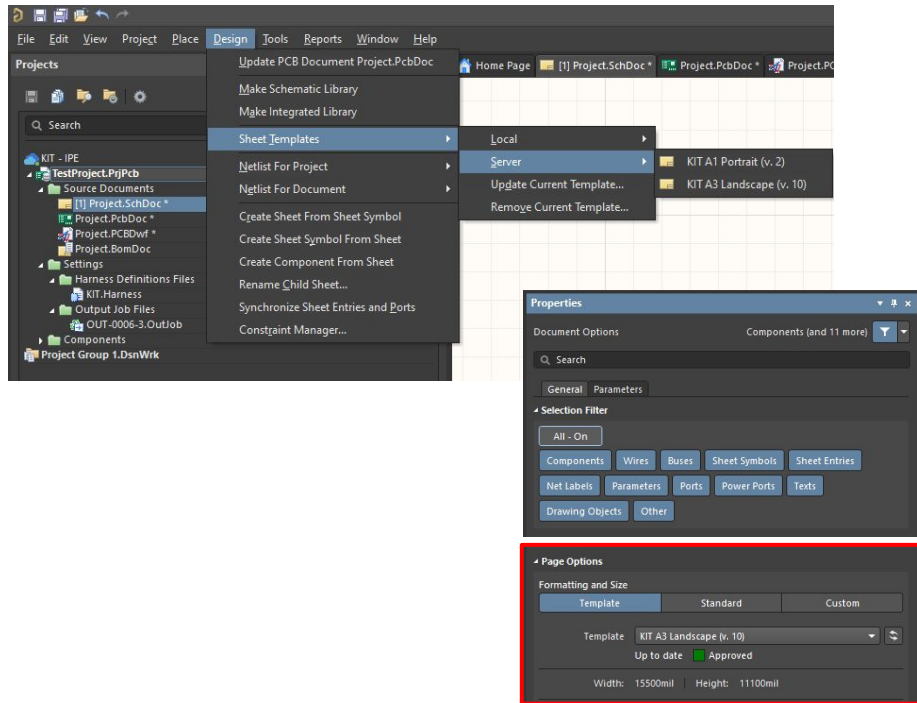
- Schematic with
  - KIT Logo
  - Board specifications
  - 6 Fiducials
- Empty Layout
- Assembly Drawing
- Interactive BOM
- KIT Harness Definition (I2C, UART, JTAG, ETH, ...)
- Output Job File





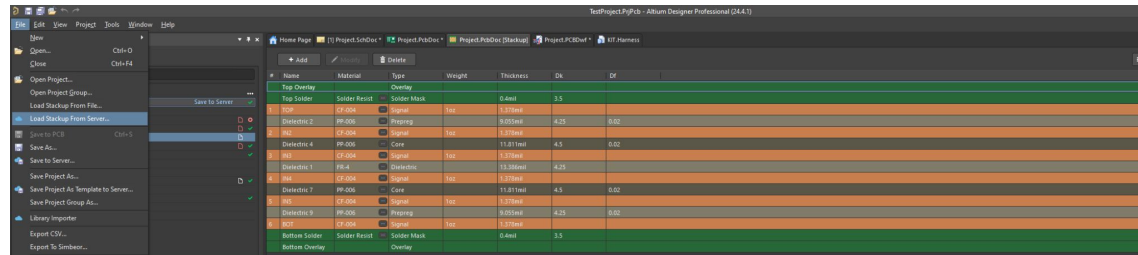
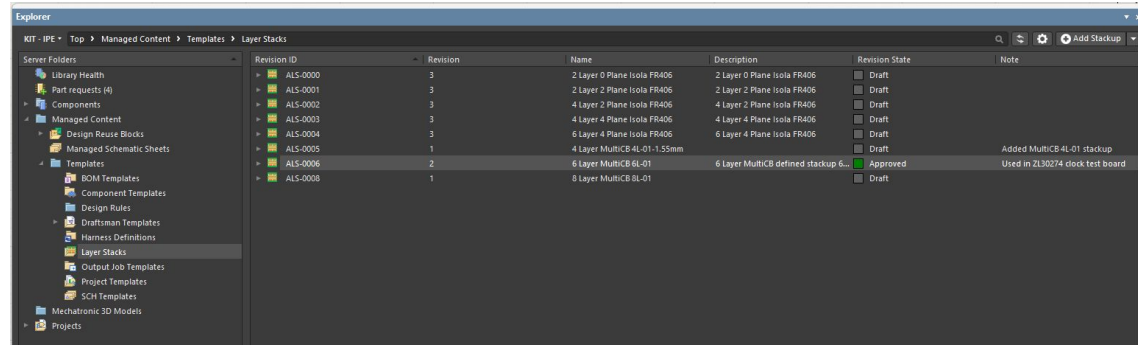
# Where do I find the KIT Schematic Template?

- Either in the properties panel
- Or Design - Sheet Templates - Server
- Project parameters
  - License
  - ProjectName
  - ProjectNumber
  - Project Revision
- Sheet parameters
  - Title
  - DrawnBy



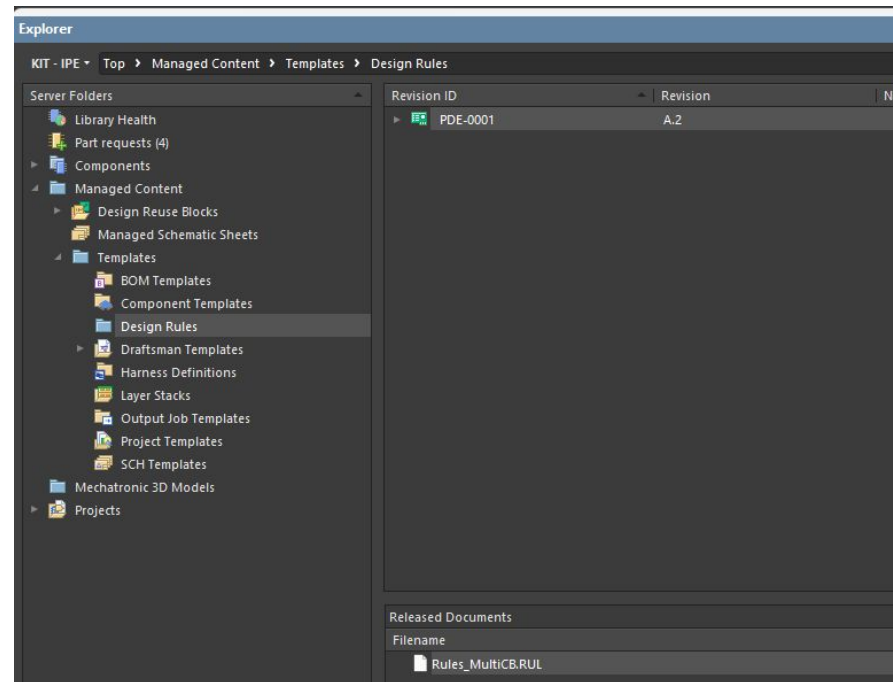
# Where do I find PCB Layer Stacks?

- Templates found in the “Explorer”-panel under “Managed Content - Templates”
- Loaded by opening the current PCB Stackup and then clicking “File - Load Stackup from Server”



# Where do I find design rules?

- Rule set for MultiCB is accessible in “Explorer Panel - Managed Content - Templates - Design Rules”  
Deprecated since AD24
- Constraints management has changed in Altium Designer 24
- *TODO*: Update to Constraints Manager



# Questions?