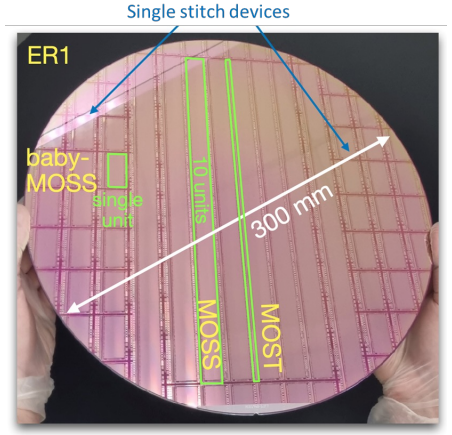
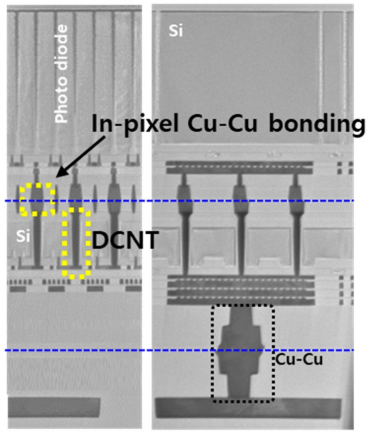
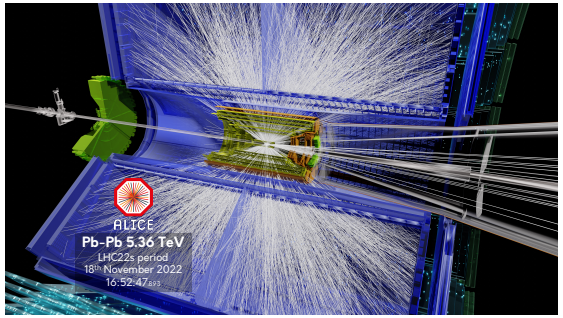
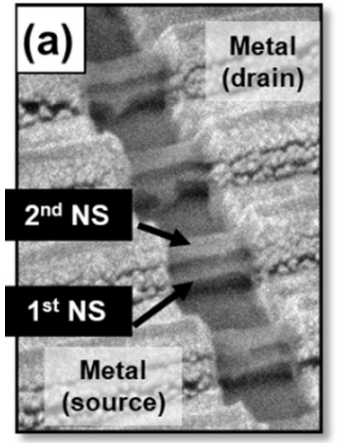
Monolithic Active Pixel Development and the next frontier in CMOS sensor technology: implications for future detectors in High Energy Physics









Walter Snoeys

DRD7.6b meeting, September 2nd, 2025

Massive contributions from many colleagues at CERN, ALICE, ESE, EP R&D WP1.2, …

DRD7.6

Complex imaging ASICs and technologies – Work Package overview

Project 7.6b: Shared Access to 3D Integration -> see Michele Caselle's presentation

Project 7.6a: Common Access to Selected Imaging Technologies

Project Description

This project aims to provide common access to advanced imaging technologies through the organization of common fabrication runs. These are initially envisaged for the *TowerJazz 180 nm*, *TPSCo 65 nm ISC*, and the *LFoundry 110 nm IS* CMOS imaging technologies. IP development is also foreseen to accelerate and streamline the design effort.

Contributors:

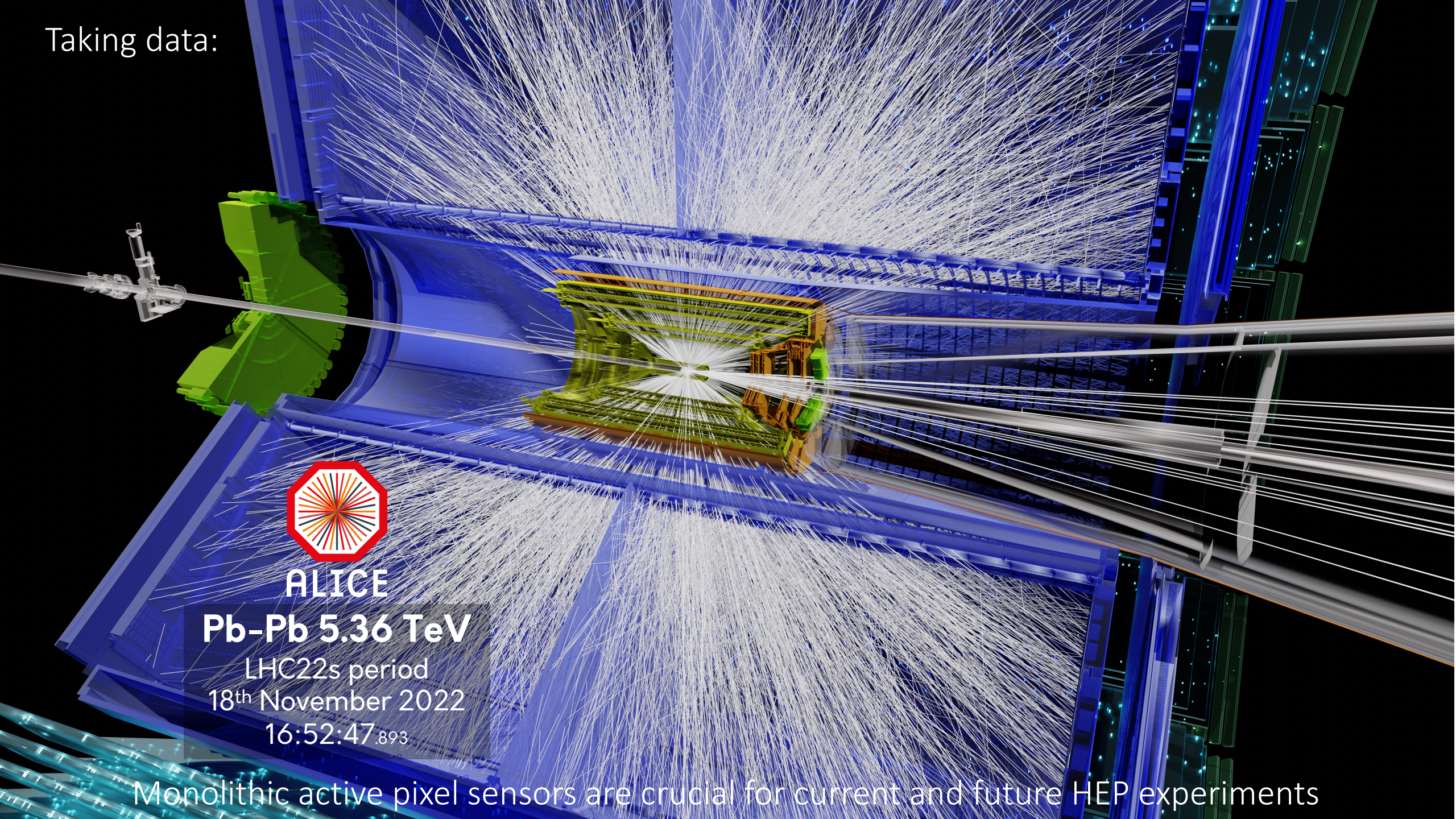
CERN, IN2P3: CPPM, IPHC, IP2I + others, INFN(TO, TIFPA, MI, BO, PD, PV, PG, PI), NIKHEF, UiB, UiO and USN, STFC and SLAC already doing effort

Contact persons: Marlon Barbero, Jerome Baudot, Iain Sedgwick, Manuel Rolo, Walter Snoeys

OUTLINE

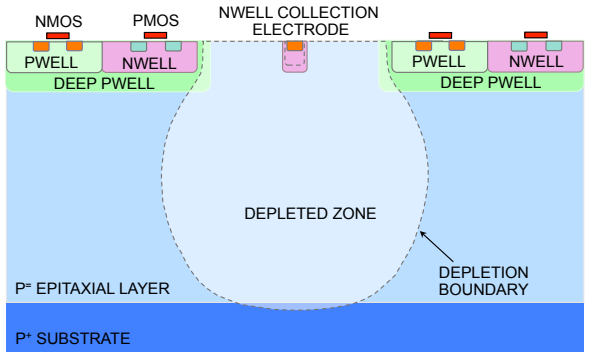
- Monolithic sensors in EP RD WP1.2 & ALICE
  - Sensor optimization: importance of capacitance and perspectives for improvement
  - Large, wafer-scale sensors via stitching
- General trends in imaging and standard technologies
- Relevance for ALICE3 and future detectors in HEP

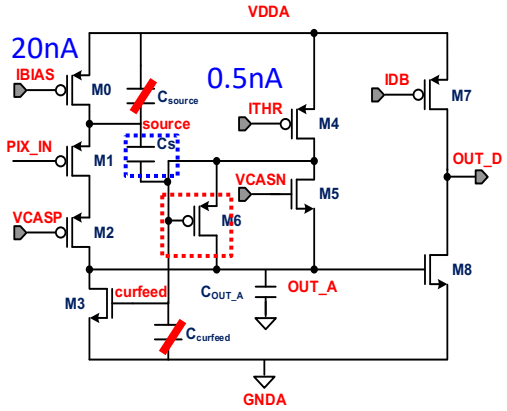
Taking data:



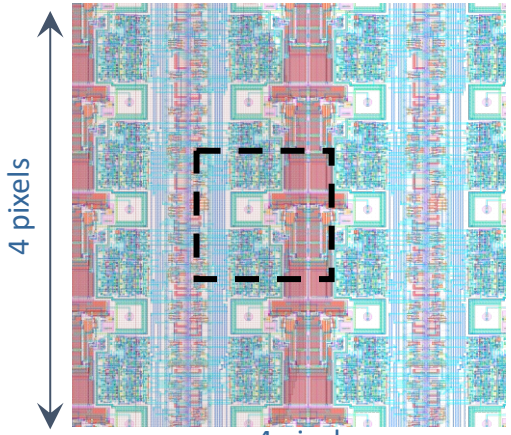
Monolithic active pixel sensors are crucial for current and future HEP experiments

ALPIDE chip in ALICE ITS2

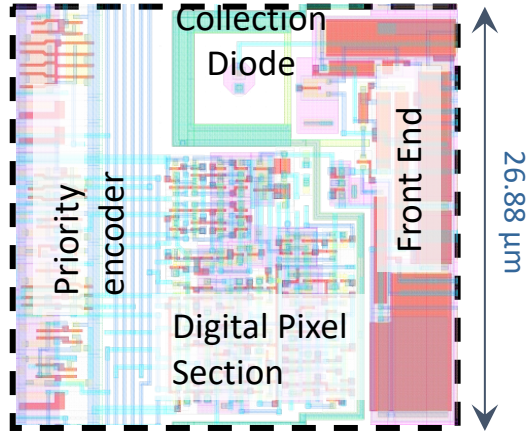




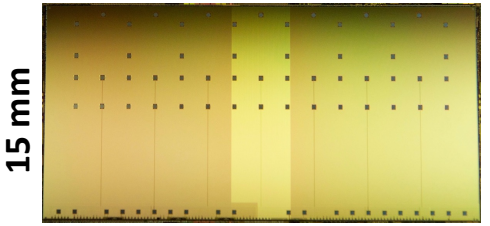
Matrix layout

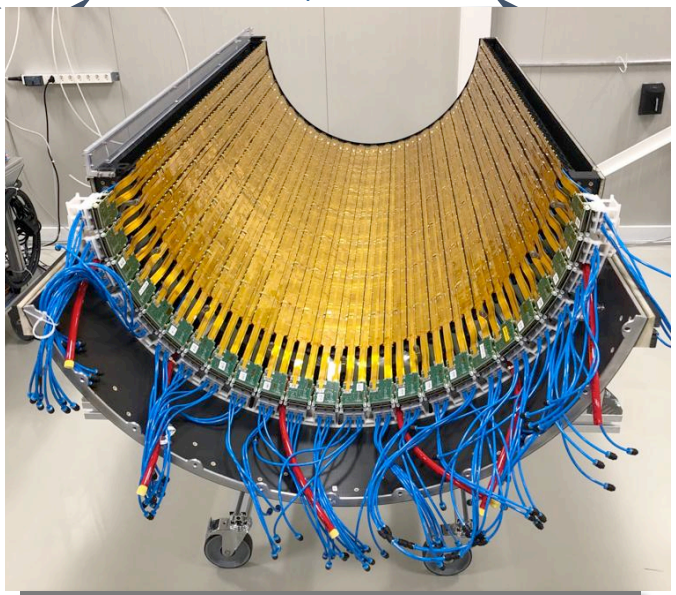


Pixel layout

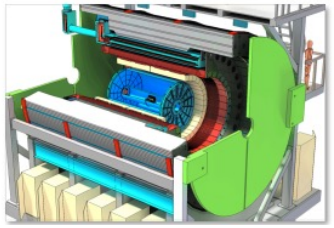


- TJ CMOS 180 nm INMAPS imaging process (TJ) > 1kΩ cm p-type epitaxial layer
- Small 2 µm n-well diode and reverse bias for low capacitance C(sensor+circuit) < 5 fF
- 40 nW continuously active front end D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042
- Q_{in}/C ~ 50 mV, analog power ~ $(Q/C)^{-2}$ NIM A 731 (2013) 125
- Zero-suppressed readout, no hits no digital power G. Aglieri et al. NIM A 845 (2017) 583-587
- Ratio between 15 x 30 mm² and 10 m² in the experiment not ideal -> stitching
- ALPIDE (ALICE Pixel Detector) to be used for several other physics experiments, in space and for medical applications

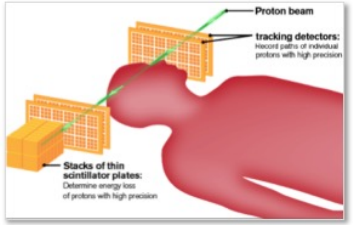




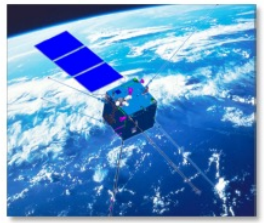
Half outer barrel (layer 6)
~ 2.47 Gpixels covering ~ 2 m² sensitive area



sPHENIX



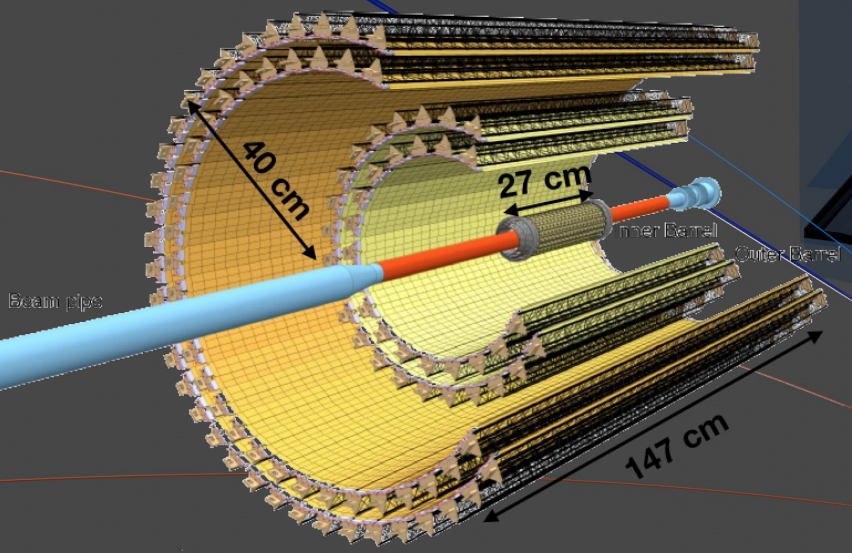
Proton CT (tracking)



CSES – HEPD2

Design team: G. Aglieri, C. Cavicchioli, Y. Degerli, C. Flouzat, D. Gajanana, C. Gao, F. Guilloux, S. Hristozkov, D. Kim, T. Kugathasan, A. Lattuca, S. Lee, M. Lupi, D. Marras, C.A. Marin Tobon, G. Mazza, H. Mugnier, J. Rousset, G. Usai, A. Dorokhov, H. Pham, P. Yang, W. Snoeys (Institutes: CERN, INFN, CCNU, YONSEI, NIKHEF, IRFU, IPHC) and comparable team for test
1 MPW run and 5 engineering runs 2012-2016, production 2017-2018

ALICE Inner Tracker System 2 (ITS2) taking data



ITS 3 upgrade: replace 3 inner layers with wafer scale stitched sensors[1]

(1) https://indico.cern.ch/event/1071914, *ALICE ITS3 – a next generation vertex detector based on bent, wafer-scale CMOS* sensors, Magnus Mager (CERN)
(1) https://cds.cern.ch/record/2703140/files/LHCC-I-034.pdf - *Letter of Intent for an ALICE ITS Upgrade in LS3*

ALICE

R&D for monolithic active pixel sensors

CERN EP R&D WP 1.2 targets the development of monolithic CMOS sensors for future HEP detectors in sub-100 nm technologies to achieve smaller pixel pitch, higher data rate, increased radiation tolerance and fabrication of wafer-scale sensors on 300 mm wafers.

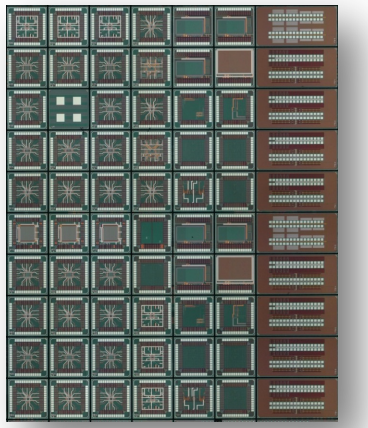
The first technology retained is the TPSCo 65 nm, and significant development in this technology was carried out in collaboration with the ALICE experiment for the upgrade of its inner tracking detector ITS3.

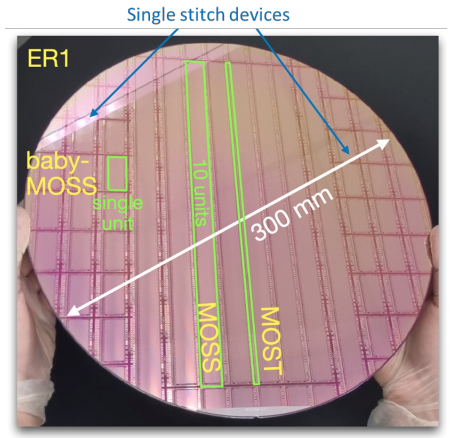
Main goals and activities:

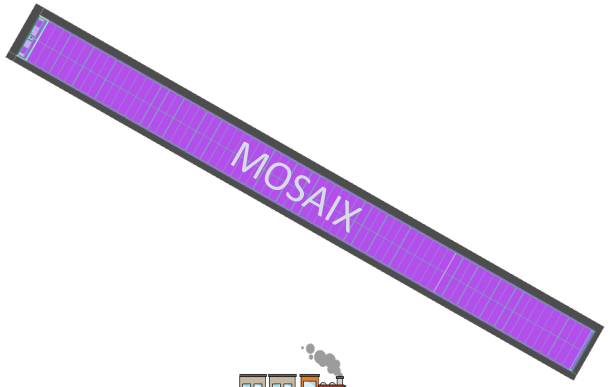
- Design of wafer-scale stitched sensor (application for ALICE vertex detector, ITS3)
- Investigate new concepts for CMOS sensors:
  - Porting of hybrid pixel detector architecture into monolithic (hybrid to monolithic H2M)
- Performance optimization for future applications
  - Fast timing
  - Low power
  - Radiation tolerance
- Provide support and access to TPSCo 65 nm ISC imaging technology (and TJ 180nm IS and LF 110nm IS)
  - Continued in DRD7.6a (workshop September 10th last year https://indico.cern.ch/event/1436991/)
  - DRD7.6a session: https://indico.cern.ch/event/1582781/ (Sept 23)
  - DRD7 plenary: https://indico.cern.ch/event/1556239/ (Sept 24-26)

CERN EP R&D day May 7th: https://indico.cern.ch/event/1524303/overview

Timeline







MPR2

Shared engineering run

WP 1.2 "rail"

ALICE "rail"

MLR1 (Multi-Layer Reticle, Dec 2020):

Learn about the technology, process optimization, characterize pixels, transistors and building blocks

1.5 x 1.5 mm^2 test chips

>50 chiplets from: DESY, IPHC, RAL, NIKHEF, CPPM, Yonsei, CERN

ER1 (Engineering Run, Dec. 2022):

Prove we can design wafer-scale stitched sensors

MOSS (1.4 x 25.9 cm)

MOST (0.25 x 25.9 cm)

Hybrid-To-Monolithic (H2M)

51 chiplets from: DESY, IPHC, RAL, NIKHEF, SLAC, INFN, CERN

ER2 (08/2025):

Full-scale stitched sensor prototype for ITS3

MOSAIX (1.9 x 26.6 cm)

~30 chiplets from: IPHC, SLAC, CPPM, BNL, INFN, Universität Heidelberg, CERN

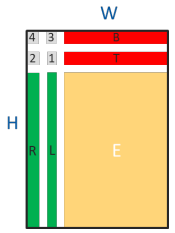
ER3 (2026):

Stitched sensor production for ITS3 (ALICE-specific)

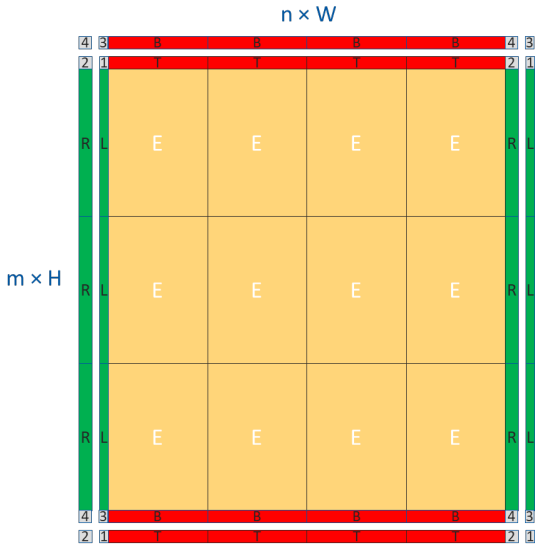
ER1: learning stitching and handling procedures

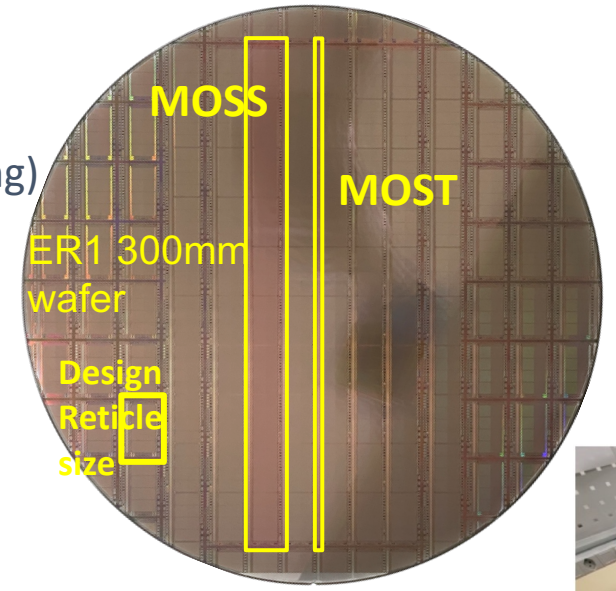
- Two wafer-scale stitched sensor chips
  - MOSS (Monolithic Stitched Sensor)
  - MOST (Monolithic Stitched Sensor with Timing)

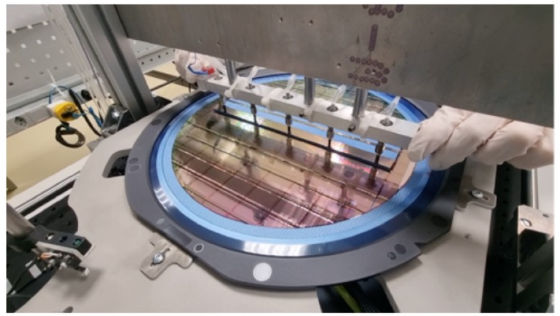
Design Reticle (typ. 2x3 cm)

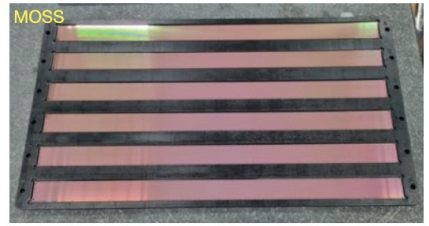


Stitched circuit on wafer

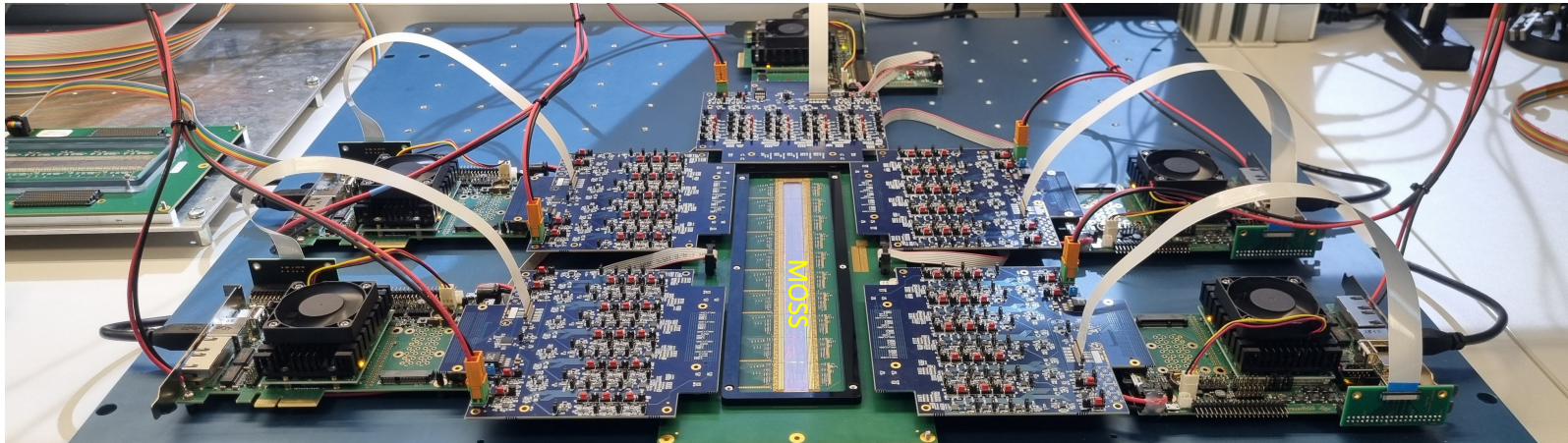








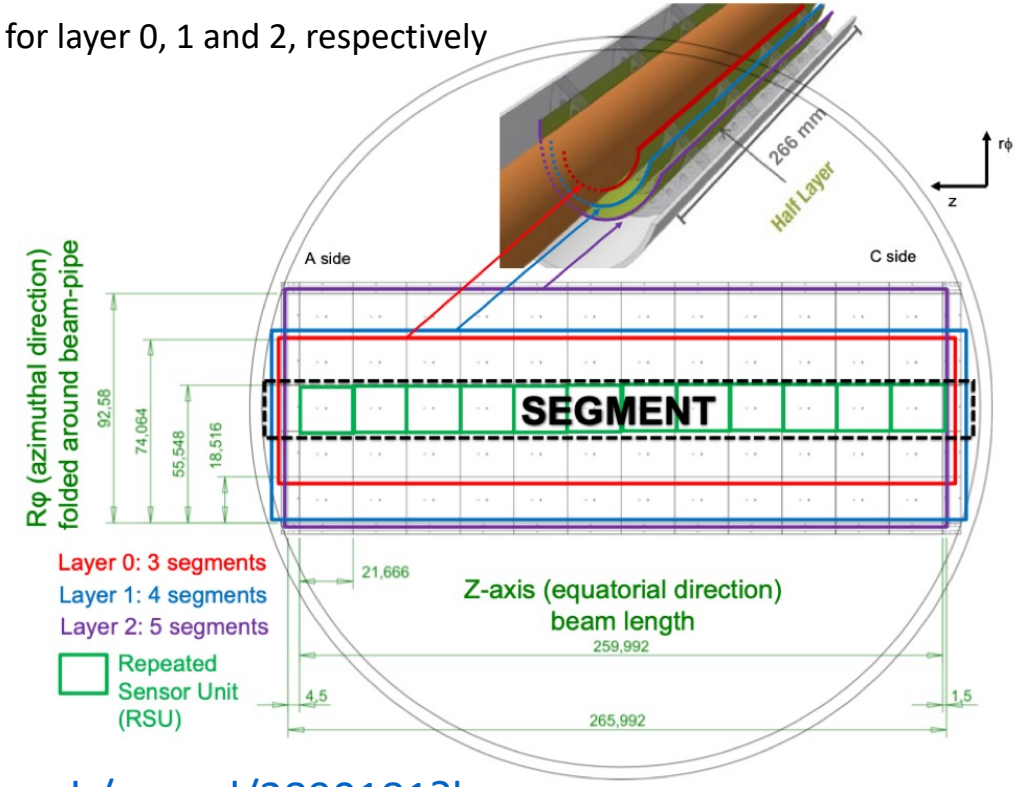
- Lots of learning on chip handling
- Several small test chips (1.5 mm × 1.5 mm)
  H2M, PLL, pixel prototypes, fast serial links, SEU test chips, …

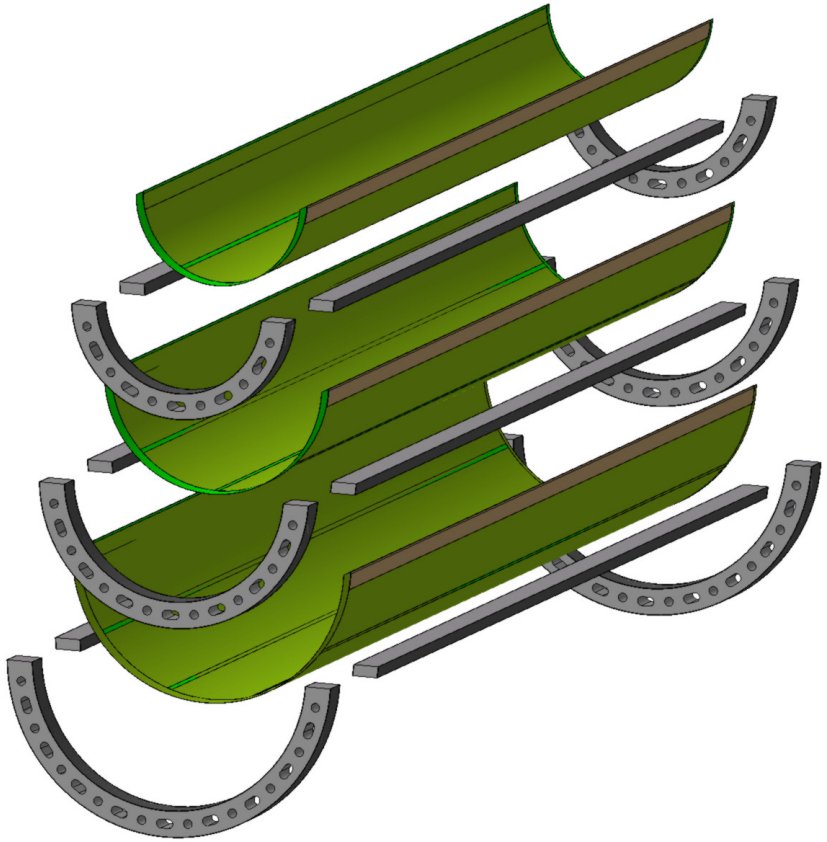


MOSAIX for the ALICE ITS3 upgrade

MOSAIX chip was just submitted (mask making in progress)

- 12 repeated sensor units
- Learnings from MOSS and MOST on stitching are fed back into the design
- Use power switches with power granularity from 20 in MOSS to 144 per segment here
- 3, 4 and 5 segments for layer 0, 1 and 2, respectively



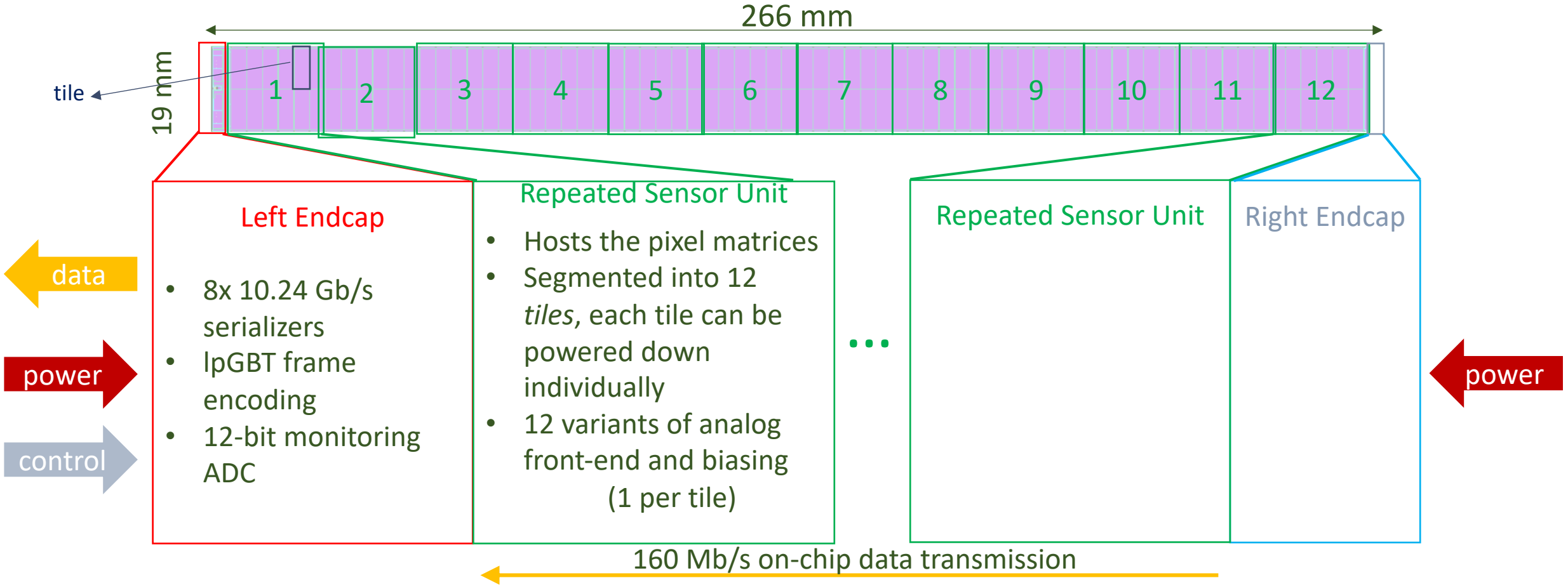


ITS3 TDR: https://cds.cern.ch/record/2890181?ln=en

MOSAIX (Monolithic Stitched Active pIXEL) SYSTEM ON CHIP

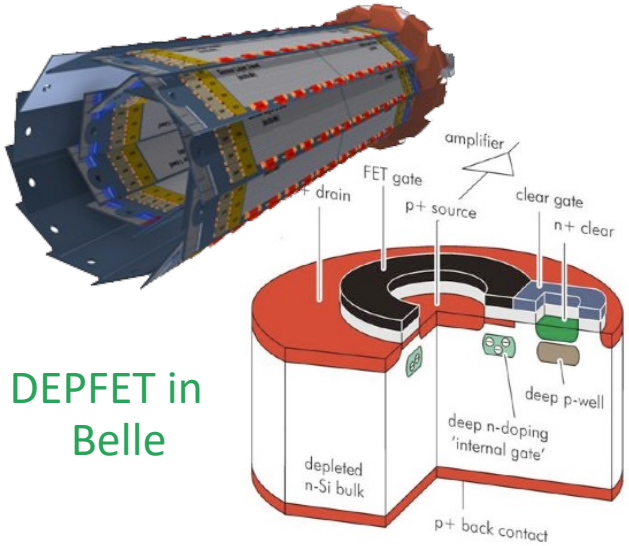
MOSAIX is the full-size, full-functionality, stitched sensor prototype for ALICE ITS3. 22.8 x 20.8 µm pixels, 9.97 Mpixels. MOSAIX inherits some of its features from MOSS (synchronous read-out, conservative layout) and MOST (power segmentation, data transmission on chip), but it includes many more complex functionalities. Attention to YIELD

Unprecedented level of integration and complexity in HEP

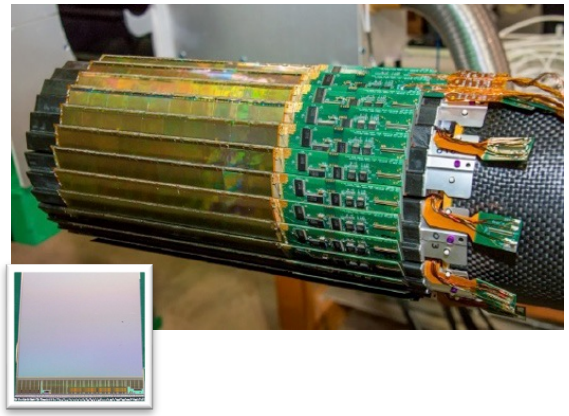


[9] P. Vicente Leitao. "Development of the MOSAIX chip for the ALICE ITS3 upgrade". In: Topical Workshop for Electronics in Particle Physics (Glasgow, September 2024).

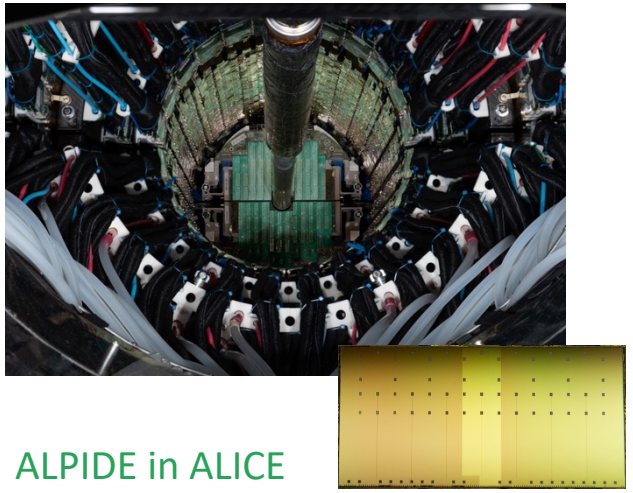
Monolithic sensors in HEP move into mainstream CMOS technology



DEPFET in Belle

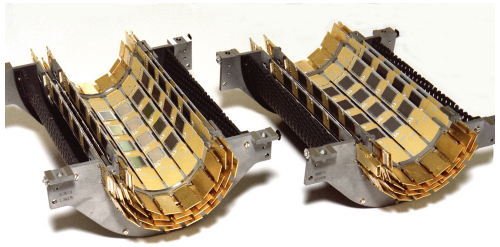


MIMOSA28 (ULTIMATE) in STAR
IPHC Strasbourg
First MAPS system in HEP
Twin well 0.35 µm CMOS



ALPIDE in ALICE
First MAPS in HEP with sparse readout similar to hybrid sensors
Quadruple well 0.18 µm CMOS
- Integration time <10 µs
- Reverse bias but no full depletion -> NIEL ~10^{14} 1 MeV n_{eq}/cm^2

DEPLETED MAPS for better time resolution and radiation tolerance
Large collection electrode
LF Monopix, MuPix, Monolith…
Extreme radiation tolerance and timing uniformity, but large capacitance
Small collection electrode
ARCADIA LF, TJ Malta, TJ Monopix, Fastpix, CLICTD, ALICE ITS3…
- Sub-ns timing
- NIEL >10^{15} 1 MeV n_{eq}/cm^2 and beyond

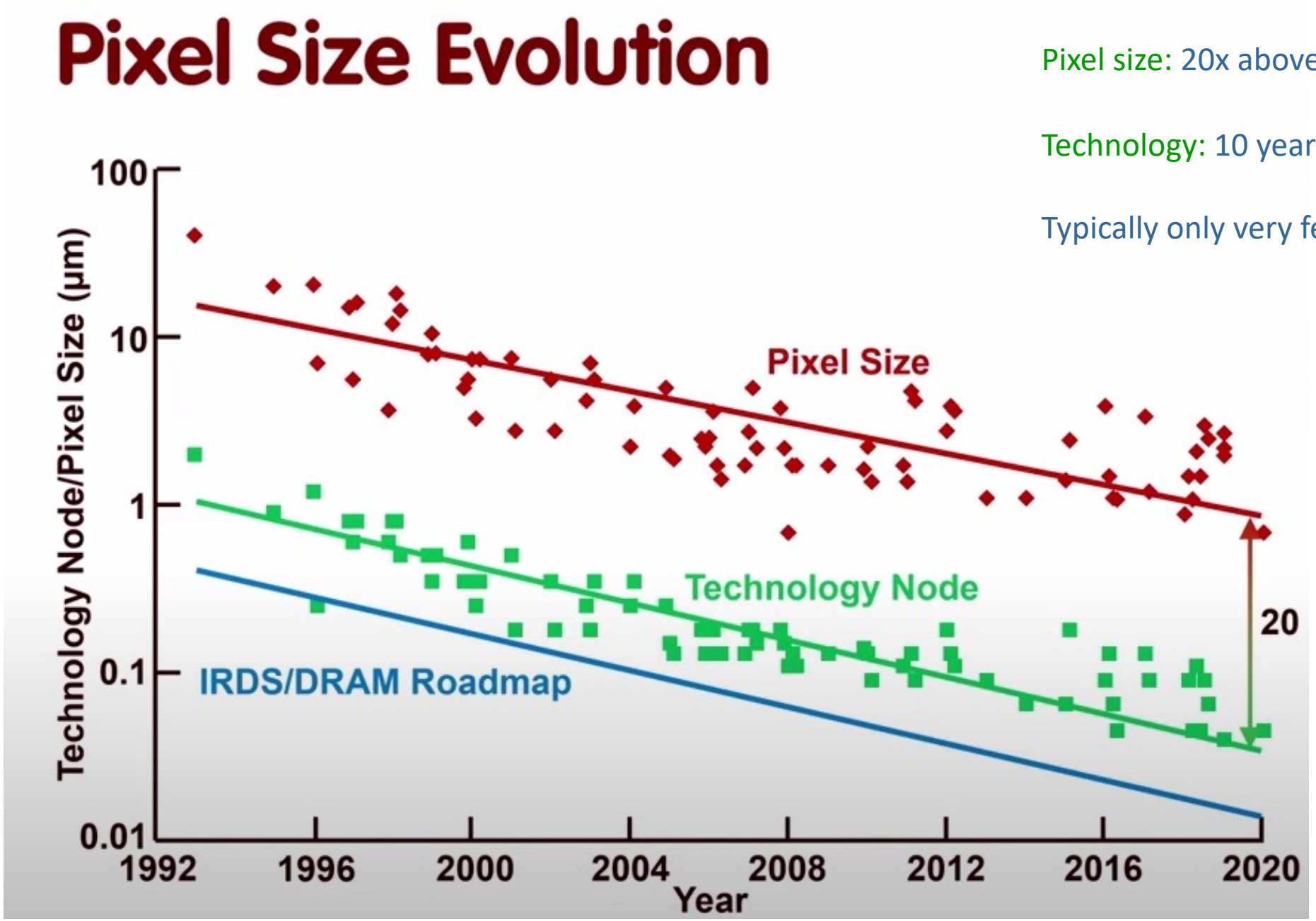


CCDs in SLD detector at SLAC, C. Damerell et al.

Other developments: See also backup slides and EP detector seminar (https://indico.cern.ch/event/1461789/)

Commercial deep submicron CMOS technology evolved "naturally" towards
- Very high tolerance to ionizing radiation, some caveats, cfr G. Borghello, F. Faccio, requires extensive irradiation campaigns
- Availability of substrates compatible with particle detection
- Imaging technology not required, but some flexibility/features very beneficial for sensor optimization, both for small and large collection electrode structures.

Evolution of pixel size and technology node for standard visible imaging:



Pixel size: 20x above technology feature size

Technology: 10 years behind DRAM technology

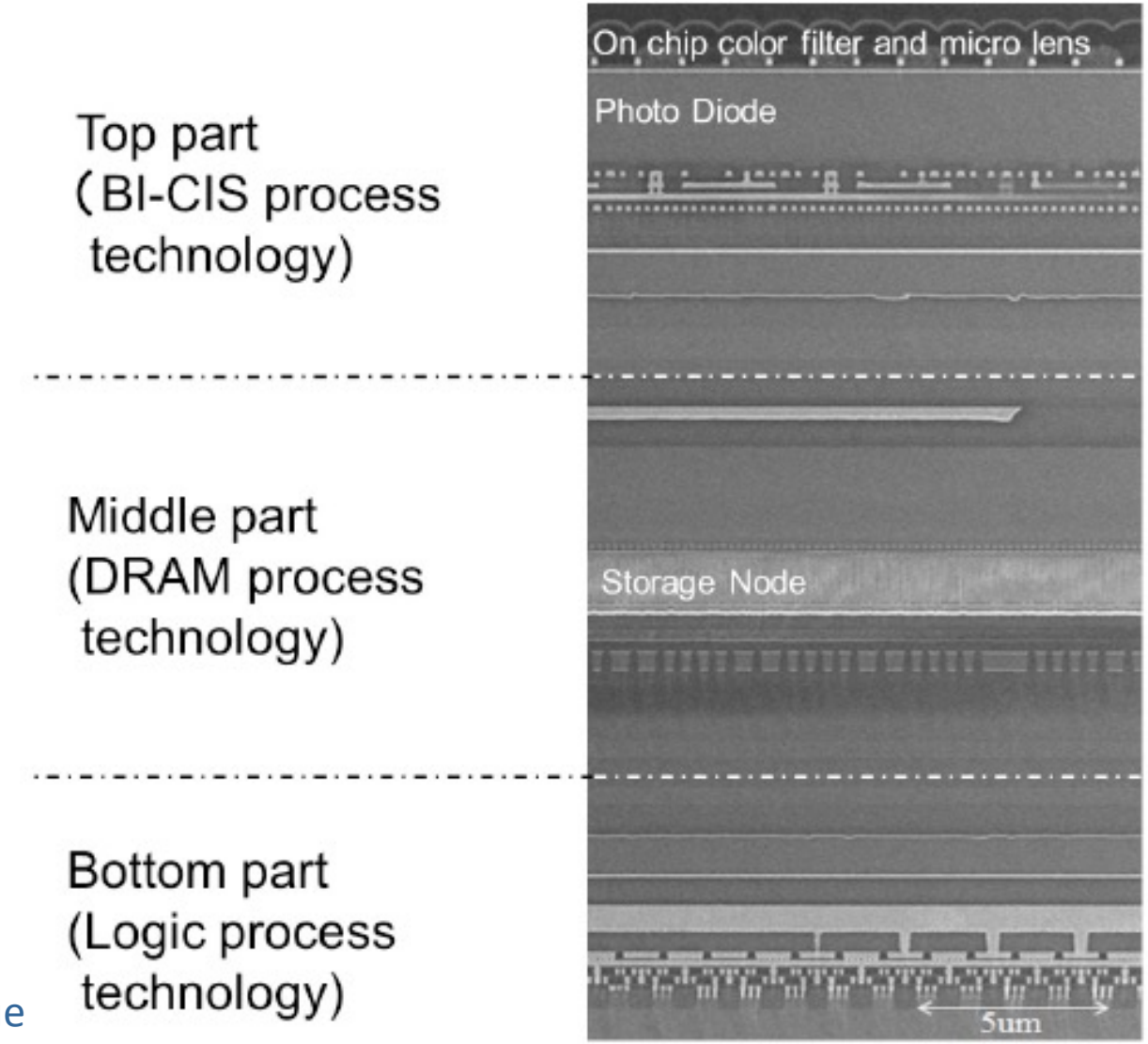
Typically only very few (1-4) transistors per pixel

Albert Theuwissen, ISSCC 2021

CMOS Monolithic Active Pixel Sensors revolutionized the imaging world

reaching:

- less than 1 e^- noise
- > 40 Mpixels
- Wafer scale integration
- Wafer stacking
- …



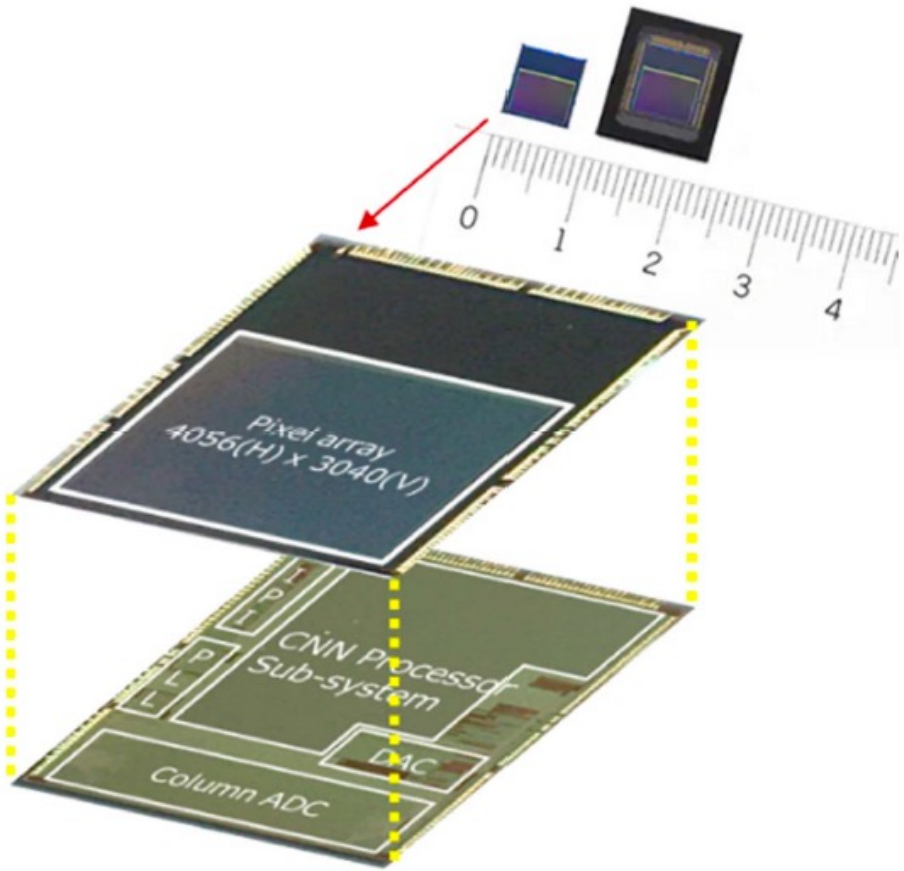
Sony, ISSCC 2017

Wafer stacking now offered by several foundries !

The distinction between hybrid and monolithic becomes more vague

Stacking does not imply significant thickness increase !!

Sony: Intelligent Vision Sensor and Edge Computing Envisage the Future

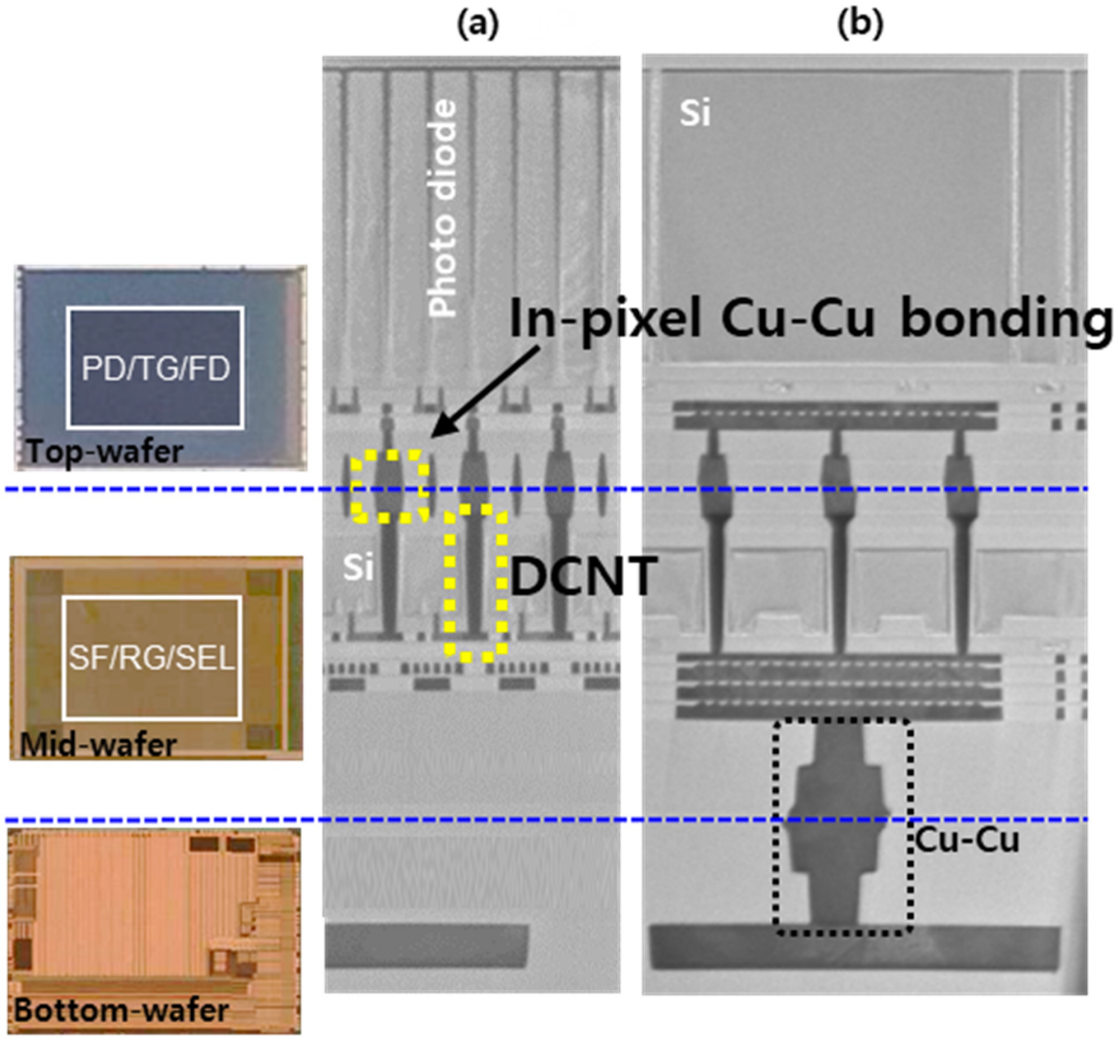


Fabrication Process		Top chip 65nm / Bottom chip 22nm
Chip size		7.558mm(H) x 8.206mm(V)
Number of effective pixels		4056(H) x 3040(V)
Image size		Diagonal 7.857 mm
Pixel size		1.55μm(H) x 1.55μm(V)
Supply voltage		Pixel and Analog 2.6V/Interface 1.7V/Logic 0.8V
Input clock		12~27MHz
Output I/F	Option1	MIPI(CSI-2) 4 lane DPHY 2.1Gbps/lane
	Option2	SPI 35Mbps
DSP	Number of MACs	2304MACs
	Peak Power efficiency	4.97TOPS/W
	Processor Clock	262.5MHz
Sensor Readout time	12.3M[4056(H)x3040(V)]	16.52msec
	3.1M [2028(H)x1520(V)]	5.52msec
Power consumption	12.3M[4056(H)x3040(V)] 30fps	278.8mW
	3.1M [2028(H)x1520(V)] 120fps	379.1mW
Image output format	Sensor	Bayer RAW
	Input tensor	RGB or YUV

Fig. 1 A photo of the intelligent vision sensor in stacked architecture with a pixel chip and a logic chip.

- Stacked device with neural network for image recognition
- Discusses different architectures of Neural Networks for this application, outperforms traditional imagers for image recognition.

Samsung: A 0.5 µm Pixel 3-layer Stacked CMOS Image Sensor with Deep Contact and In-pixel Cu-Cu Bonding 40.1 IEDM 2023



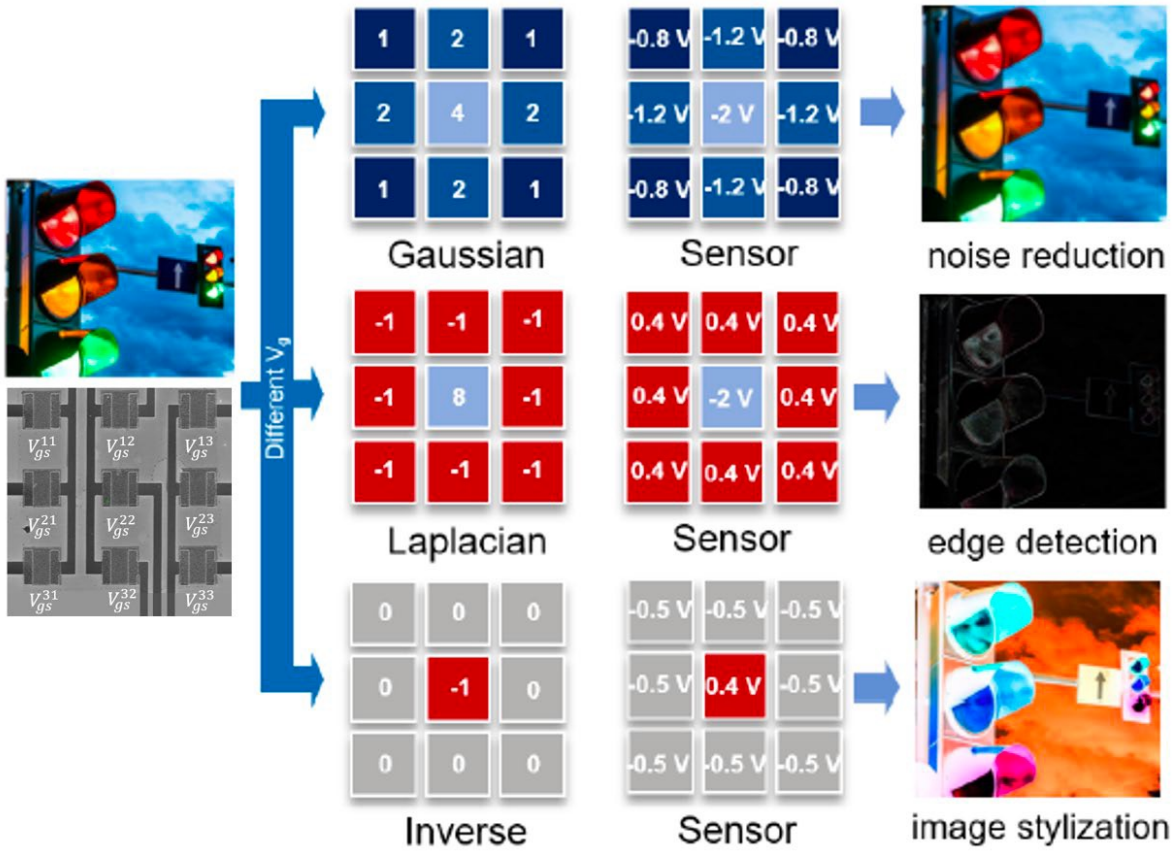
- Top tier Photo diode and Transmission Gate
- Middle tier in-pixel transistors
- Bottom Analog and digital CMOS

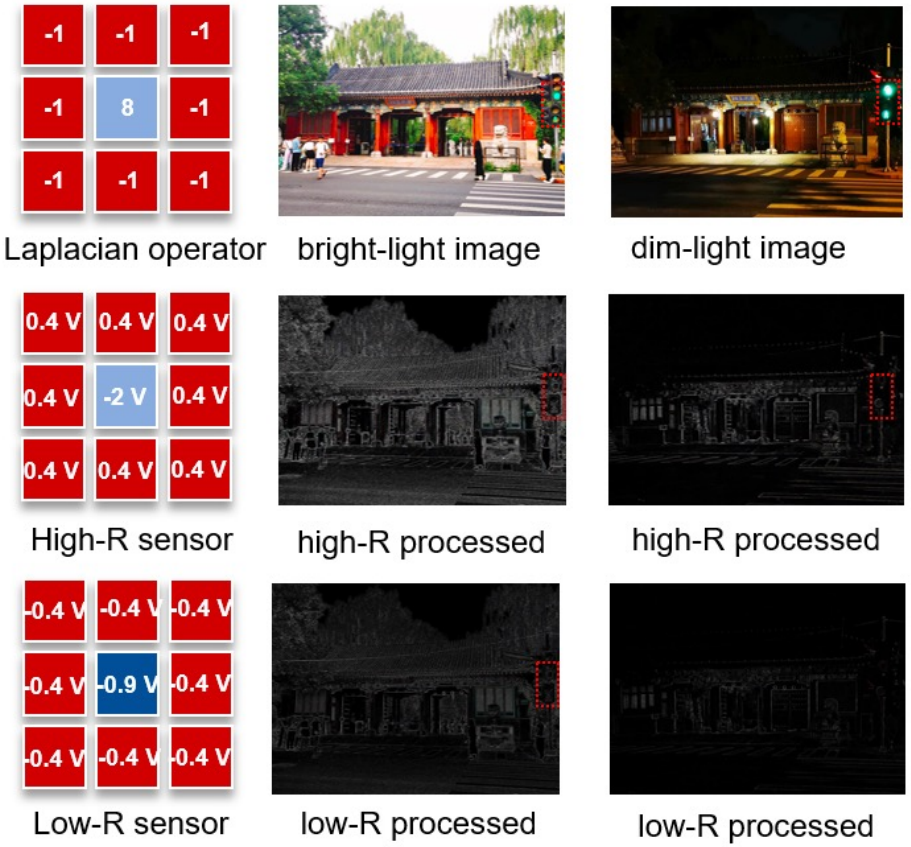
- (a) Pixel array (b) periphery

Wafer stacking and Artificial Intelligence more and more widespread in commercial imaging !

Peking University: Ultrasensitive Retinomorphic Dim-light Vision with In-Sensor Convolutional Processing Based on Reconfigurable Perovskite Bi_2O_2Se Heterotransistors 33.3

IEDM 2023



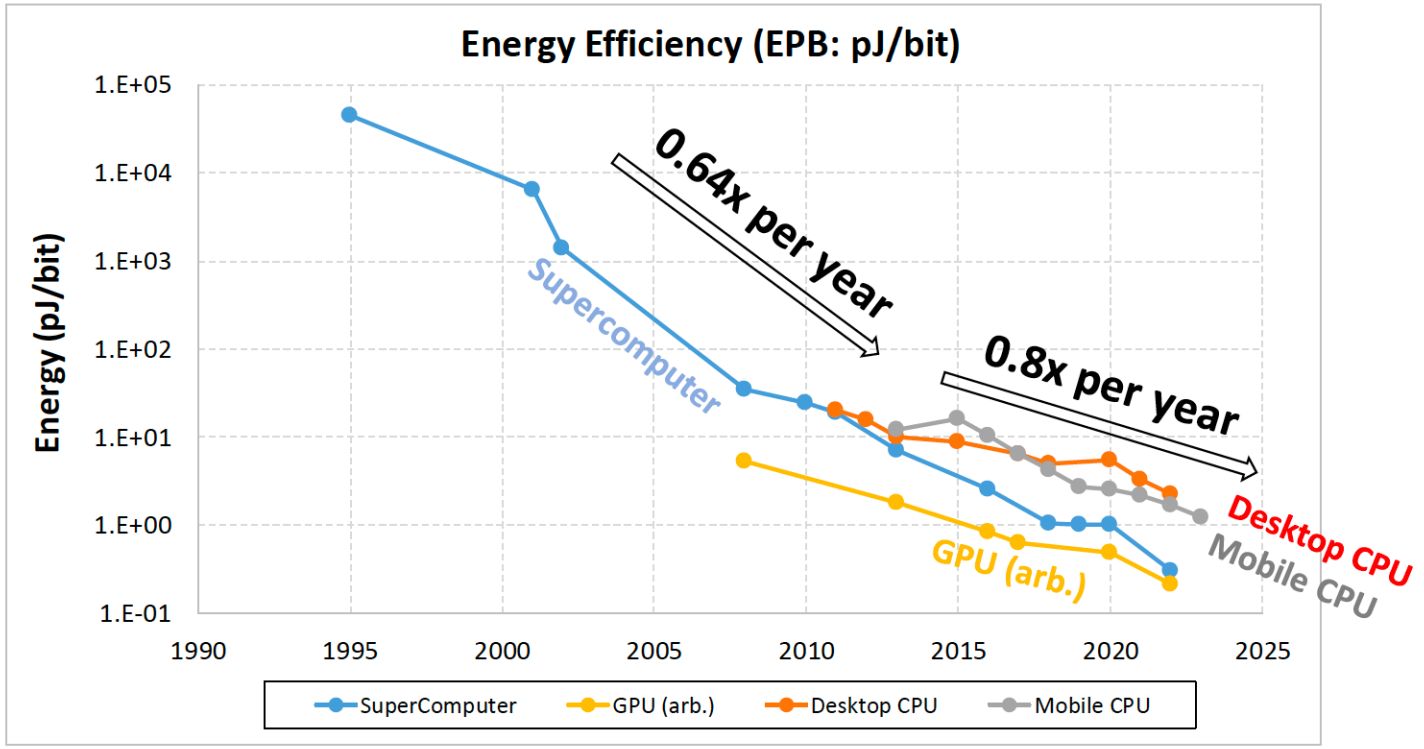


- Can modulate the photo-responsitivity with voltage, and can use this for convolution operations and in-sensor compute, for applications like noise-reduction, edge detection and other purposes.

CMOS Imaging technologies vs mainstream technologies

- Wafer stacking well established in commercial imaging sensors
- Artificial Intelligence enters for enhanced performance and in sensor compute

- How about mainstream technologies ? (we do not necessarily need an imaging technology…)
  - Pushed by computing needs for artificial intelligence.
  - Computing enhancement power limited
  - Needs addressed by:
    - Transistors
    - On-chip interconnect
    - Heterogeneous integration
    - In-memory compute



Jie Deng Qualcomm
IEDM 2023

Transistor: Finfet is running out of steam, replaced by Gate All Around

- Gate All Around (GAA) faster, more current drive, and more uniform
- All major players are moving to GAA, eg IEDM 2023
- Even moving to stacked nanosheet and PMOS and NMOS

PMOS and NMOS can even be stacked from different wafers

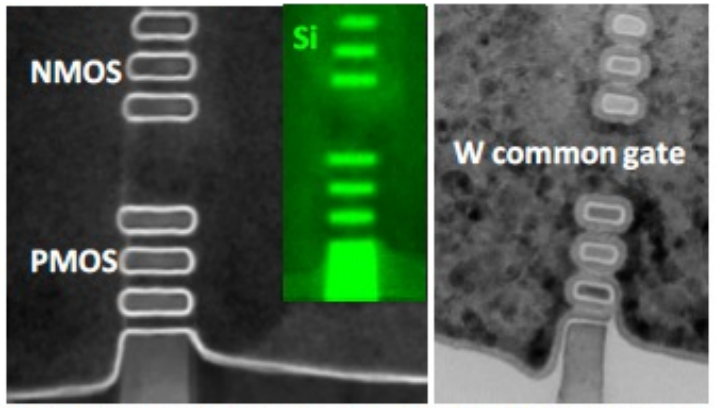
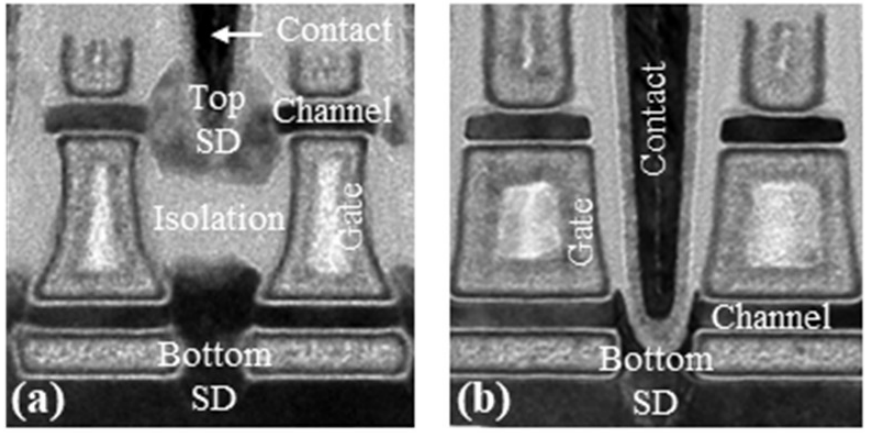
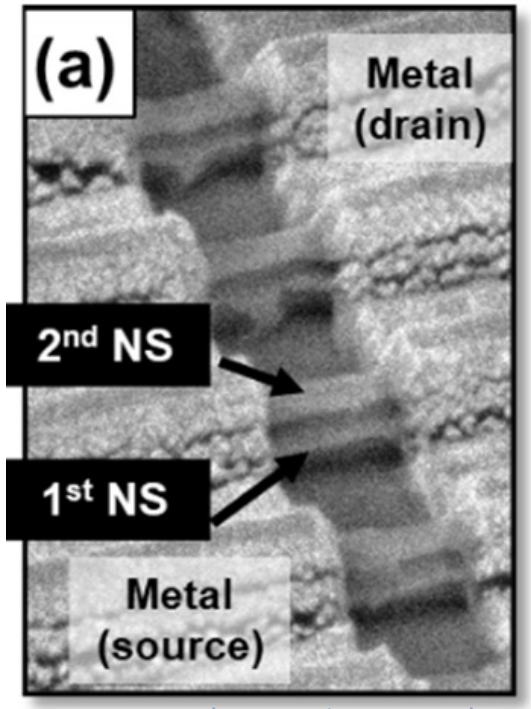


Fig. 5. TEM micrograph shows CFET device after ribbon release on the left demonstrating capable process despite high aspect ratio. TEM micrograph on the right is captured after common-gate fill and polish, showing that the gates of top n-MOS and bottom p-MOS are connected.

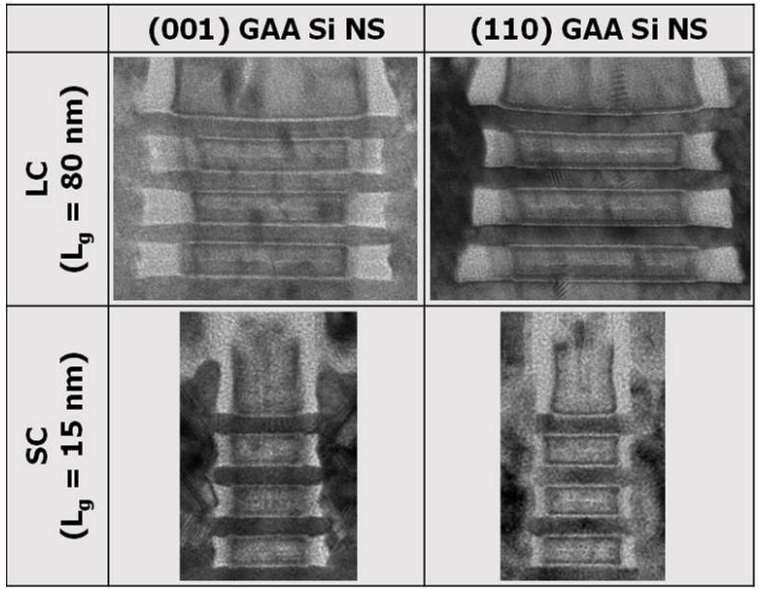
Intel 29.2



Samsung 29.4
Stacked NMOS and PMOS



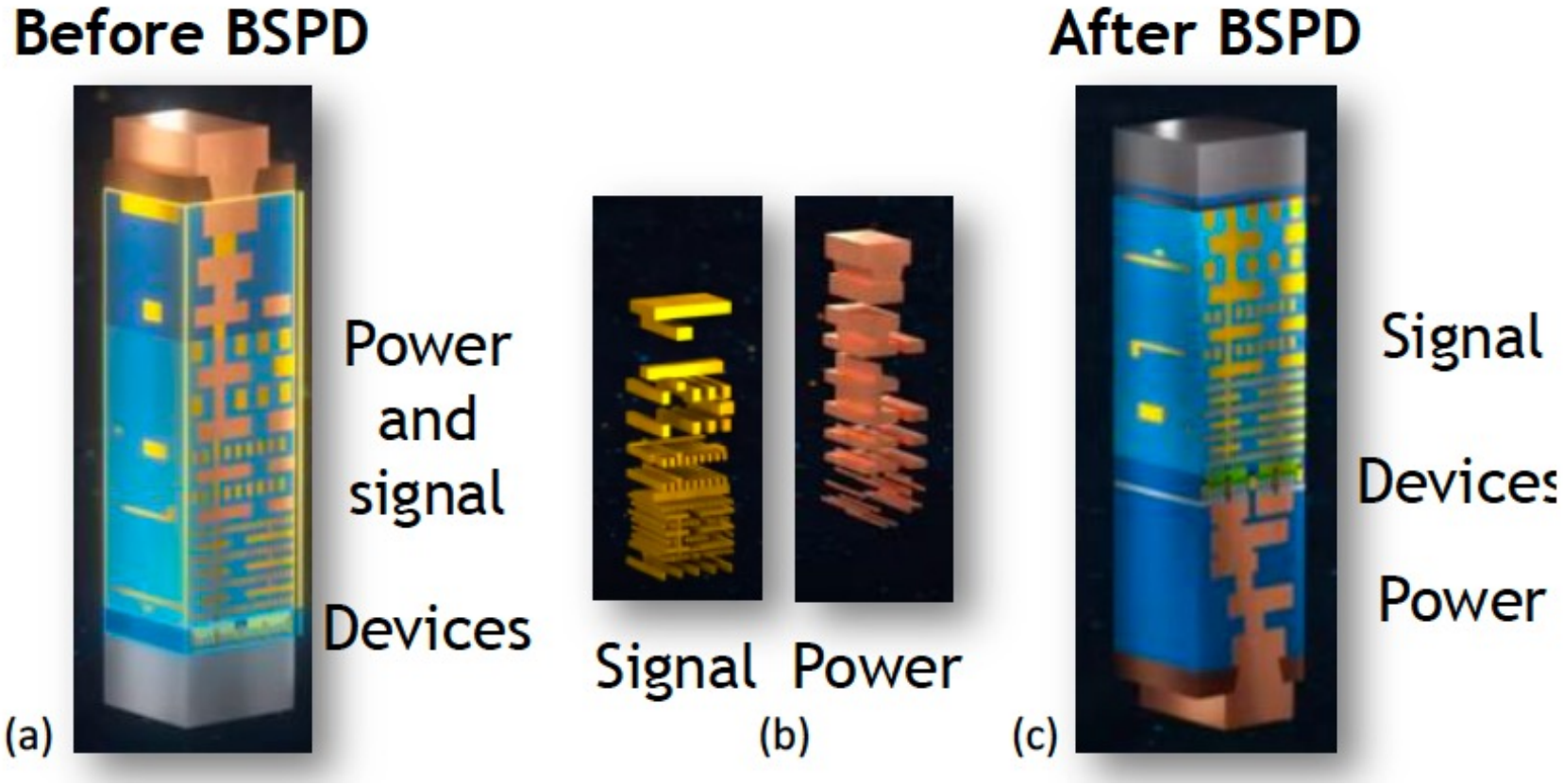
TSMC 2.1
Channel width 50 nm
length 150 nm

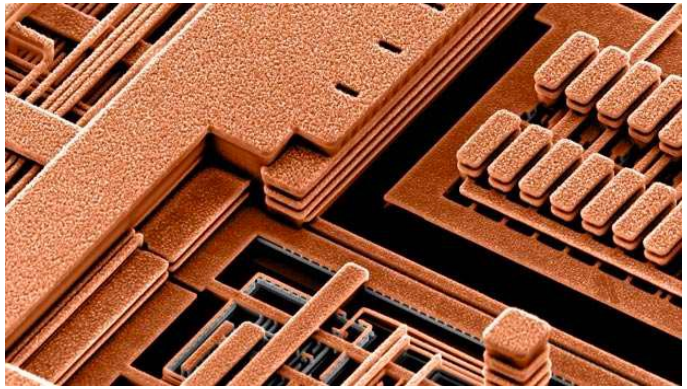


IBM research
2.5

IEDM 2023

Intel: Process innovations for future technology nodes with back side power delivery network and 3D device stacking. 19.1 IEDM 2023



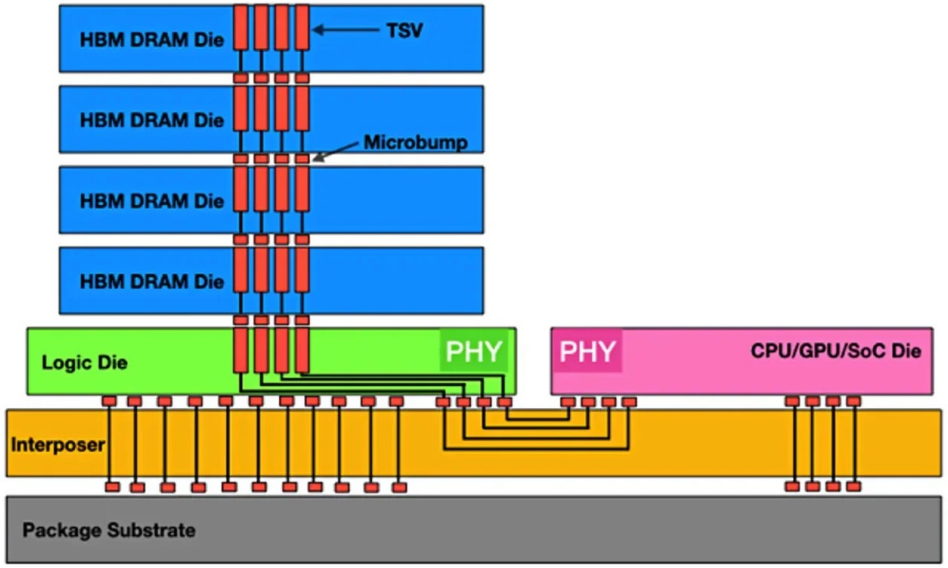


D. Edelstein et al. IEDM 1997

- One shot improvement after Cu introduced by IBM in 1997
- Lower cost, less scaling for same performance, more flexibility …
- Expect ultimately also to route signals on the back side…

Heterogenous integration

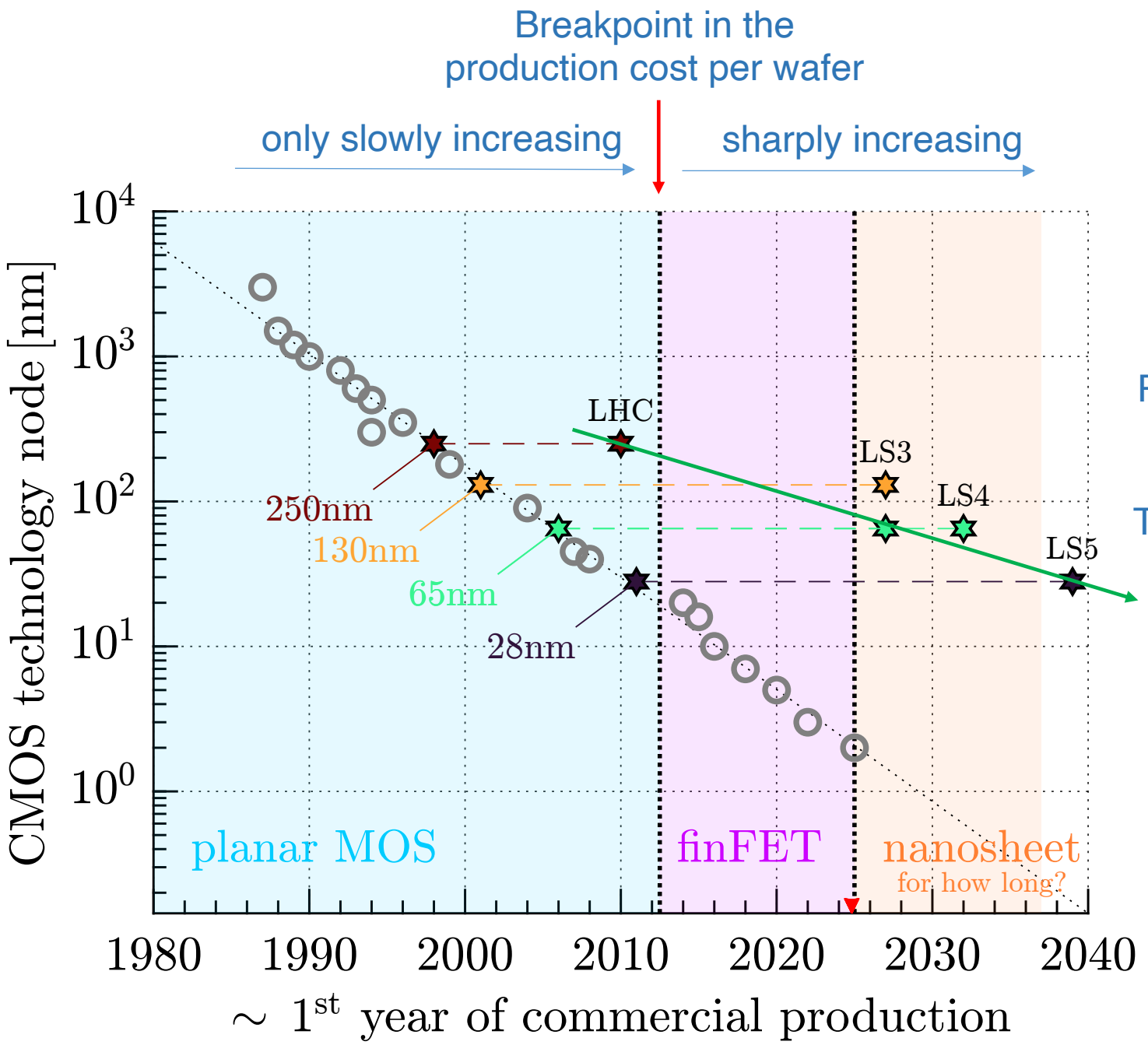
- Transistor cost scaling (0.7x) per generation down to 28 nm, and then much flatter from one generation to the other.
- Memory, logic and analog scale differently (logic size scales, but this is much less the case for analog (often almost constant area) and memory
- Cost benefit from density scaling therefore diminishes. Therefore pushing for alternate design strategies enabled by 2.5 and 3D integration, wafer stacking, chiplets, etc.



HBM High Bandwidth Memory

Source: semiengineering

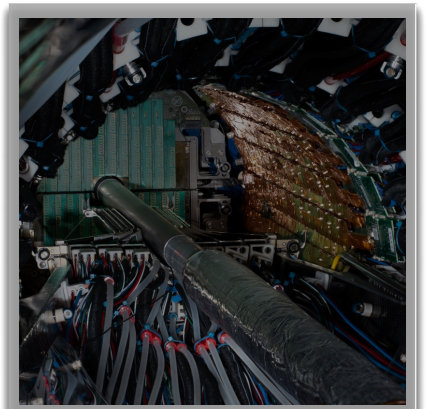
Mainstream goes 2.5, 3D, potentially also very relevant for HEP !

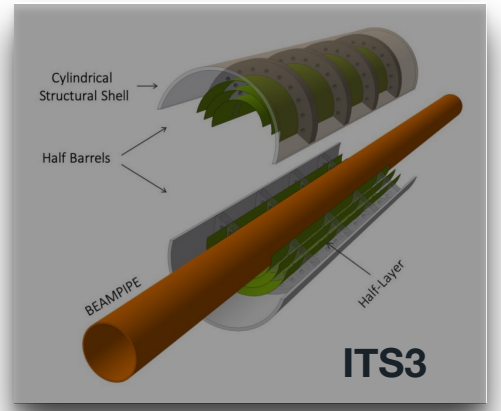


Production cost per 300 mm wafer relatively flat until reaching finFET

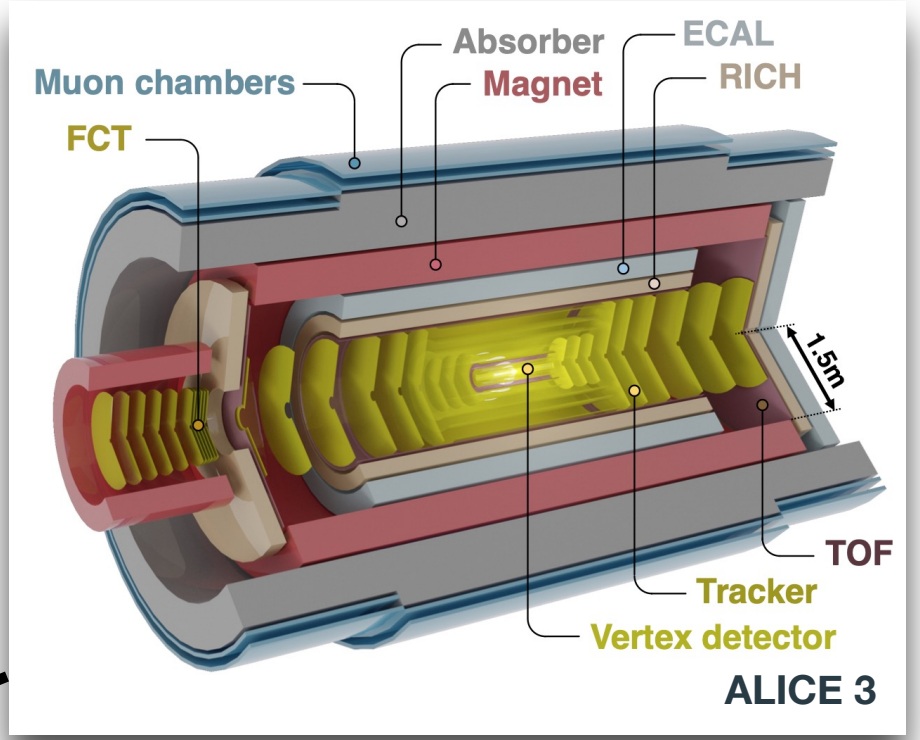
The gap between state-of-the-art technology and what we use for HEP is increasing.

ALICE 3


ITS 2



ITS3



ALICE 3

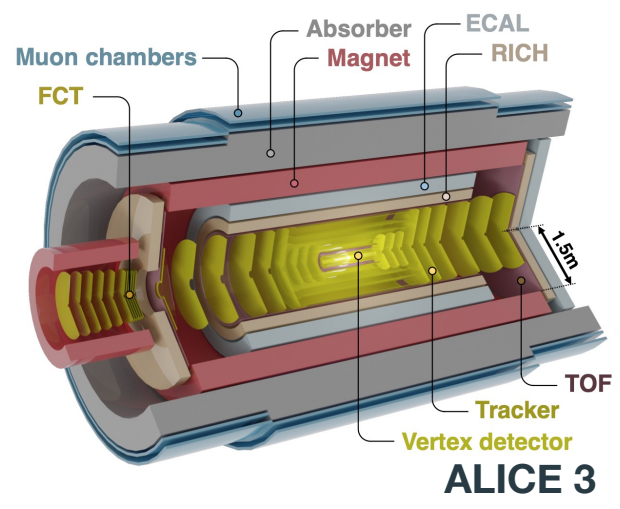
Today

ALICE 2 | ALICE 2.1 | ALICE 3

LHC Run 3 | LHC LS3 | LHC Run 4 | LHC LS4 | LHC Run 5 | LHC LS5 | LHC Run 6

2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037 2038 2039 2040 2041

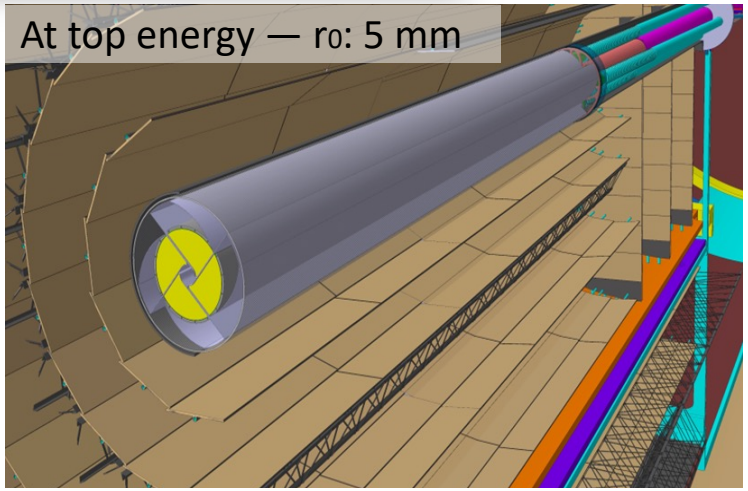
ALICE 3:



Detector concept

https://arxiv.org/pdf/2211.02491.pdf

- Compact, low-mass all-silicon tracker
- Retractable vertex detector
- Excellent vertex reconstruction and PID capabilities
- Large acceptance
- Super conduction magnet system
- Continuous readout and online processing



Vertex detector: key characteristics

- 3 detection layers
- Retractable: r_0 = 5 mm
- Material budget: 0.1% X0 / layer
- Spatial resolution 2.5 µm

main R & D challenges

- 10 µm pixel pitch
- Hit rate in the inner layer 1 MHz/mm^2 for a 50 cm barrel
- Tolerant to 10^{16} 1 MeV n_{eq}/cm^2 + 300 Mrad (numbers to be reviewed)
- Light-weight in-vacuum mechanics and cooling

Specifications of tracker/vertex detector very similar/equivalent to those of FCCee, except at higher radiation levels.
Ideal as a stepping stone towards an FCCee detector.

Off-detector transmission:

ISSCC 2013 / SESSION 2 / ULTRA-HIGH-SPEE

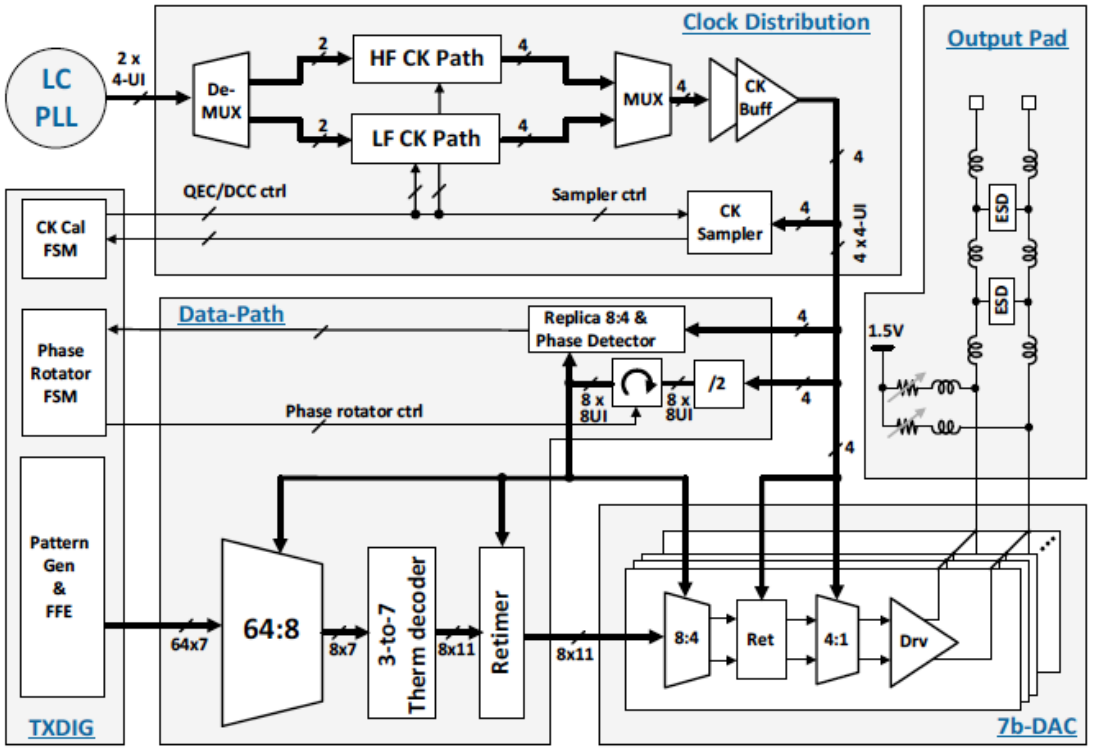
2.6 A 32-to-48Gb/s Serializing Transmitter Using Multiphase Sampling in 65nm CMOS

Amr Amin Hafez, Ming-Shuan Chen, Chih-Kong Ken Yang

University of California, Los Angeles, CA

Block	Power (mW)	Fraction (%)
VCO	26.6	30.2
Divider Chain	18	20.5
Buffer/PFD/CP	2	2.3
Predriver/Driver	26.4	30
Serializer	15	17
Total	88	100

INTEL, ISSCC2021, 224Gbps, PAM-4, 1.7 pJ/bit, 10 nm technology



State of the art: a few mW/Gbps, already earlier but also now at much higher bandwidths

Significant circuit complexity

For HEP important penalty for SEU robustness due to triplication/larger devices…

Important: data concentration, physical volume for material budget, and technology

Perspectives for future HEP detectors

- For ‘monolithic’ CMOS sensors for visible light 3D wafer stacking, and artificial intelligence within the imagers become more widespread
- Mainstream CMOS technology is driven by system and computing needs related to Artificial Intelligence:
  - Transistor optimization goes 3D, back side power delivery, heterogenous integration, in-memory compute
  - Device and Technology Co-Optimization (DTCO) & System and Technology Co-Optimization (STCO) required to meet the challenges
  - Smaller feature size for the sensor wafer could bring deeper sub-fF sensor, smaller pitch and easier sensor depletion
- MLR1, ER1 and ER2 experience crucial to learn about the technology, stitching, powering, and also yield.
- Clear path for sensor and front-end improvement in non-stacked 65 nm ISC
- 2-layer wafer stacking will increase cost, but not the thickness, could stack 65 nm sensor to a 28 nm readout.
- A smaller pixel pitch, and increased reverse bias, are also very beneficial for sensor radiation tolerance.

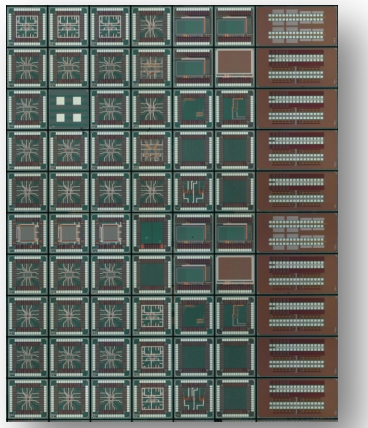
Challenges and opportunities for ALICE3 and other future HEP detectors

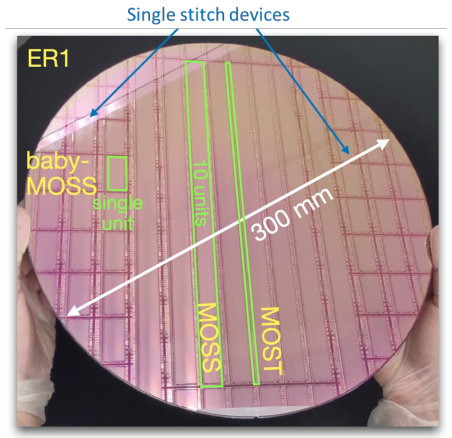
- 3D wafer stacking now allows the connection of a readout wafer to a detector wafer, and deliver the fully finished diced assemblies to the customer. This reduces the distinction with hybrid sensors, but provides opportunities well beyond with multiple connections within each pixel and stacking of even more than two wafers.

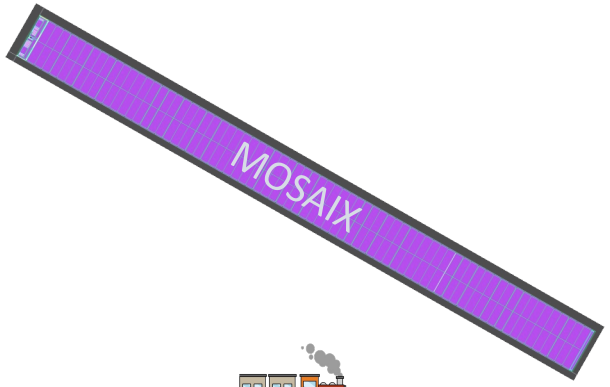
- Outer layers:
  - Volume in HEP is in the outer layers. Foundry can deliver wafers at very high volume. How do we take advantage of the technology trends to construct large areas in an efficient way using standard processes, so volume production, test, assembly and mounting?
  - Stitched vs non-stitched?
  - ~ 10 mW/cm^2 = 10 nW/(10 µm x 10 µm pixel) = 1 W/(10x10 cm^2) (pixel pitch may be higher in the outer layers)
  - Need efficient data concentration in the outer layers as hit rates drop significantly.

- Inner layers:
  - power density order of magnitude larger
  - Increased data rates O(10 Gb/s/cm^2) are a significantly constraint: need a small form factor and optimization for low power consumption. (-> chiplets, Si-photonics, opto-electronics…)

Timeline







MLR1 (Multi-Layer Reticle, Dec 2020):

Learn about the technology, process optimization, characterize pixels, transistors and building blocks

ER1 (Engineering Run, Dec. 2022):

Prove we can design wafer-scale stitched sensors

ER2 (08/2025):

Full-scale stitched sensor prototype for ITS3

MOSAIX (1.9 x 26.6 cm)

MPR2

Shared engineering run

WP 1.2 "rail"

ALICE "rail"

ER3 (2026):

Stitched sensor production for ITS3 (ALICE-specific)

Future runs -> MPR2 and ER3 (2026)

Also sensor prototypes on ER2.

- > to be discussed.

Perspectives for ALICE3 and other future HEP detectors

- Not only CMOS imaging technologies, but also mainstream CMOS and assembly technologies evolve fast, in directions very relevant for ALICE 3 and other future HEP detectors

- Profiting from this:
  - assembly techniques need to help us to construct large area detectors more efficiently
  - may significantly improve physics and sensor performance, especially for the inner layers
  - exploration and development will be more costly financially and in terms of workforce
  - may be worth it and presents an opportunity to reduce the gap between HEP and state of the art technology.

Perspectives for ALICE3 and other future HEP detectors

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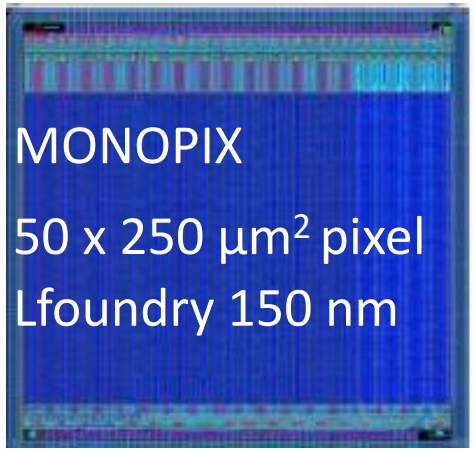
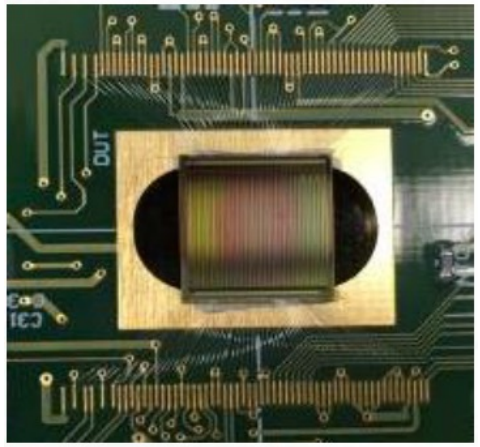
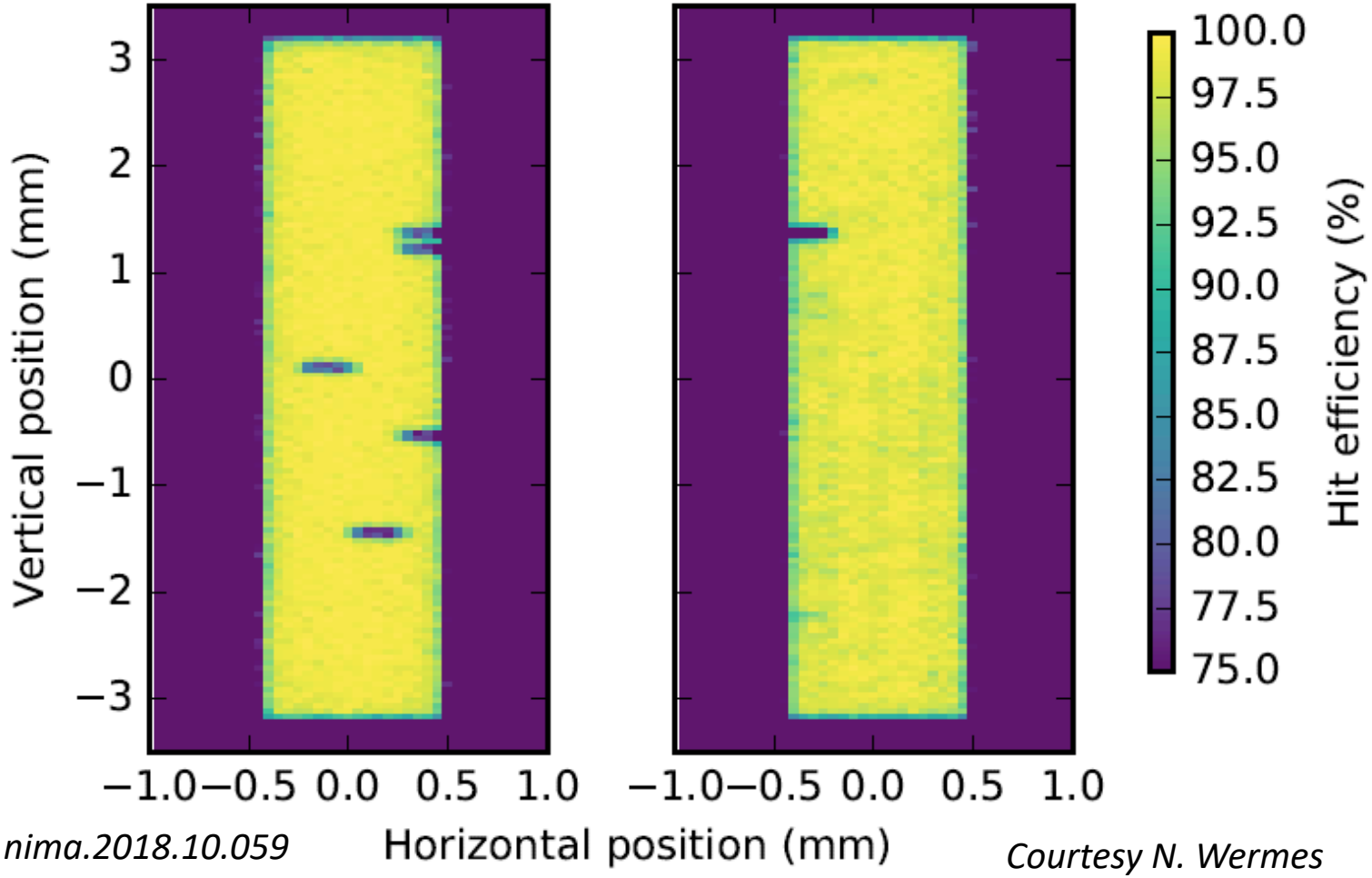
Thank you !

Other monolithic sensor developments for HEP

Better sensor radiation tolerance and timing: Large collection electrode: rad hard, but large C (100fF or more)







T. Hirono et al., https://doi.org/10.1016/j.nima.2018.10.059

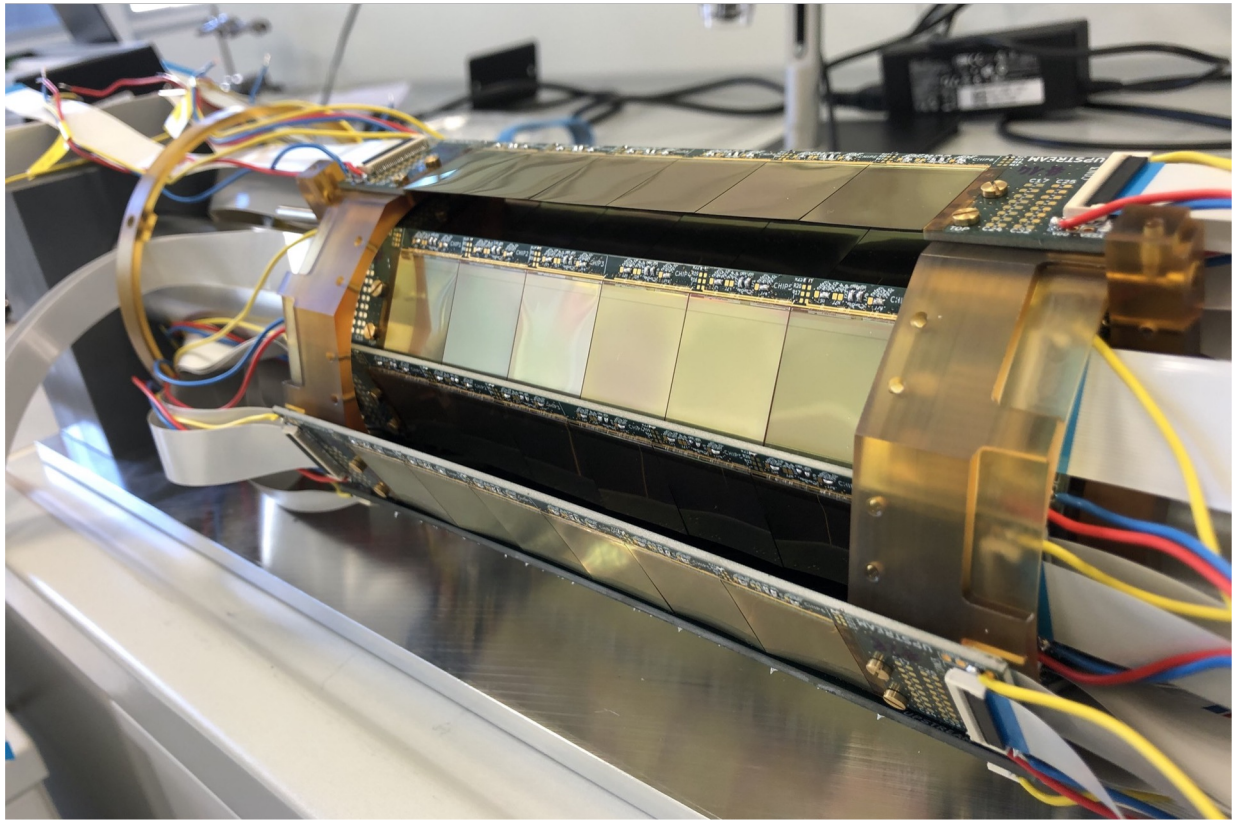
Courtesy N. Wermes

Other developments in same technology:

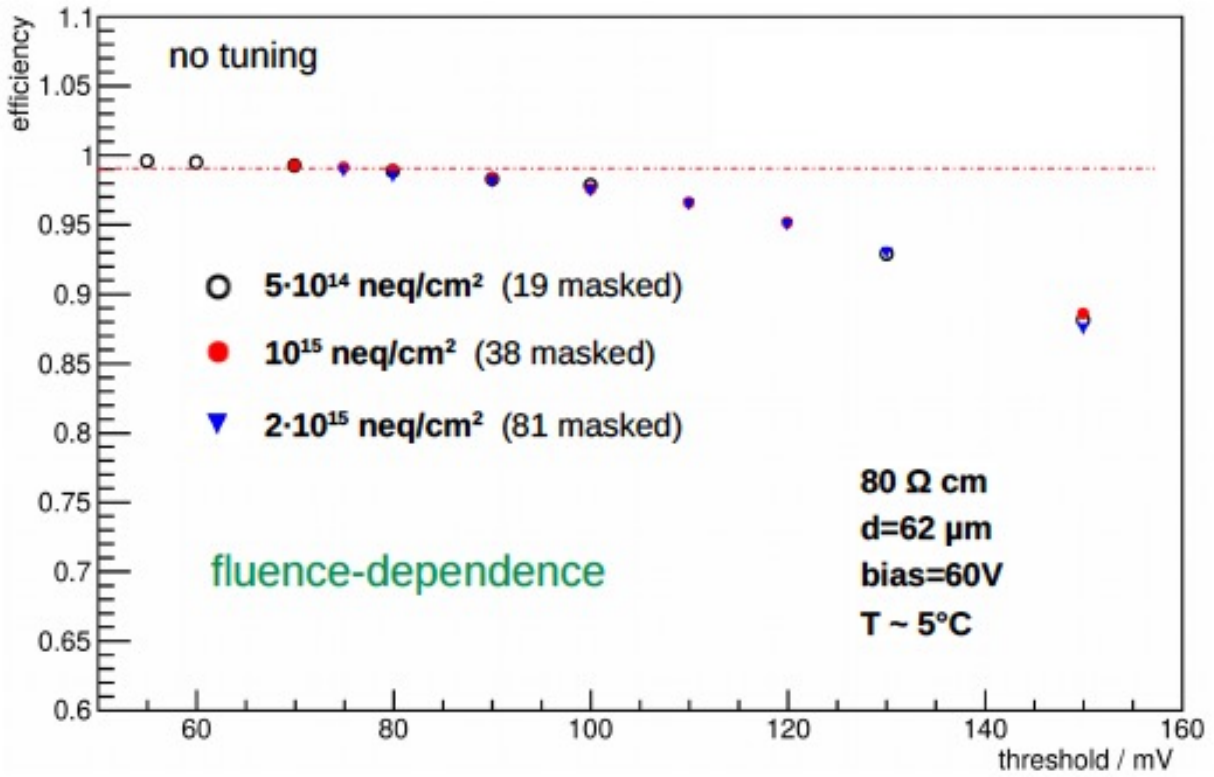
CACTUS Y. Degerli et al. doi:10.1088/1748-0221/15/06/P06011, VCI 2022, NIM A 1039 (2022) 167022, PIXEL 2024

RD-50 E. Vilella et al. doi:10.22323/1.373.0019

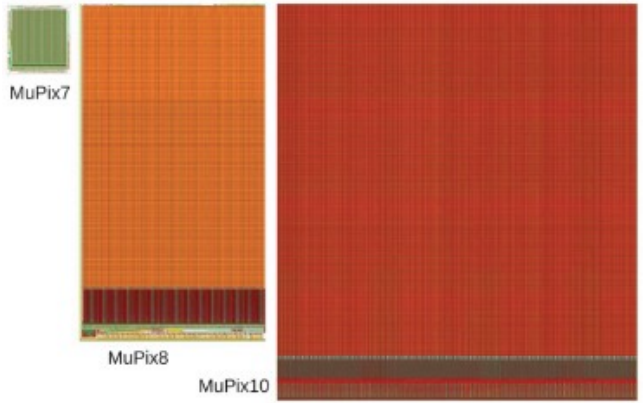
Better sensor radiation tolerance and timing: Large collection electrode: rad hard, but large C (100fF or more)



MuPix vertex detector prototype

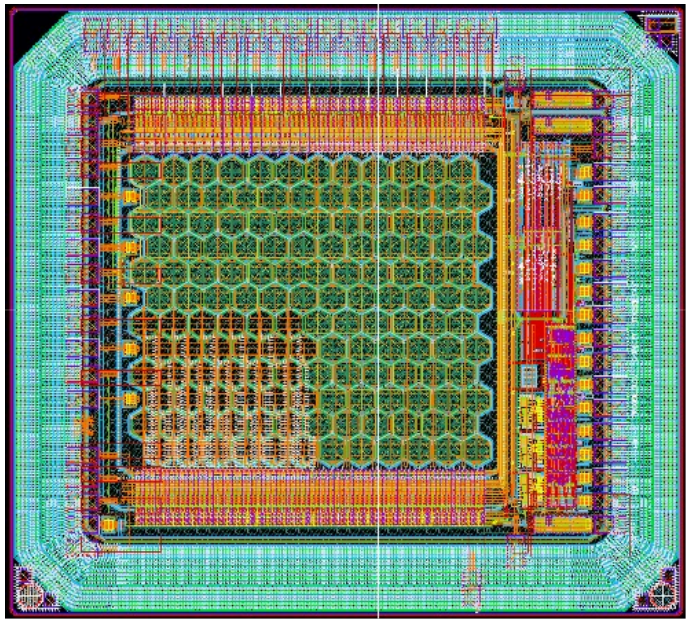


Courtesy I.Peric and A. Schoening

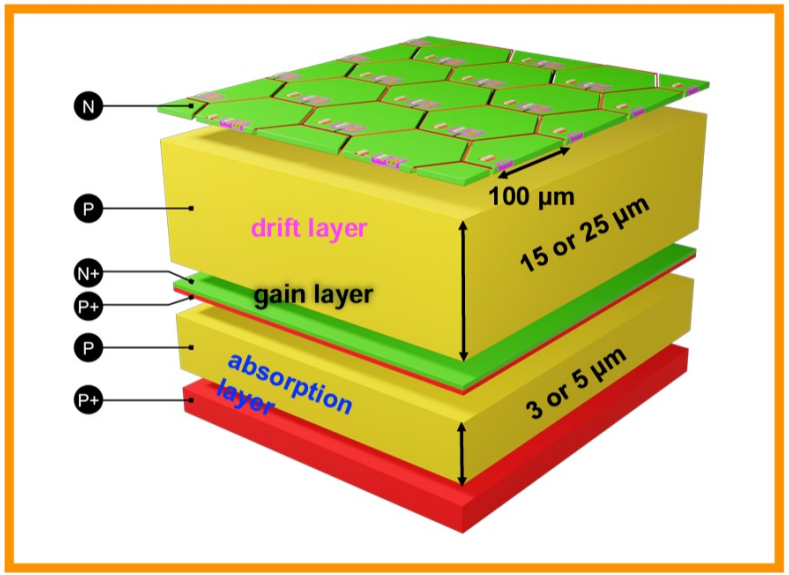


AMS/TSI 180nm, also used for ATLASPIX

MONOLITH: SiGe BiCMOS development, L. Paolozzi et al. PIXEL 2024

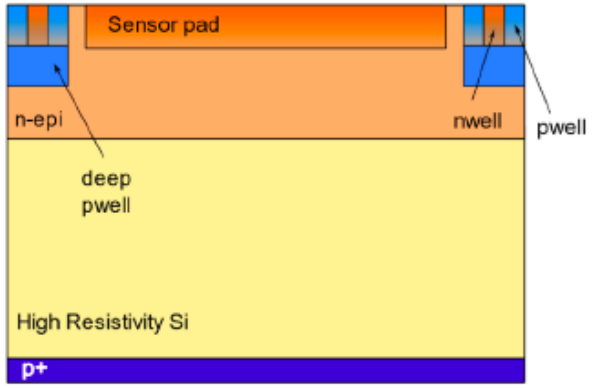


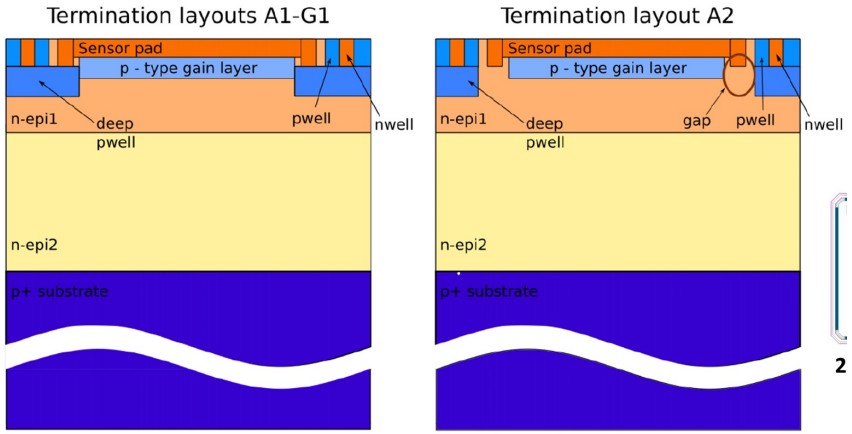
Courtesy G. Iacobucci



- Heterojunction Bipolar Transistor (HBT) gives cut-off frequencies otherwise only reached in more advanced CMOS technologies
- Large collection electrode hexagonal pixel arrangement (100 micron pitch)
- Without gain layer (50 um thick absorption layer)
  - 99.9 % efficiency, 20 ps time resolution before irradiation
  - 99.7 % efficiency, 45 ps time resolution after 10^{16} n_{eq}/cm^2
- With gain layer PicoAD, Pico Avalanche Detector
  - Full fill factor, thin absorption layer for reduced timing spread
  - 11.5 ps time resolution
- Further process modification to improve transistor isolation and parasitic capacitance, submitted in August

ARCADIA Sensor: LF 110 nm, L. Pancheri et al. PIXEL 2024



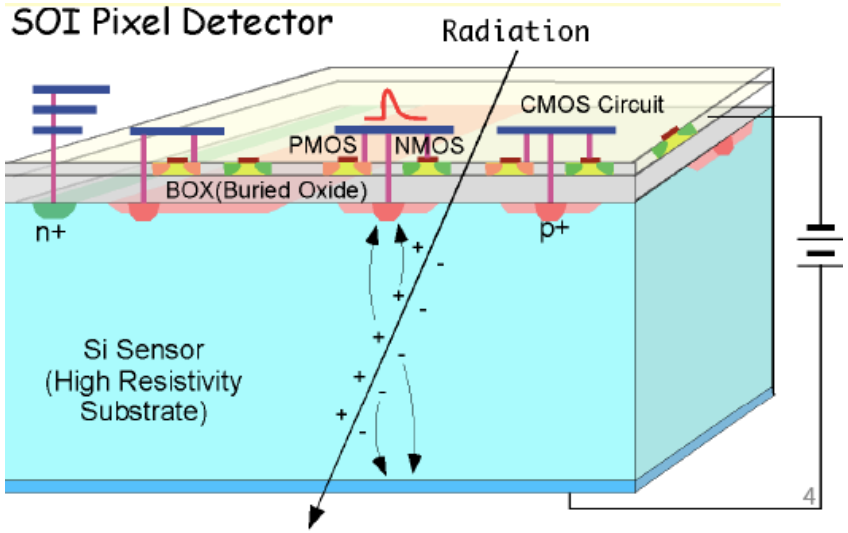


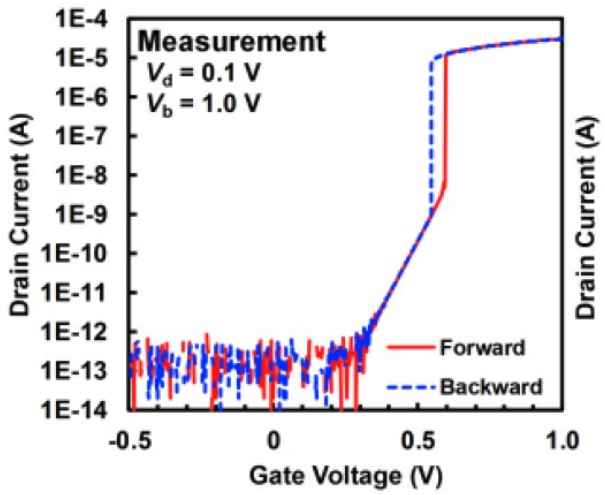
100 % fill factor

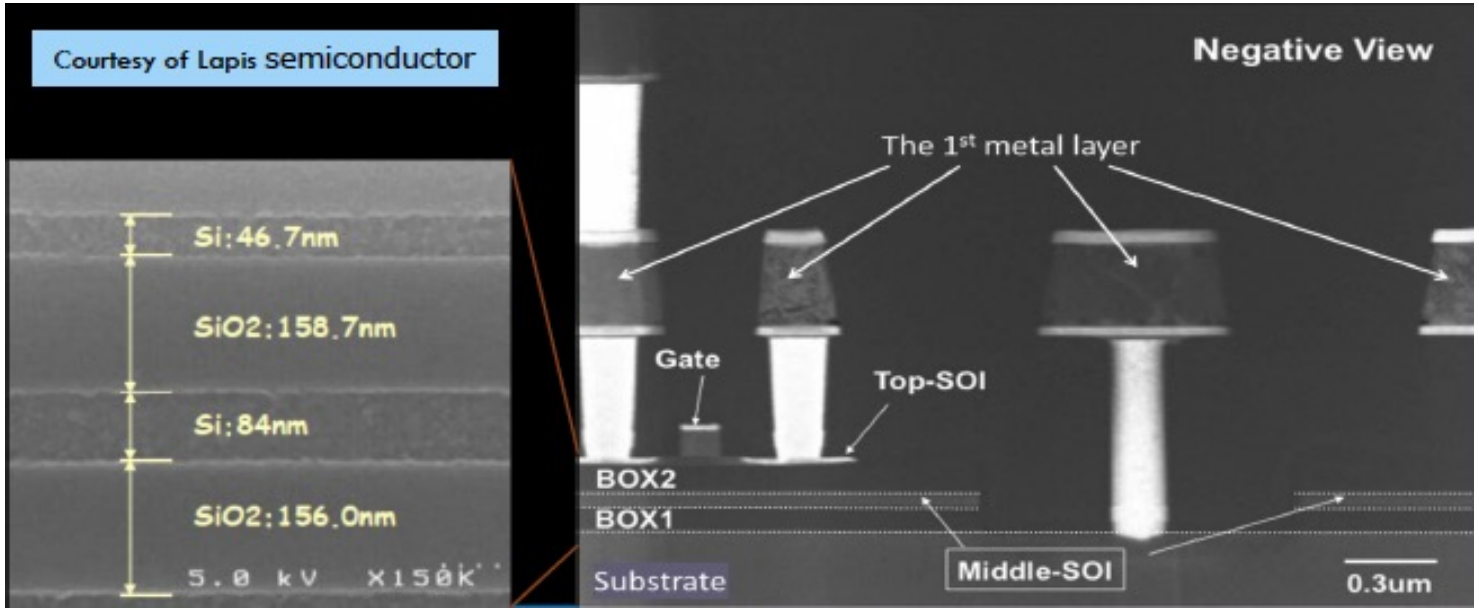
Efficient under gain layer
Better timing uniformity

- Depleted MAPS, developed in a collaboration between INFN and Lfoundry
- One of the three technologies offered by DRD7
- 110 nm CMOS, 6 metal layers, three runs so far
- Adding gain layer to reach 20 ps resolution, main driver now ALICE3 Time of Flight detector
- Prototypes with gain received in recent run (MADPIX)
  - Sensor size: 250 x 80 μm^2
  - Power 0.18 mW/channel
  - Time resolution 74 ps with gain ~ 13 (preliminary analysis of October testbeam)
- Compromise between timing uniformity and fill factor
- To be improved: reduced sensitive thickness, sensor geometry and readout circuit

Other development: SOI development in Japan



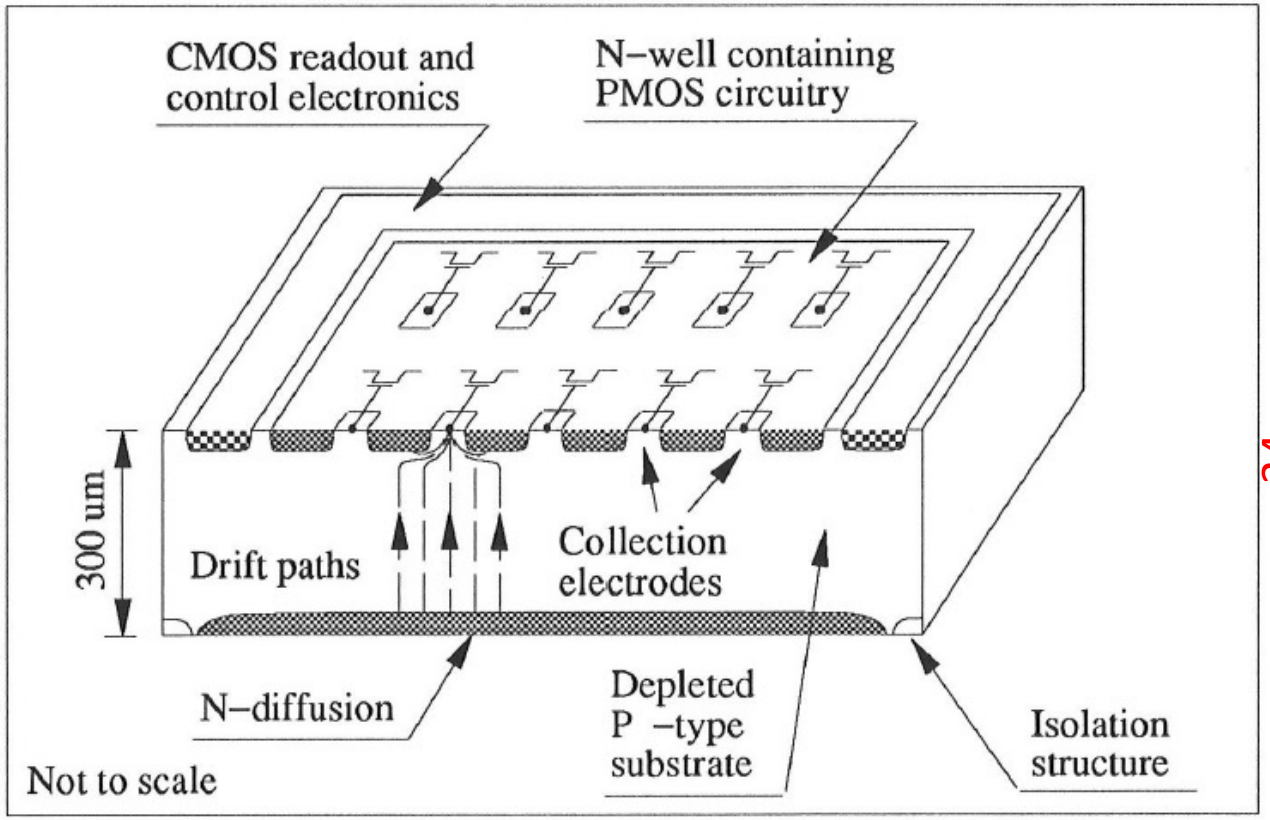


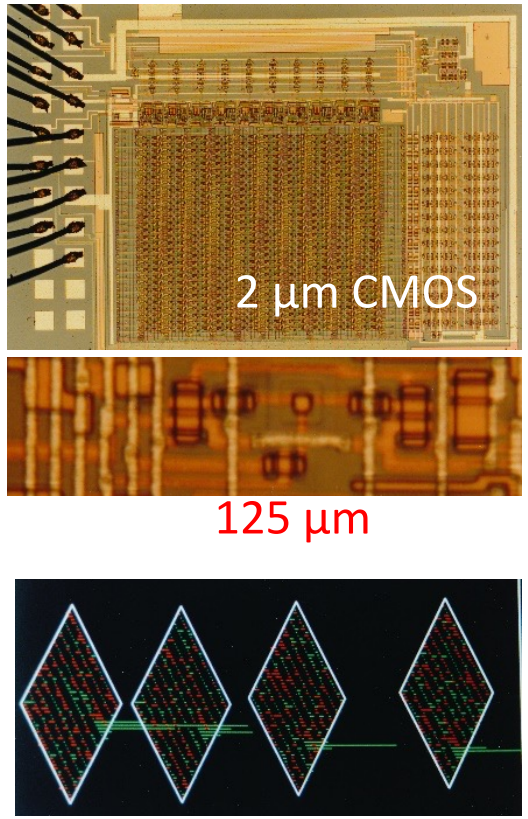


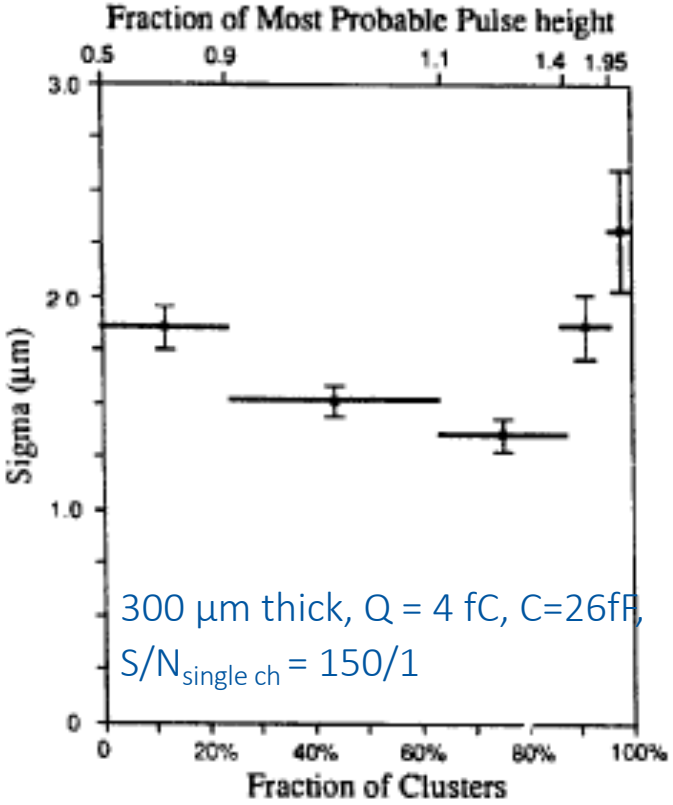
- Fully depleted 0.15 and 0.2 µm SOI technologies, impressive technology development
- Large user base, more than 20 MPWs so far in addition to dedicated runs
- Some freedom on sensor material
- Buried oxide causes reduced radiation tolerance, several measures for improvement, like double buried oxide, see bottom left
- Also research on
  - steep slope transistors doi:10.1109/SISPAD.2019.8870519
  - pinned diodes doi:10.3390/s18010027
  - …
- Funded by Japan MEXT KAKENHI Grant-in-Aid for Scientific Research on Innovative Areas 25109001

Courtesy Y. Arai

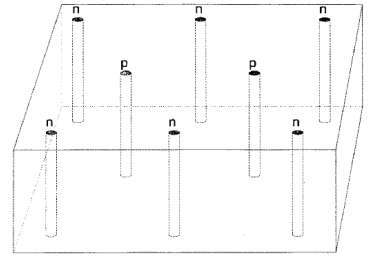
Small collection electrode: double sided CMOS process in this example







- Separation of junction from small collection electrode
- Better than 2 µm position resolution even at 34 µm pitch due to good S/N
- Improved back side trench isolation led to sensors with 3D electrodes (S.Parker, J. Segal) →



C. Kenney, S. Parker, J. Plummer, J. Segal, W. Snoeys et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

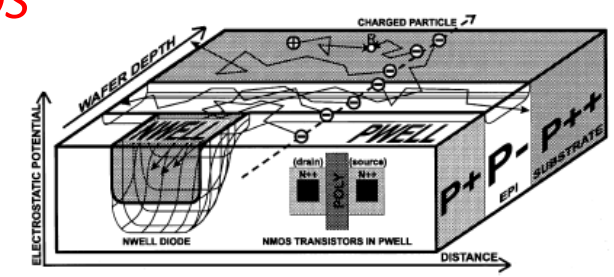
Other similar developments for fast charge collection and depletion:

T.G. Etoh et al., Sensors 17(3) (2017) 483, https://doi.org/10.3390/s17030483
H. Kamehama et al., Sensors 18(1) (2017) 27, https://doi.org/10.3390/s18010027…
L. Pancheri et al., PIXEL 2018 and PIXEL 2024, https://doi.org/10.3390/s18010027 (see below)
D. Sekigawa et al. TIPP 2017, https://doi.org/10.1007/978-981-13-1316-5_62 -> 0.59–0.83 µm position resolution

KEY ENABLERS: Mimosa series – IPHC Strasbourg - Move to standard CMOS

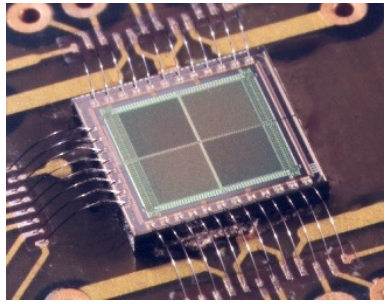
A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

R. Turchetta[a,*], J.D. Berst[a], B. Casadei[a], G. Claus[a], C. Colledani[a], W. Dulinski[a], Y. Hu[a], D. Husson[a], J.P. Le Normand[a], J.L. Riester[a], G. Deptuch[b,1], U. Goerlach[b], S. Higueret[b], M. Winter[b]



NIM A 458 (2001) 677-689

Mimosa1 – 1999
AMS 0.6 µm

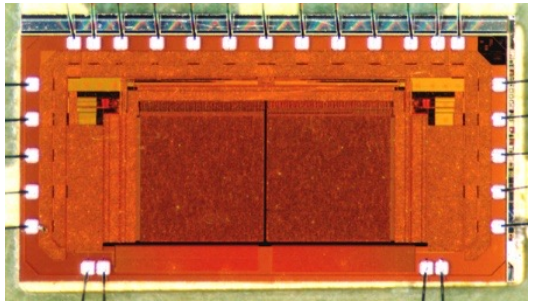


20µm pixel

Mimosa2 – 2000
MIETEC 0.35 µm

20µm pixel

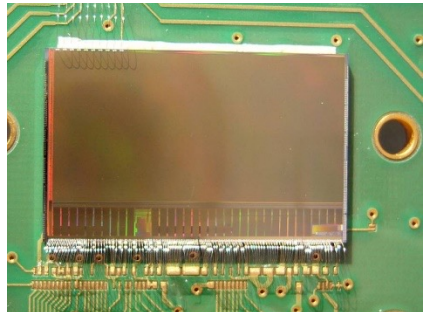
Mimosa3 – 2001
IBM 0.25 µm



8µm pixel

....

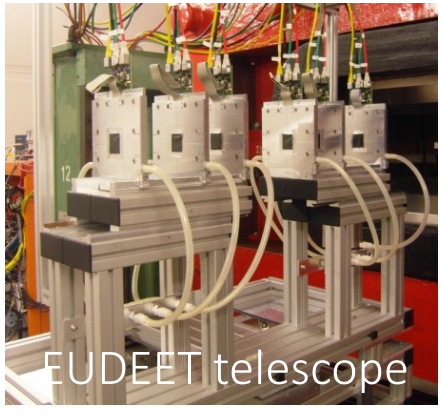
Mimosa26 – 2008
AMS 0.35 µm



18.4 µm pixel

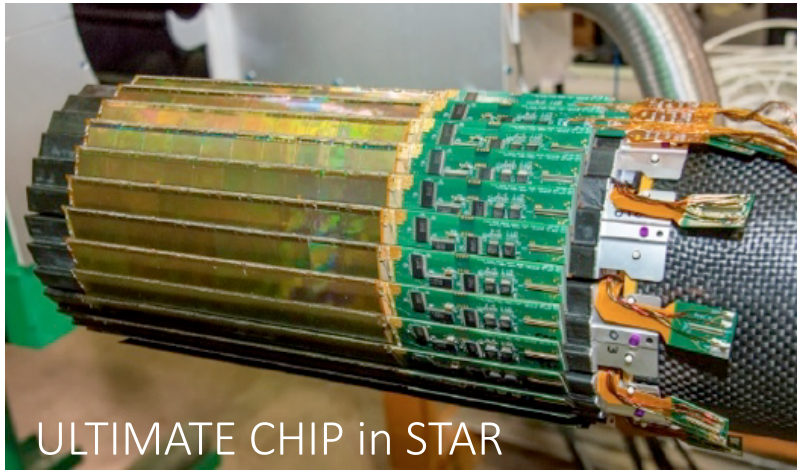
....

Mimosa26 – 2008 in the EUDET Telescope,



EUDEET telescope

First use of MAPS in HEP



ULTIMATE CHIP in STAR

KEY ENABLERS: The INMAPS process: STFC development, in collaboration with TowerJazz: a game changer

Additional deep p-well implant allows full CMOS in the pixel and 100 % fill factor

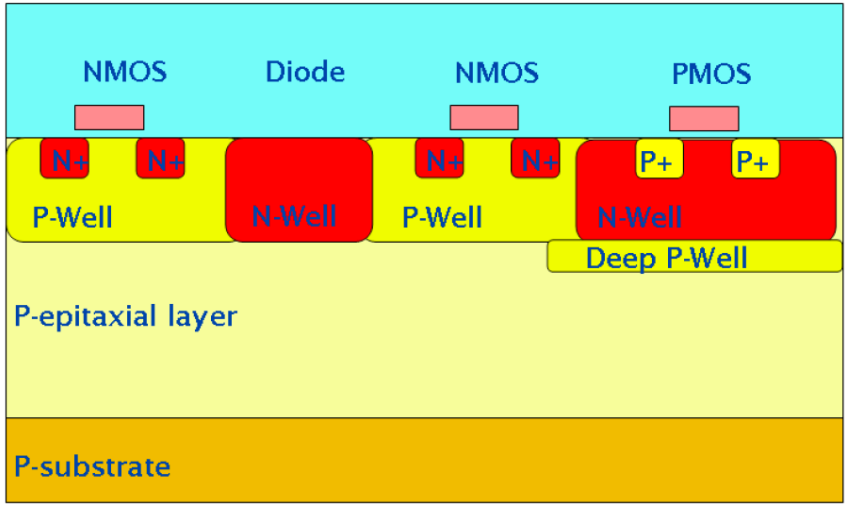
Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixels

Jamie Alexander Ballin [2], Jamie Phillip Crooks [1], Paul Dominic Dauncey [2], Anne-Marie Magnan [2], Yoshinari Mikami [3,**], Owen Daniel Miller [1,3], Matthew Noy [2], Vladimir Rajovic [3,***], Marcel Stanitzki [1], Konstantin Stefanov [1], Renato Turchetta [1,*], Mike Tyndel [1], Enrico Giulio Villani [1], Nigel Keith Watson [3], John Allan Wilson [3]

[1] Rutherford Appleton Laboratory, Science and Technology Facilities Council (STFC), Harwell Science and Innovation Campus, Didcot, OX11 0QX, U.K

[2] Department of Physics, Blackett Laboratory, Imperial College London, London, SW7 2AZ, U.K

[3] School of Physics and Astronomy, University of Birmingham, Birmingham, B15 2TT, U.K

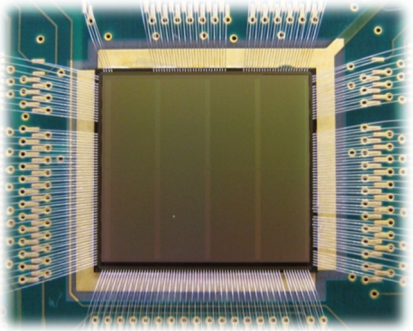


Sensors 2008 (8) 5336, DOI:10.3390/s8095336

New generation of CMOS sensors for scientific applications in TowerJazz CIS 180nm

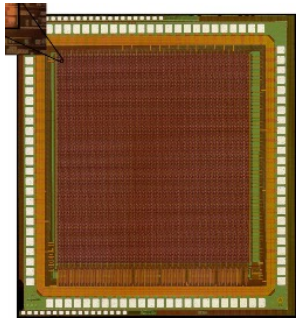
courtesy of STFC

TPAC
ILC ECAL (CALICE)



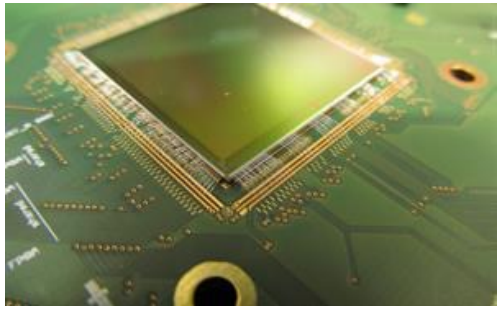
50μm pixel

DECAL
Calorimetry



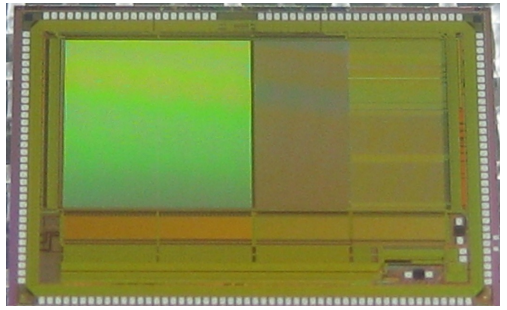
50μm pixel

PIMMS
TOF mass spectroscopy

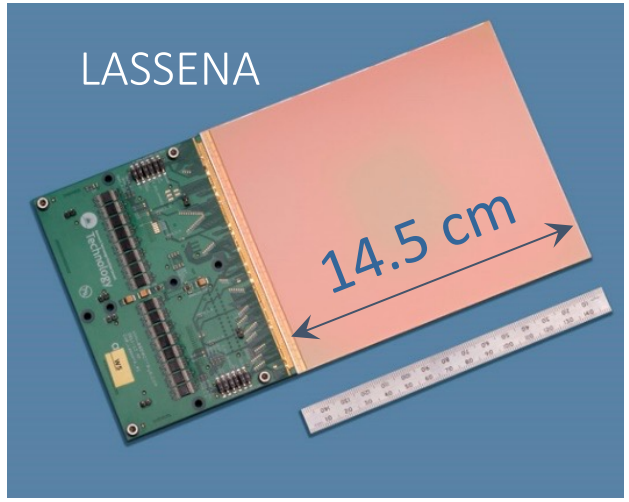


70μm pixel

CHERWELL
Calorimetry/Tracking



48 μm x 96 μm pixel



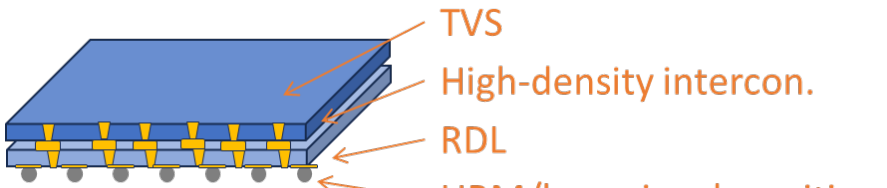
50μm pixel, waferscale

Standard INMAPS process also used for the ALPIDE (27 μm x 29 μm pixel) and MIMOSIS (CBM)

Backup

Project 7.6b: Shared Access to 3D Integration

Develop and facilitate access to 2.5D/chiplet and 3D integration technologies by coordinating efforts across contributing institutes, leveraging in-house expertise and strategic collaborations with industry



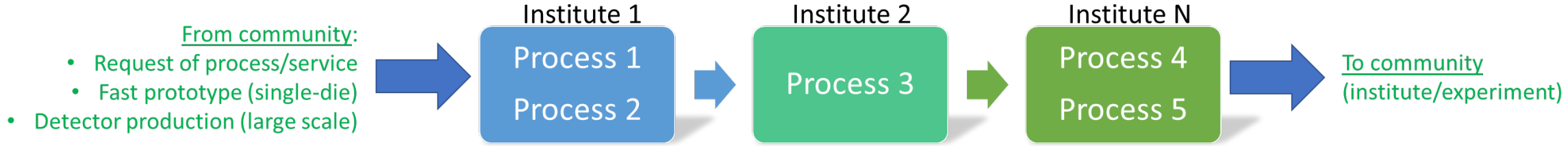
Work Topics and Areas of Contribution

- Provide the access to critical technologies include the formation of *TSV, RDL, back-side metallization* on custom-designed silicon interposer layers
- Towards the implementation of *3D-ASIC* integration at the level of a single assembly (e.g. Multi-Project Wafer)
- *Integration of SiPh* chip and optical fibers on detector module

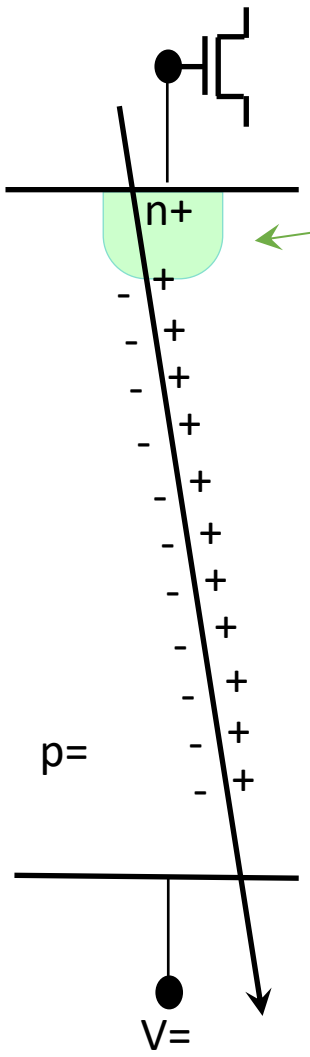
Integration of Silicon Photonics (SiPh) Chips into wafer-level Monolithic Detector Modules

International Distributed Detector Laboratory

- Establish a distributed laboratory that operates as a hub-service for the community
- Each institute highly specialized in one or more technological processes



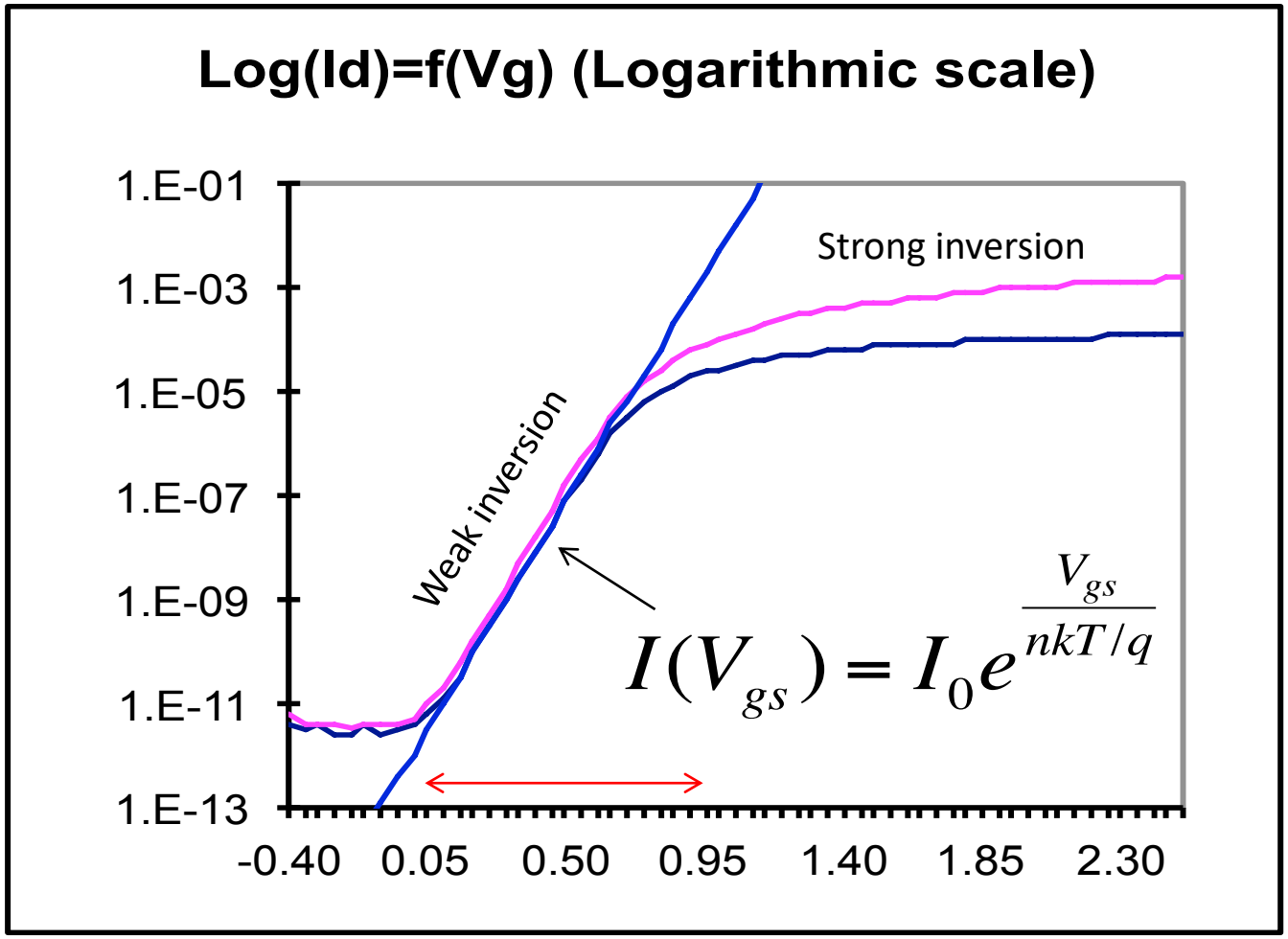
Analog power consumption ~ $(Q/C)^{-2}$ (NIM A 731 (2013) 125)



$$C_{spherical} = \frac{4\pi\varepsilon}{\frac{1}{R_1} - \frac{1}{R_2}} \approx 4\pi\varepsilon R_1$$

Add connection
&
circuit

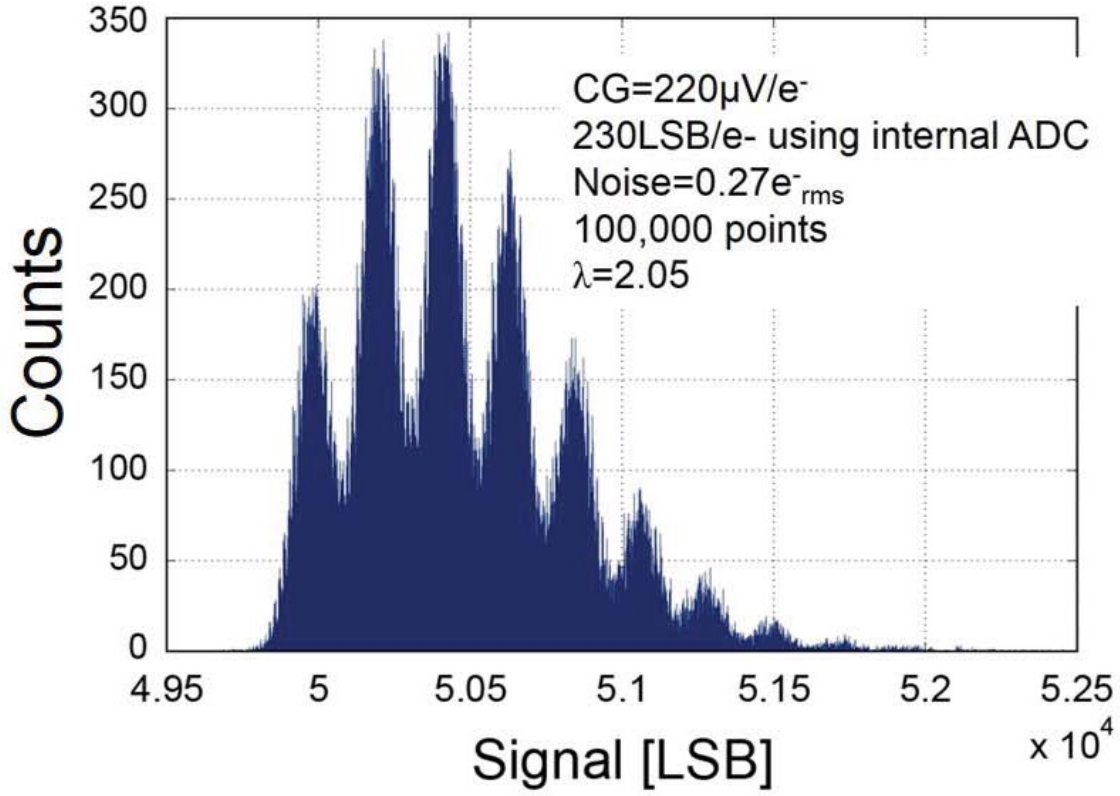
Non-linearity, exponential behavior in weak inversion



Importance of low C, can also exploit the exponential behavior

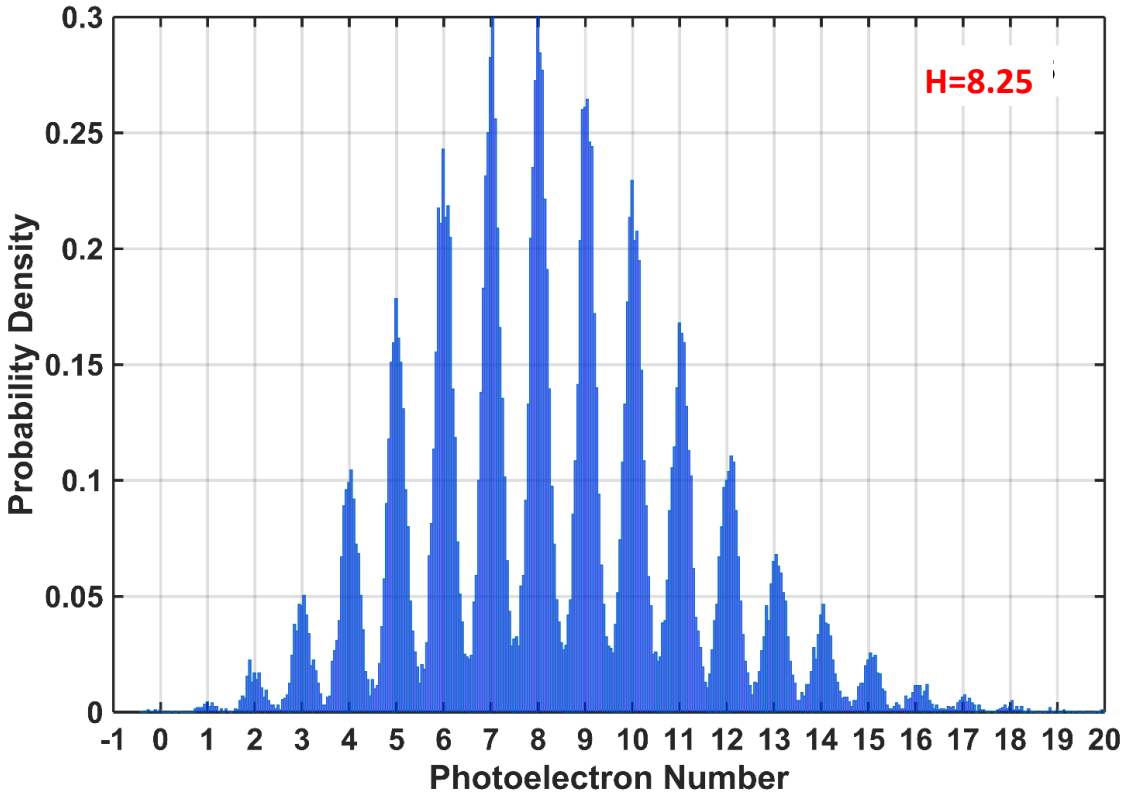
Analog power consumption ~ $(Q/C)^{-2}$ (NIM A 731 (2013) 125)

M.W. Seo and S. Kawahito EDL 2015



220 μV/e⁻ in 0.11 μm, C=0.73 fF

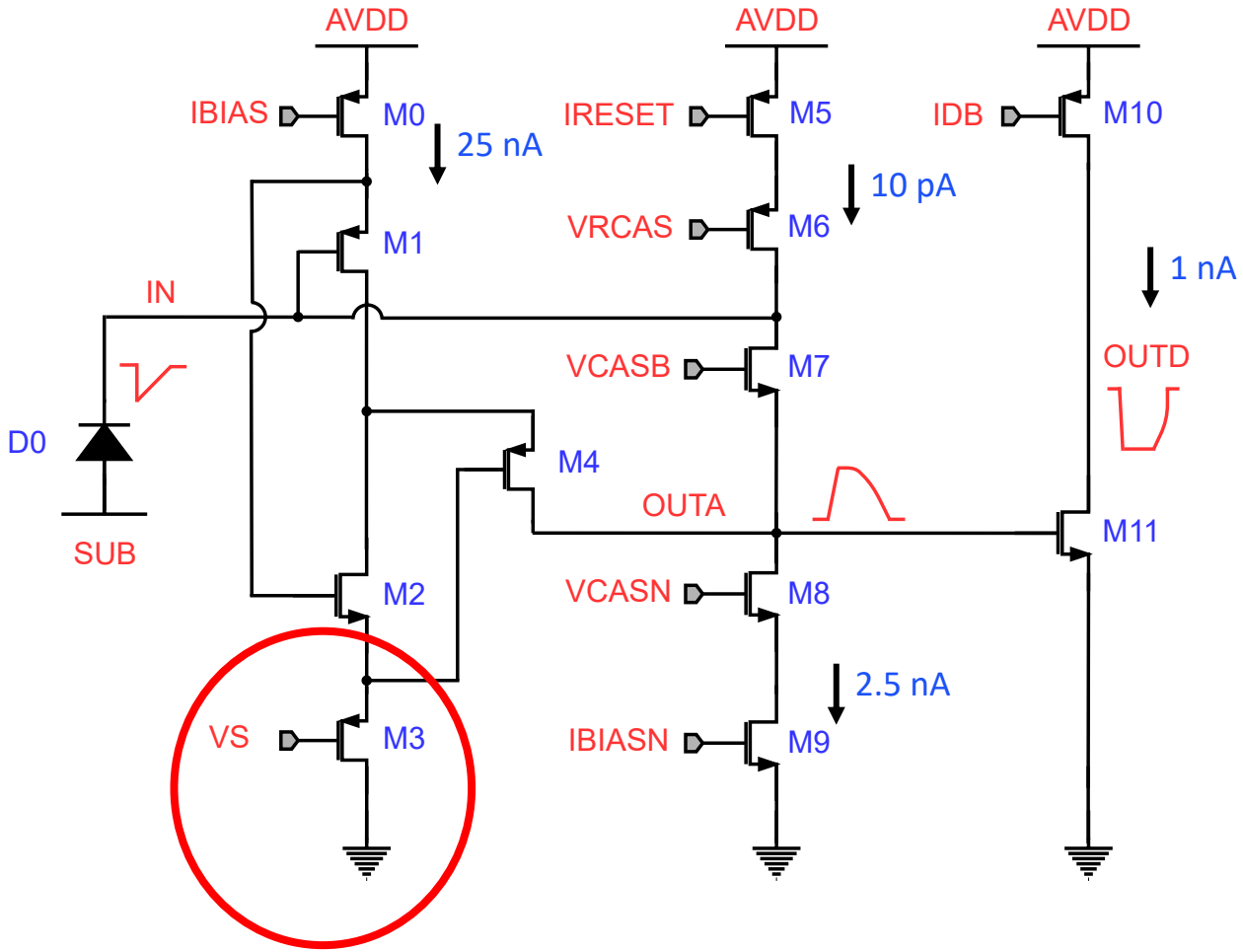
Ma, Masoodian, Wang, Fossum 2017



350 μV/e⁻ in 45 nm, C=0.46 fF

Visible light imagers, noise less than 1 e-

MOSS front-end



Conservative layout to respect DFM rules.

PWELL/PSUB to be kept at ground for high yield:

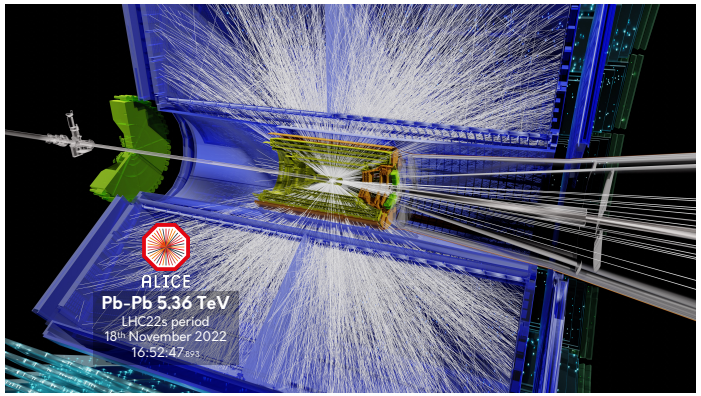
- Transistor M3 converted to a PMOS to be able to shift up the collection electrode voltage through front-end settings and increase sensor reverse bias.

Higher current for more margin

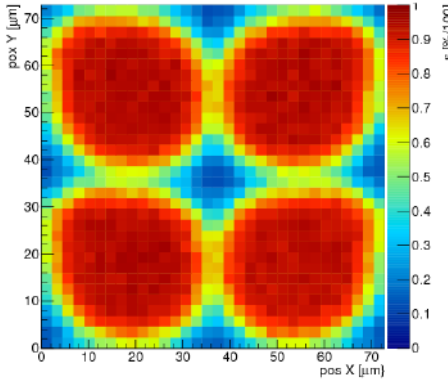
Pixel optimization for better margin: move junction away from the collection electrode for full depletion:
Better time resolution, radiation hardness and … efficiency, especially for thin sensors

EP R&D

in 180 nm



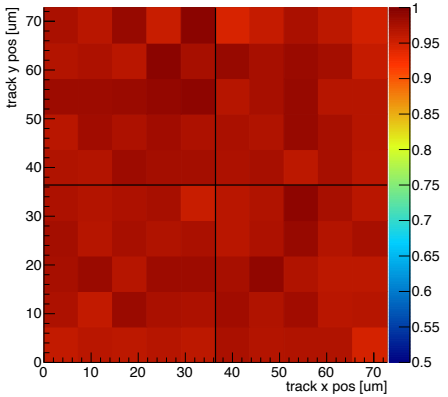
ALPIDE and ITS2 in ALICE (10 m^2)



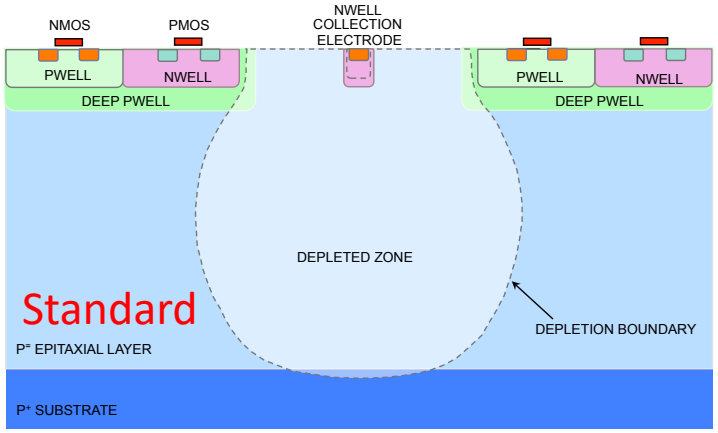
E. Schioppa et al, VCI 2019

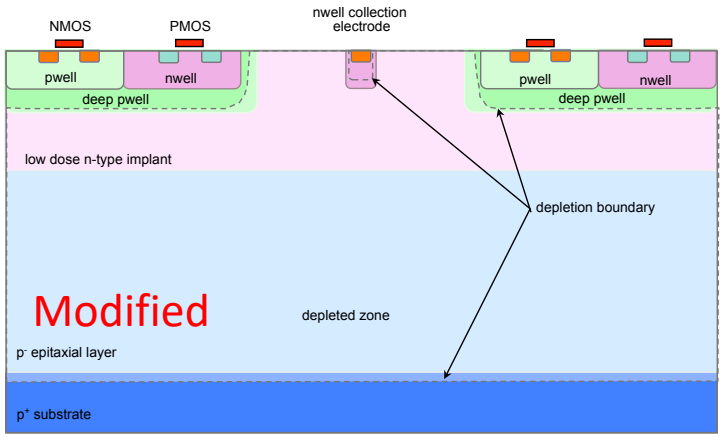
efficiency loss at
~ 10^{15} n_{eq}/cm^2

ALICE clic ATLAS EXPERIMENT STREAM

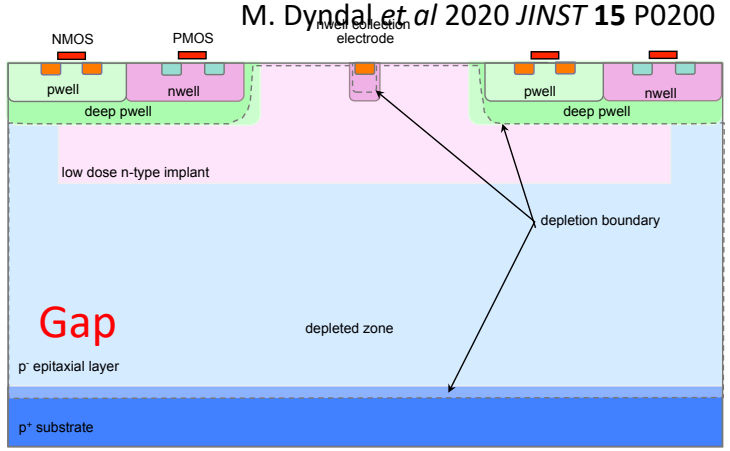


H. Pernegger et al., Hiroshima 2019,
M. Dyndal *et al* 2020 *JINST* **15** P0200





M. Munker et al.
https://doi.org/10.1016/j.nima.2017.07.046 (180nm)



https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

Charge collection speed

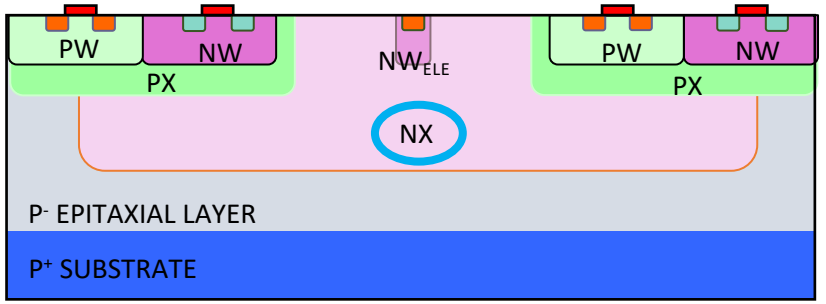
Charge sharing

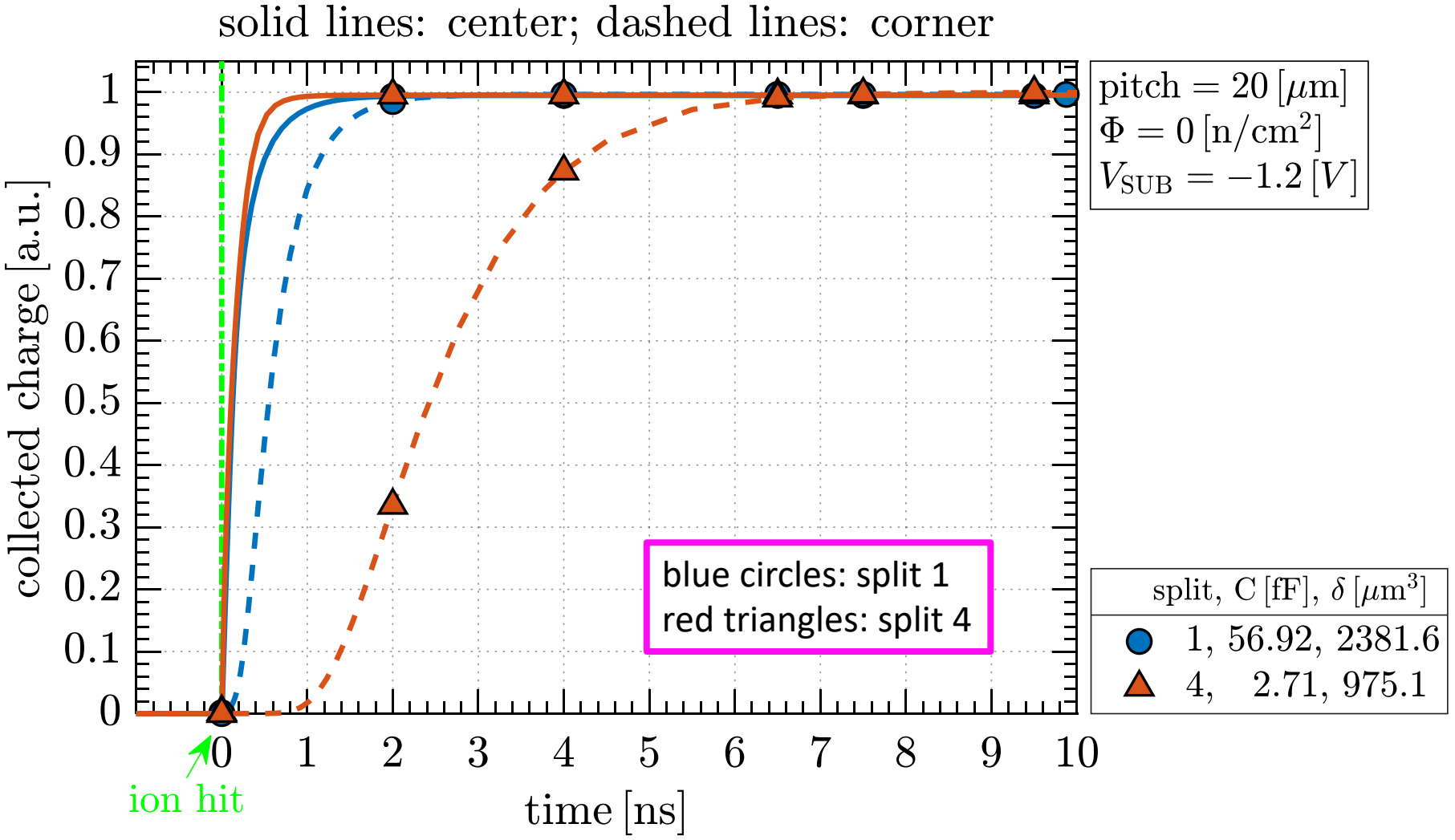
DOI: https://doi.org/10.22323/1.420.0001 (65nm)

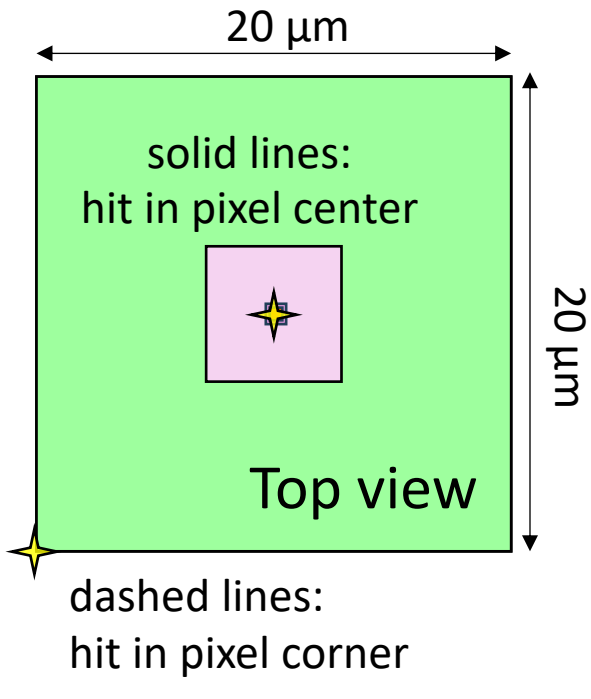
65 nm very similar, profited significantly from 10 years experience in 180 nm, modifications more needed in 65 nm

Sensor optimization: splits in ER1

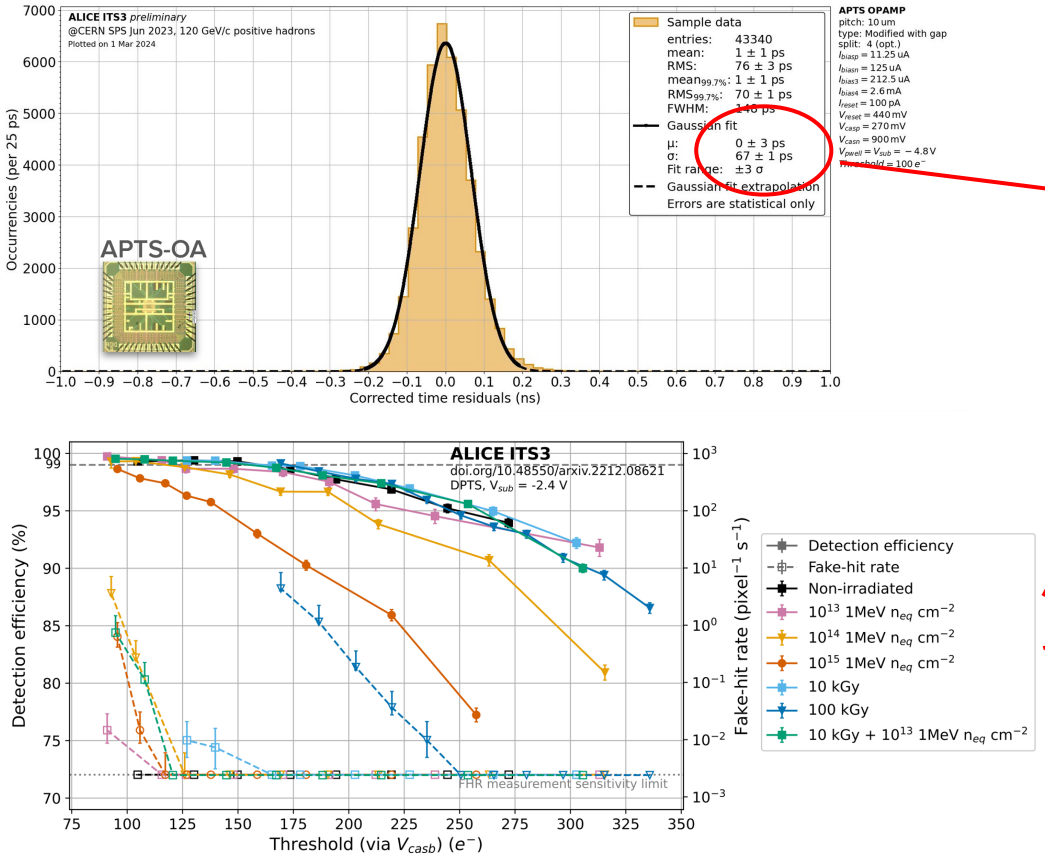
Split 1: foundry doping
Split 4: reduced deep n-type implant (NX)







MLR1: learning on sensor, front-end and readout



Lessons learned from MLR1:

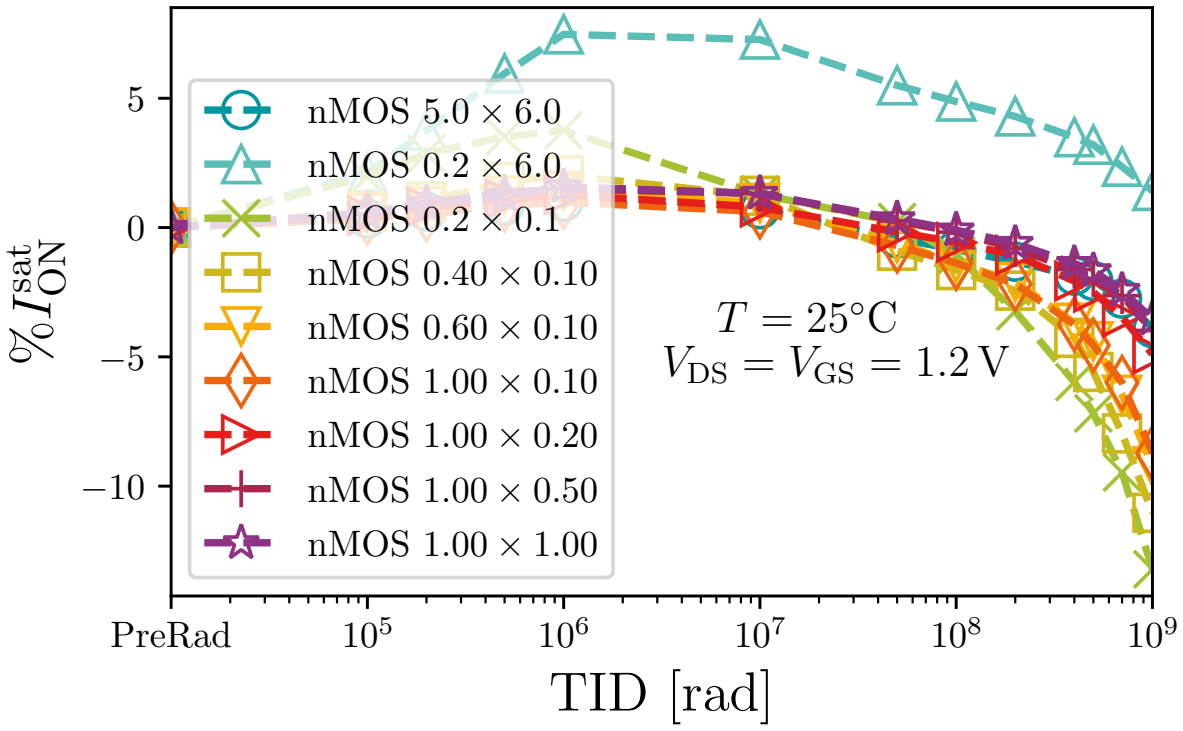
- < 100 ps timing precision (sensor + front-end only) [2]
- Fully efficient sensor, analog front end, digital readout chain with 15 x 15 µm^2 pixel [3]
- Transistor total ionizing dose tolerance and SEU in line with other 65 nm technologies
- Proof-of-principle that we can reach ~ 99 % detection efficiency at $10^{15}\ 1MeV\ neq\ cm^{-2}$ at room temperature

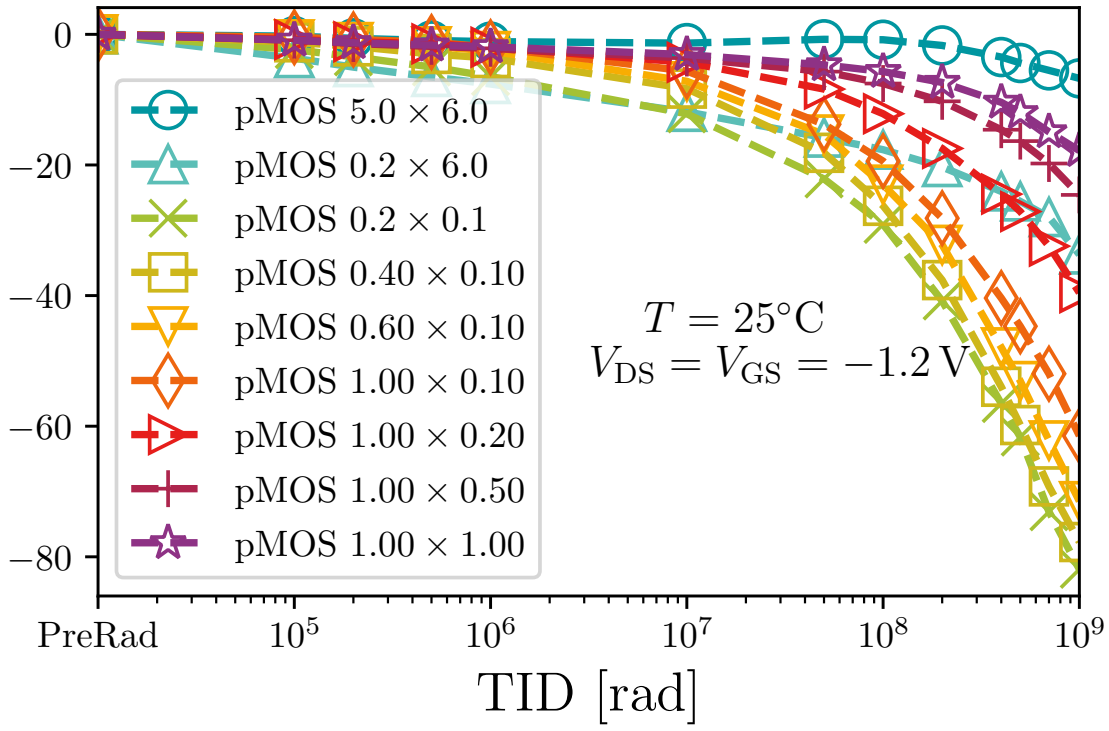
[1] “Characterization of analogue Monolithic Active Pixel Sensor test structures implemented in a 65 nm CMOS imaging process”. In: Nucl. Instr. and Meth. A 1070 (2025), 169896. doi: 10.1016/j.nima.2024.169896.

[2] “Time performance of Analog Pixel Test Structures with in-chip operational amplifier implemented in 65 nm CMOS imaging process”, In: Nucl. Instr. and Meth. A 1070 (2025), 170034. doi: 10.1016/j.nima.2024.170034.

[3] “Digital pixel test structures implemented in a 65 nm CMOS process” , In: Nucl. Instr. and Meth. A 1070 (2025), 168589. doi: 10.1016/j.nima.2024.168589.

Transistor radiation tolerance

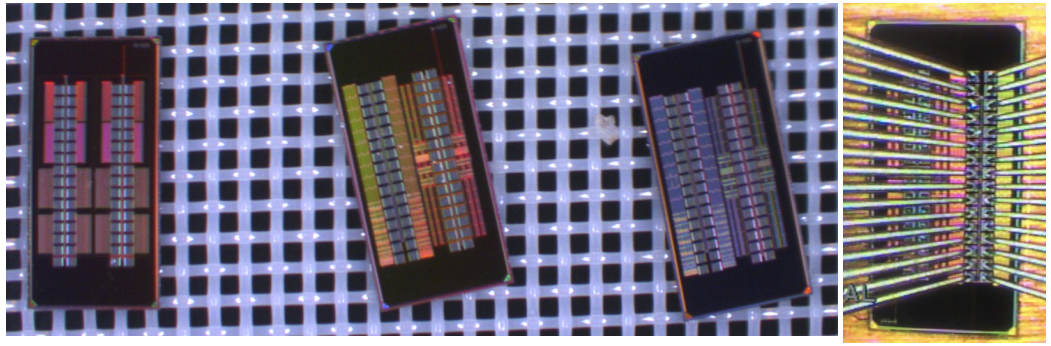




In line with other 65 nm technologies, no showstoppers.

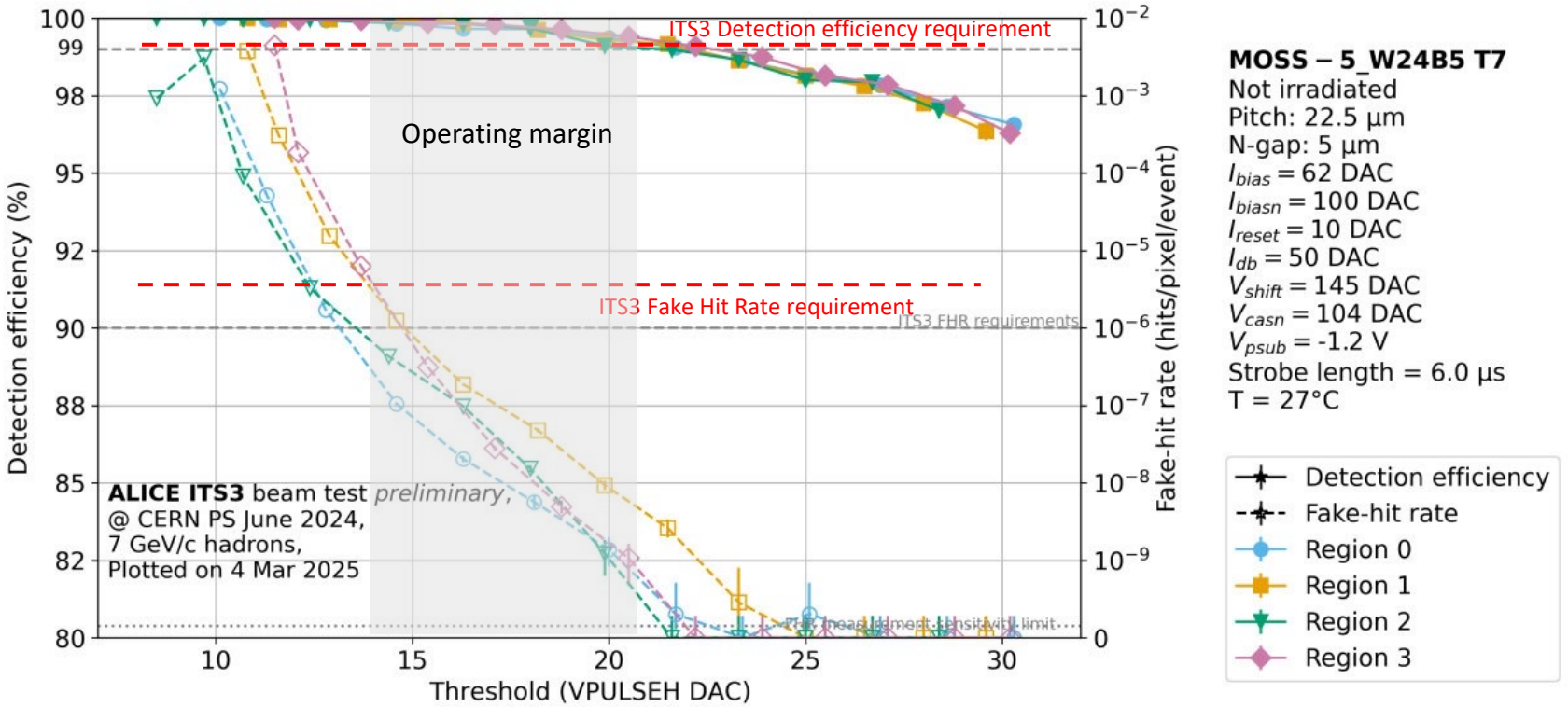
Small size PMOS transistors degrade significantly after several hundred Mrad.

Caveat: modeling of transistors with significant reverse bias



[4] A. Dorda Martin et al. “Measurements of total ionizing dose effects in TPSCo 65 nm and influence of NMOS bulk bias”. doi: 10.1088/1748-0221/18/02/C02036

MOSS Test beam results



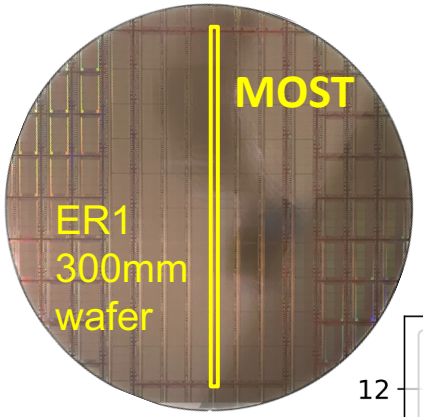
Before irradiation: good operating margin.

After irradiation: satisfactory operating margin at the radiation load estimated for ITS3 (~ 400 krad, ~ 4 x 10^{12} 1 MeV n_{eq}/cm^2, see [5]).

[5] L. Terlizzi. “Characterization of silicon Monolithic Stitched Sensors (MOSS) for the ALICE ITS3 for the LHC Run 4”. In: Eleventh Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Strasbourg, November 2024).

MOST (Monolithic Stitched Sensor with timing)

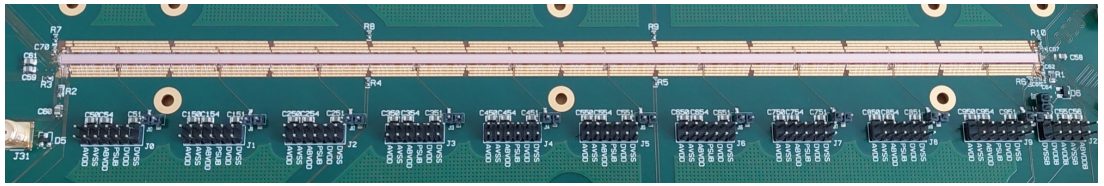
- MOST other stitched sensor on ER1
  - 259 x 2.5 mm
  - 18 micron pixel pitch



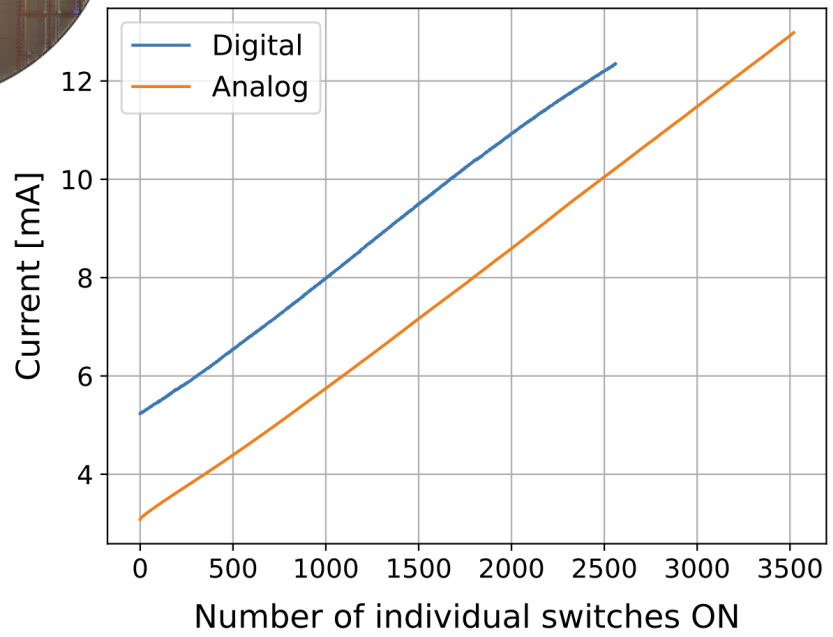
- Main differences with MOSS
  - Powering: global power distribution with power switches to switch off faulty parts, very densely designed circuit
  - Asynchronous, hit-driven readout for timing information + low power consumption
  - High-speed data transmission on chip
  - Reverse bias is applied to the sensor via the front-end

Significant testing effort, also at NIKHEF, more details in [6]

MOST on carrier board



25.9 cm



MOST current consumption vs. powered pixel groups (powered through power switches)

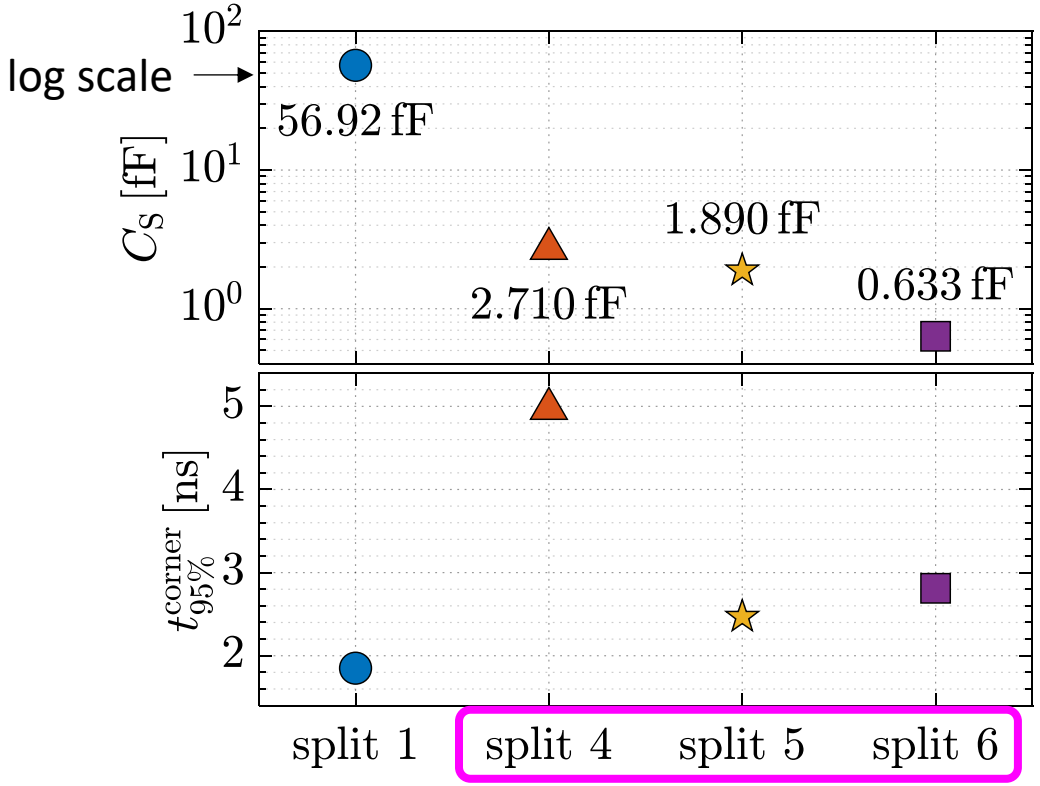
[6] M. Selina. “Exploring ALICE ITS3 MOST: Early Results on Power Segmentation and Asynchronous Readout for Timing in a Monolithic Stitched Sensor”. In: Eleventh Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Strasbourg, November 2024), https://arxiv.org/pdf/2504.13696

Sensor optimization in ER2:

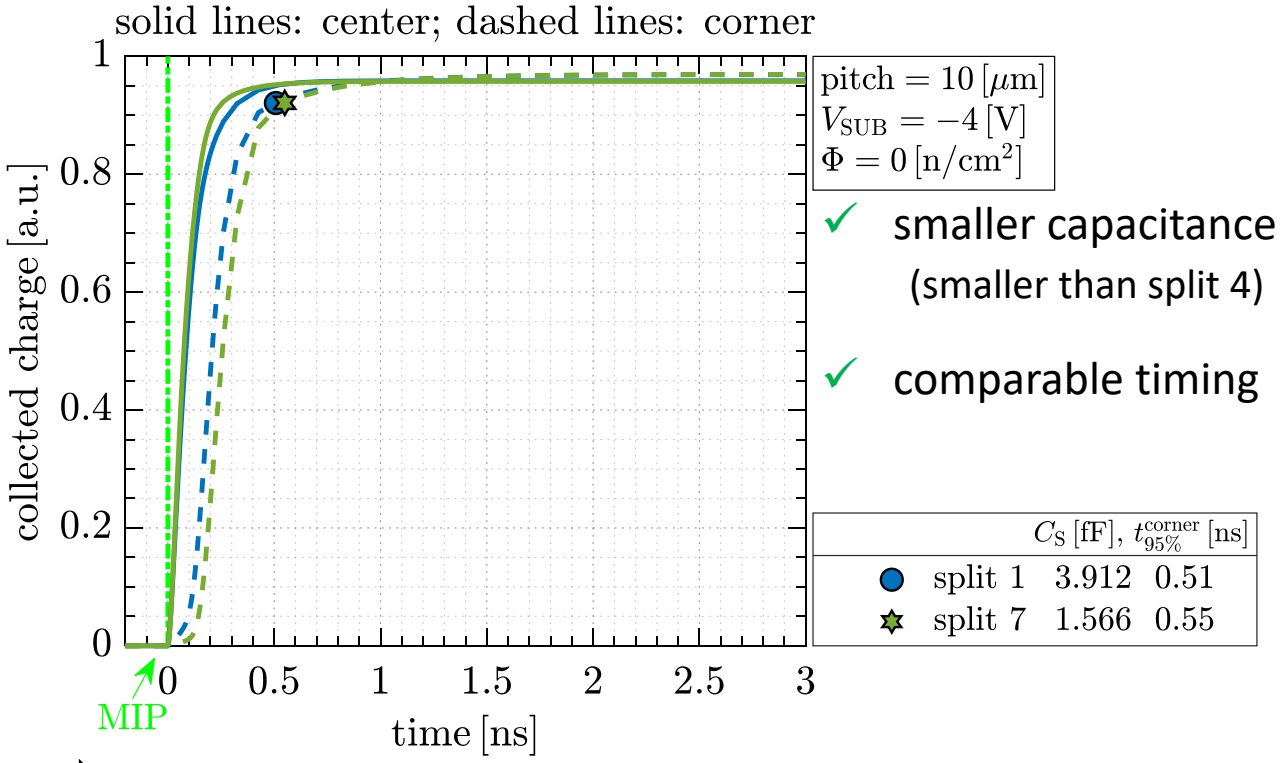
process modification in close collaboration with the foundry

EP R&D

FOR ITS3: split 1 vs split 4 vs split 5 vs split 6



FOR FUTURE UPGRADES: split 7



✓ smaller capacitance (smaller than split 4)

✓ comparable timing

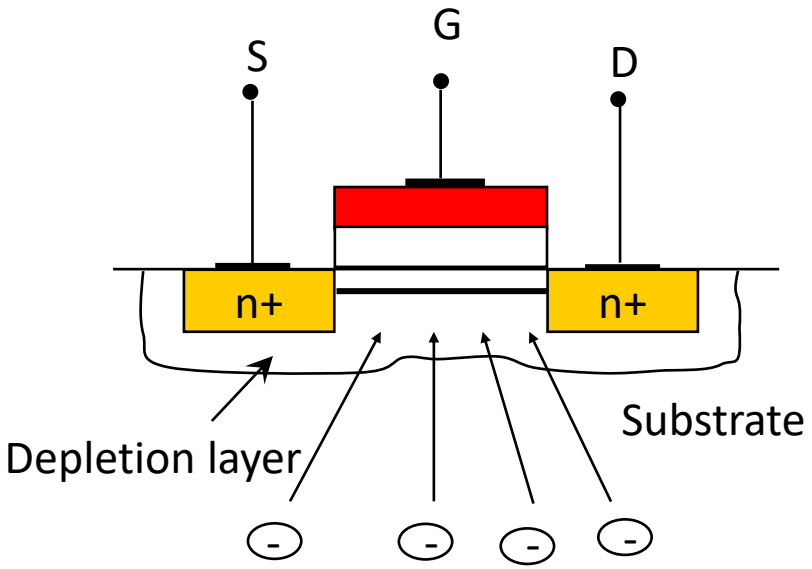
increasing deviations from standard profiles

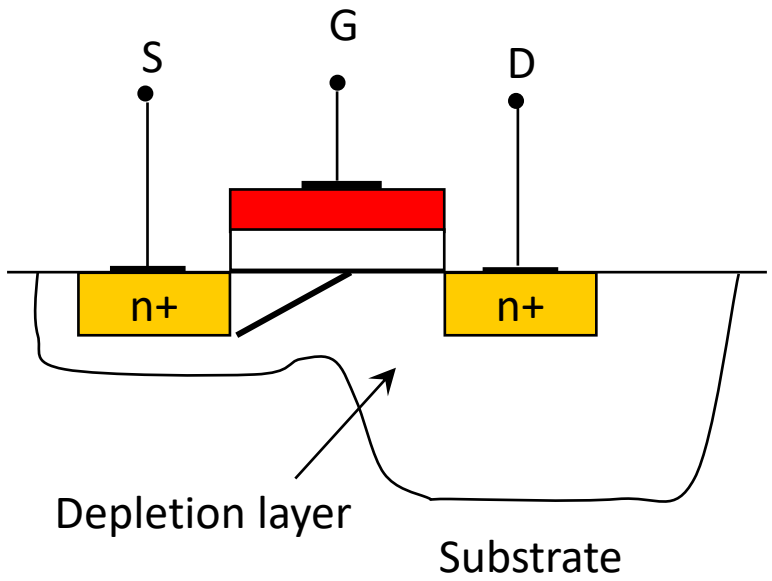
10 μm pitch, -4 V reverse bias.

3 of the 4 splits for MOSAIX, the ITS3 prototype
~ 20 μm pitch, -1.2 V reverse bias.

Giulio Borghello *et al* 2025 *JINST* **20** C07053

Transistor: traditional





Linear region (low VDS)

For a sufficiently positive gate voltage, electrons are attracted to the SiO2-Si interface => conductive layer (channel) is formed (P-substrate gets inverted locally). The channel which links source and drain, forms a resistor between the two. Current increases with increasing VDS.

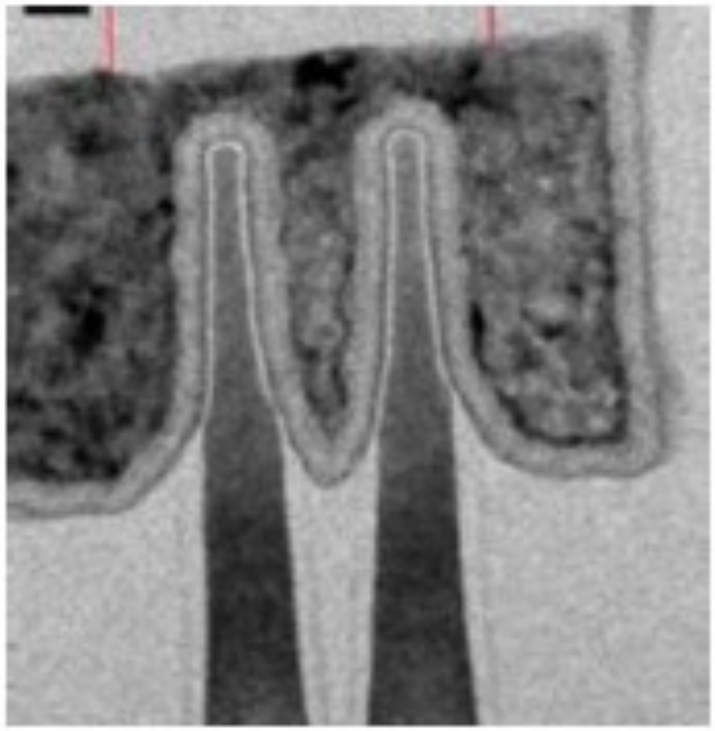
Saturation region (high VDS)

Significant current flow and resistive drop in the channel. Electrons near the drain are insufficiently attracted by the gate, and the channel gets pinched off. Beyond that point increasing VDS does/should not change current significantly.

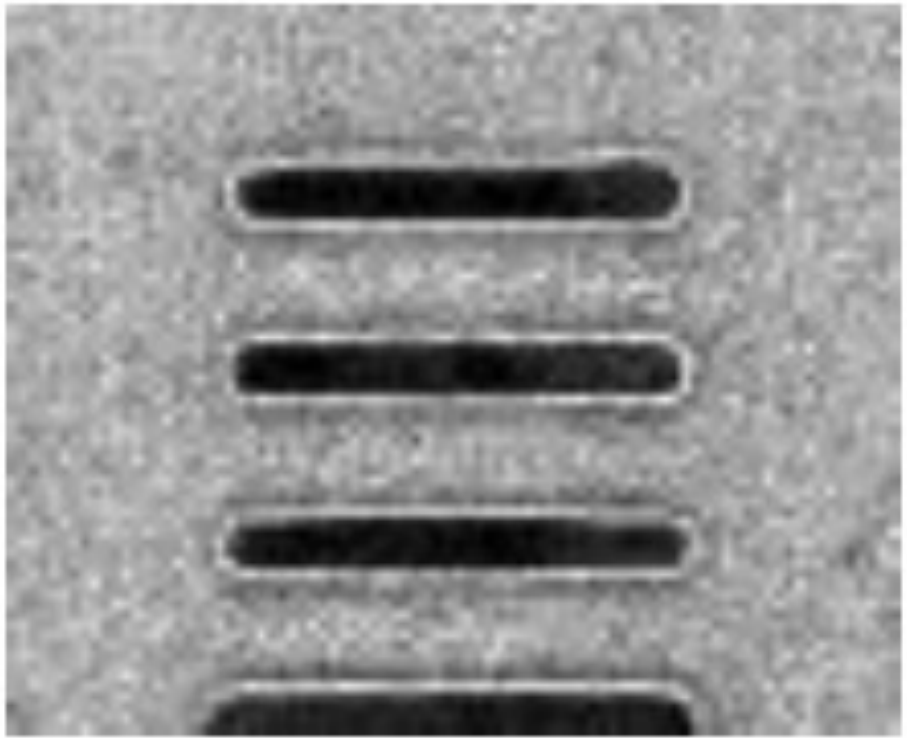
However, for very small gate length and conventional transistors, drain-induced barrier lowering has to be avoided, or coupling of the drain voltage into the channel-region near the source.

In Finfet and Gate All Around this effect is much better suppressed.

Transistor: Finfet and Gate All Around Transistor



Finfet: INTEL



Gate All Around : SAMSUNG

In Finfet and Gate All Around bulk volume suppressed, much better electrostatics, much lower Drain Induced Barrier Lowering (DIBL).

1st Finfet 14 nm. GAA superior to Finfet, will take over from 3 nm.

More revolutionary innovation steps in transistor improvement than in interconnect