

Upgrade of Belle II and Future Detector Requirements

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Belle II experiment at SuperKEKB

- ▶ Belle II searches for new physics beyond standard model at luminosity frontier
- ▶ SuperKEKB collider: asymmetric e^+e^- collisions at $\Upsilon(4S)$ resonance at 10.58 GeV
⇒ aims at reaching higher luminosity but with challenging background conditions

Operation started in 2019,
achieved luminosity

$$\mathcal{L} = 5.1 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$$

$$\int \mathcal{L} dt = 575 \text{fb}^{-1}$$



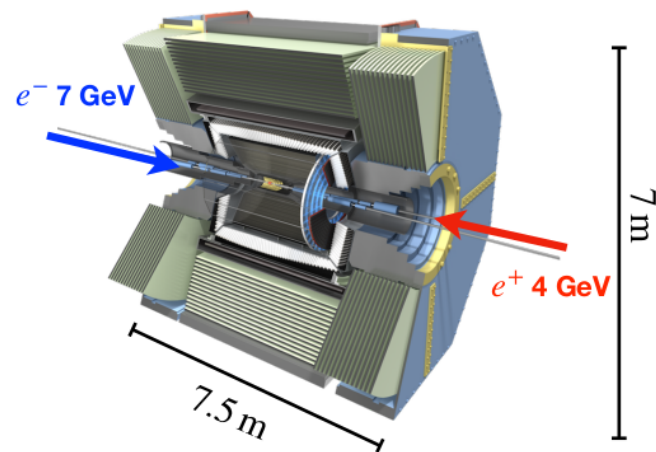
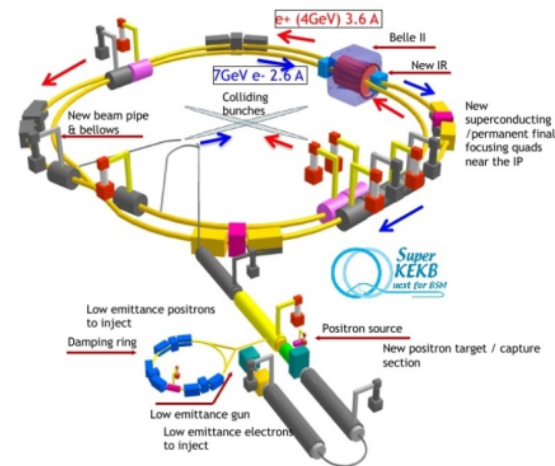
Target luminosity

$$\mathcal{L} = 6 \times 10^{35} \text{cm}^{-2}\text{s}^{-1}$$

$$\int \mathcal{L} dt = 50 \text{ab}^{-1}$$

- ▶ Require an upgrade of accelerator complex to reach the target luminosity, which may include a major redesign of the Interaction Region (IR)

⇒ Long Shutdown 2 ~ 2032 with detector upgrade now being proposed



The current Belle II Vertex Detector (VXD)

- Tracking of particle at low momentum with the **Vertex Detector (VXD)**:

→ 2 inner layers of **Pixel Detector (PXD)** using DEPFET pixel sensors [1]

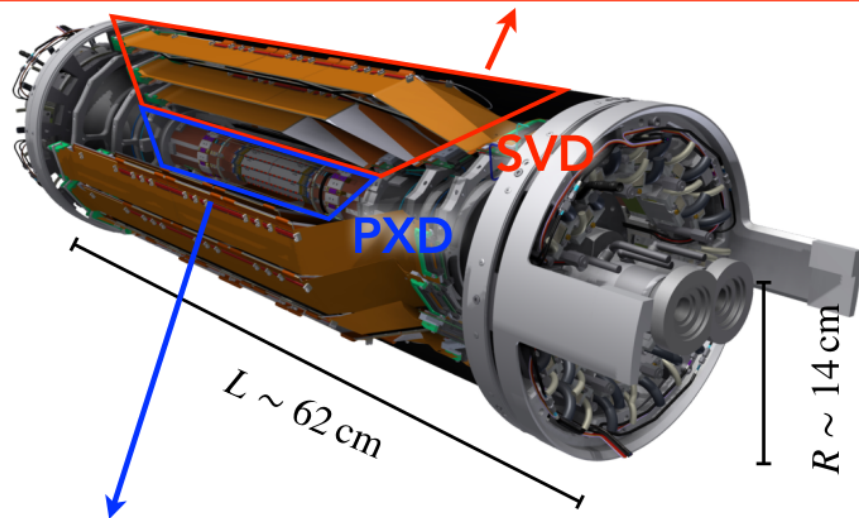
→ 4 layers of **Silicon Vertex Detector (SVD)** using double-sided strip sensors [2]

- Excellent performance for current occupancy $< 1\%$
- Large uncertainty on background extrapolation at target luminosity and with a possible upgrade of the IR
- Limited safety margin and performance degradation in high background scenario at target luminosity.
- Background extrapolation at target luminosity:
 - **PXD layer 1**: up to 2% occupancy (32 MHz/cm^2)
 - **SVD layer 3**: up to 9% occupancy (9 MHz/cm^2)

⇒ need higher granularity and time resolution in all layers keeping the total material budget $\leq 3.5\% X_0$

- 300 μm thick sensors & 2-phase CO_2 cooling - $0.75\% X_0/\text{layer}$
- Excellent time resolution of 3ns but strip length up to 12cm
- Occupancy limit 6%, using hit-time for BG rejection
- Trigger latency limited to $5\mu\text{s}$ by readout

SVD



- Thin sensors ($75 \mu\text{m}$) & $\text{N}_2 + \text{CO}_2$ cooling - $0.25\% X_0/\text{layer}$
- Small pitch of 50-70 μm but long integration time of $20 \mu\text{s}$
- Occupancy limit 3%

PXD

VXD Total material budget of $3.5\% X_0$

The current Belle II Vertex Detector (VXD)

- ▶ Tracking of particle at low momentum with the **Vertex Detector (VXD)**:

→ 2 inner layer
DEPFET pixel sensors

→ 4 layers of
double-sided strip sensors

- ▶ Excellent performance for background rejection

- ▶ Large uncertainty in target luminosity measurement at IR

- ▶ Limited safety margin in high background

- ▶ Background extraction

→ PXD layer1: up to 100 MHz/cm²

→ SVD layer 3: up to 100 MHz/cm²

- ▶ 300 μ m thick sensors & 2-phase CO₂ cooling - 0.75% X₀/layer

- ▶ Excellent time resolution of 3ns but strip length up to 12cm

→ BG rejection

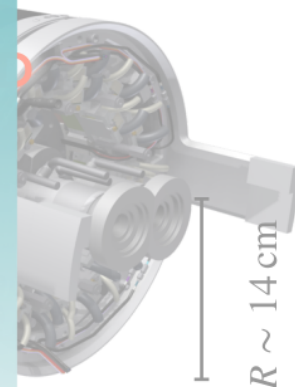
cut

SVD

Upgrade of Belle II VXD - initial requirements [ref. CDR 2024]

- ▶ Hit rate up to 120 MHz/cm²
- ▶ Fast time stamping 50-100ns
- ▶ Resolution <15 μ m → pitch of 30-40 μ m
- ▶ Aiming power dissipation ≤ 200 mW/cm²
- ▶ Operation simplicity and reduced services
- ▶ Radiation tolerance:
 - TID ~ 100 Mrad
 - NIEL ~ 5×10^{14} neq/cm²
- ▶ Light material budget

⇒ **Depleted Monolithic Active Pixel Sensors (DMAPS)**



g - 0.25% X₀/layer

gratiation time of 20 μ s

PXD

⇒ need higher granularity and time resolution in all layers keeping the total material budget $\leq 3.5\%$ X₀

VXD Total material budget of 3.5% X₀

VTX proposal

Proposal = 6 straight layers with DMAPS pixel sensors

- ▶ Higher space-time granularity & lower material budget
- ▶ Reduce occupancy to improve tracking in high background
- ▶ Better tracking & vertex resolution at low momentum
- ▶ Adaptable to potential changes of Interaction Region

Technical choices

- ▶ Identical pixel sensor on all layers: **Optimized BELle II pIXel (OBELIX) chip**
- ▶ VTX design

iVTX (L1 & L2): “all-silicon”, self supported, **different cooling options under study**, assuming expected power consumption $\sim 300\text{mW}/\text{cm}^2$ and chip performance degradation with temperature after irradiation:

- ▶ liquid in Al-thin pipes; ▶ thermal conduction with thermal pyrolytic graphite;
→ $\sim 0.3\%$ X_0 /ladder for perpendicular tracks

oVTX (L3 to L6): carbon fiber frame, water cooled

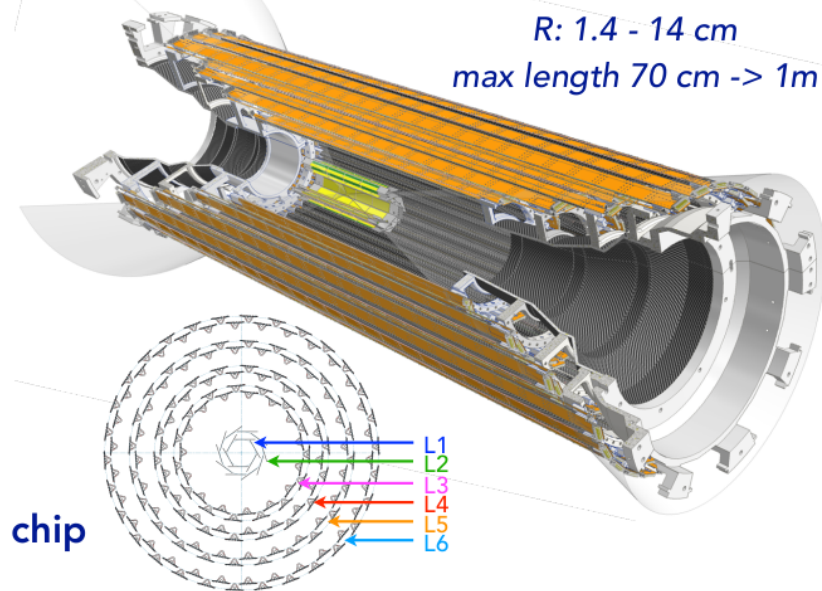
- $\sim 0.6\%$ X_0 /ladder for perpendicular tracks

⇒ **Total material budget reduced to $\sim 3\%$ X_0**

Baseline VTX layout with 6 layers

R: 1.4 - 14 cm

max length 70 cm → 1m



*Tracking performance studies carried out for different detector geometries (5 or 6 layers, with L3 placed at 39 mm or 69 mm) and material budgets
⇒ **specs evolved due to more detailed simulations***

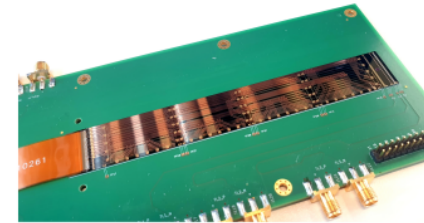
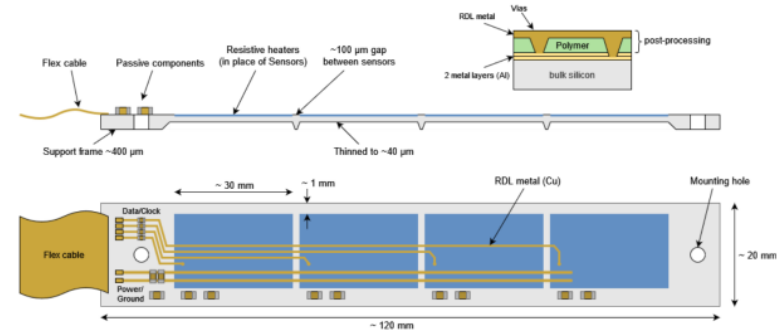
- ▶ All-silicon module, 4 contiguous OBELIX sensors diced as a block from the wafer, thinned to $50\ \mu\text{m}$, except in some border area $\sim 400\ \mu\text{m}$ thick, to ensure stiffness
- ▶ Post-process redistribution layer (RDL) for interconnection

Prototypes:

- ▶ Thermal and electrical tests on first real-size ladder with resistive heaters and two redistribution layers
 $\Rightarrow$ temperature on top of metal layers of 53°C for $1.5\ \text{W}$ dissipated/sensor

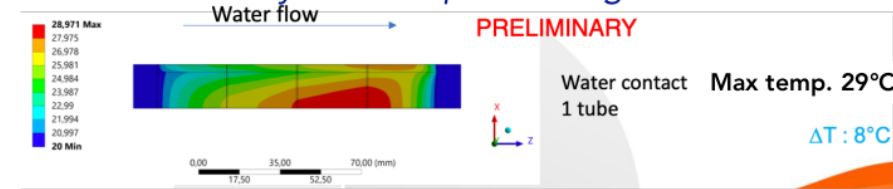
Different cooling solutions under investigation:

- ▶ Non uniform power on the chip surface: the highest density on the periphery x 10 w.r.t. matrix
 $\Rightarrow$ average power $\sim 300\ \text{mW}/\text{cm}^2$ @ hit-rate of $120\ \text{MHz}/\text{cm}^2$
- ▶ Air cooling alone might be marginal
 $\Rightarrow$ several cooling options under evaluation, liquid cooling in Al-thin pipes ($\sim 0.4\% X_0/\text{ladder}$) or thermal conduction with Thermal Pyrolytic Graphite ($\sim 0.3\% X_0/\text{ladder}$)

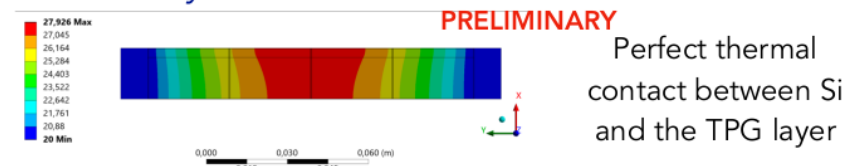


iVTX RDL demonstrator tested

Preliminary results liquid cooling simulation



Preliminary results thermal conduction simulation



Max Temperature $27,9^\circ\text{C}$ and Max 6°C gradient on modules

Ladder structure (ALICE ITS2-inspired):

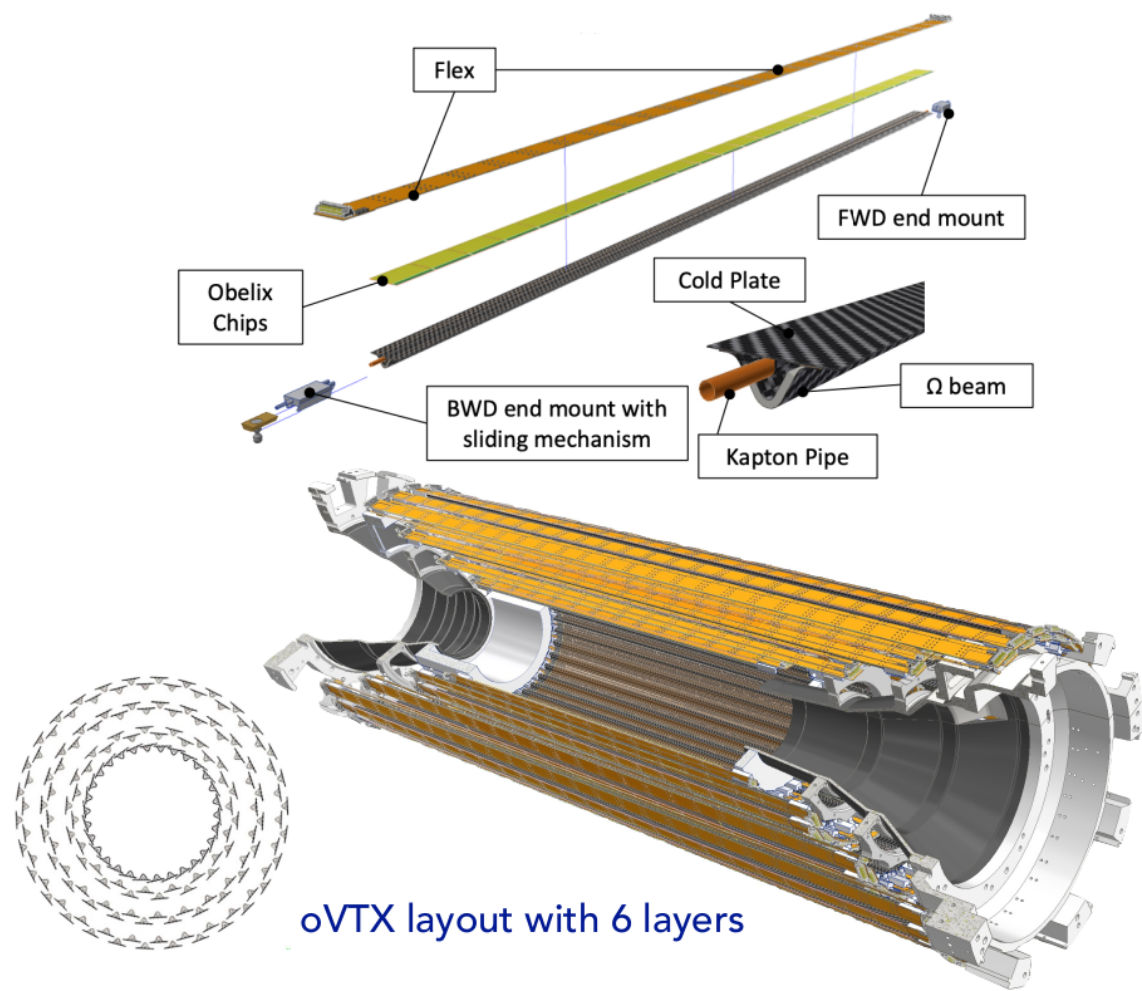
- ▶ Carbon Fiber support structure (Ω beam), cold-plate with pipes (2 or 1 pipe) with liquid cooling
- ▶ Sensor glued on cold plate, flex cables connecting each half ladder

Prototypes:

- ▶ Mechanical and thermal characterisation for the longer ladder ~70 cm (outermost layer)
- ▶ Completed the first version of the FLEX design, submitted for production at the CERN workshop after closing the chip design

Mechanical design already advanced:

⇒ 6 layer design implemented, started integration of hydraulic services



Layer	L3	L4	L5	L6	Unit
Radius	62.5-69 (*)	82.5-89 (*)	108-114.5 (*)	133.5-140 (*)	mm
#ladders	30	36	48	60	
#Sensors	12	16	20	24	/ladder

(*) staggered ladder design with two different radii per layer

VTX tracking performance

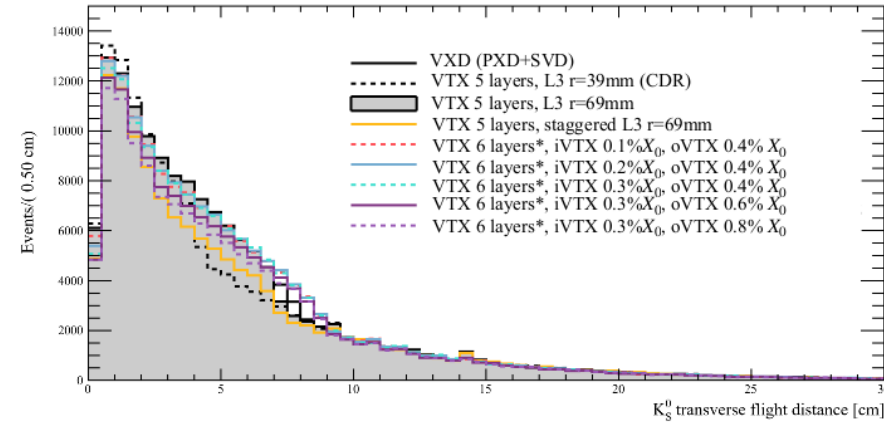
- ▶ Benchmark physics channels simulated under various background scenarios to assess VTX performance.
- ▶ Studied reconstruction efficiency (K_S and slow π), exploring:

Geometry: 5 vs. 6 layers (L3 at two different radii)

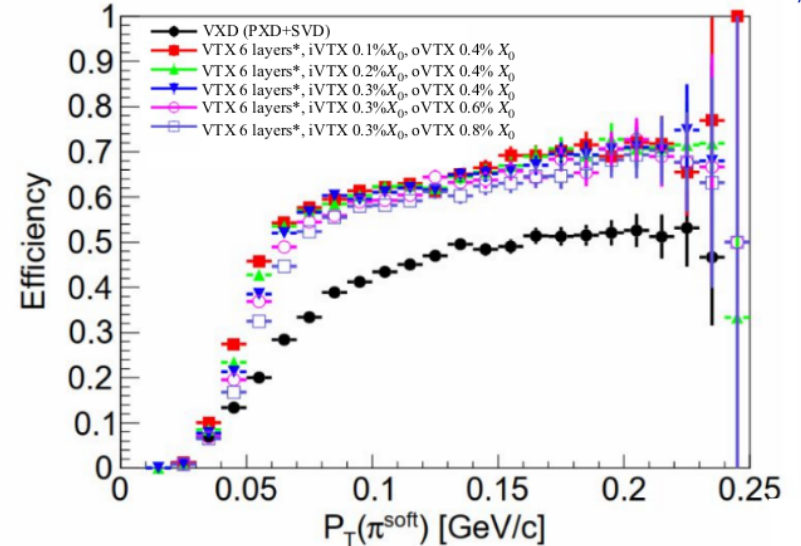
Material budget: $\rightarrow$ iVTX: 0.1%, 0.2%, 0.3%
 $\rightarrow$ oVTX: 0.4%, 0.6%, 0.8%

- ▶ For the highest background scenario better tracking efficiency than current VXD for full tracking, better vertex resolution, less sensitive to the background level than current VXD
- ▶ 6-layer geometry shows superior tracking performance compared to VTX 5 layers geometry, still good also with maximum material budget (iVTX: 0.3%, oVTX: 0.8%)

K_S^0 reconstruction efficiency (from $B^0 \rightarrow J/\Psi + K_S^0$)



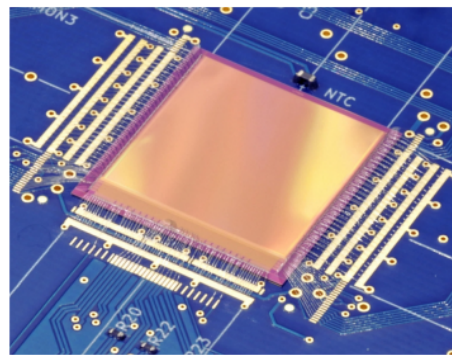
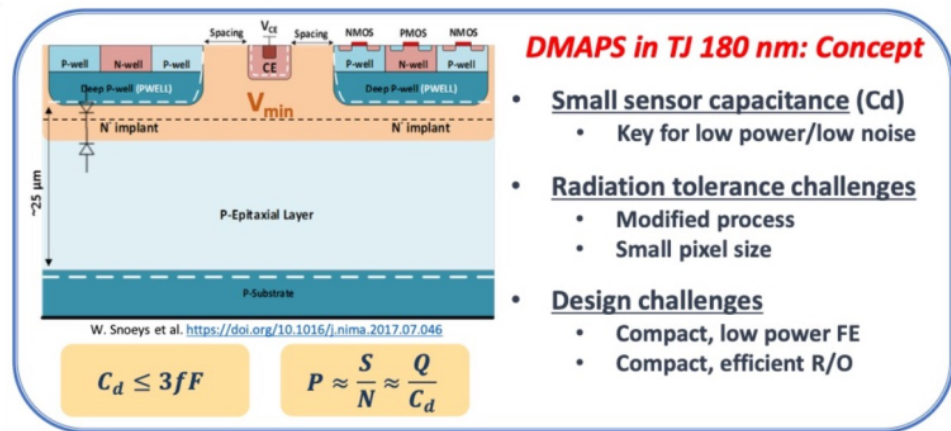
Soft π reconstruction (from $B^0 \rightarrow (D^0 + \pi^-) + \mu^+ \nu_\mu$)



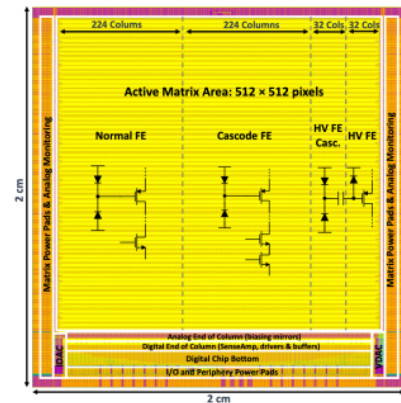
TJ-Monopix2 (TJMP2) as forerunner of OBELIX

Developed for ATLAS (ITK outer layers), DMAPS Tower Semiconductor 180 nm CMOS process but modified process to improve rad-hardness & faster readout (verified good performance for high fluence at low temperature)

- ▶ $33 \times 33 \mu\text{m}^2$ pitch, 25 ns integration, large matrix 512×512 pixels ($2 \times 2 \text{ cm}^2$)
- ▶ 7 bit ToT information, 3 bit in-pixel threshold tuning
- ▶ Column drain readout capable to handle $>> 120 \text{ MHz/cm}^2 \rightarrow$ triggerless in TJMP2
- ▶ Various sensing volume thicknesses (epi- $30 \mu\text{m}$, CZ-bulk)
- ▶ 4 front-end flavors with differences in the amplifier and detector input coupling (AC- or DC-coupled)



TJ-Monopix2 sensor bonded on a test board



Layout of TJMP2 sensor: divided in 4 regions with different FE

Test of TJMonopix2 for OBELIX and VTX design

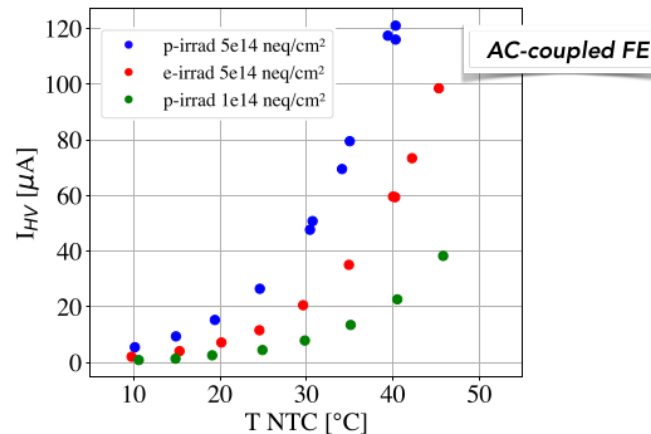
Additional characterisation of all FEs at higher temperature to validate performance critical for OBELIX and VTX design (e.g. cooling requirements)

- ▶ Focus on degradation after irradiation as temperature increases
⇒ define safe and efficient operating temperature range
- ▶ Tests performed with heating/cooling setup using Peltier cell
⇒ wide temperature range explored

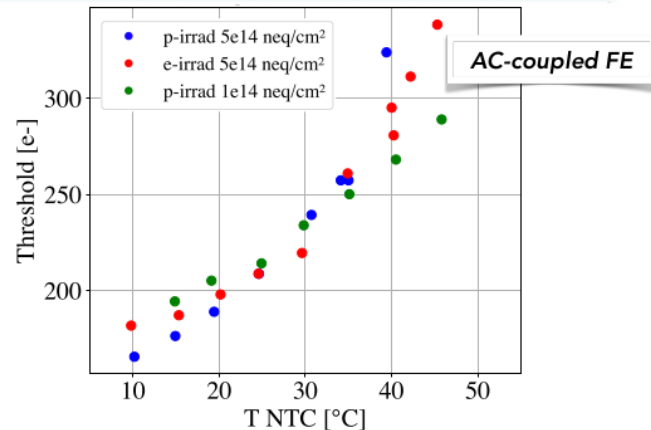
Sensor temperature (T_{chip}) $\sim 7^\circ\text{C}$ higher than PCB (T_{NTC})

- ▶ After irradiation leakage current significantly increases, as expected from bulk damage, and scales with temperature
- ▶ **e-irradiated** chip shows lower leakage current (about factor 2) than **p-irradiated** one at the same 1MeV equivalent fluence (NIEL $5 \times 10^{14} n_{\text{eq}}/\text{cm}^2$) ⇒ lower bulk damage at the same 1MeV equivalent fluence
- ▶ After irradiation also threshold increase with temperature, effect of the higher leakage current causing a faster discharge of the collecting electrode

Leakage current vs Temperature at max bias



Threshold () vs Temperature at max bias*



() optimised settings in each sensor to reach similar threshold*

TJMP2 Test Beam

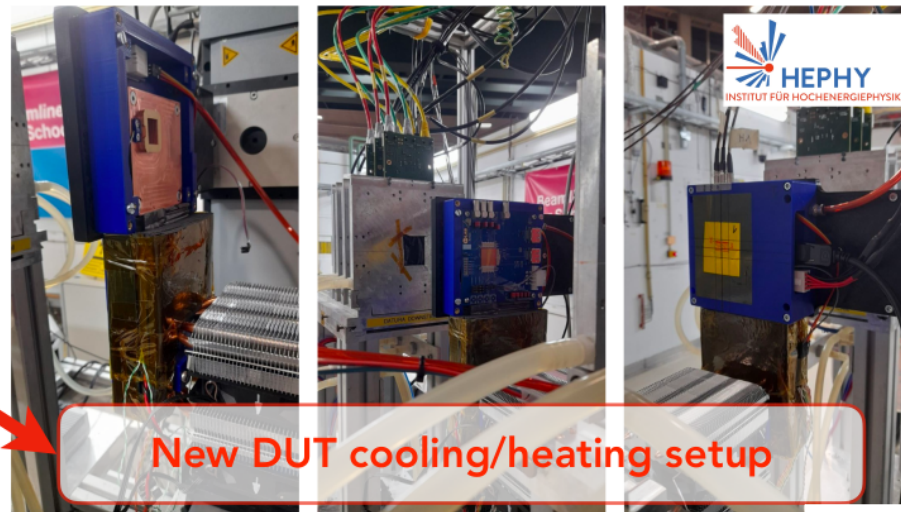
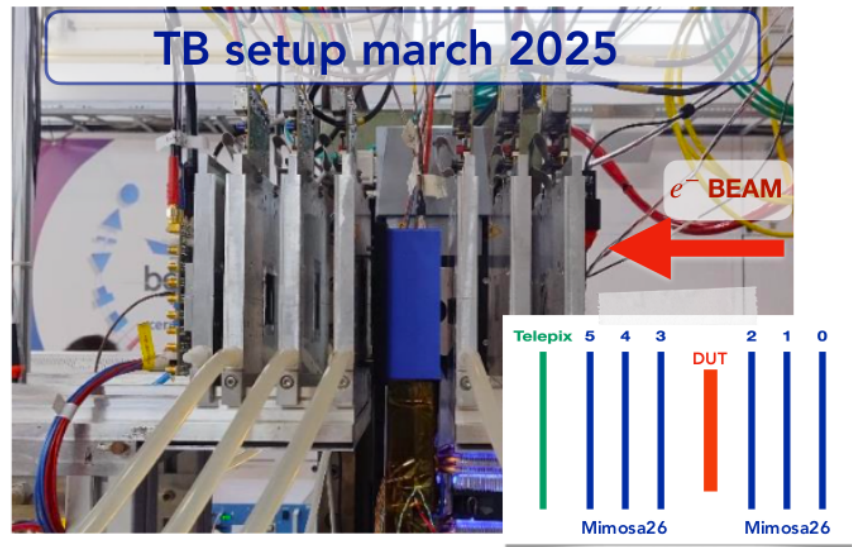
- ▶ Multiple test beam campaigns with **3–5 GeV electrons** at DESY from **2022 to 2024**. Confirmed expected performance of non-irradiated sensors (see backup)
- ▶ Test beam in March **2025** to study irradiated sensors at **different NIEL fluences** and for a wider **operating temperature range**

→ Tested **4 different irradiated** chips:

3 p-irradiated ($\text{NIEL } 1 \times 10^{14} \text{ to } 5 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$)

1 e-irradiated ($\text{NIEL } 5 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$)

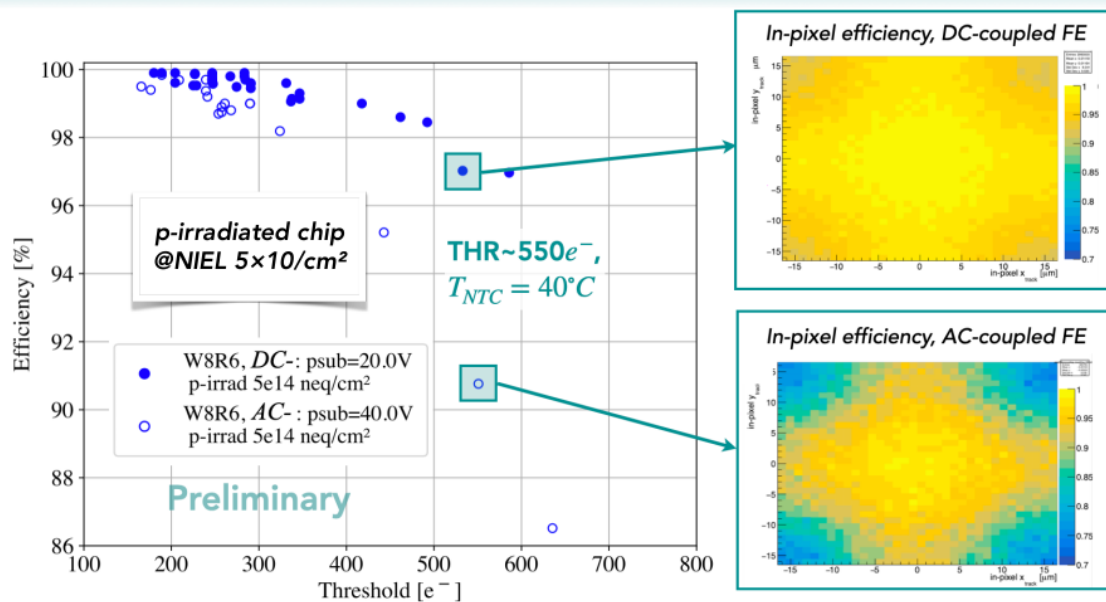
→ **New DUT cooling/heating setup** using Peltier cell: precise and stable temperature control in wide temperature range, calibrated pre-TB



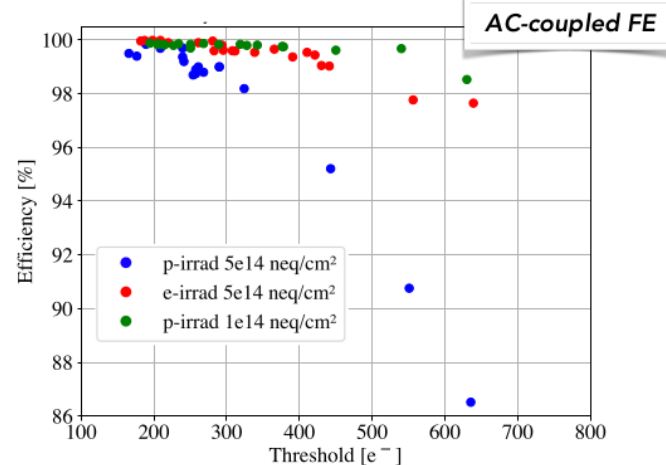
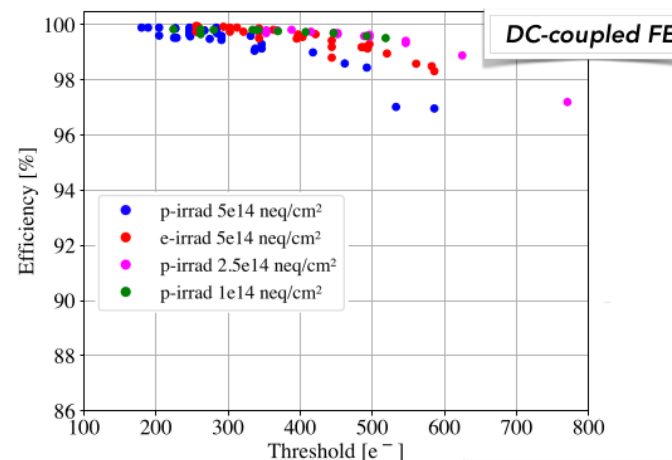
TJMP2 Test Beam 2025 - preliminary results (1)

- Efficiency depends on irradiation level: Less irradiated chips show higher efficiency, even at higher thresholds
- e-irradiated chip** has clearly higher efficiency than the **p-irradiated chip** at the same fluence ($\text{NIEL } 5 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$), suggesting lower bulk damage
- At the same threshold p-irradiated chip ($\text{NIEL } 5 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$) shows stronger degradation on AC- compared to DC-coupled frontend

Comparison between DC vs AC-coupled FE - Efficiency vs Threshold (*) at max bias



Efficiency vs Threshold (*) at max bias



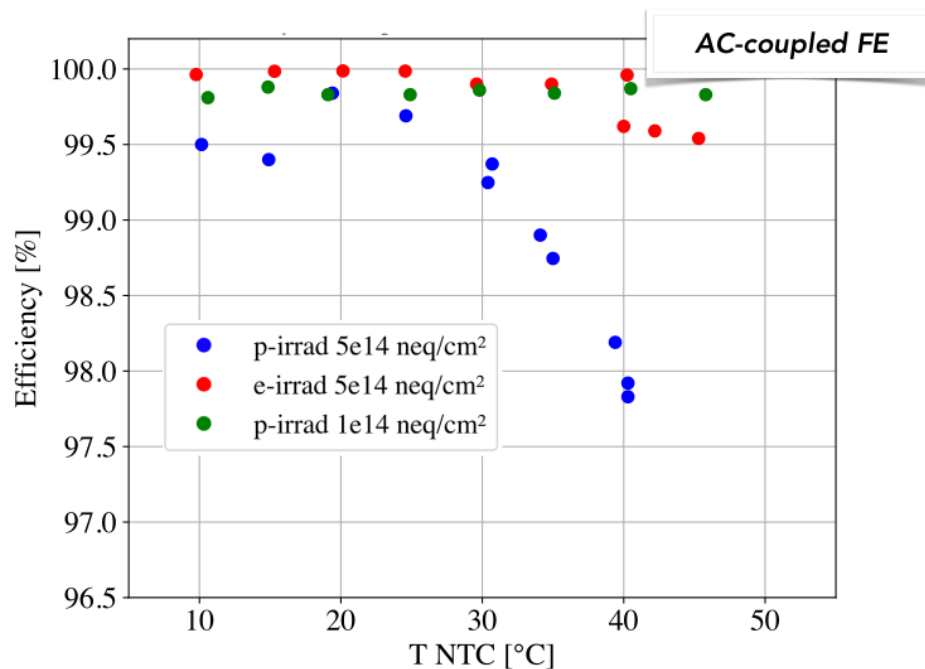
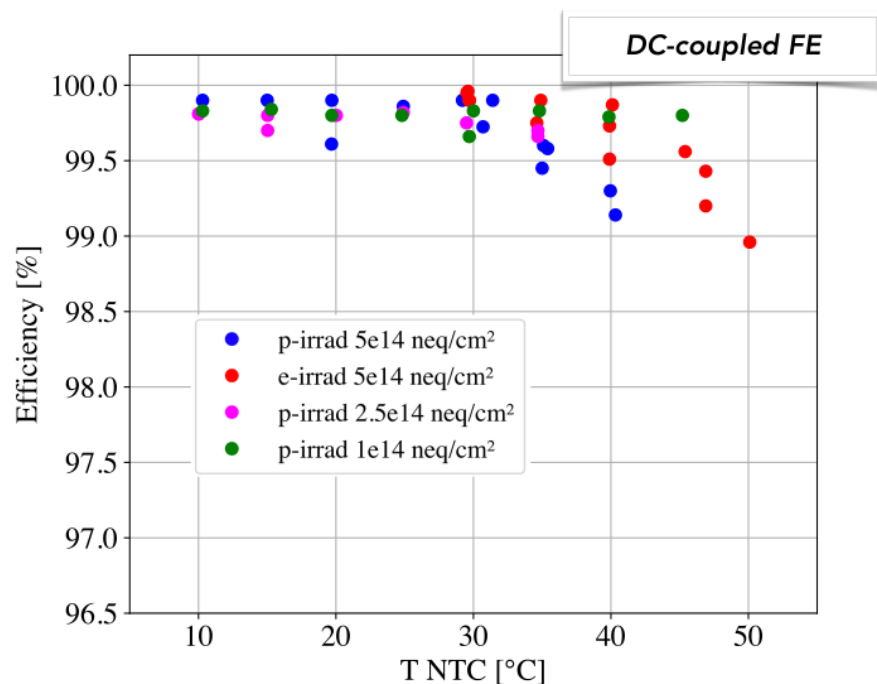
(*) different FE settings and temperature

TJMP2 Test Beam 2025 - preliminary results (2)

- ▶ Efficiency degrades with temperature after irradiation, especially for AC-coupled FE; DC-coupled remains >99% efficient up to $T_{\text{NTC}} \sim 40^\circ\text{C}$
- ▶ Operation above 40°C is challenging due to increased leakage current and noise

Efficiency vs Temperature for same FE settings at max bias

$$T_{\text{Chip}} \sim T_{\text{NTC}} + 7^\circ\text{C}$$

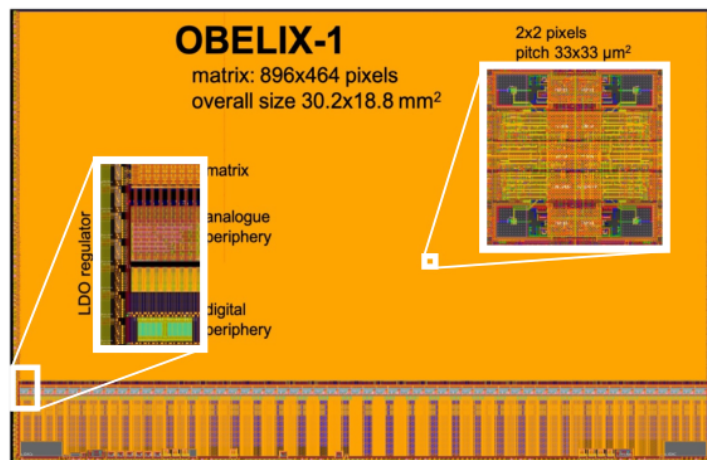


OBELIX sensor design

- ▶ Based on current characterisation results on TJMP2, 2 FE flavors are chosen for OBELIX on equal area
- ▶ OBELIX design with new digital periphery with trigger logic for Belle II and optional features to allow Track Trigger capability and finer time-stamping for outer layer hits (low rate)
- ▶ First full scale prototype OBELIX-1 sensor ~ ready submission in winter 2025

Pitch	33 μm
Signal ToT	7 bits
Time stamping	50 to 100 ns
Fine time * stamping	~5 ns for hit rate <10 MHz/cm ²
Hit rate max for 100% eff.	120 MHz/cm ²
Trigger handling	30 kHz with 10 μs delay
Trigger * output	~10 ns resolution with low granularity
Power (with hit rate)	200 to 300 mW/cm ² (1 to 120 MHz /cm ²)
Bandwidth	1 output 320 MHz

* optional features



*Matrix inherit from TJ-Monopix2,
size adjusted*

⇒ Values obtained from post-layout simulations

Analog:

- ▶ Column drain architecture from TJ-Monopix2
- ▶ Monitoring ADC
- ▶ Temperature sensors

Power pads:

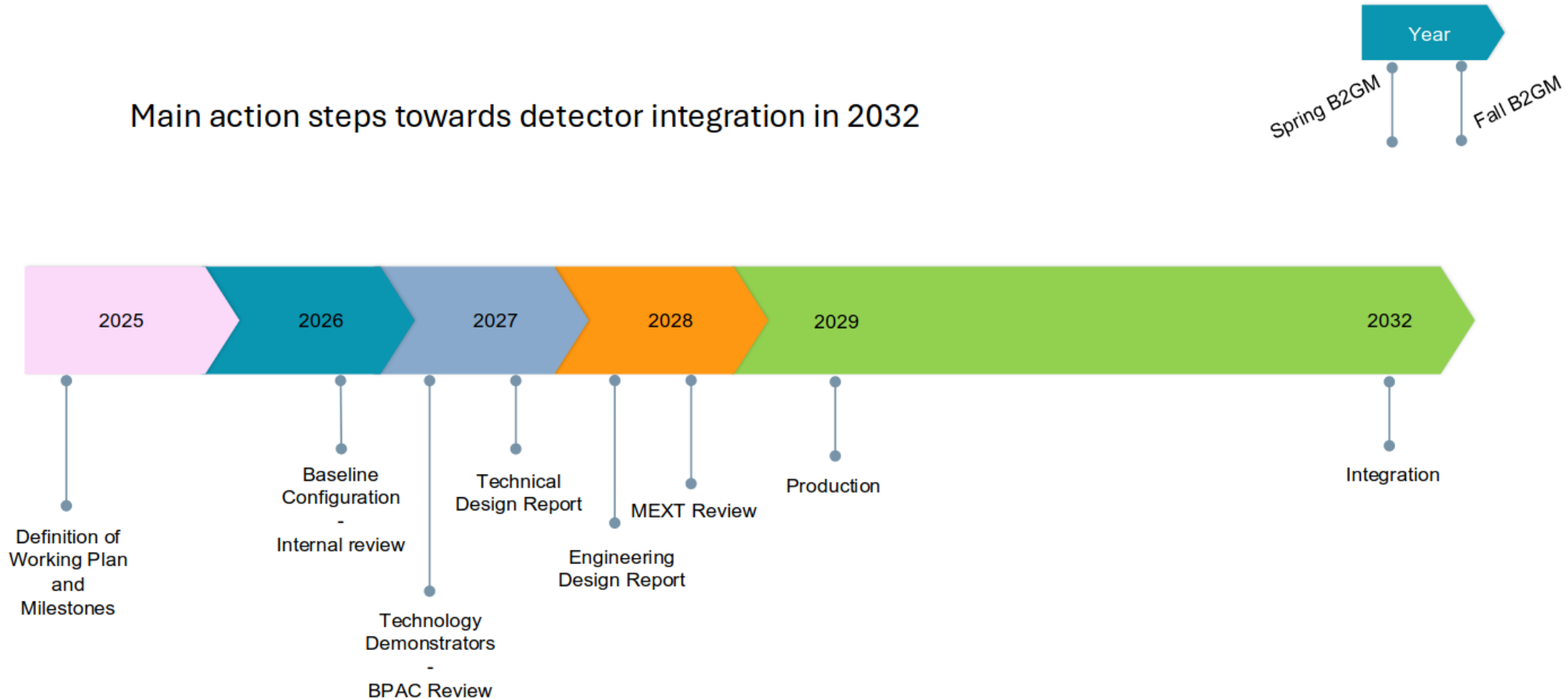
- ▶ On-chip LDOs voltage regulators

Digital periphery:

- ▶ Two new modules adapted for Belle II trigger:
 - ⇒ TRU: Pixel readout, trigger processing
 - ⇒ TTT: Fast transmission in parallel

Proposed Steps Towards LS2 (2032)

Main action steps towards detector integration in 2032



Summary

- ▶ SuperKEKB upgrade required to reach target luminosity $6 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$, including a possible major redesign of the Interaction Region (IR)
- ▶ The current VXD performs well, but has a limited safety margin under high background conditions
- ▶ Upgrade proposed: new vertex detector (VTX) based on DMAPS with new development of a new OBELIX sensor
- ▶ Extensive lab tests and test beam campaigns on TJ-Monopix2 to validate performance for OBELIX and VTX
- ▶ March 2025 test beam with TJMP2 successfully completed on irradiated chips (various fluences), with improved temperature control.
 - Efficiency after irradiation shows temperature-dependent degradation, especially for AC-coupled frontend
 - DC-coupled frontend after irradiation maintains >99% efficiency up to $\sim 40^\circ \text{C}$ with $\text{THR} \sim 350 \text{ e}^-$
 - Stable operation with $\text{THR} \sim 200 \text{ e}^-$ at lower temperature

Thanks for your attention!

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

VTX collaboration

IGFAE, Santiago
University of Bergamo
University of Bonn
University of Dortmund
University of Göttingen

Jilin University
KIT, Karlsruhe
IPMU, Kashiwa
Queen Mary University of London
CPPM, Marseille

IJCLab, Orsay
RAL, Oxford
INFN & University of Pavia
INFN & University of Pisa
IFCA (CSIC-UC), Santander

IPHC, Strasbourg
University of Tokyo
KEK, Tsukuba
IFIC (CSIC-UV), Valencia
HEPHY, Vienna

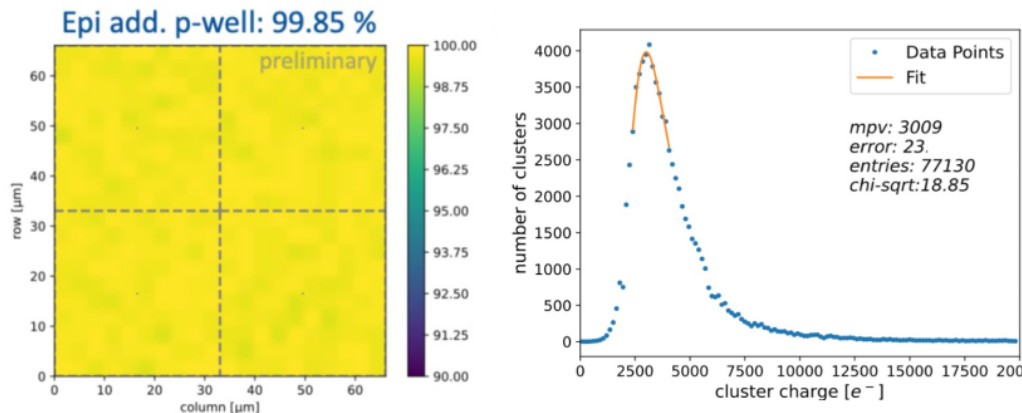
TJMP2 Test Beam

Several beam test campaigns
(DESY, 3-5 GeV electrons)

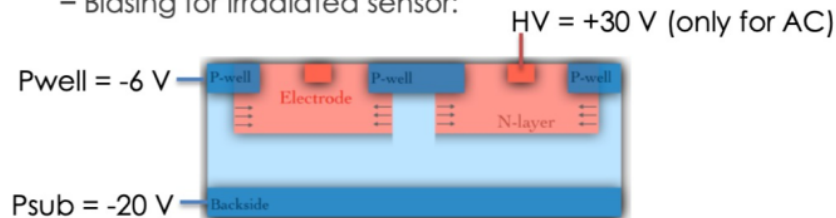
- **July 2022:** non-irradiated sensors and high threshold $500 e^-$ (un-tuned chips)
 - Efficiency $\sim 99\%$
 - Position resolution $\sim 9 \mu\text{m}$
- **July 2023:** low threshold $250\text{-}300 e^-$ and irradiated sensor $5 \times 10^{14} \text{ neq/cm}^2$ with 24 MeV protons
 - Confirmed good performance and high efficiency after irradiation, increasing bias

Room temperature, without NTC temperature monitoring

Results TB July 2022



– Biasing for irradiated sensor:



Results TB July 2023

FE amplifier	Coupling	Efficiency [%]
Normal	DC	99.99
Cascode	DC	99.79
Normal	AC	98.11
Cascode	AC	99.13

