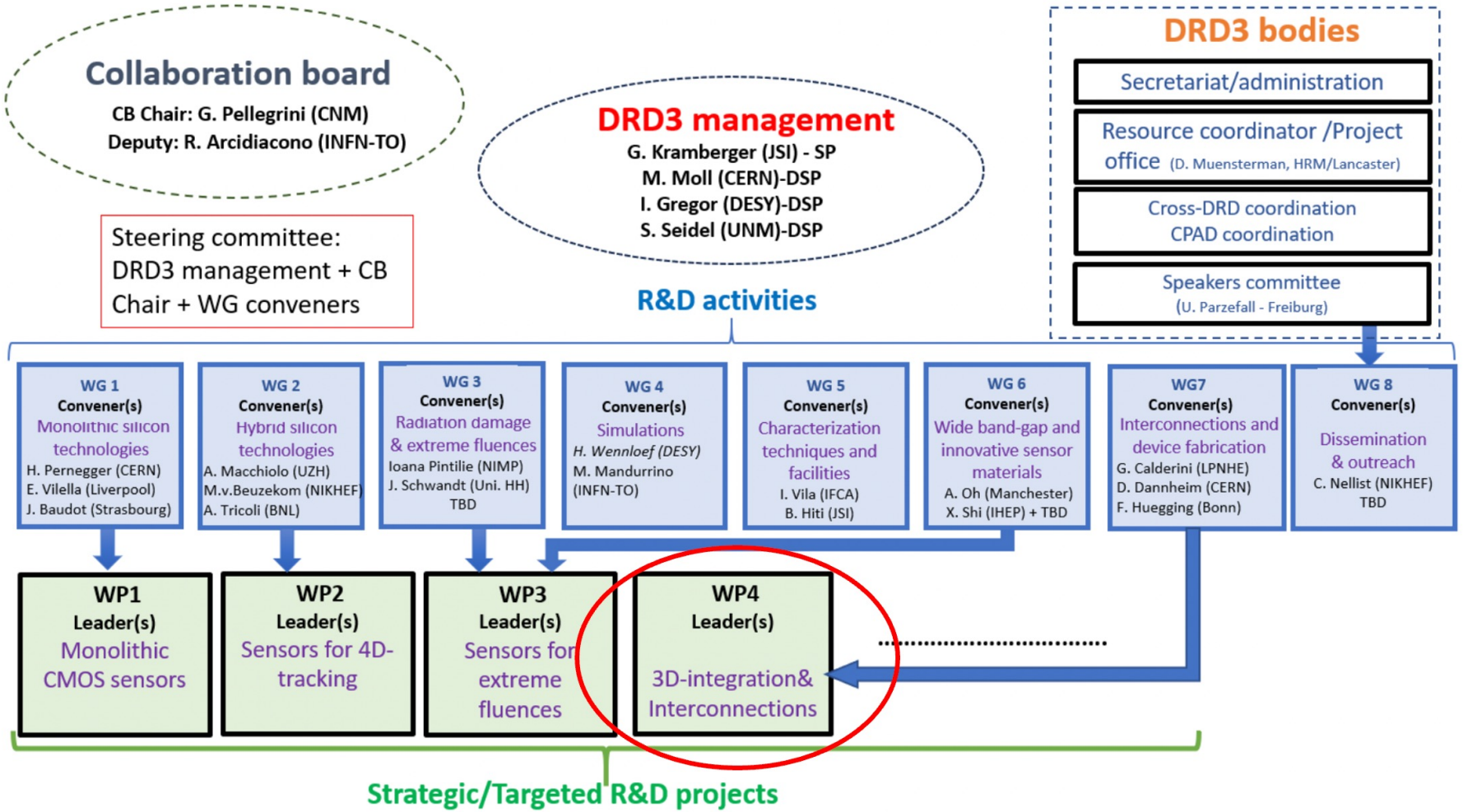
Some DRD3/WP4 highlights

DRD3 WP4: Interconnection technologies



One of the four ECFA strategic axes for solid state detectors, translated in the 4 WP of DRD3

Interconnections

In-house plating, hybridization and module integration technologies for pixel detectors

DRD3 WP4: Context for fast interconnections

Need to provide fast, cheap and reliable interconnection technology (pixel die-to-die but also die-to-flex)

This will boost the R&D in laboratories

Desired advantages:

- Single die processing
- Adaptable to the application
- Low temperature process
- Maskless
- In-house (short turnaround time, quick adjustments)
- Cheap

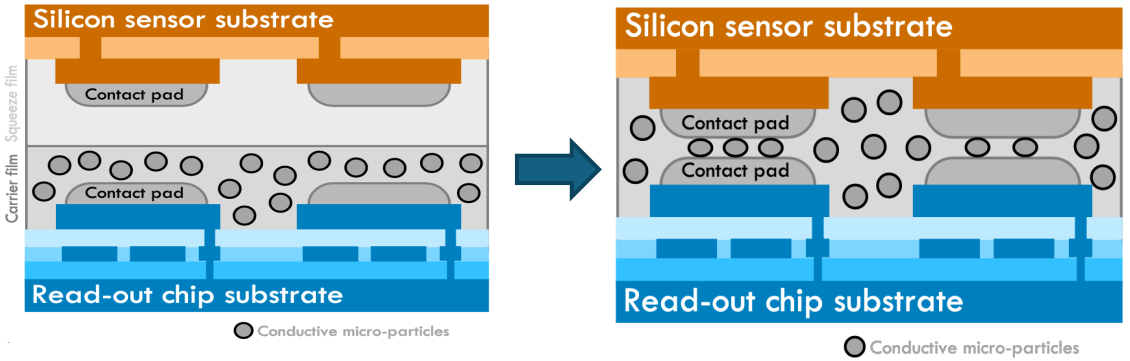
Some possible solutions

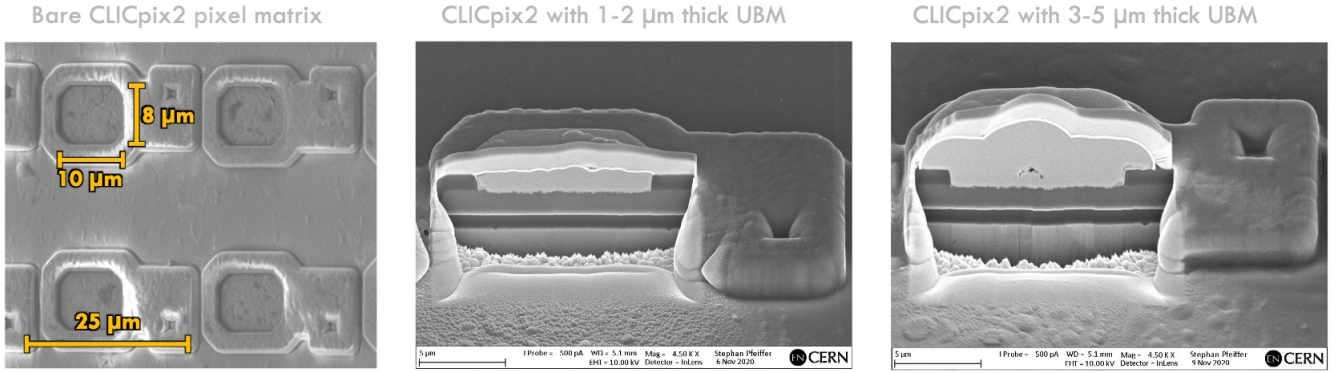
- Use of Anisotropic Conductive Films (ACF) or Pastes (ACP)

  UBM is still required to obtain the particle adhesion, but it is a wet chemical deposition of Ni and Au (maskless process, low cost)
- Interconnection via gold stud deposition

Activity ACF/ACP

Started in the framework of AIDAInnova (and now DRD3 project)





See: P. Svihra,
https://indico.cern.ch/event/1104064/contributions/4789884/attachments/2416826/4135907/svihra_AIDA2022_ACF_update.pdf
or A. Lale et al. "Pixel detector hybridization with anisotropic conductive adhesives" PIXEL 2024, Strasbourg, 18-22/11/2024
https://indico.in2p3.fr/event/32425/contributions/142775/

In-house post-processing of devices: Nickel-Gold (ENIG), mask-less

Deposition of epoxy film or compound with small (3-5µm) conductive particles

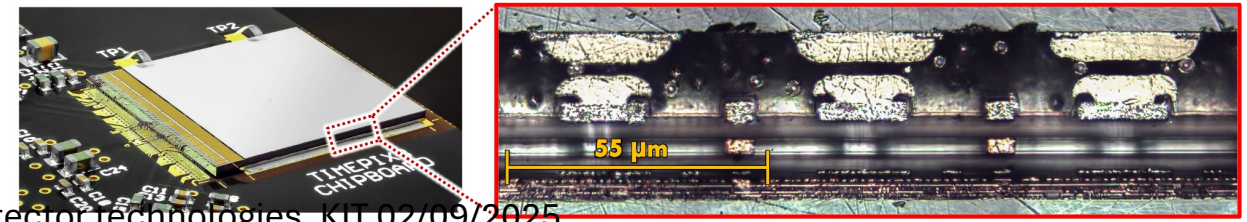
Film or paste produced by company; can be optimized depending on the device

Thermo-compression: 150C, 500N/cm2

Being demonstrated in AIDAInnova but only preliminary results

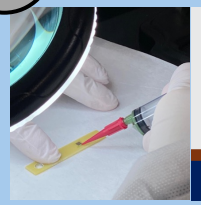
Need full process optimization and validation in real conditions

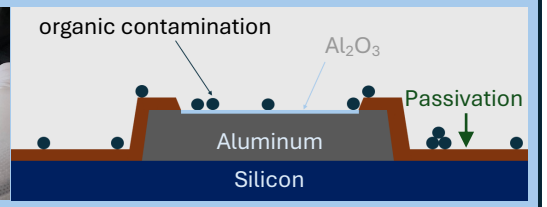
(mechanical and thermal stress, radiation hardness)



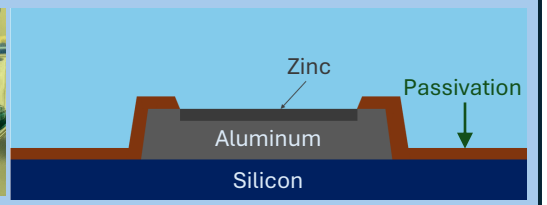
ENIG process

1 Pre-treatment & zincation

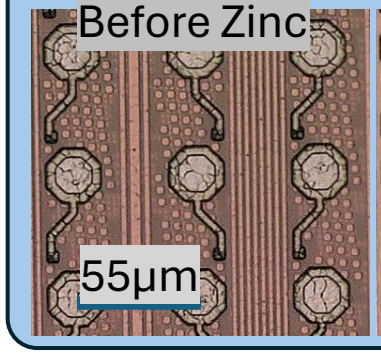




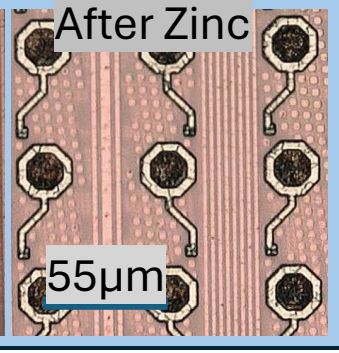
1. Glue chip on holder
2. Plasma cleaning
3. Conditioner/Etching
4. Zincation



Before Zinc

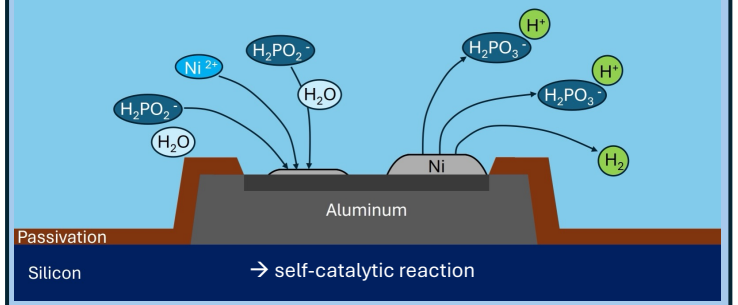


After Zinc



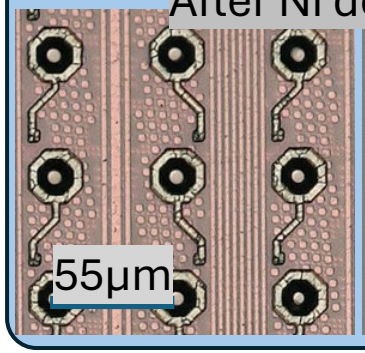
2 Electroless Nickel deposition (creation of the bump)

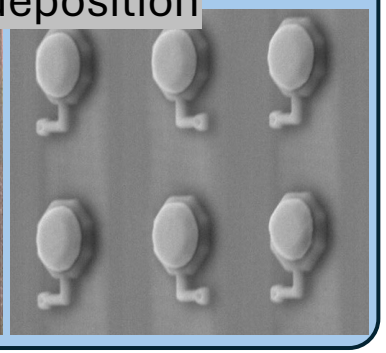
$$2H_2PO_2^- + Ni^{2+} + 2H_2O \rightarrow 2H_2PO_3^- + H_2 + 2H^+ + Ni^0$$



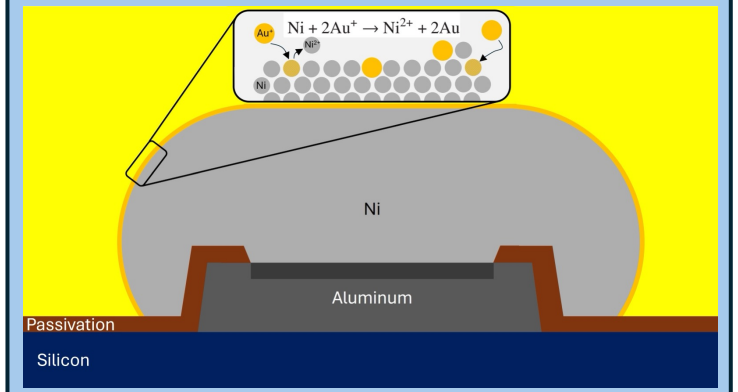
→ Uniformity, Reproducibility
Time, Stirring, Temperature, pH,...

After Ni deposition



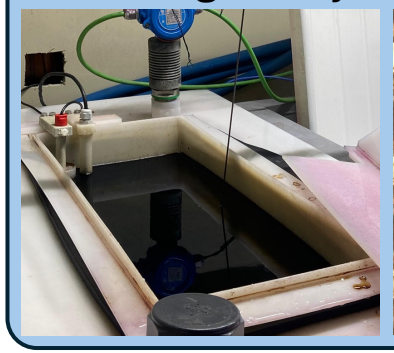


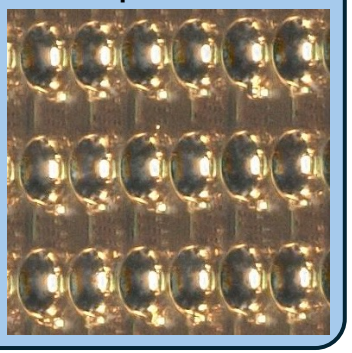
3 Immersion Gold



→ Corrosion protection

Thin gold layer of <1µm

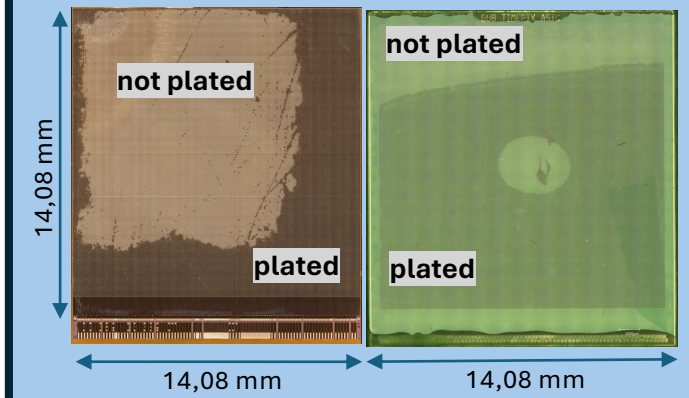




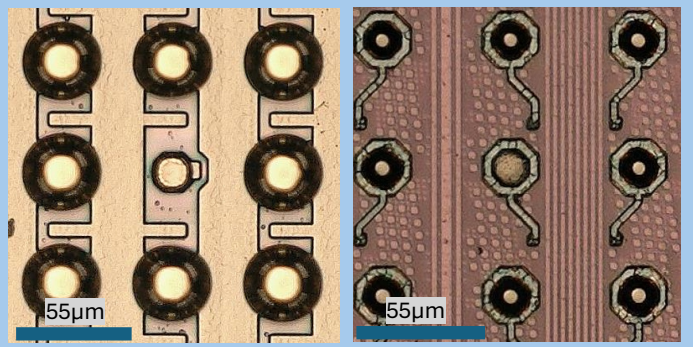
https://indico.cern.ch/event/1507215/contributions/6536927/attachments/3081924/5455260/DRD3_Week_Amsterdam_Lauser.pdf

Solved issues

Skipped areas

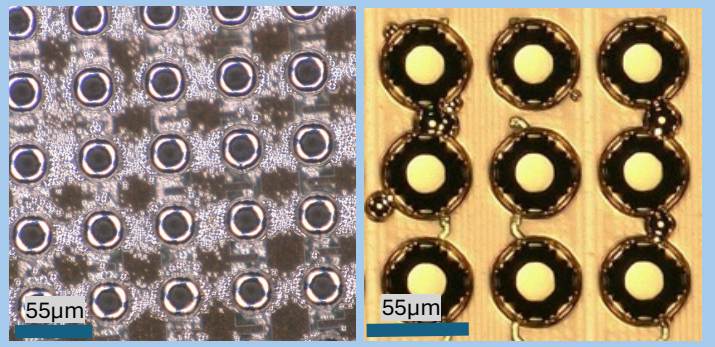


Skipped pads



Poor zinc coating or contamination that shields the pad during nickel plating

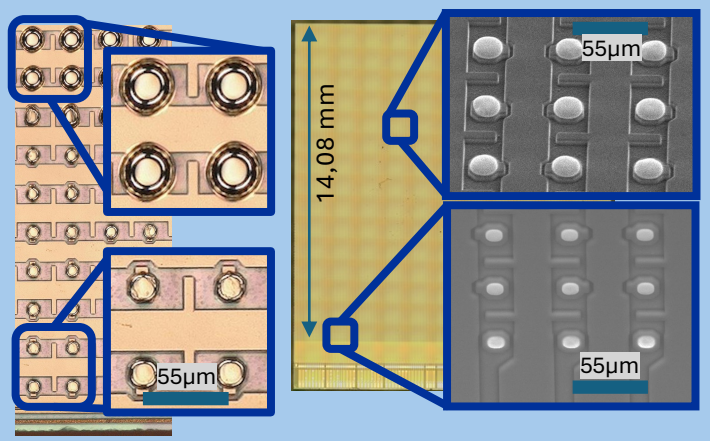
Over-plated areas



unwanted nickel deposition due to unstable nickel solution or porous passivation

Current Focus

Uniformity



- Sometimes the bumps are smaller at the edge than in the center of some chips
- Good uniformity is important for reliable bonding with high yield and connections

→ Systematic study to analyze uniformity

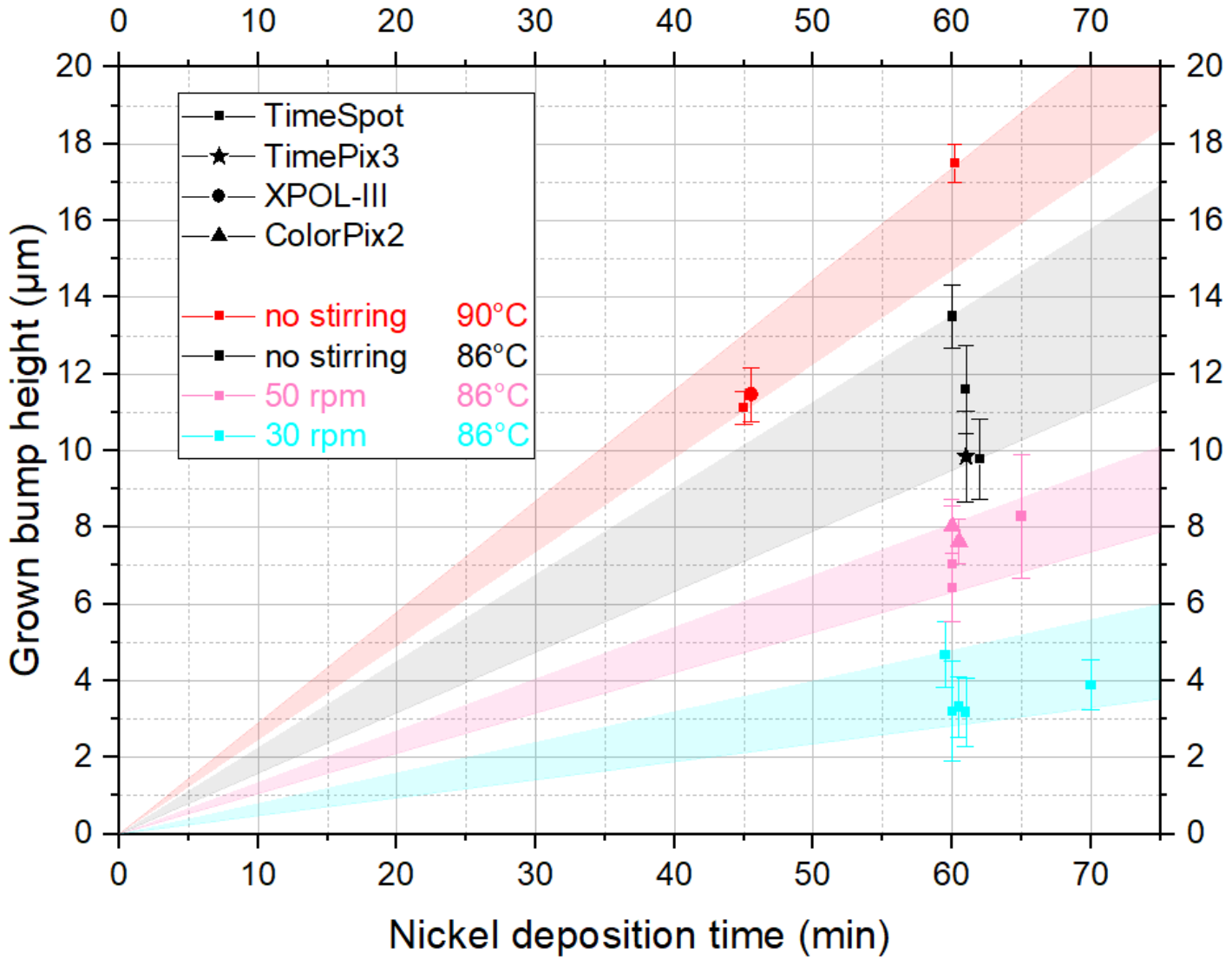
Goal: Improvement of uniformity for all types and sizes of chips

Process parameters

Uniform bump height over the entire chip

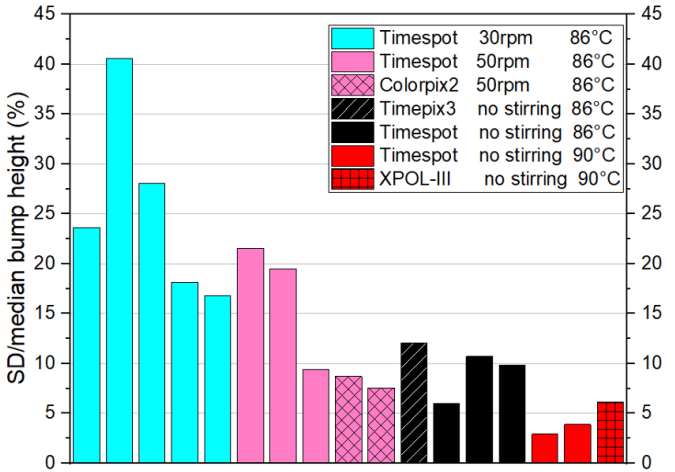
See presentation of Moritz Lauser in tomorrow's session

Systematic process development



1. Processing temperature and stirring affect the deposition rate
2. Different chips behave similarly for similar treatment

Percentage standard deviation in relation to the bump height



Flip-chip hybridisation

Our goal is to develop single-die hybridisation techniques that offer the community a reliable solution for prototyping and sensor/ASIC development

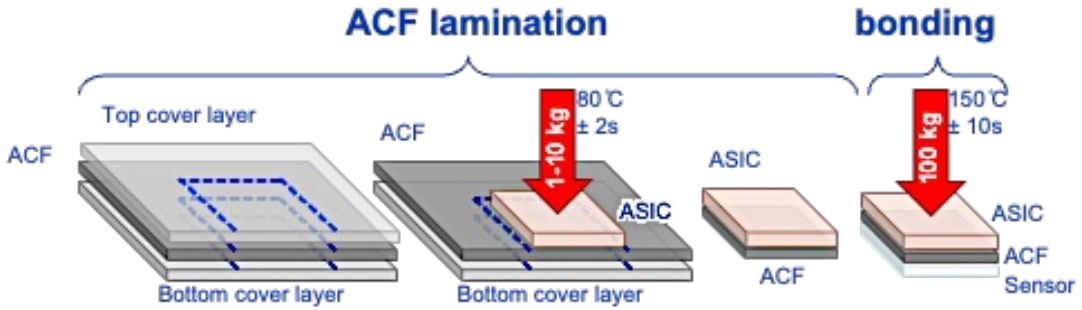
UNIVERSITÉ DE GENÈVE
FACULTÈ DES SCIENCES

- Bonding done at Geneva University using semi-automatic flip-chip bonder
  - Precise temperature, pressure and alignment control (post bonding accuracy from 1 to 2 µm)
  - Heating up to 400 ℃ and force applied up to 100 kgf
  - Available for bonding with Gold Studs and **A**nisotropic **C**onductive or **N**on-conductive **F**ilm/**P**aste – **ACF/ACP/NCP**

Flip-chip bonder SET ACCµRA100

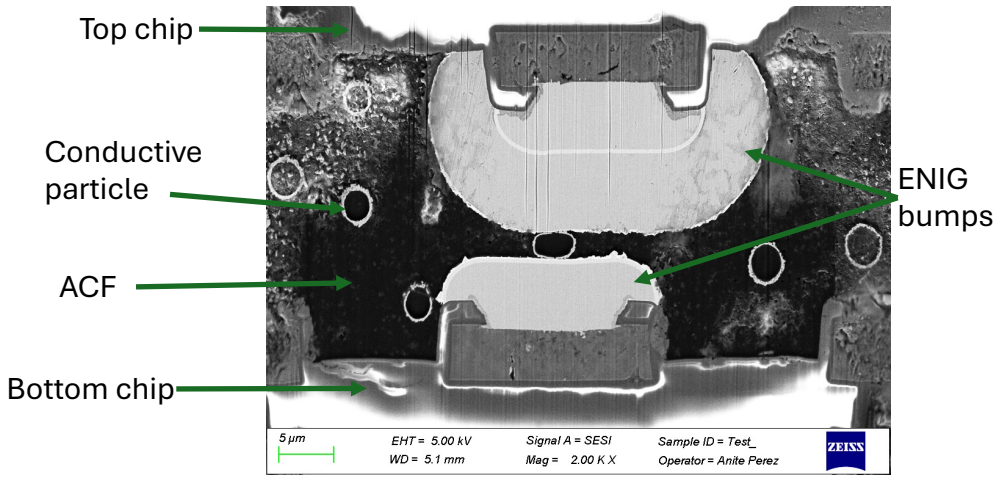
ACF bonding has two steps:

- Lamination of an adhesive film containing conductive microparticles
- Flip-chip bonding



Previously, we presented ACF hybridisation results on test chips with a 55 µm pitch, showing connection yields around 98% and good resistance to thermal cycling.

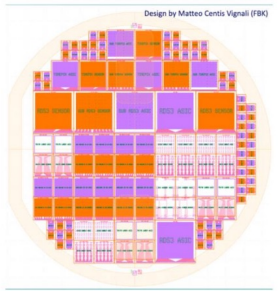
Cross-section of ACA bonded chips

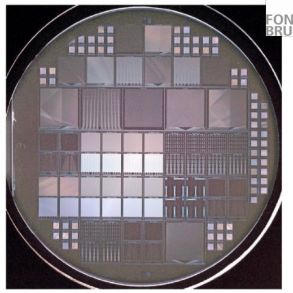


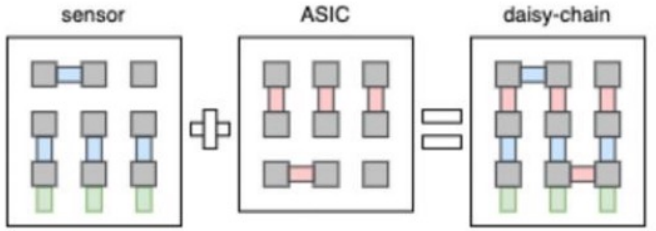
Characterisation tools

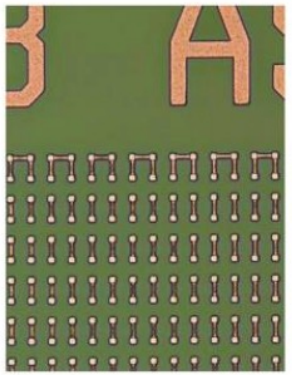
Yield optimization depending on device characteristics (pixel pitch, device size etc)

Wafer layout with different sensor types has been designed at LPNHE in collaboration with CERN and FBK which then produced it; system of conductive chains to measure the interconnection reliability and yield

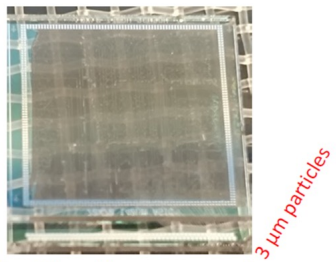




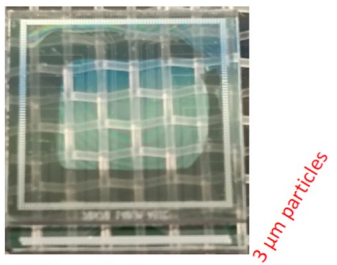




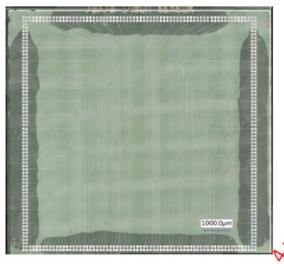
	pitch	size in mm	connections	per wafer	type
160x160 20um	20 um	3.2 x 3.2	25600	36	grid
CLICpix2	25 um	3.2 x 3.2	16384	34	grid
400x400 25um	25 um	20 x 20	640000	5	grid
Timepix3	55 um	14 x 14	65536	4	grid
Timepix3 islands	55 um	14 x 14	65536	4	grid
RD53	50 um	20 x 20	160000	4	grid
RD53 islands	50 um	20 x 20	160000	2	grid
70x70 140um	140 um	20 x 20	2112	3	peripheral
10x10 1000um	1000 um	20 x 20	400	3	grid
3x3 4500um	4500 um	20 x 20	36	1	grid



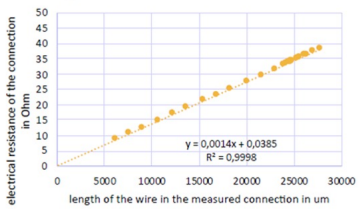
18 µm ACF – resistance measurement

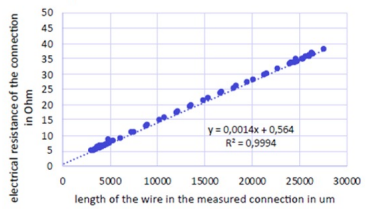


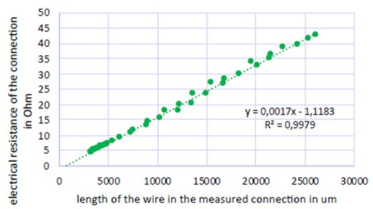
14 µm ACF – resistance measurement



ACP – resistance measurement







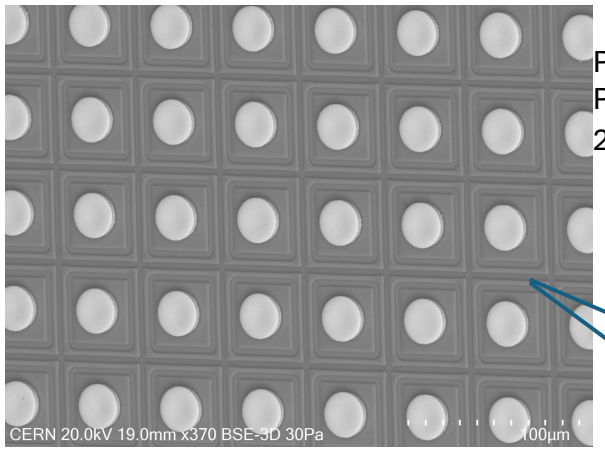
Preliminary measurements on the very first structures indicate very good conductivity (connection resistance <1 Ohm) and yield between 98 and 99%
To be studied more systematically

Hybridization of Timepepix-3 with TI-LGAD

Ti-LGAD: Trench Isolated Low Gain Avalanche Diode
64x64 pixel matrix from W2, FBK-AIDAinnova production

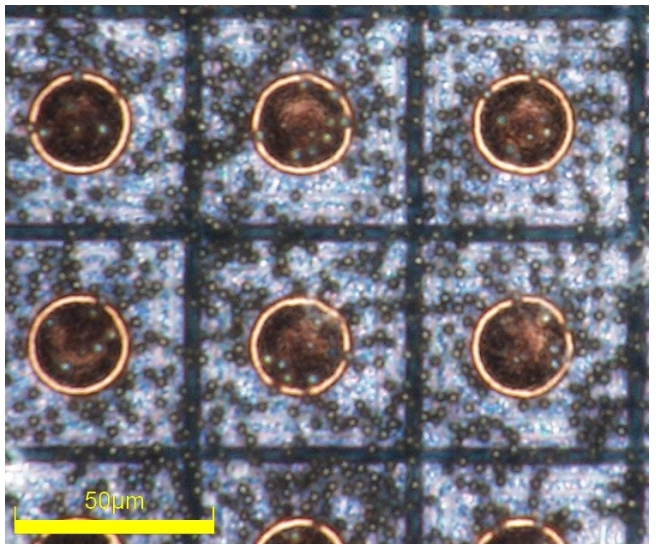
EP-DT
Detector Technologies

5 µm UBM (by IZM) on Ti-LGAD sensor

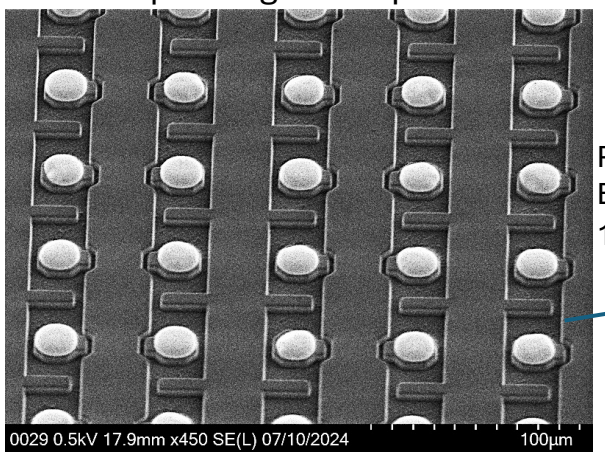


Pitch: 55 µm
Pad diameter: 25 µm

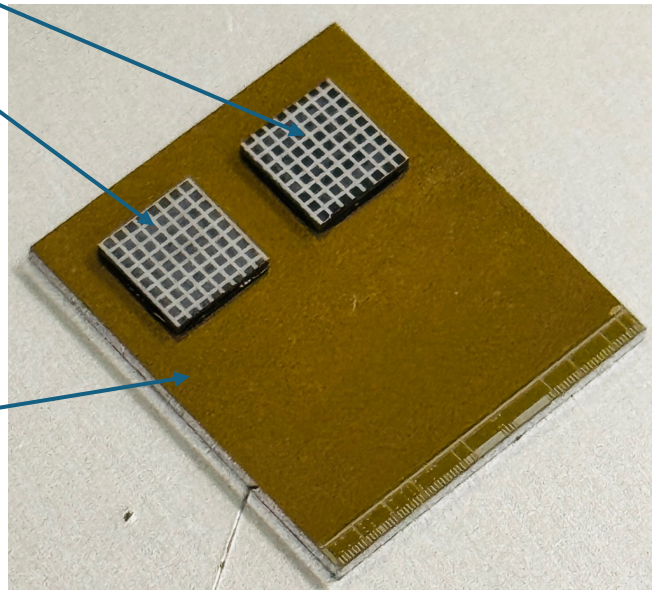
ACF laminated on Ti-LGAD



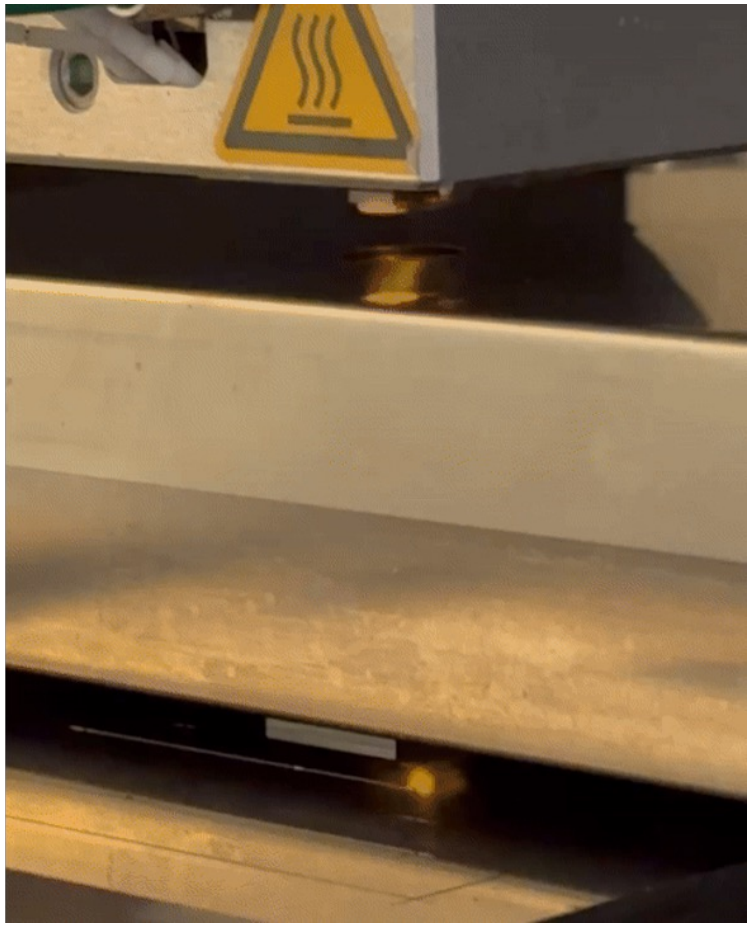
In-house ENIG plating on Timepix3 ASICs ~6 µm height bumps



Pitch: 55 µm
Bump diameter: 19 µm



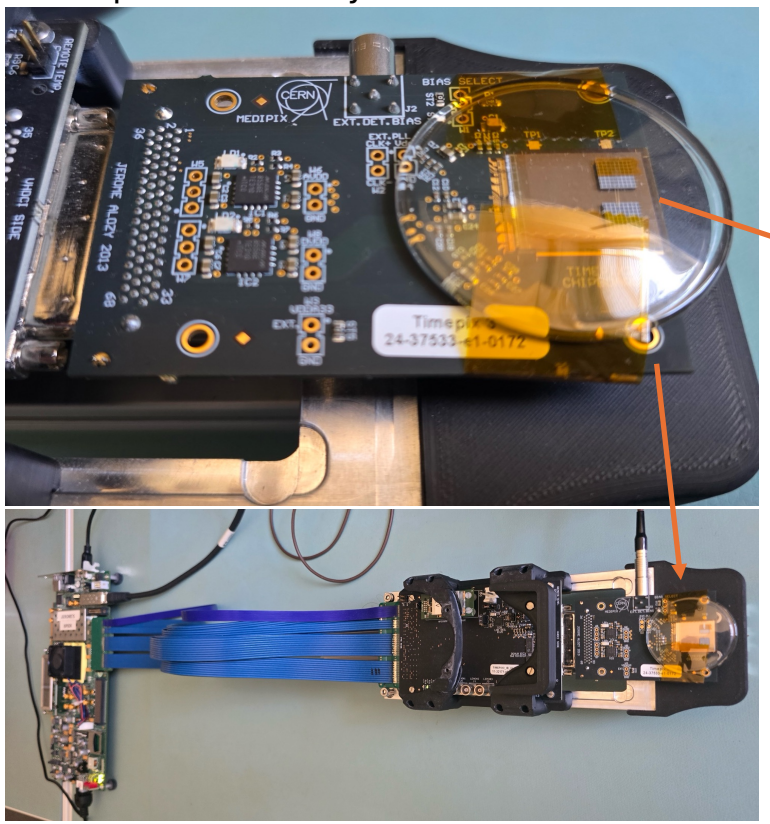
Flip-chip bonding using 18 µm thick ACF with 3 µm particles

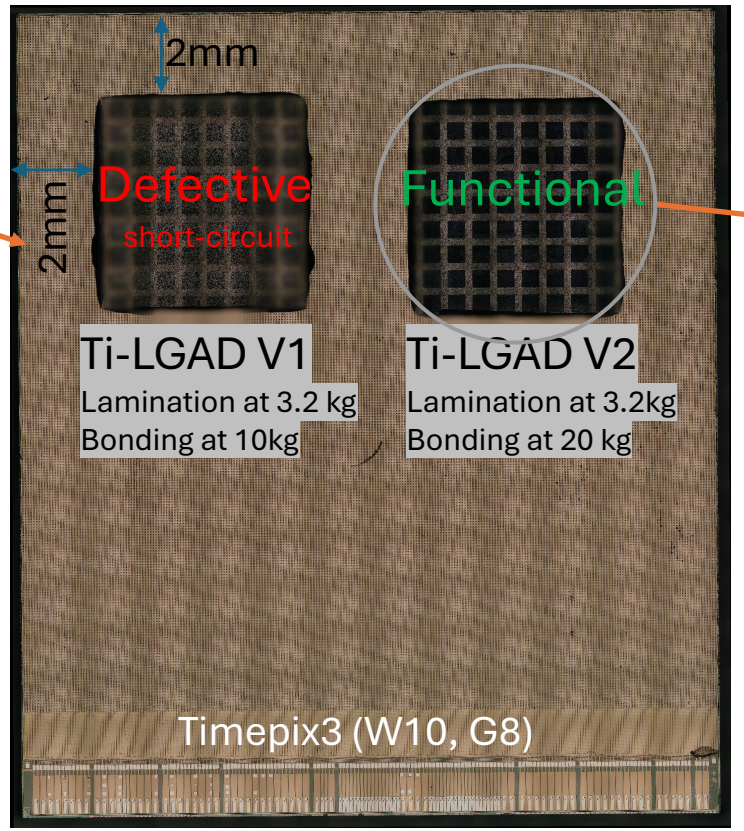


https://indico.cern.ch/event/1507215/contributions/6536930/attachments/3082160/5455757/06%2025%20Ahmet%20LALE%20DRD3%20week%203.pdf

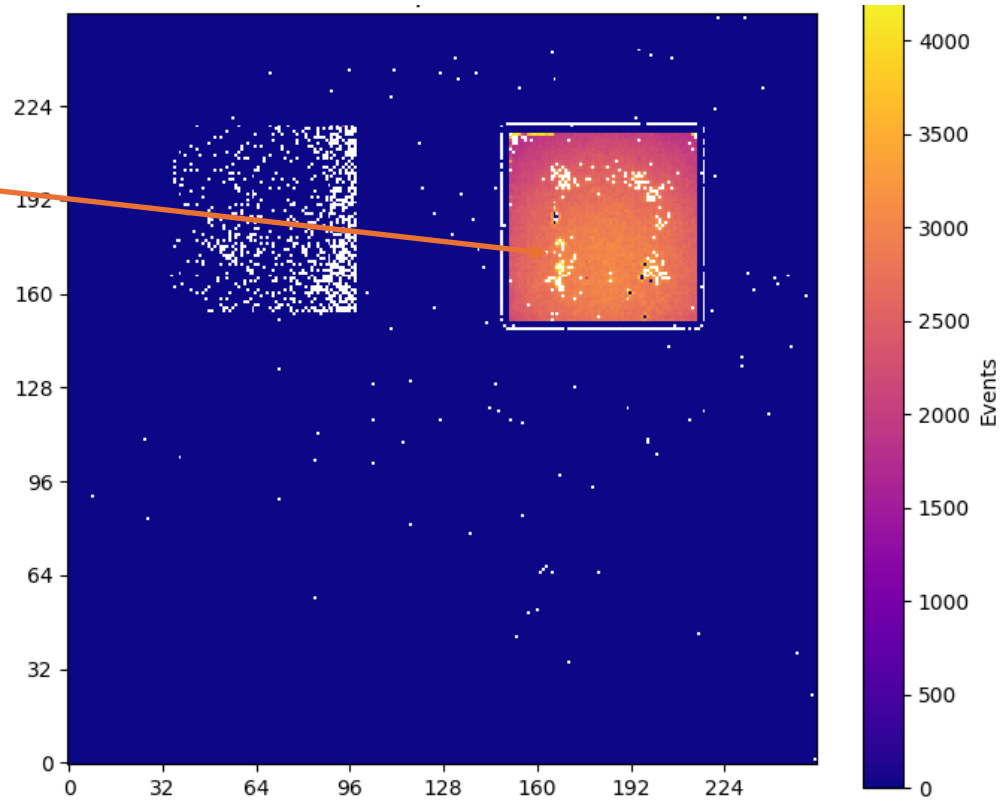
Hybridization of Timpepix-3 with TI-LGAD

Timepix3-Ti-LGAD hybrid bonded on PCB





Hit map with Strontium-90 radioactive source



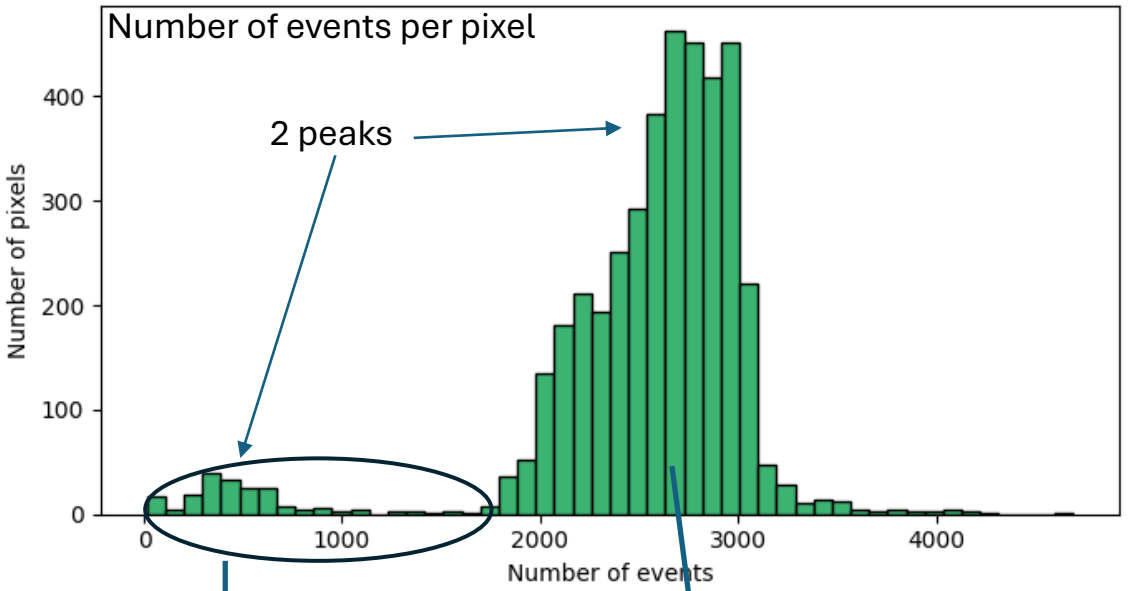
1st test:
I-V characterization to check if the Ti-LGADs behave like a diode.
1 Ti-LGAD presented a short-circuit, the other responded correctly.

V1 and V2 are 2 versions of the TiLGAD. V1 has more “aggressive” design, better performance but lower yield expected.

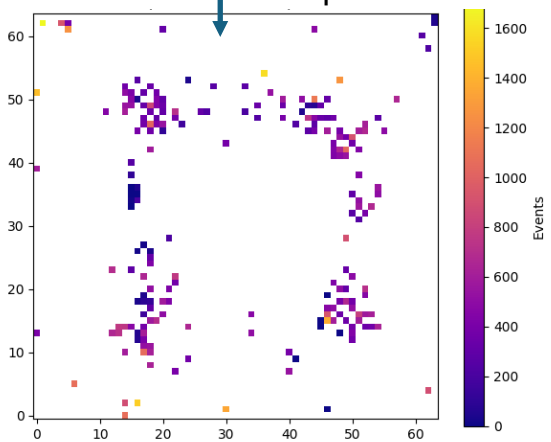
Bias voltage during this test : -100 V
Leakage current: ≈ 100 µA

EP-DT
Detector Technologies

Hybridization of Timpepix-3 with TI-LGAD

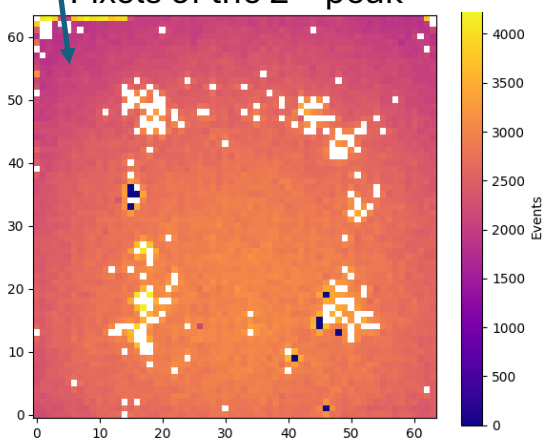


Pixels of the 1st peak



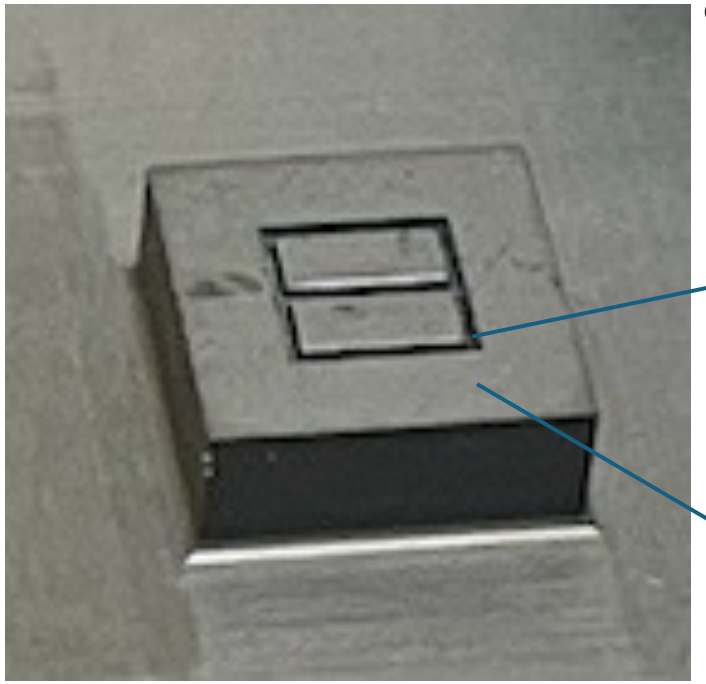
Pixels with connection problems

Pixels of the 2nd peak

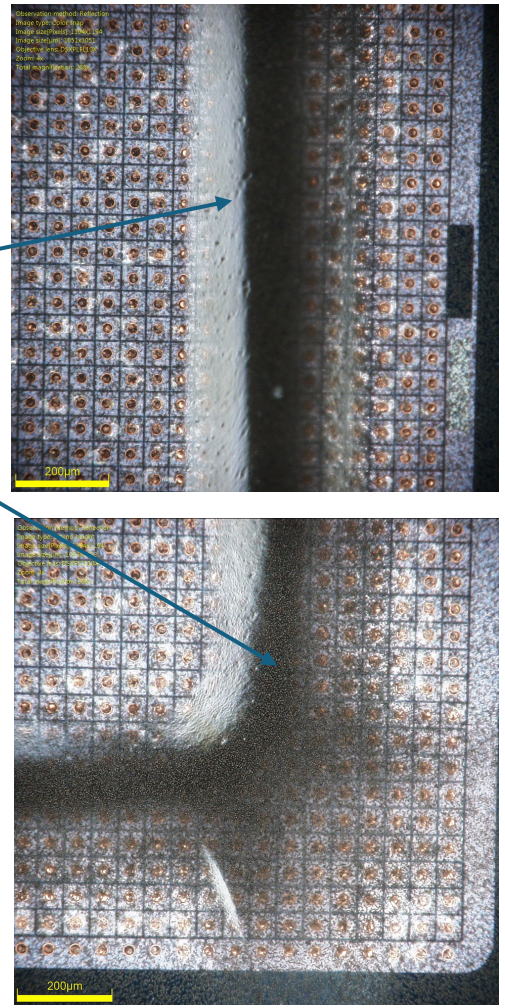


95% connection yield

Bonding tool used for the lamination of the ACF and the flipchip bonding



ACF after lamination on Ti-LGAD: Uneven thickness due to the groove on the bonding tool



- Excluding the ACF lamination defect at the centre, 21 pixels were found to be non-responsive (0.51% of 4096 pixels)
- Issue identified: will be solved using a different bonding tool already available
- Test beam planned this month

Hybridization with ACP

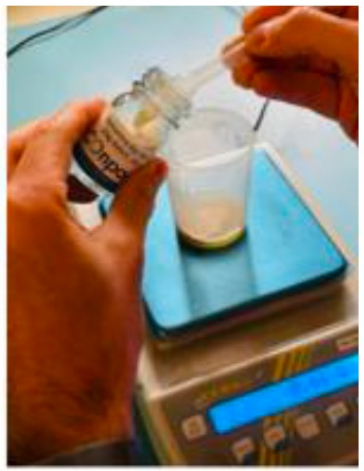
Flexibility to use the preferred adhesive, such as Araldite 2011, mixed with conductive particles

- Faster purchase of conductive particles compared to ACF
- Avoid the short shelf life of ACF. No ACF lamination step.

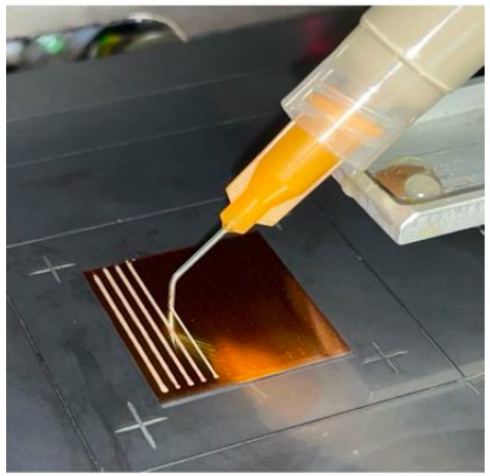
Test on ALTIROC ASICs on LGAD sensors from High Granularity Timing Detector (HGTD)

- Good bonding yield, to be further investigated

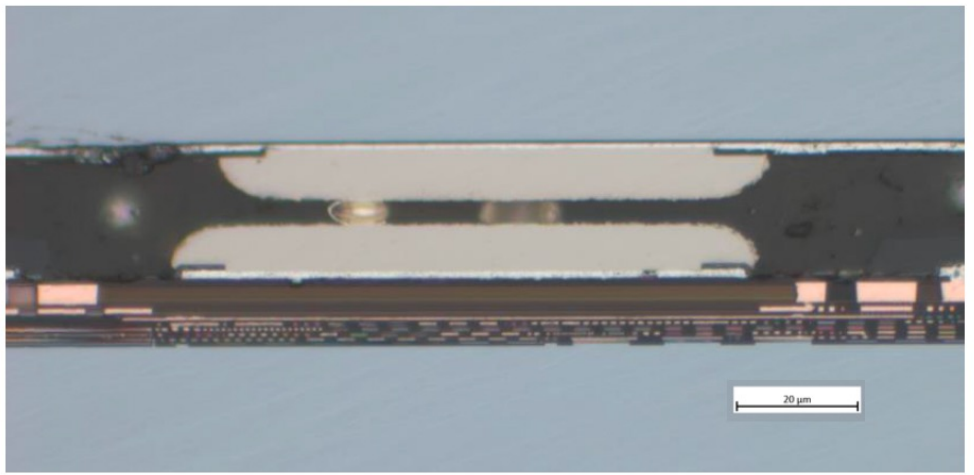
ACP mixing



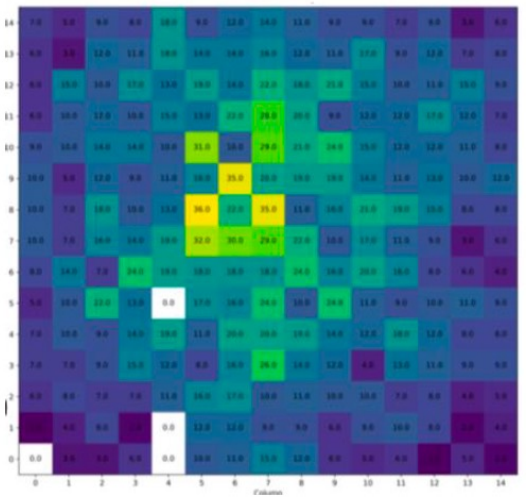
ACP dispensing



Hybrid ACP cross-section



Pixel hit map



See presentation of M. Vicente at VERTEX 2025

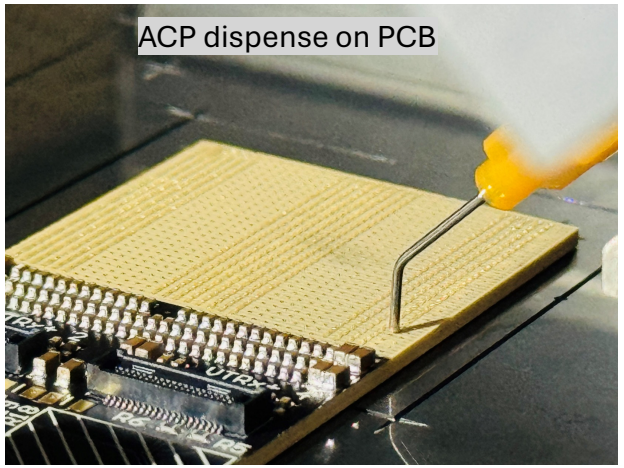
Timepix4 TSV (Through-Silicon-Via) flip-chip bonding with ACP

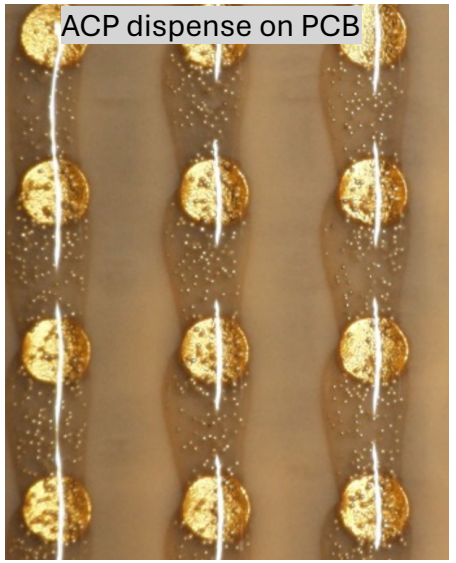
Motivation:

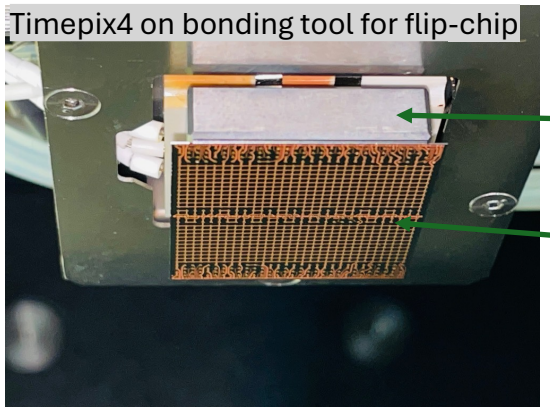
Replace wirebonds by enabling access to the active circuitry (located on the front side of the chip) from the bottom surface of the die using TSVs and ACP.

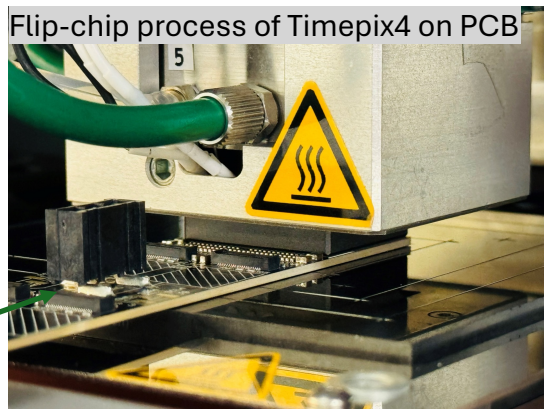
The ACP bonding process consists of the following steps:

- Mixing the micro-particles with the liquid adhesive
- Dispensing the mix on the bottom chip
- Alignment and flip-chip bonding

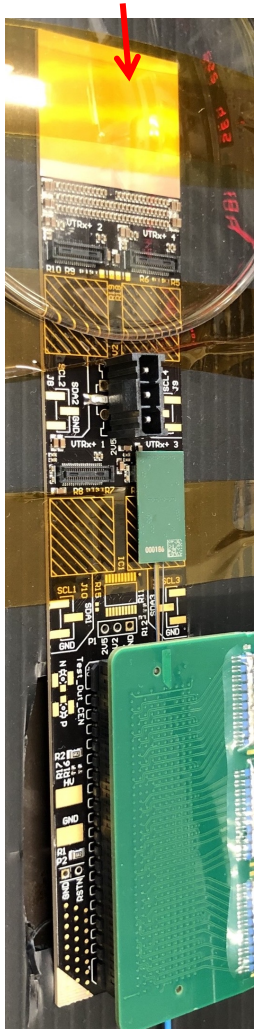






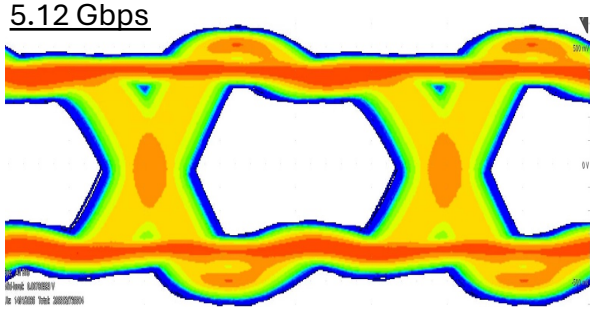


Timepix4 TSV, bonded on PCB with ACP glue

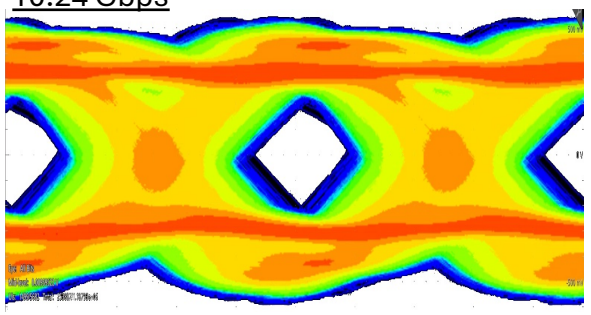


Eye Diagrams Through Optical Fiber

5.12 Gbps



10.24 Gbps



The eye diagrams show that the TSVs are powering the chip and delivering signal even at 10.24 Gbps. (The degradation observed in the 2nd eye diagram is due to limitations of the transceivers at this data rate).

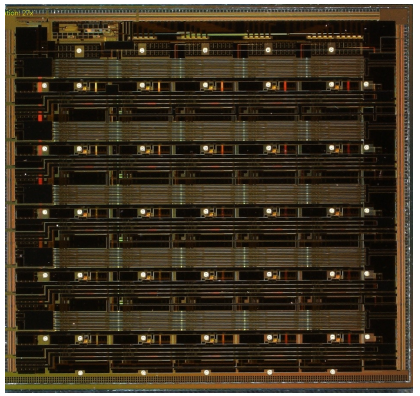
Conclusions:

- TSV with ACP is a possible alternative to wire-bonding.
- Powering and data transmission is proven at gigabit rates through TSVs and ACP bonding.

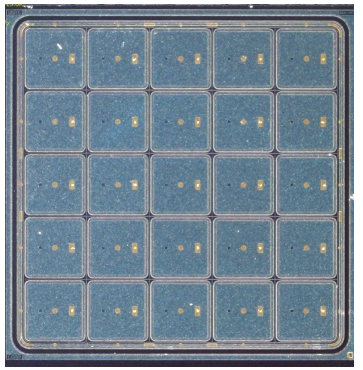
Gold stud hybridization test

- Hybridisation of 2 LATIC2 ASICs (130 nm TSMC) with 2 USTC-IME v2.1 LGAD sensors
- 5x5 pixels, 1.3mm square pitch
- Processing steps:
  - Deposition of double gold studs on LATIC2 ASICs at HybridSA
  - 10 min argon plasma cleaning for both ASICs and sensors
  - Applying Araldite 2011 glue on ASIC in 4 lines between gold studs
  - Flip-chip of ASIC and sensor, thermo-compression bonding with 5 kg force and 100°C for 7 min
  - Backside thinning of sensor (because of design issue preventing wire bonding for thick sensor)
- Test results for 1 hybrid
  - Sensor IV not affected by flip-chip and wire bonding
  - 100% interconnection yield for 24 functioning channels
    (1 channel with ASIC issues)
  - First performance results with electrical pulses, laser and Sr90

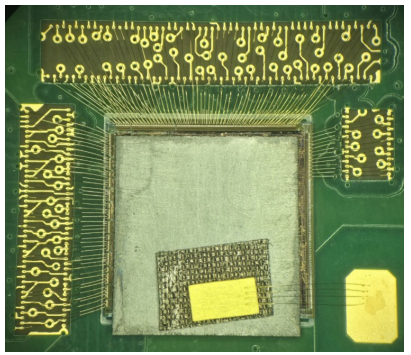
Double gold studs on LATIC2 ASIC



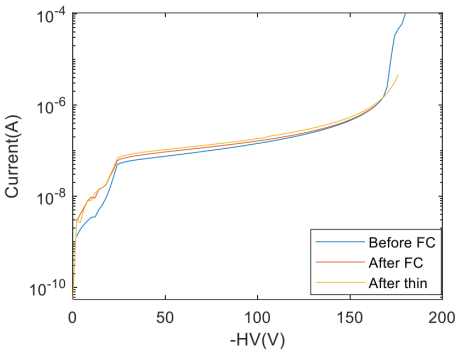
USTC-IME v2.1 sensor

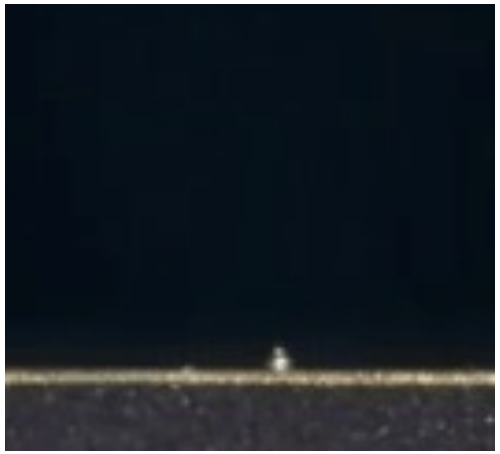


Hybrid wire bonded to PCB



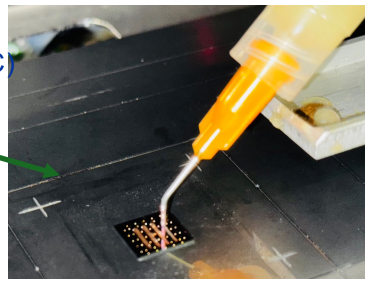
Sensor IV before and after processing



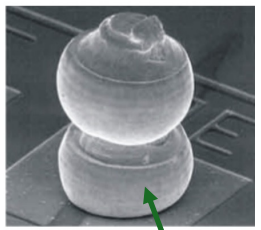


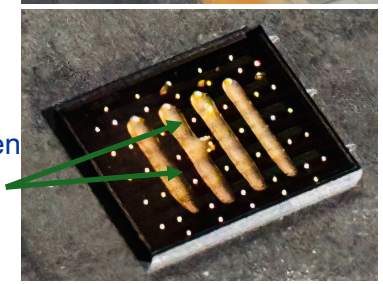
Gold studs are deposited one by one
https://www.youtube.com/watch?v=ICRDBpmev4o&t=42s&ab_channel=TPT-Wirebonder

NCP (Araldite 2011) dispense before flip-chip (on LATIC2 ASIC)



Stacked Gold studs





NCP between gold studs

35 µm gap between ASIC and sensor avoid sparks at the edges of the chips.

Conclusion:

- The hybridisation process using double gold studs was applied to a new chip.
  An excellent connection yield was achieved, allowing our colleagues to successfully test their new chips.

Solder spheres

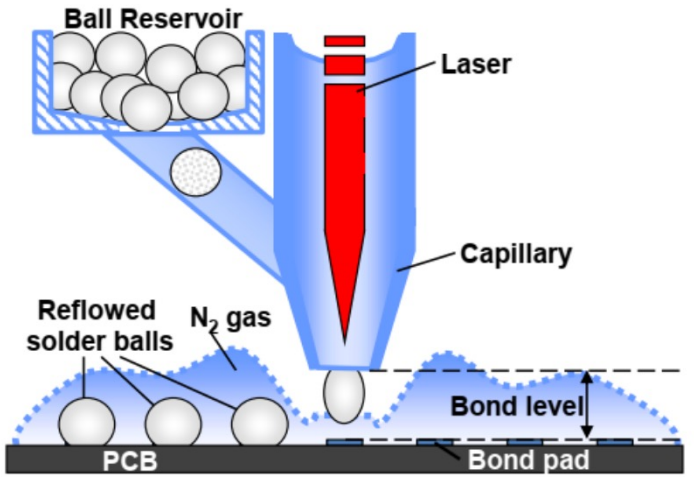
Solder deposition
First tests

Under Bump Metallization (UBM)
ENEPIG process:
- Electroless Nickel
- Electroless Palladium
- Immersion Gold

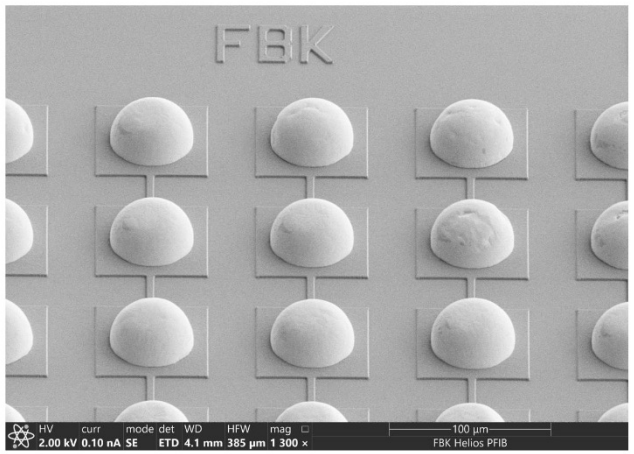
~ 5 um Ni, 0.2 um Pd, 0.05 um Au

Solder spheres
- SAC305: 96.5% Sn, 3 % Ag, 0.5% Cu
- Melting point: 220 °C
- High electrical conductivity
- Lead free & widely used

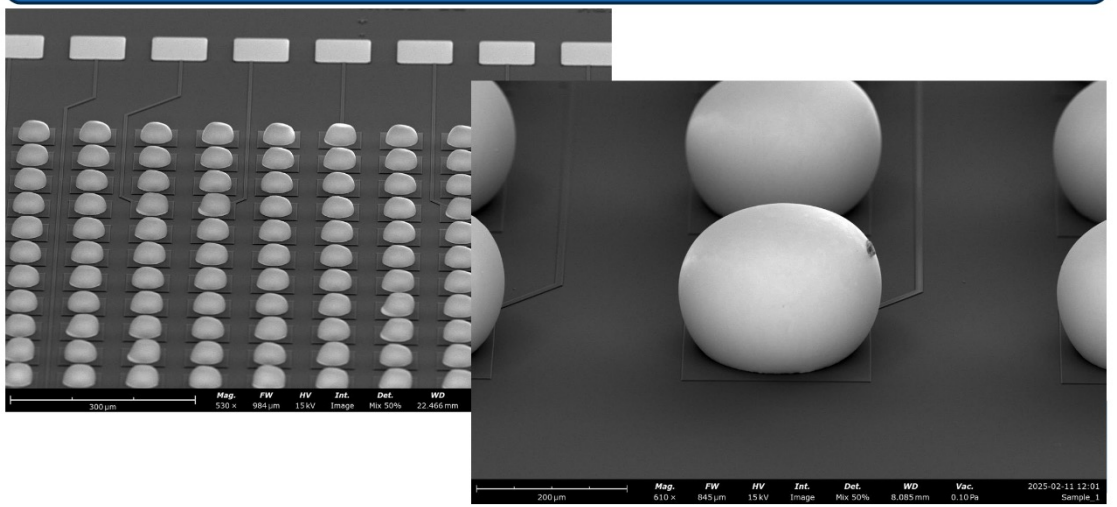
Sphere deposition (PacTech)



40 um spheres on 45 um pad, 100 um pitch



250 um spheres on 200 um pad, 500 um pitch

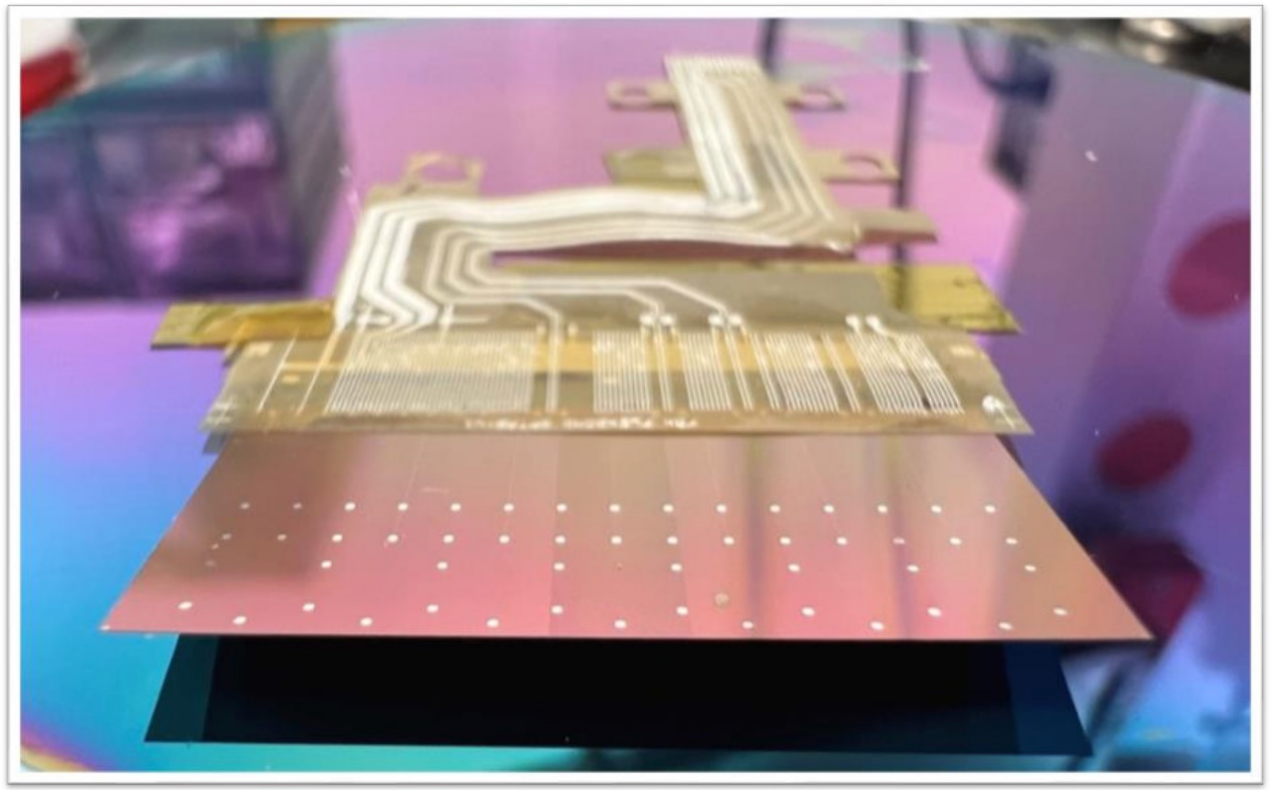


Source: Pactech promotional material

Connection to light flexes

This flexes / spTAB connections

Inspired from the state-of-the-art: LTU Kharkiv

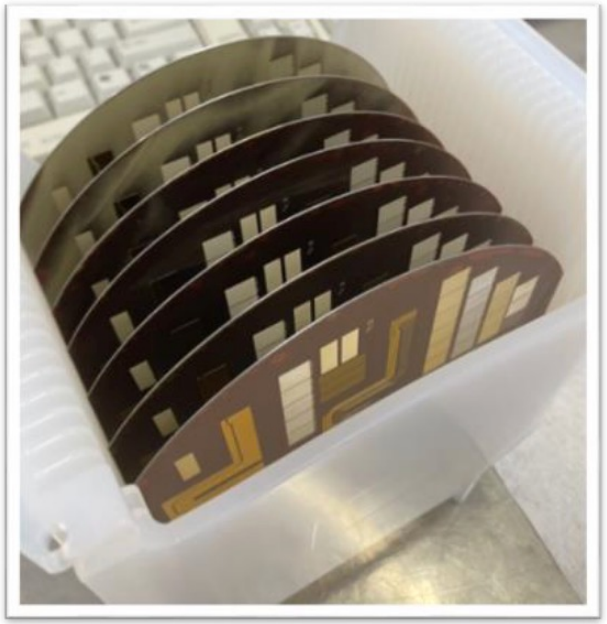


50 µm ALPIDE chip + 90 µm Aluminium-Kapton flex PCB double layer

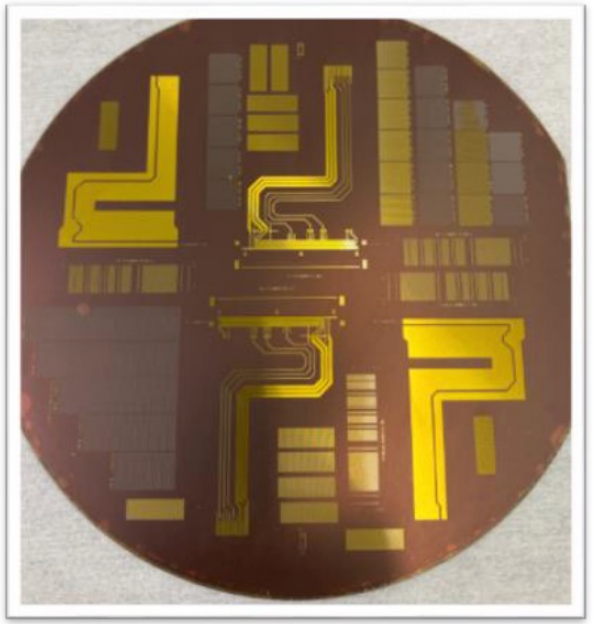
- ❑ Flex cable with Aluminium
  - (X_{0Al} = 8.9 cm, X_{0Cu} = 1.4 cm)
- ❑ Minimal thickness
  - 20 µm Al /layer
  - 25 µm Kapton /layer
  - 0.03% X/X0 /layer
- ❑ Tape Automated Bonding
  - Single point Tape Automated Bonding (spTAB)

See presentation of David Novel later in the session

Thin flexes / spTAB connections

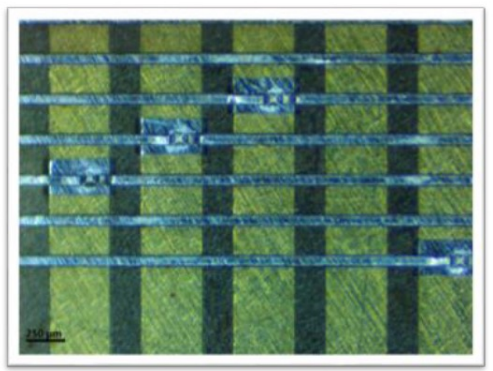


7 wafer batch of flex PCBs

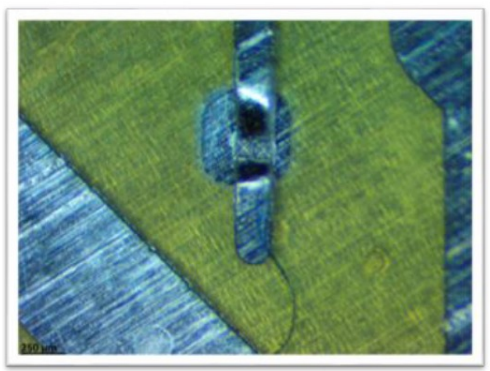


Single wafer containing flexible PCB prototypes

- Wafer-compatible process
  - Few µm precision
  - Scalable
  - No contamination
  - The PCB can be bonded in the "same" cleanroom it was manufactured



Bonding between the signal layer and the chip layer



Bonding between the signal layer and the ground

See presentation of David Novel later in the session

Thin flexes

Tests with thin flexes made also at CERN in conjunction with ACF/ACP studies

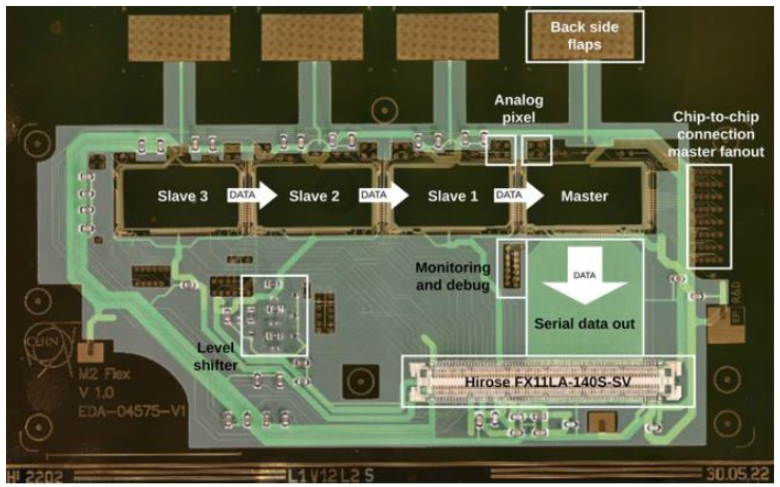
Flexible, low material, dense and reliable modules with the MALTA2 ASICs

- Two-layer flex, **~30 µm thick** with **17 µm trace** width and spacing
- Individual powering with **500 mA** per chip
- Chip-to-chip data transfer

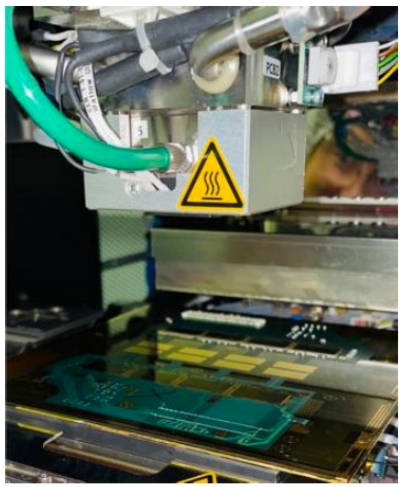
<u>Successfull connection using ENIG+ACF/ACP and SBB+NCP</u>

MALTA2 on a single-chip board

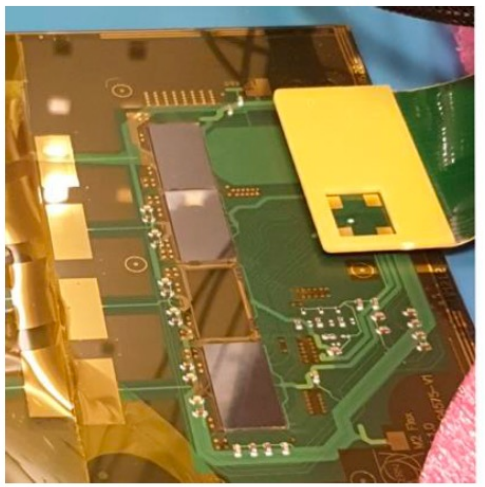
MALTA2 multi-chip flex circuit



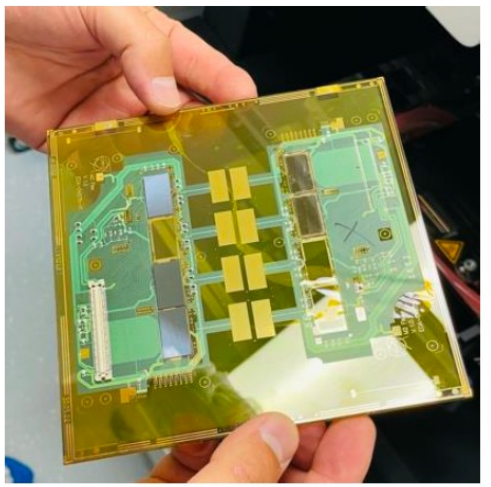
Flip-chip bonding



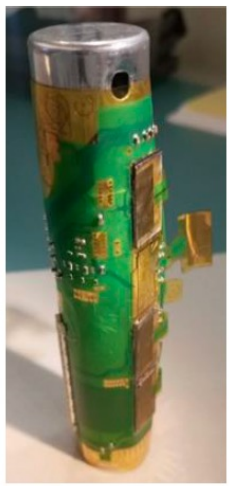
Testing bonded chips



Populated flex on support material



Flex removed from support



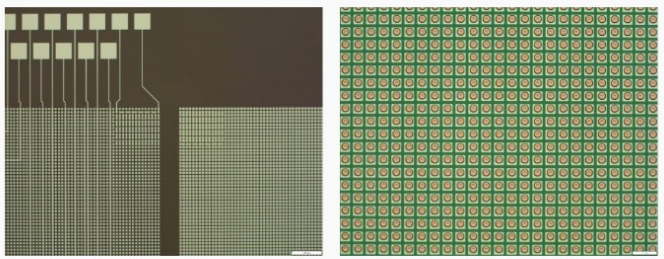
Wafer-to-wafer

Project of Univ. of Bonn / IZM

- Goal is to produce very thin hybrid modules (50-100um sensor, 20um thinned FE chip)
- 6” wafers: started with LF (150nm) ad-hoc sensor wafer TimePix3 wafer (GF 130nm, 55um pitch)
- Process set-up: thinning and interconnection on chip backside
- Longer term: transfer to more modern technologies and size (65nm or 28nm, 300mm wafer)

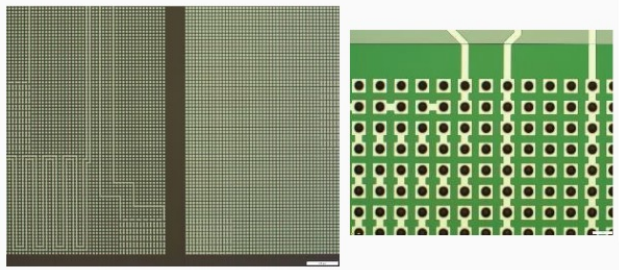
Combination of a polymer glue bonding process with the Cu-SnAg pillar bonding process

W2W bonding setup top wafer:



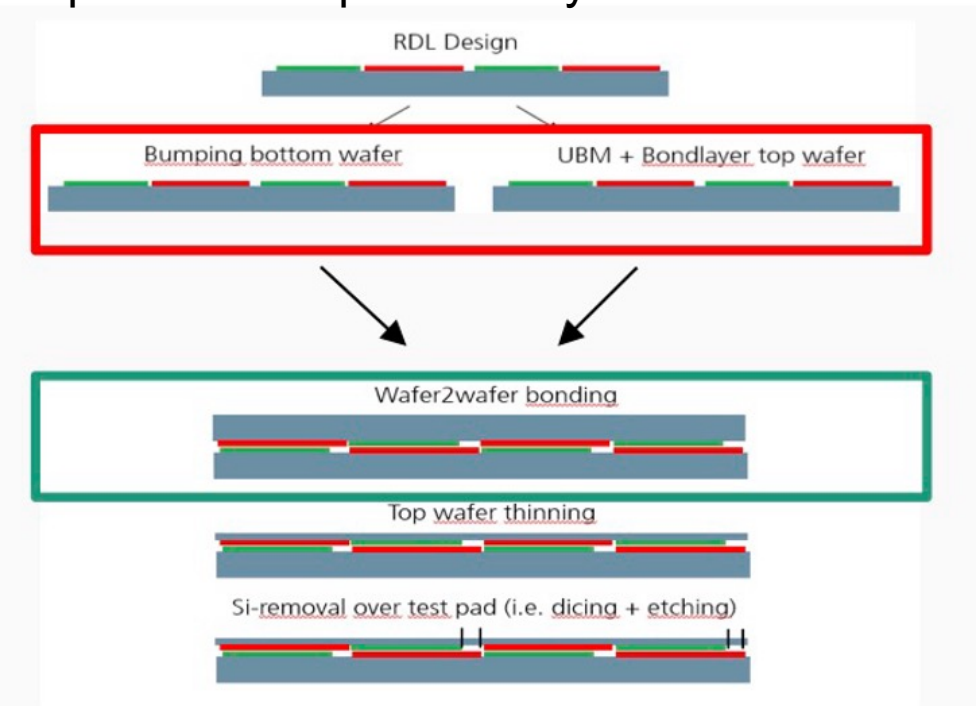
Top wafer with Cu-Pad and polymer layer

W2W bonding setup bottom wafer:



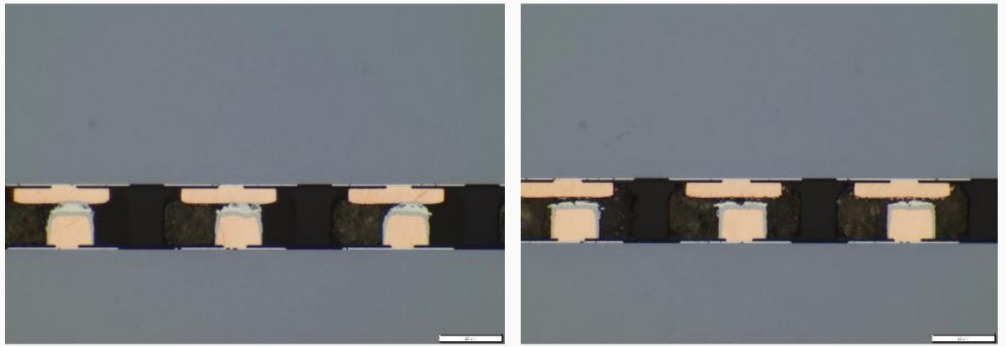
Bottom wafer with Cu-SnAg pillar

process setup with daisy chain wafers

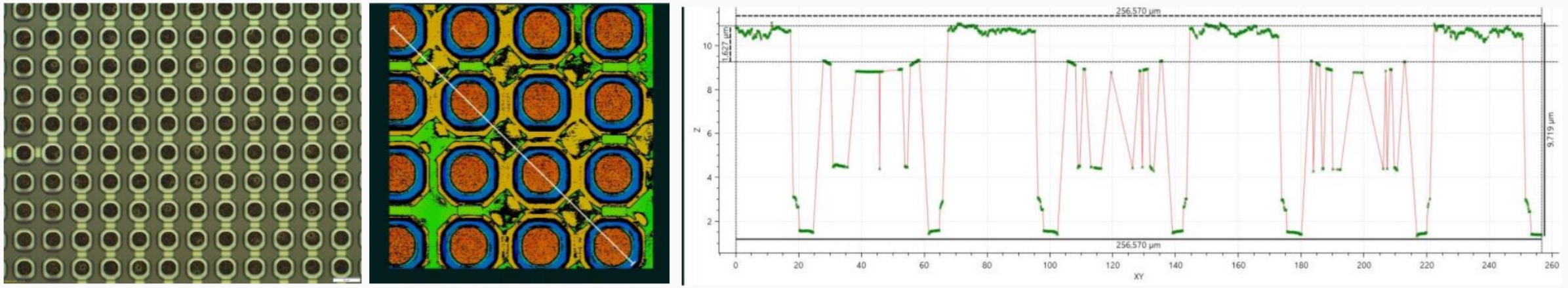


Uniformity of pillar height is a critical point, first test showed disconnection regions

Ad hoc method developed for pillar planarization and tested on dummy chains wafer



cross section after wafer to wafer bonding:
Left: slightly connected pillars, solder transfer to Cu pad (top) visible
Right: gap between pillar and pad, no solder transfer to Cu pad (top) visible



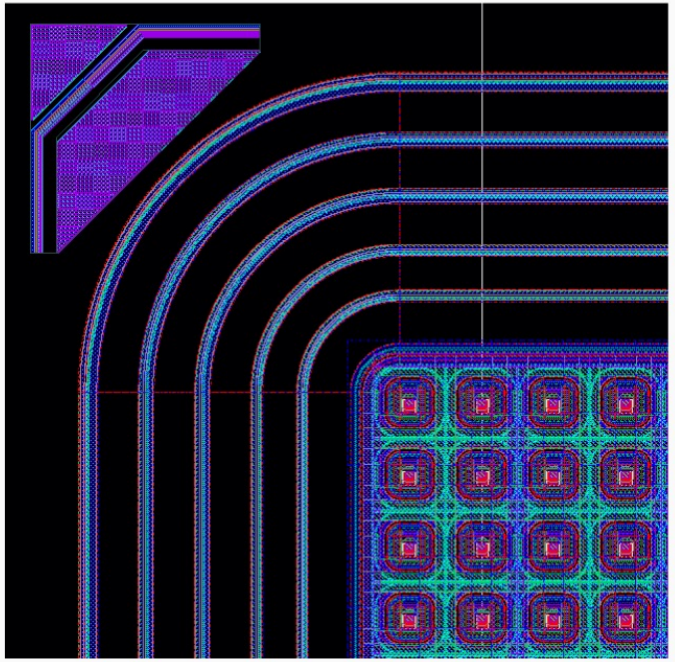
Microscopic image (100x) and 3D profile of daisy chain test structure wafer after pillar plating; height difference to planarize: ~2µm

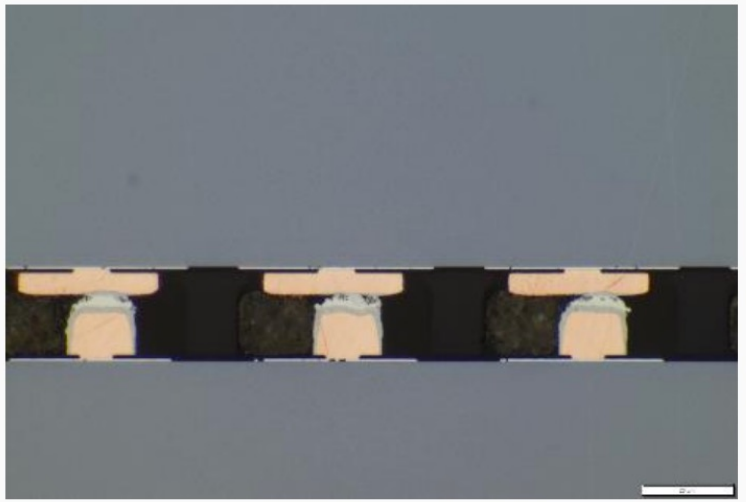
Good results obtained, at the level of 2um uniformity

UNIVERSITÄT BONN

CONCLUSIONS + NEXT STEPS

- Preparations for W2W with Timepix3 and passive CMOS sensor well progressing
  - Timepix3 wafer available and feasible for W2W bonding
  - Sensor wafer fabricated, tested and in process for W2W
  - W2W bonding process setup with daisy chain at IZM well advanced but final test of daisy chains pending
- Next steps:
  - Finishing W2W process setup and optimization including electrical test results on daisy chain wafers after pillar planarization
  - Further testing of passive CMOS sensor wafers at Bonn and Dortmund
  - Start of W2W processing with real sensor and FE wafers





Role inside DRD3

These activities represent a key axis of DRD3

- Fast interconnection goal is to bring hybridization capabilities to the regional laboratories
- Allows accelerated testing
- Synergy in the development of test setups, irradiations, testbeams
- Interconnection for sensor-readout and for readout-flex

Progress in wafer-level bonding

All these activities has very important connections to DRD7

Boundary between DRD3 and DRD7

what is more sensor-related as DRD3 activity (for instance hybridization of sensors)

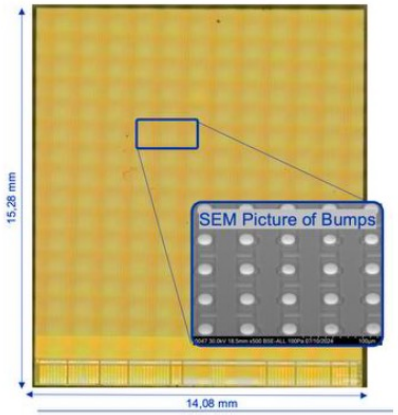
what is electronics interconnections as DRD7 activity (for instance tier-to-tier or integration)

but it's clear that there is a strong synergy among activities

DRD3 Collaboration week at CERN on week of November 10th

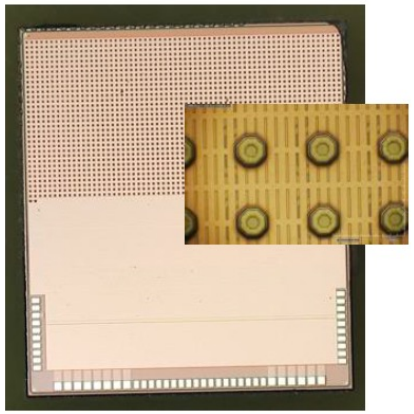
55um 130nm
14x14 mm

Timepix3



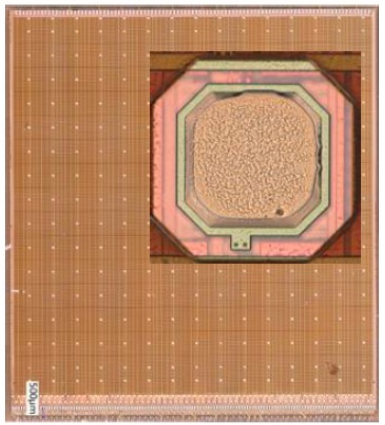
50um 40nm
1.6x3.2 mm

SPHIRD



1.3mm 130nm
20x22 mm

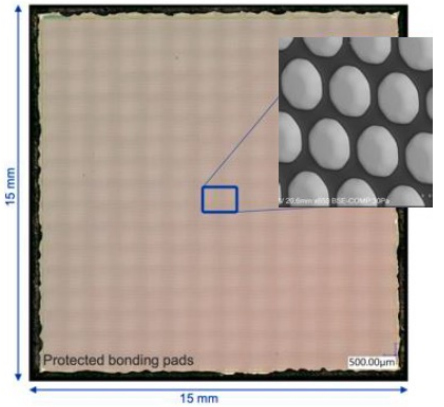
ALTIROC



SiGE KEK

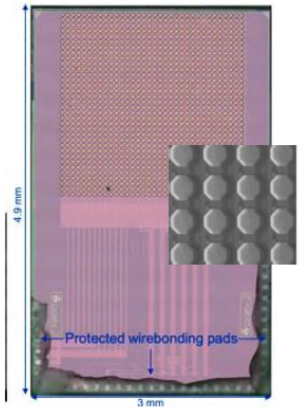
50um 180nm
15x15mm

XPOL-III

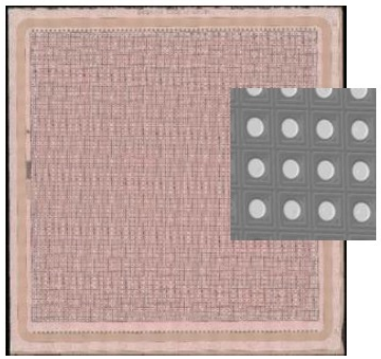


70um 65nm
22x22mm

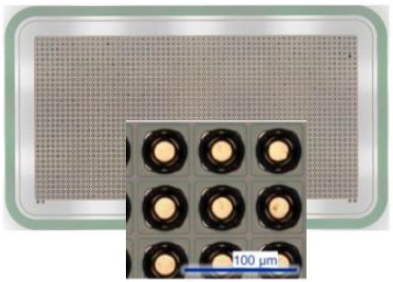
COLORPIX



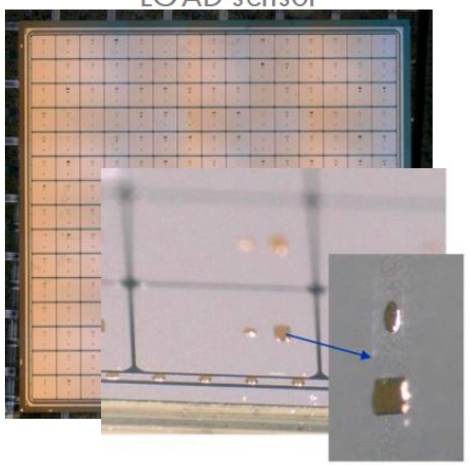
Ti-LGAD sensor



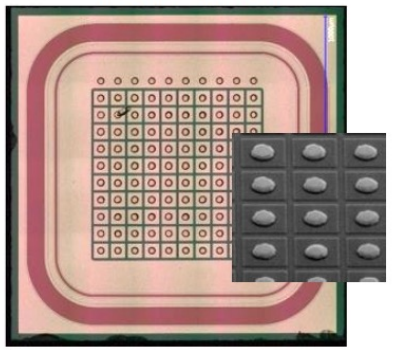
Silicon sensor



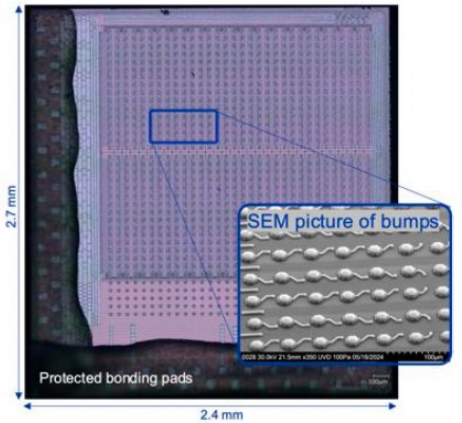
LGAD sensor



LGAD sensor



TimeSPOT



55um 28nm
2.4x2.7 mm