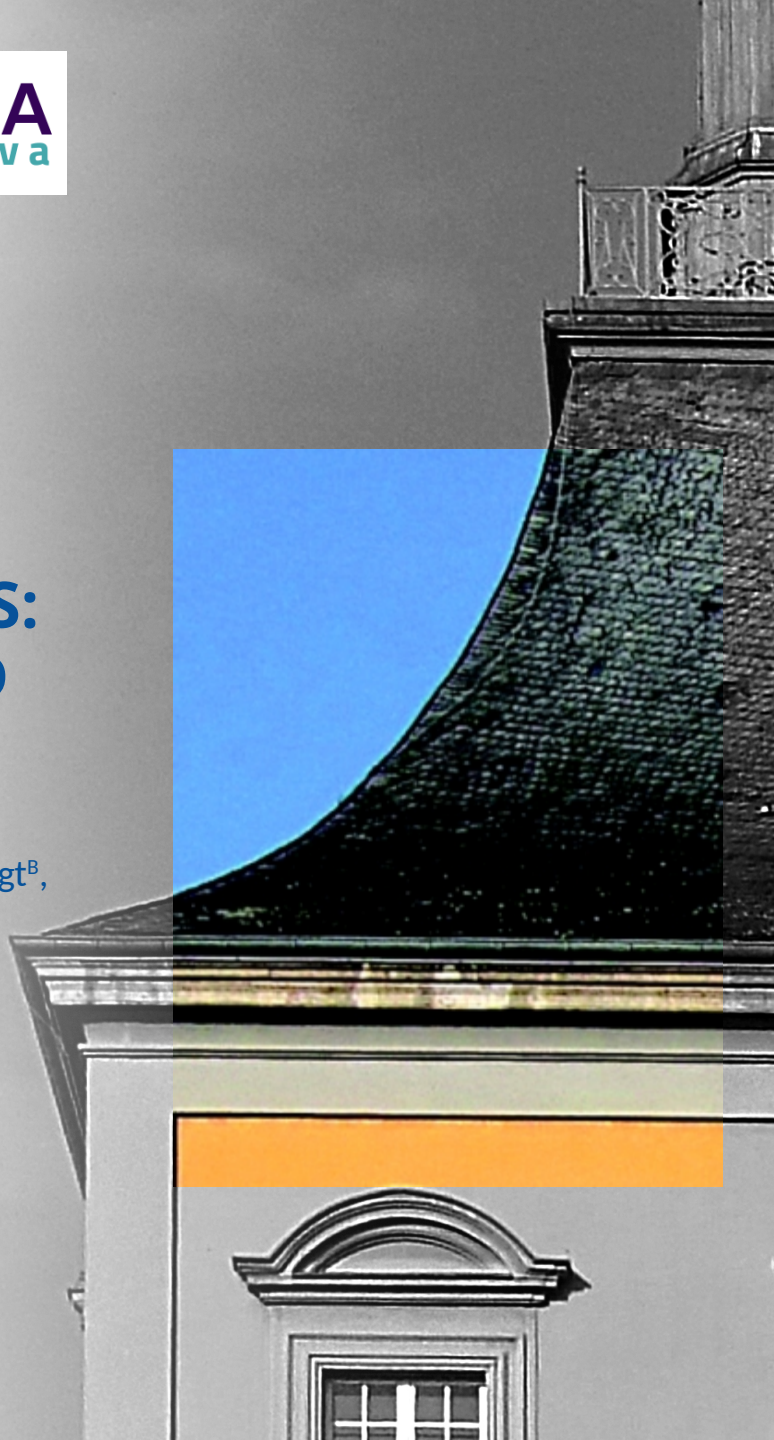


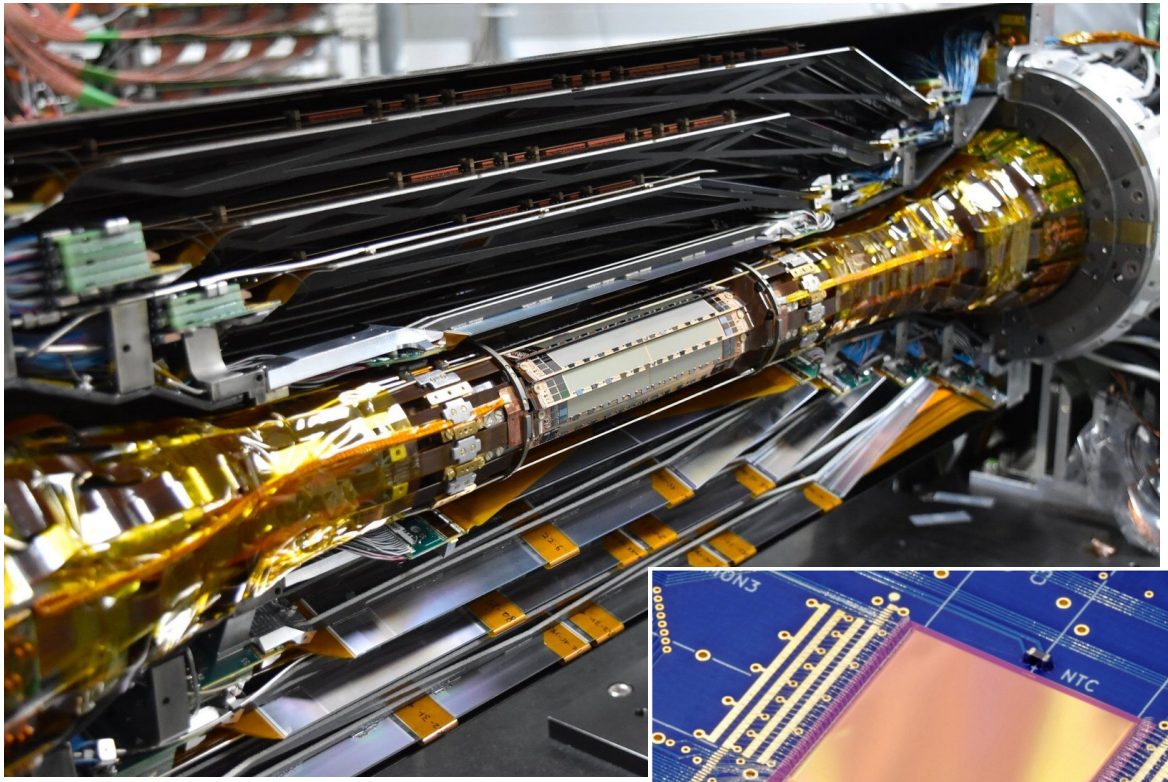
DRD 7.6B MEETING
KARLSRUHE 2025

LOW-MATERIAL PIXEL MODULES: ALL-SILICON AND THIN HYBRID MODULES

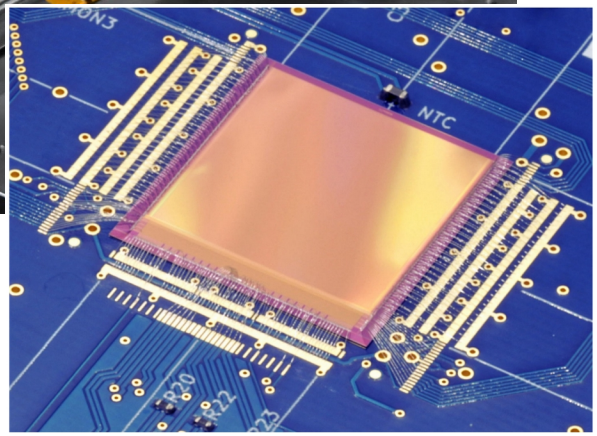
Y. Dieter[B], J. Dingfelder[B], I.-M. Gregor[B,De], T. Fritzsch[I], F. Hügging[B], K. Kröninger[Do], H. Krüger[B], M. Mucha[B], A. Ulm[B], J. Vicsher[Do], M. Vogt[B], J. Weingarten[Do], S. Zhang[B]

[B] University of Bonn
[De] DESY
[Do] TU Dortmund
[I] Fraunhofer IZM Berlin

MOTIVATION



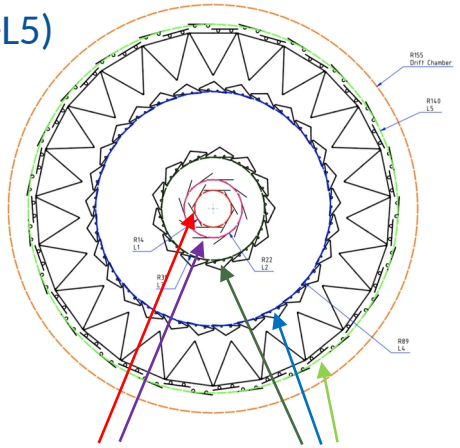
Vertex detector (VXD), Belle II



CMOS sensor TJ-Monopix2

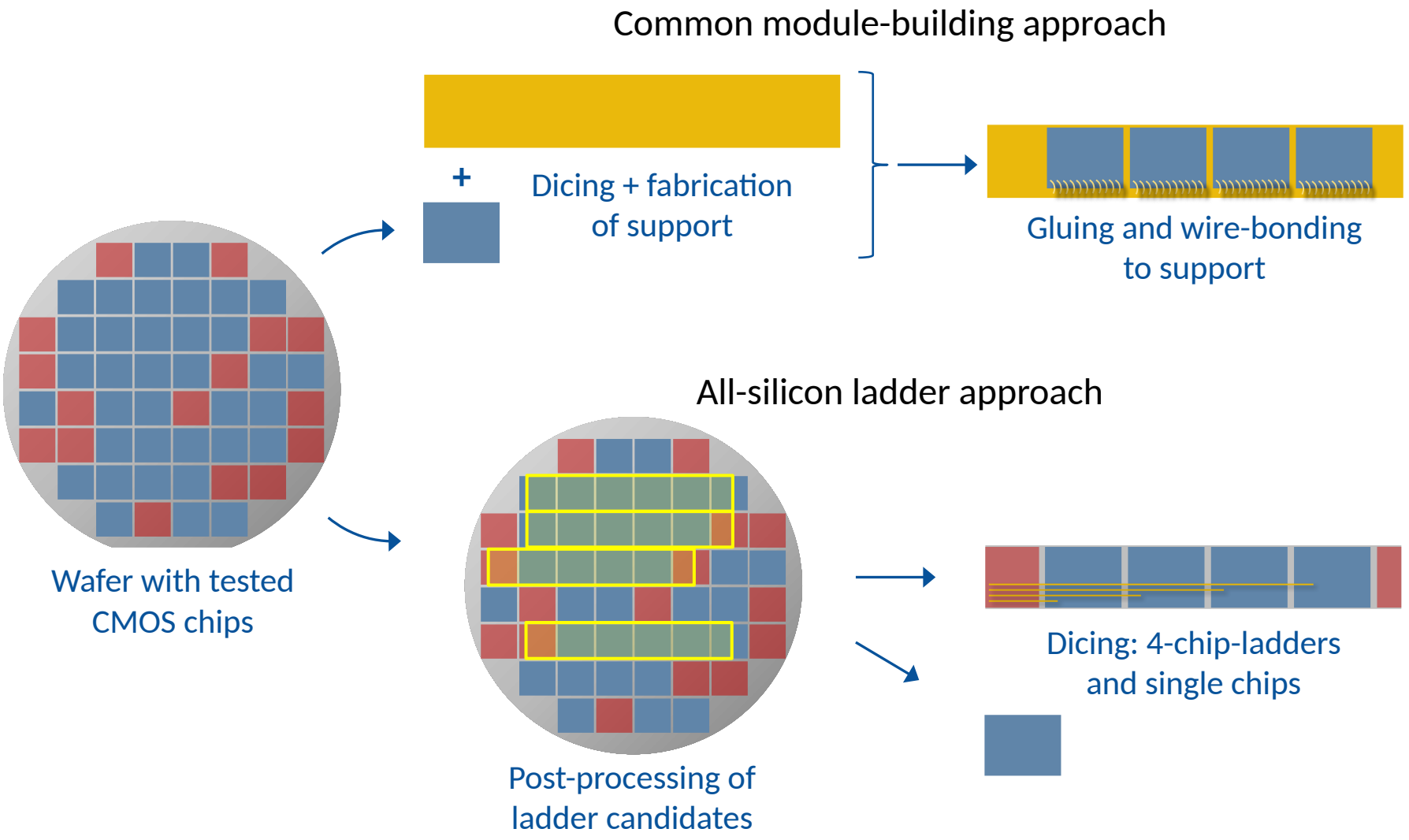
Super low material budget applications e.g. in Belle II:

- Monolithic active CMOS pixel sensor OBELIX, evolving from TJ-Monopix2
- L1+L2: self-supporting, air cooled or contact cooled
- L3-L5: CF structure, water cooled
- Low material budged: 0.2% X_0 (L1+L2) … 0.8% X_0 (L4+L5)



L1, L2: **iVTX** L3-L5: **oVTX**

ALL-SILICON LADDER CONCEPT



ALL-SILICON LADDER CONCEPT

All-silicon ladder

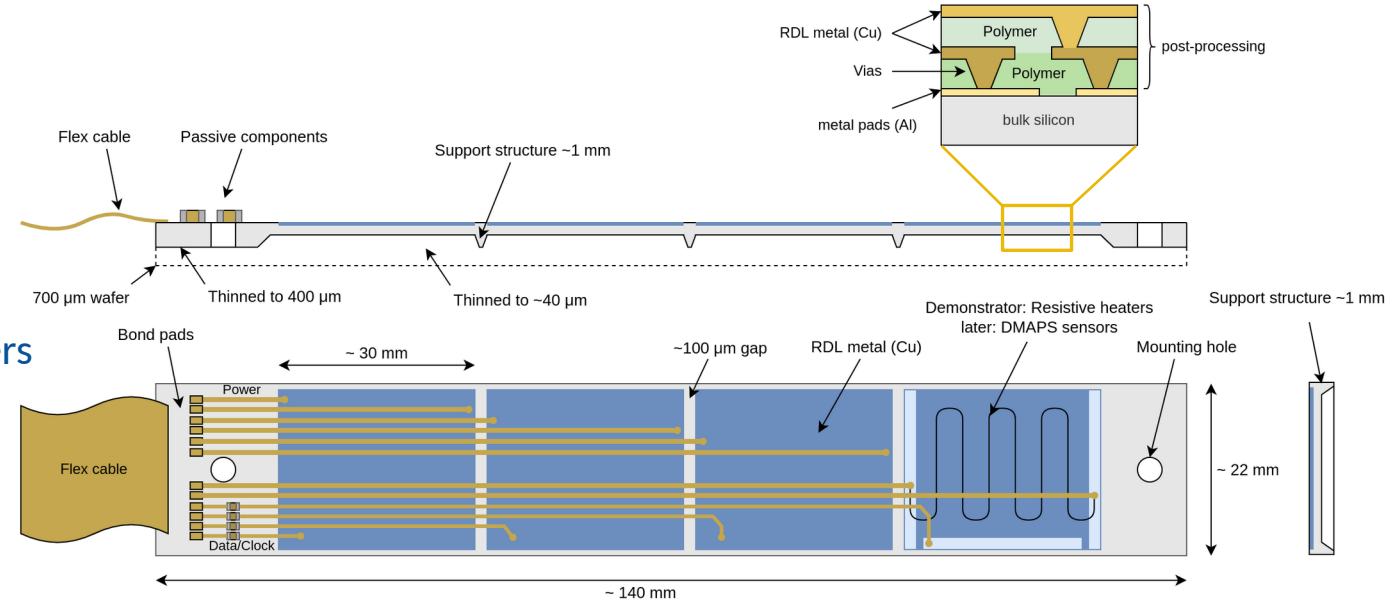
- Single piece of silicon
- 4 sensors cut in one piece from the wafer

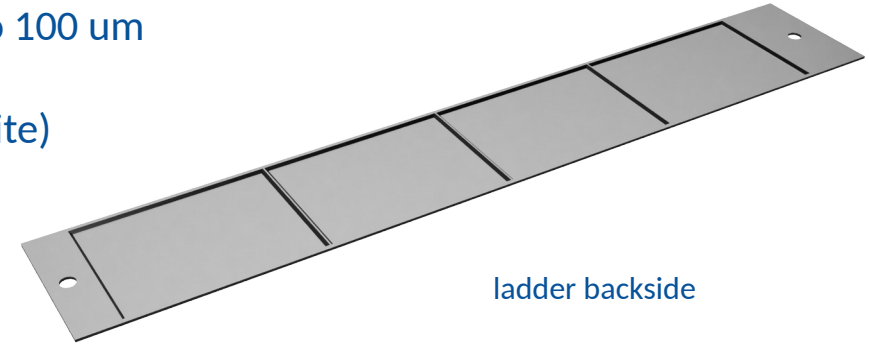
Post-processing of wafer

- Redistribution metal layers for data and power
- Heterogeneous backside thinning

  or

- Homgeneous thinning to 100 um and application of TPG (thermal pyrolytic graphite)

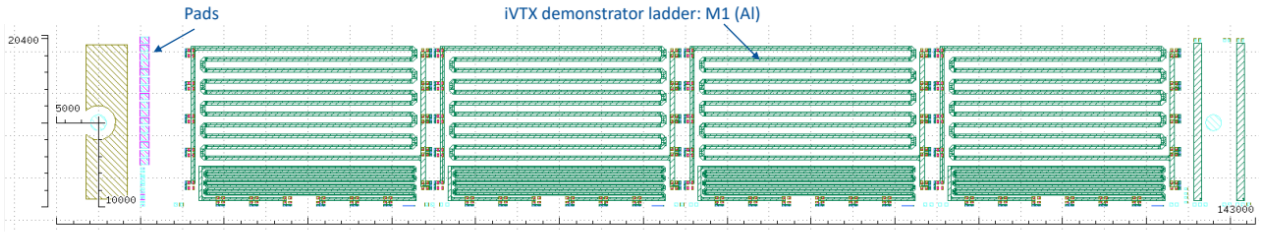


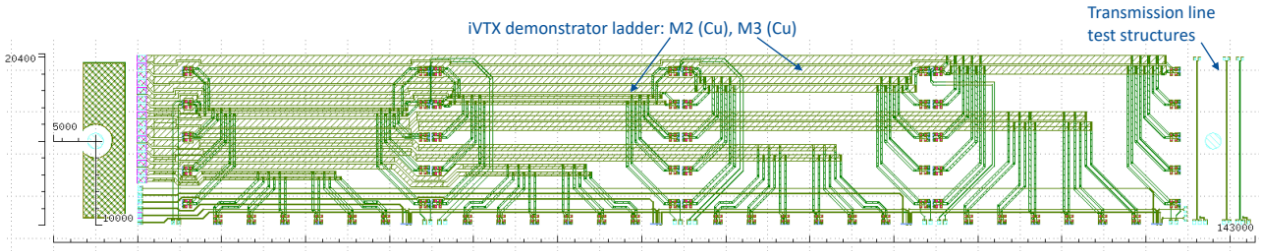


ladder backside

ALL-SILICON LADDER LAYOUT

First RDL demonstrator with resistive heaters instead of CMOS sensors

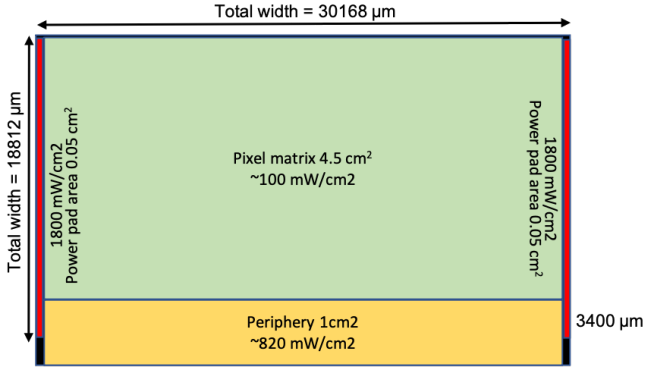




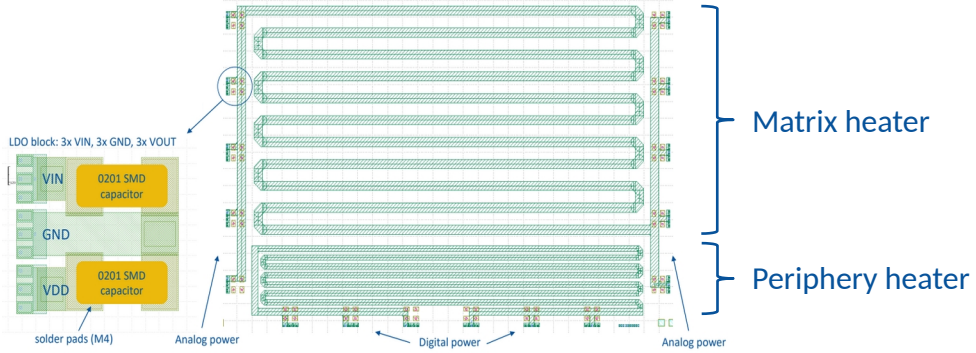
Metal system:

- Resistive heaters: 1.5 µm Al
- 2 RDL metal layers: 4 µm Cu
- Top metal finish: NiAu for wire-bonding, SMD soldering

Ladder dimension: 143 x 20.4 mm²
Dummy heaters (~10 Ω): 30 x 20 mm²



CMOS sensor example: Power domains, power pad locations

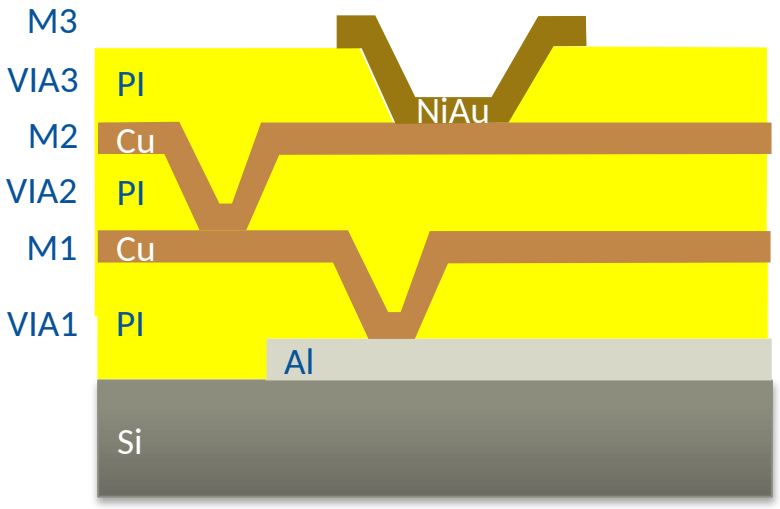


L1 might get a 3 chip ladder

ALL-SILICON LADDER PROTOTYPE FABRICATION

Main fabrication steps:

- Alternating deposition of metal (3 µm Cu) and polymer (7 µm Polyimide)
- Photo lithography, wet chemical patterning

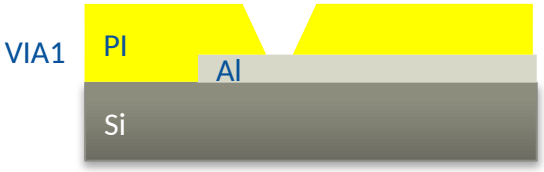


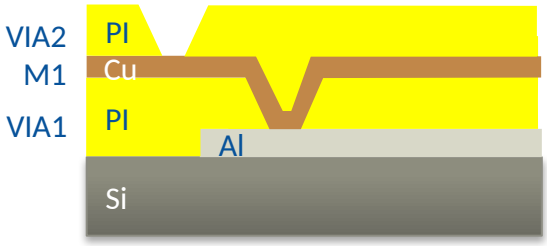
- First polymer layer “VIA1”
  - Openings above sensor bond pads
- First RDL metal “M1”
  - Contacts to sensor bond pads
- Second polymer layer “VIA2”
  - Openings to M1
- Second RDL metal “M2”
  - Contacts to M1
- Passivation layer “VIA3”
  - Openings to M2
- NiAu bond pads “M3”
  - Contacts to M2

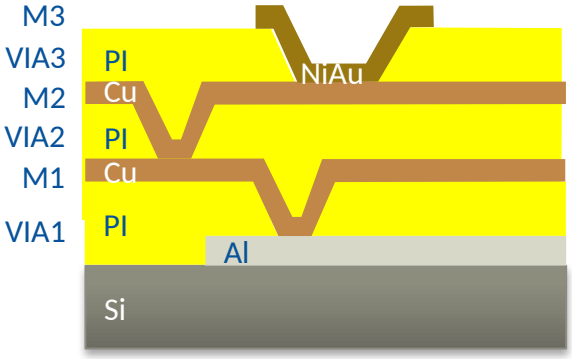
ALL-SILICON LADDER FABRICATION

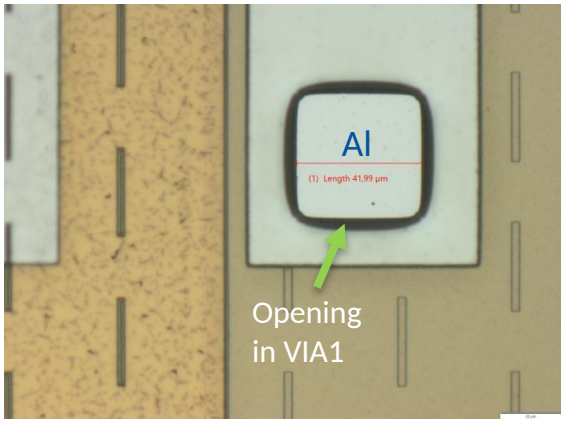
RDL process documentation of the first demonstrator produced by IZM Berlin

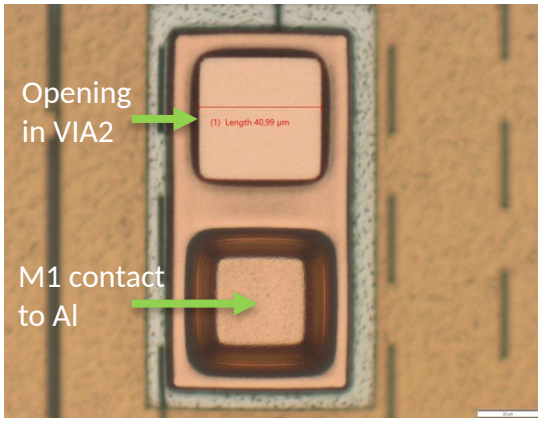
Characterization of layer topography, wafer flatness etc.

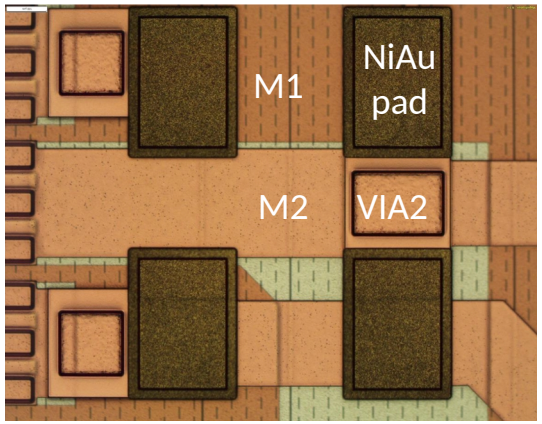










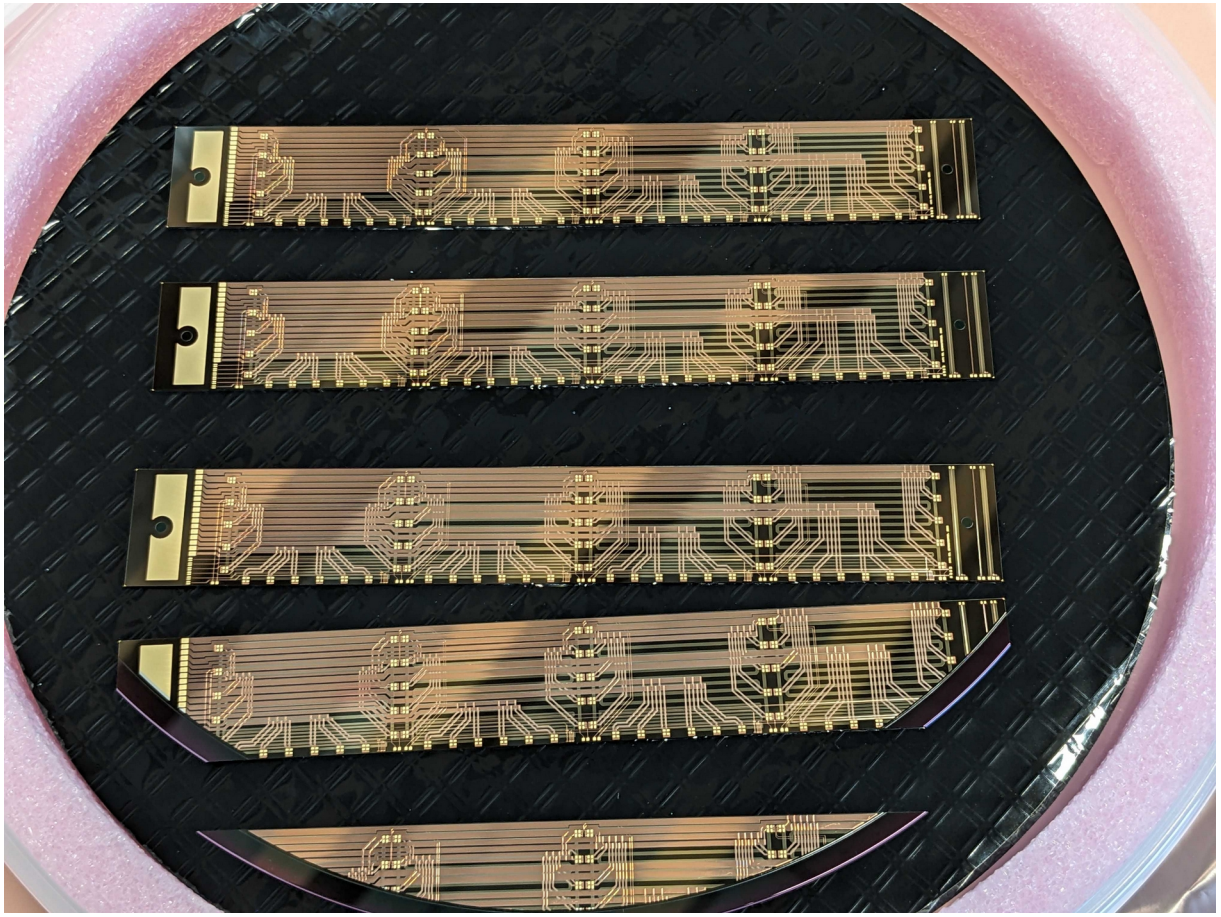


Pictures by IZM Berlin

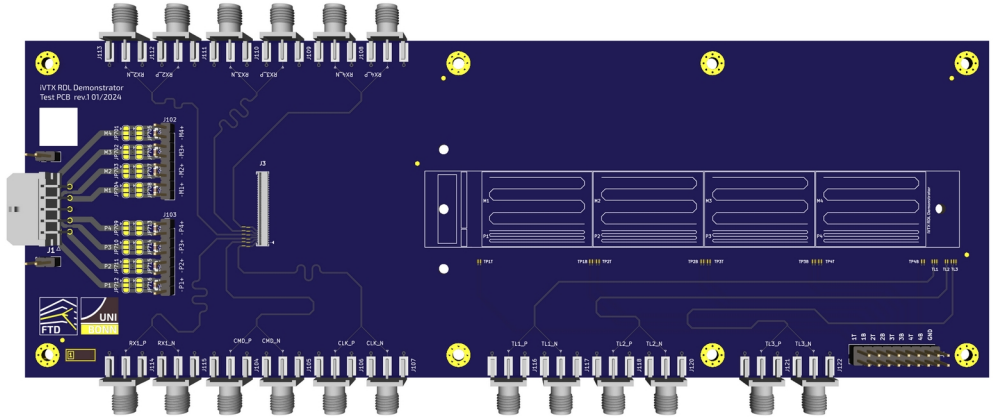
ALL-SILICON LADDER DEMONSTRATOR

First RDL demonstrators: 8 Wafers (725 µm, 400 µm, 300 µm)

Production finished smoothly

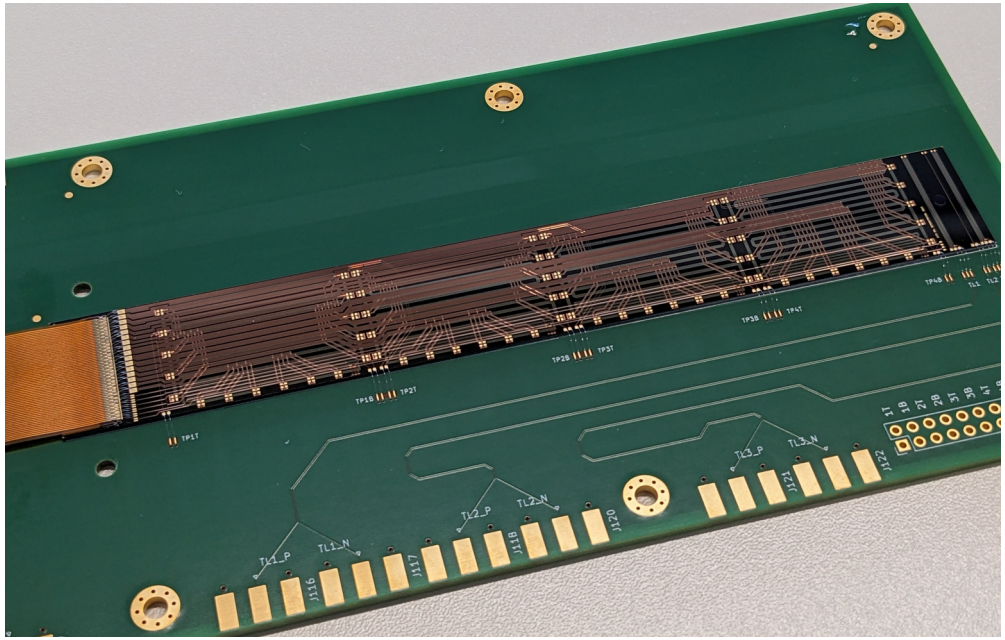


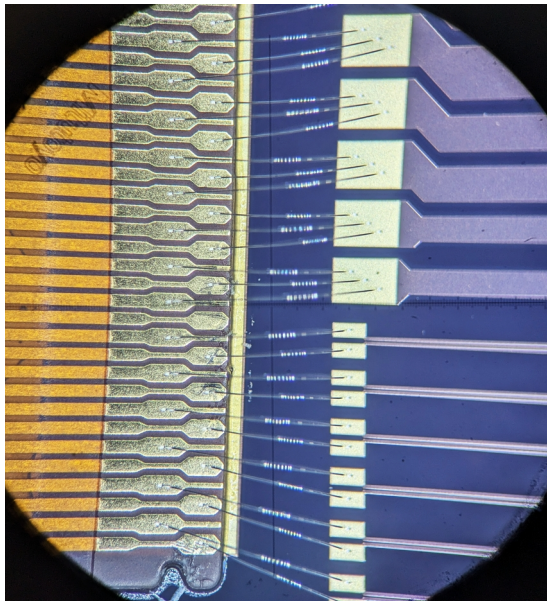
ALL-SILICON LADDER DEMONSTRATOR



PCBs for electrical tests

- Configurable power routing and test points for I*R drop measurements
- SMA connectors for differential lanes
- PCB mockups of the ladder for SMD soldering studies

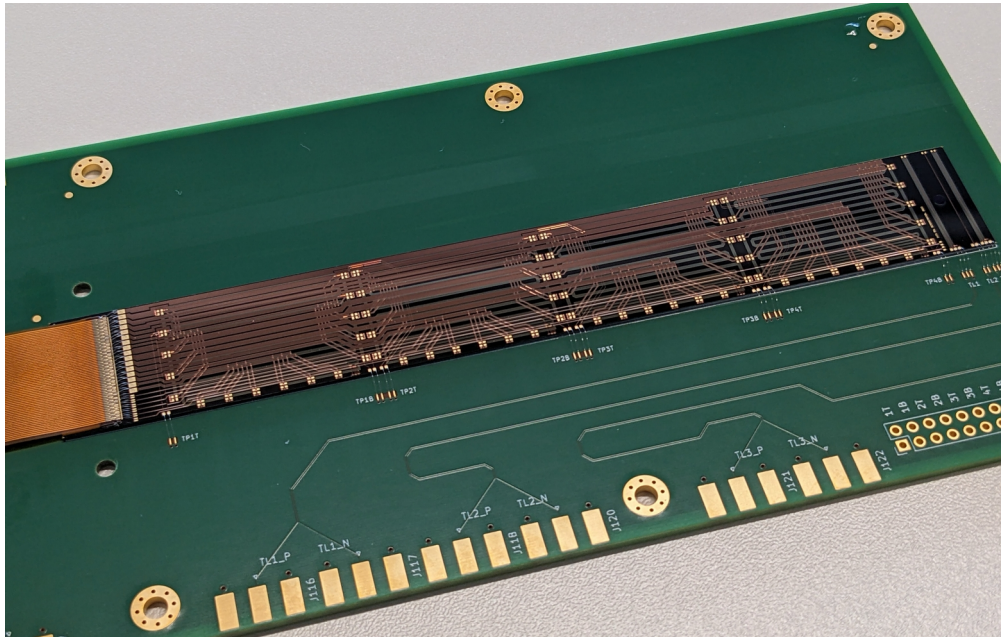




ALL-SILICON LADDER DEMONSTRATOR RESISTIVITY MEASUREMENTS

- Measured matrix resistance
- Measured Voltage and current to simulate power consumption

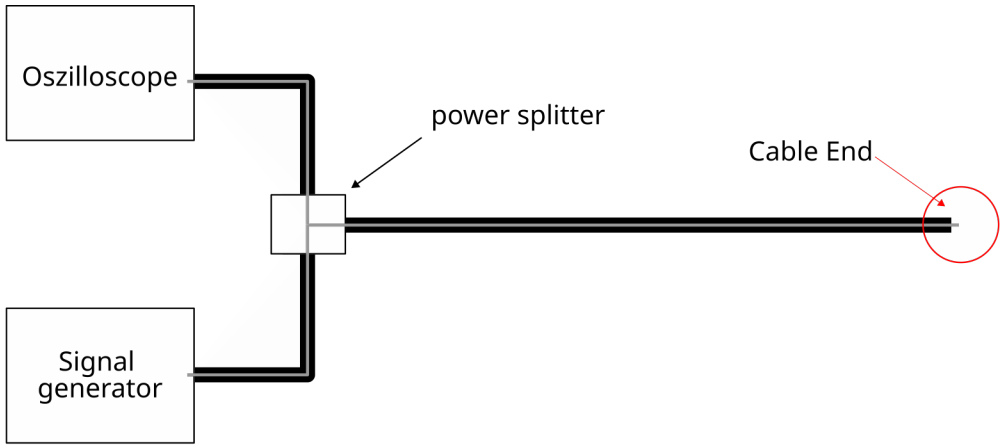
Matrix	Resistance
M4	16.425 Ω
M3	16.08 Ω
M2	15.75 Ω
M1	15.083 Ω

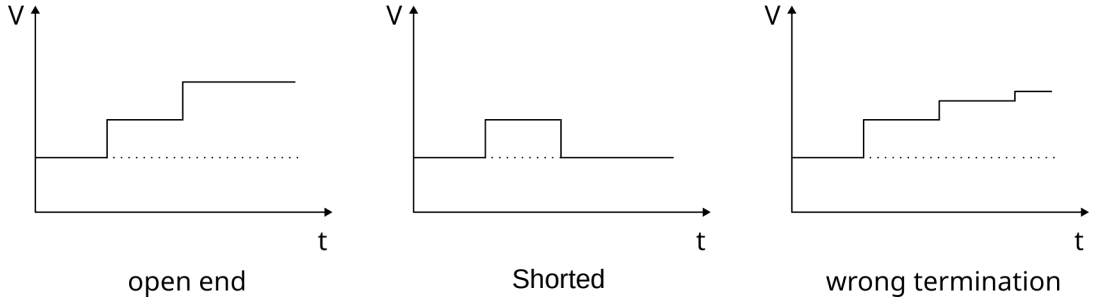


	Matrix 4		Periphery 4
V_{in}	V_{meas} (mV)	A_{in} (mA)	A_{in} (mA)
500	437	33	31
1000	873	66	61
1500	1308	98	92
2000	1744	130	122
2500	2180	162	152
3000	2617	194	182
3500			211
4000			240
4200			251
Total		508 mW	1054 mW

TIME DOMAIN REFLECTOMETRY

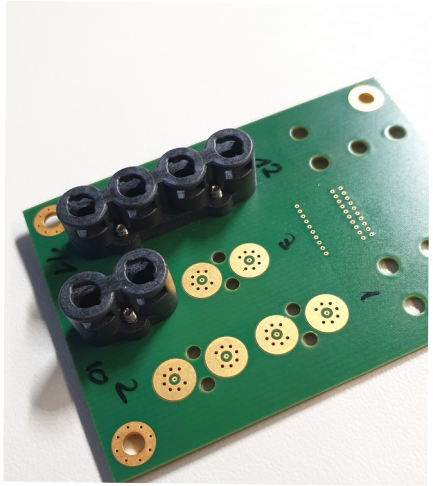
- Send electrical pulse and measure reflection
- Important is sharp edge at the beginning
- Method used to measure
  - Cable length
  - Defects
  - Shorts
  - Changes of impedance
  - Etc.

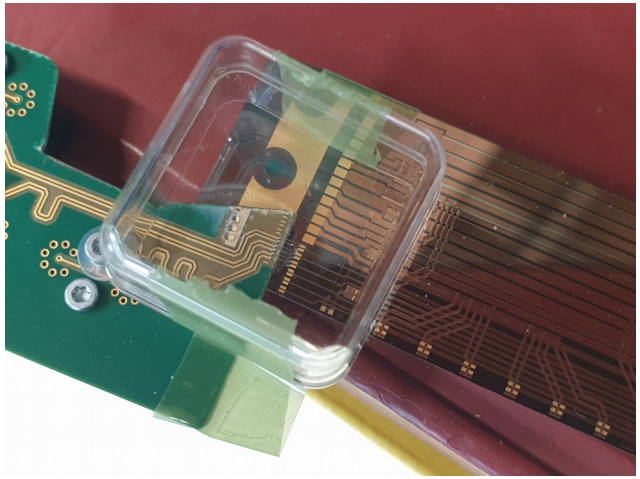


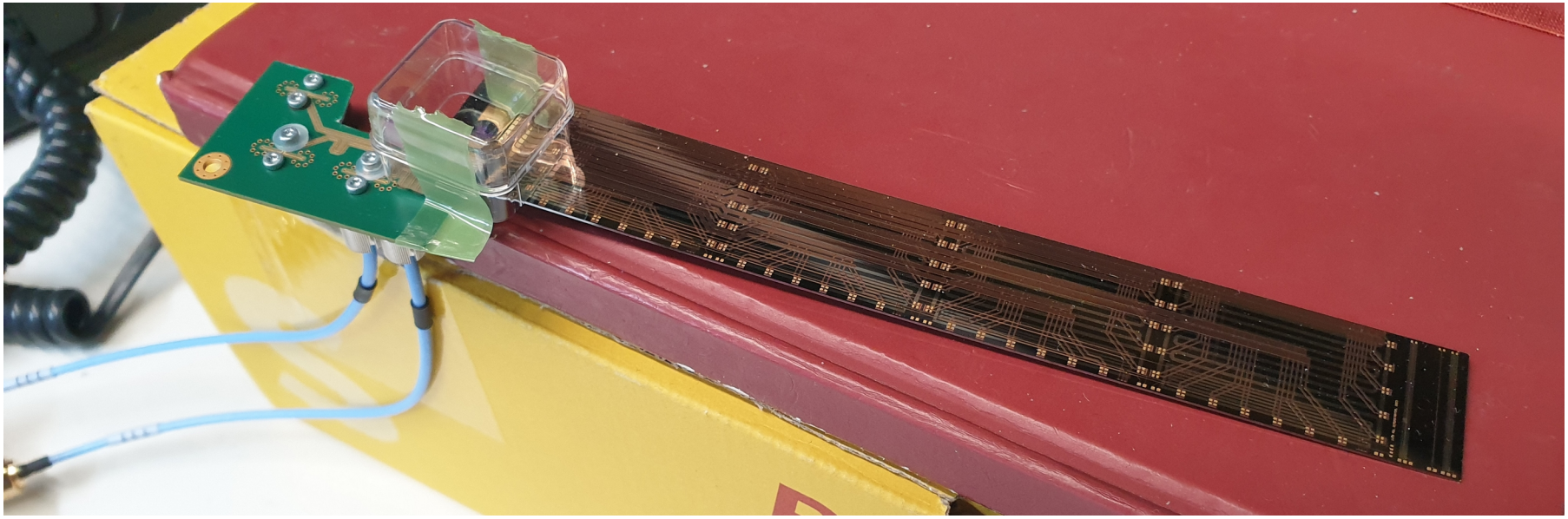


TDR MEASUREMENT SETUP

- Cut old test PCB with high frequency connector
- Wirebonded PCB to test traces

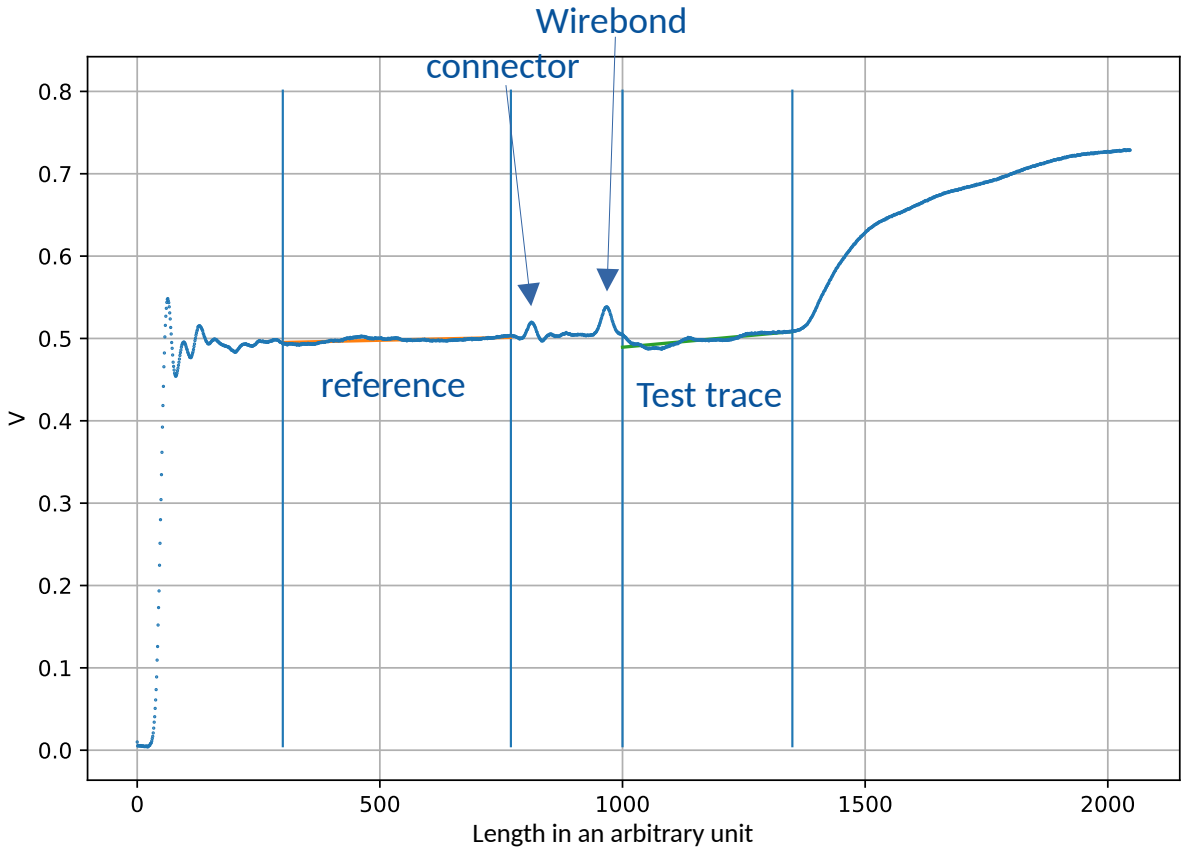






TDR RESULTS ON GOOD TEST TRACE

- Average over cable as reference (100 Ω, differential)
- Fit linear eq. to trace to calculate impedance of trace
- Results:
  - 96.4 Ω at beginning
  - 104.4 Ω at end
  - 100.2 Ω average



Reflection coefficient:

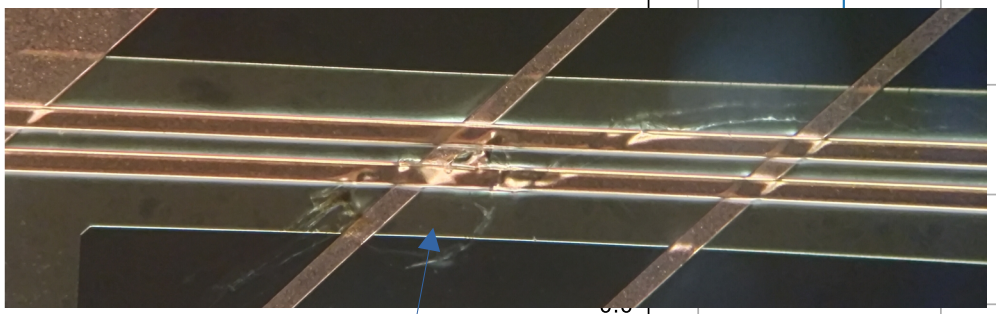
$$\rho_{test} = (V_{test} - V_{in}) / (V_{in} - V_0)$$

Test trace impedance:

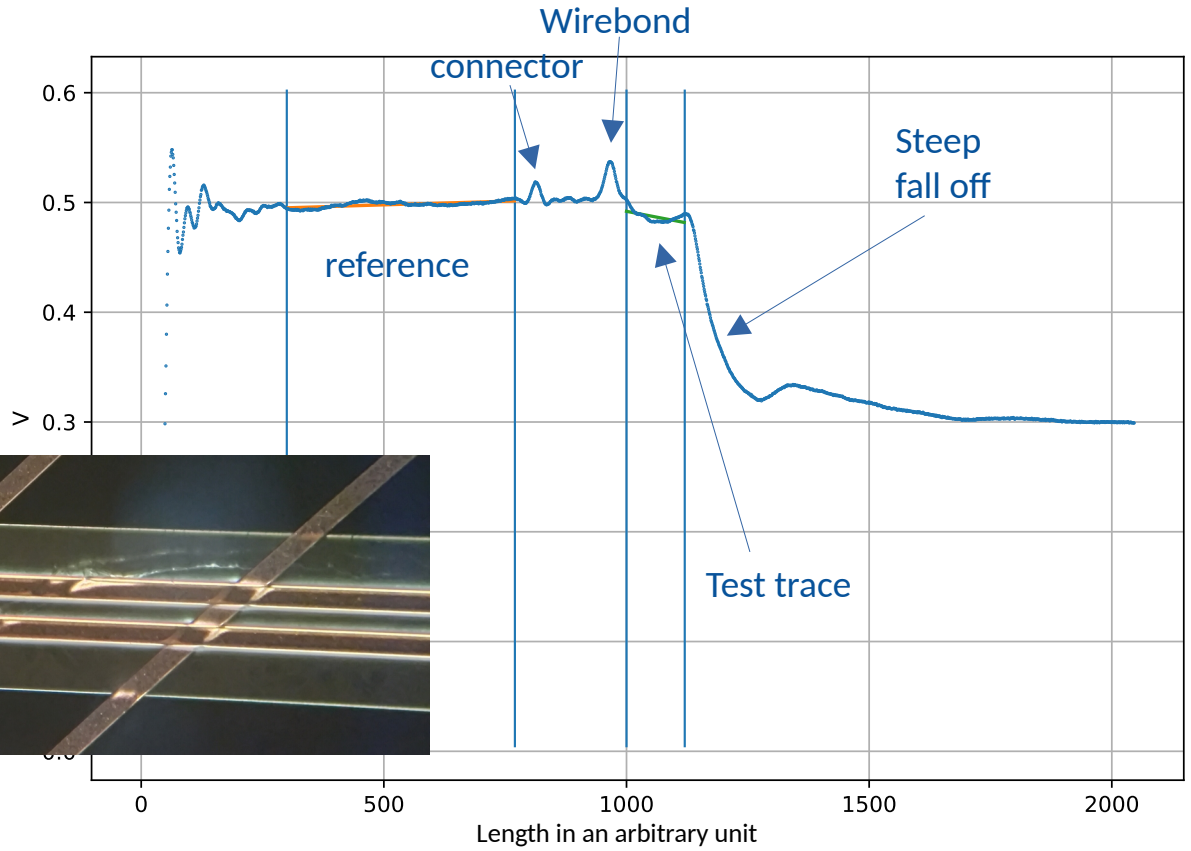
$$Z_{test} = Z_0 * (1 + \rho) / (1 - \rho)$$

TDR RESULTS ON BAD TEST TRACE

- Test trace seems to short
- Impedance falls off at the end
  → Short circuit
- Problem shows under microscope
- Resistance between differential lines 10 Ω



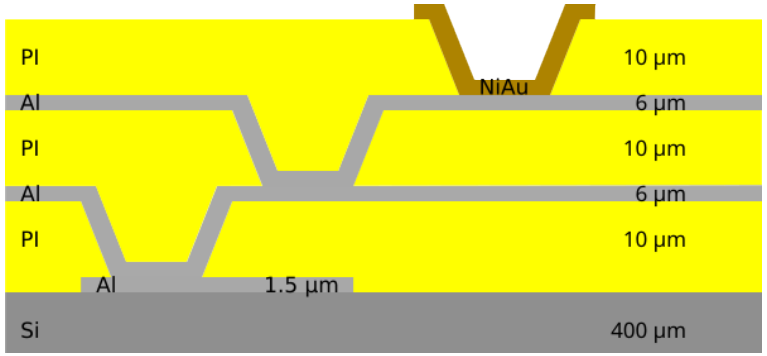
Damaged photo resist



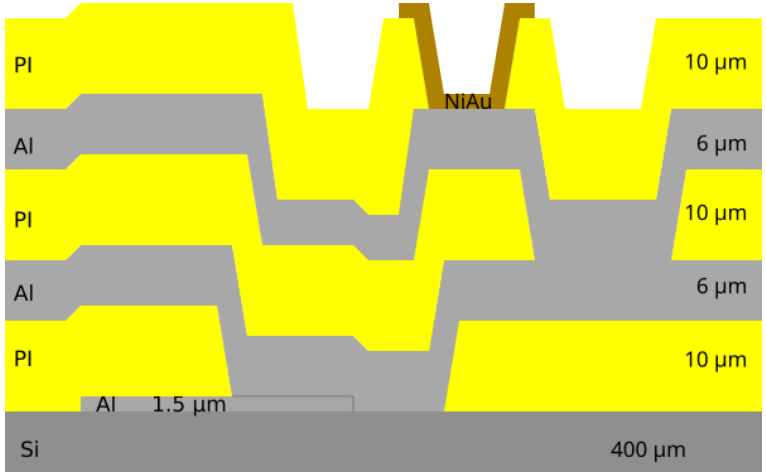
ALL-SILICON LADDER SECOND PROTOTYPE FABRICATION IN FTD CLEANROOM

Main fabrication steps:

- Alternating deposition of metal (6 µm Al) and polymer (10 µm Polyimide)
- Photo lithography, wet chemical patterning



conceptual



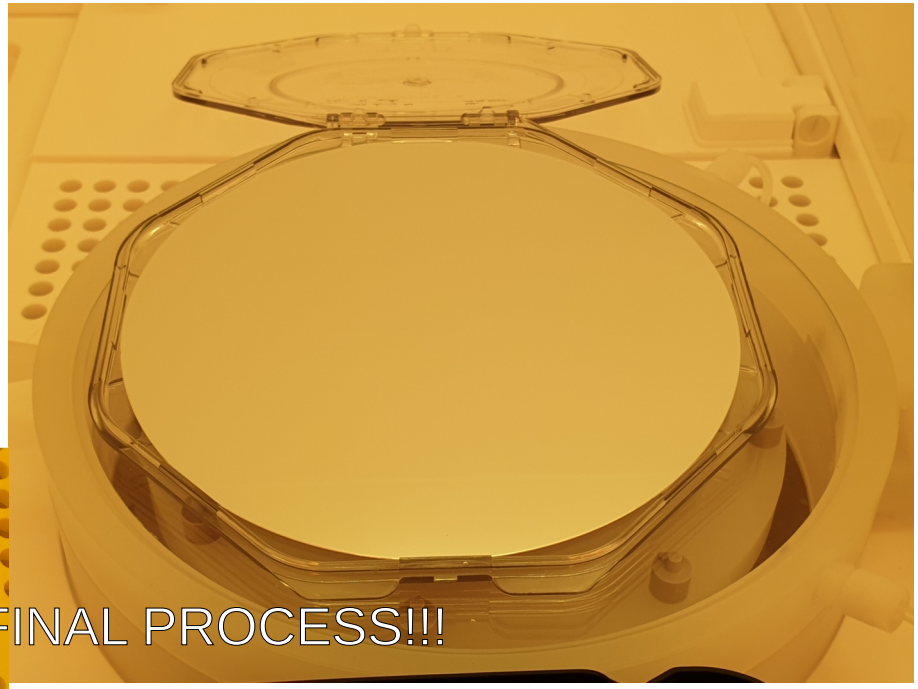
More realistic

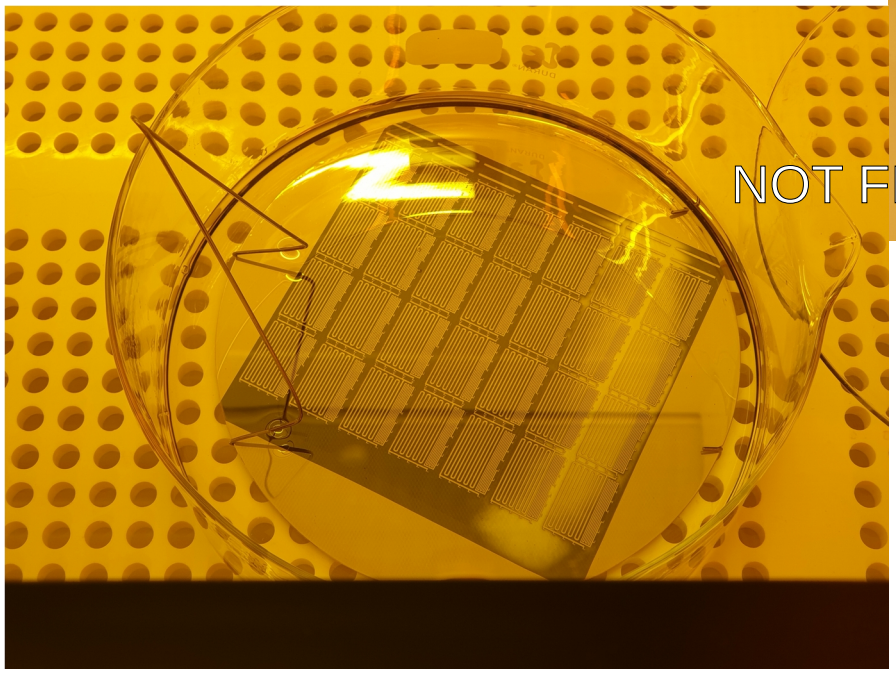
- First polymer layer “VIA1”
  - Openings above sensor bond pads
- First RDL metal “M1”
  - Contacts to sensor bond pads
- Second polymer layer “VIA2”
  - Openings to M1
- Second RDL metal “M2”
  - Contacts to M1
- Passivation layer “VIA3”
  - Openings to M2
- (NiAu bond pads “M3”)
  - Contacts to M2

ALL-SILICON LADDER SECOND PROTOTYPE FABRICATION IN FTD CLEANROOM

1) Deposit first metal layer

2) Deposit photo resist for etching



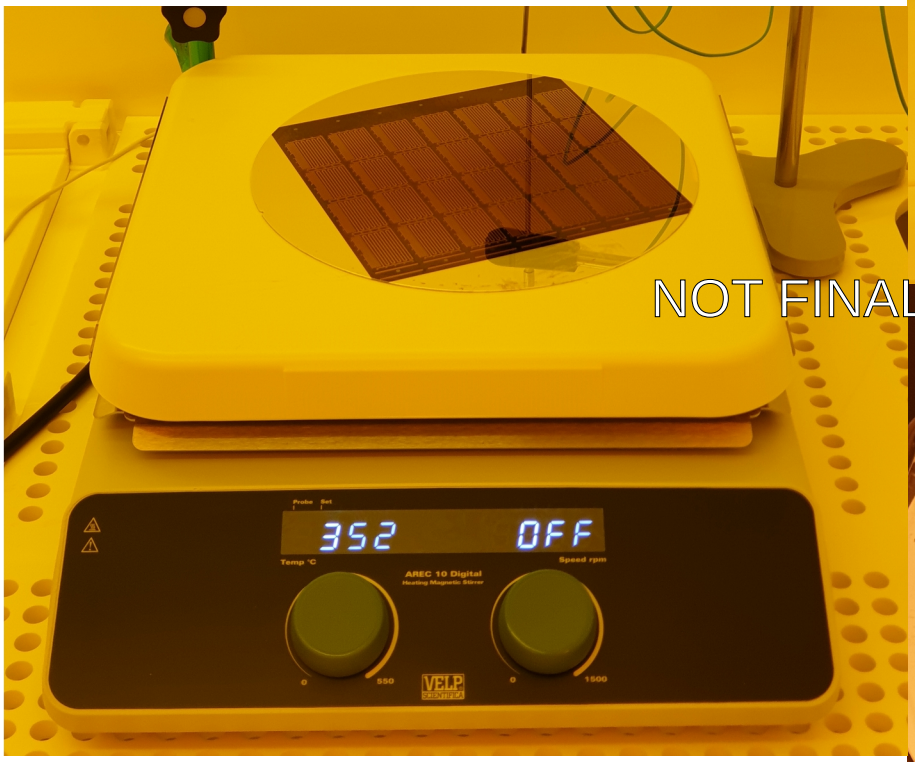


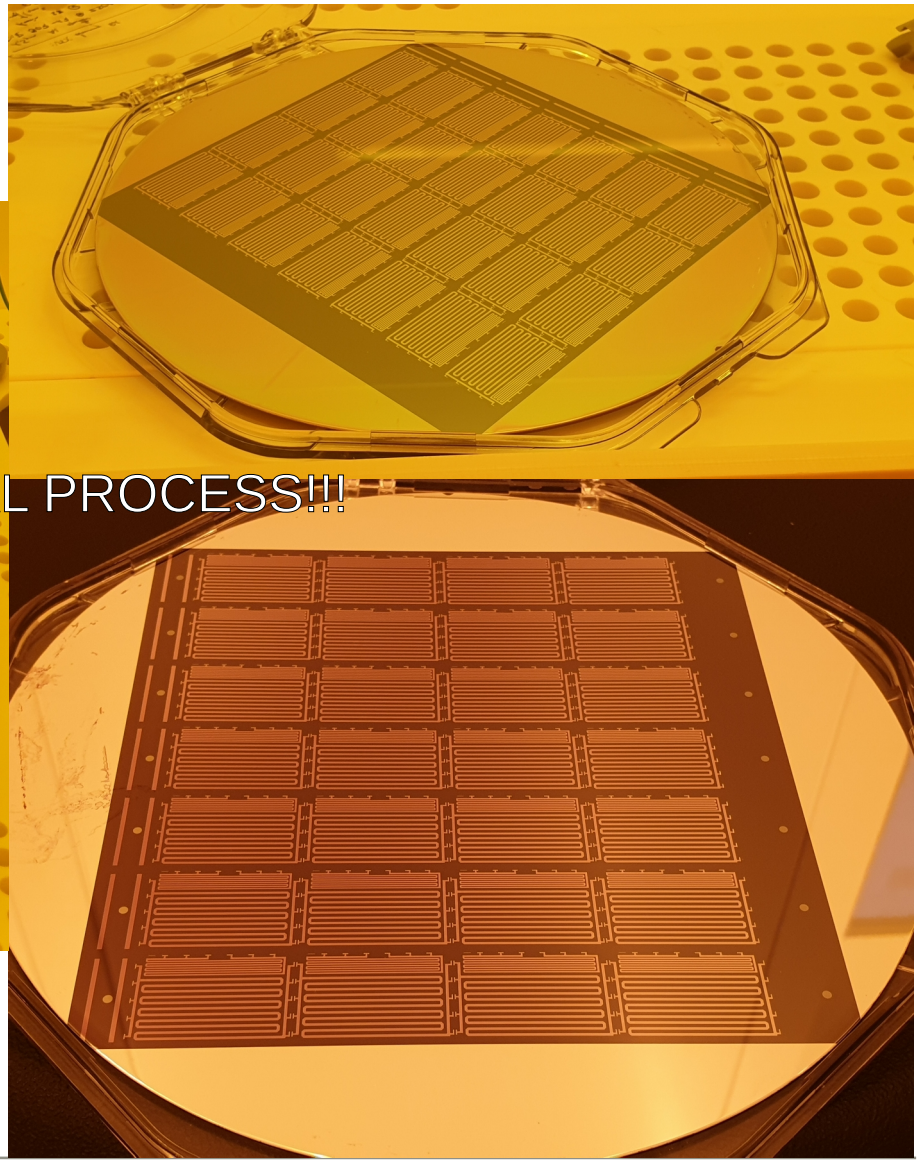
3) Wet etching of aluminum

4) Application of polyimide photo resist

ALL-SILICON LADDER SECOND PROTOTYPE FABRICATION IN FTD CLEANROOM

4) Application of polyimide photo resist





NOT FINAL PROCESS!!!

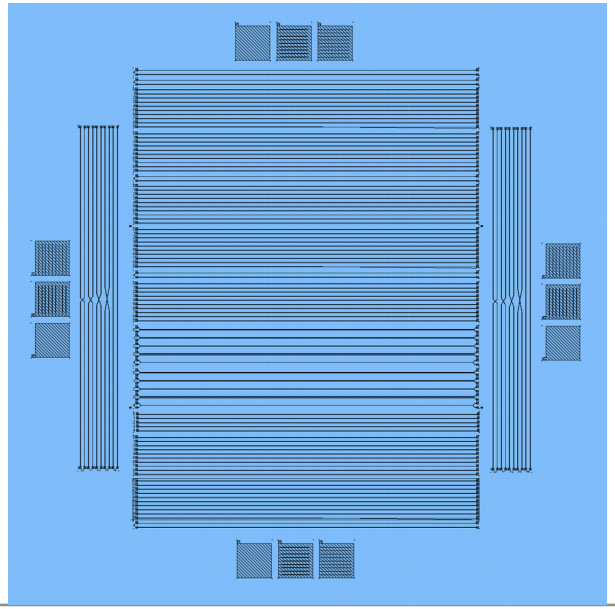
5) Baking of photo resist

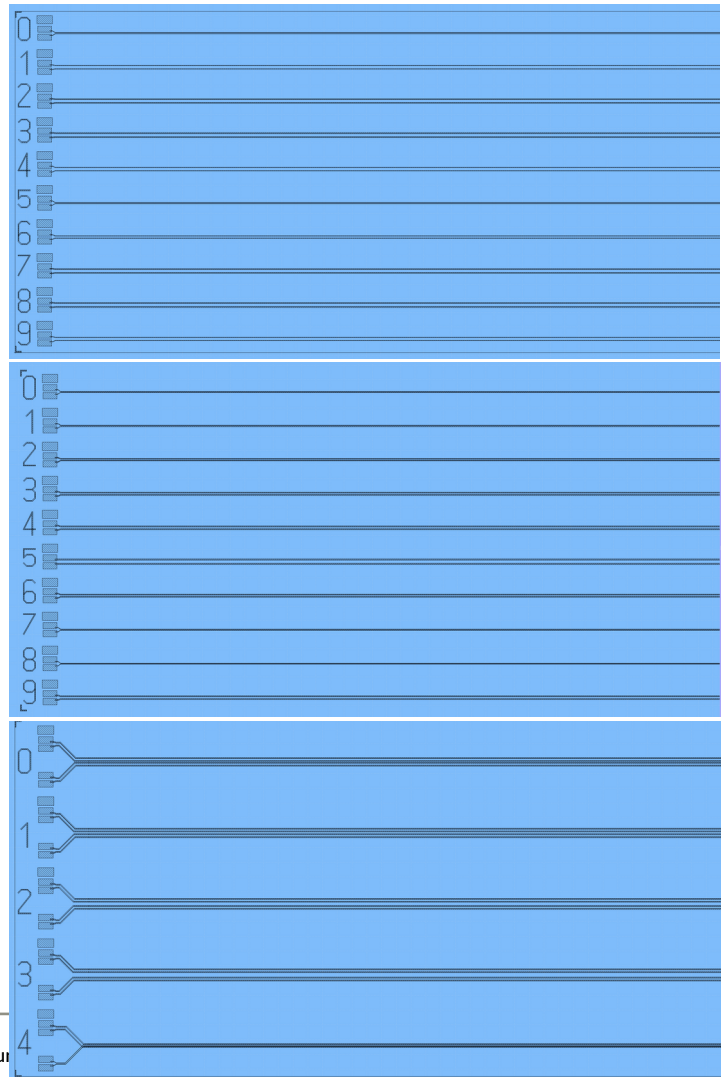
6) repeat from 1)

ELECTRICAL TEST STRUCTURES

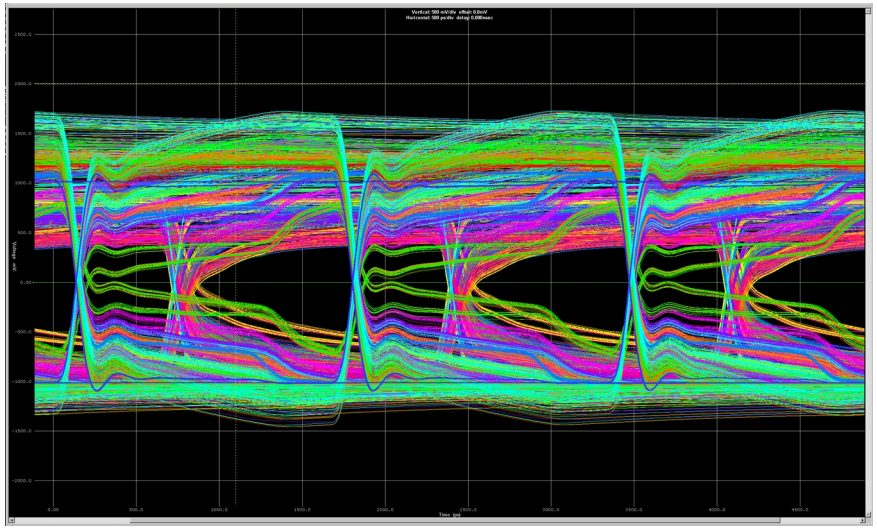
For better and more measurements we designed some test structures to test the properties of traces and our process:

- Different trace width and spacing
- Impedance matching
- Different polyimid thicknesses
- Crosstalk test structures
- Vias & Quality controll
- Capacities
- Bond pads
- Alignment





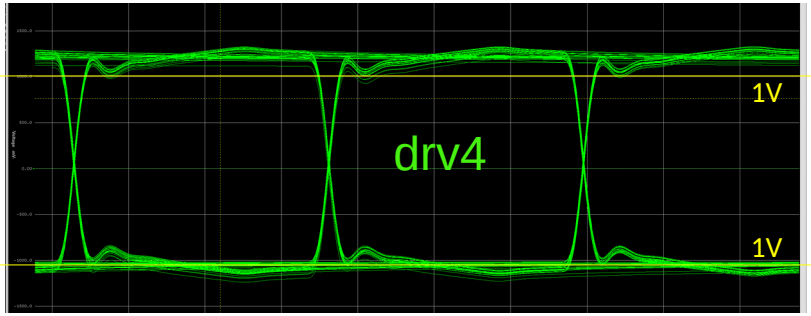
ELECTRICAL SIMULATIONS (PRELIMINARY)

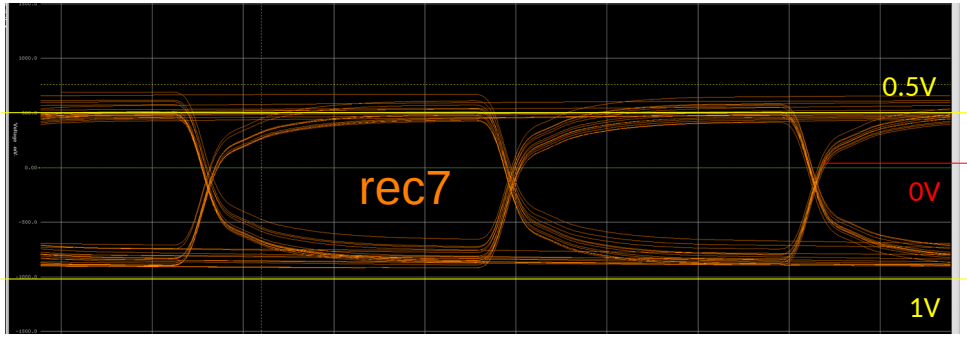


Trace design originates from simulation:

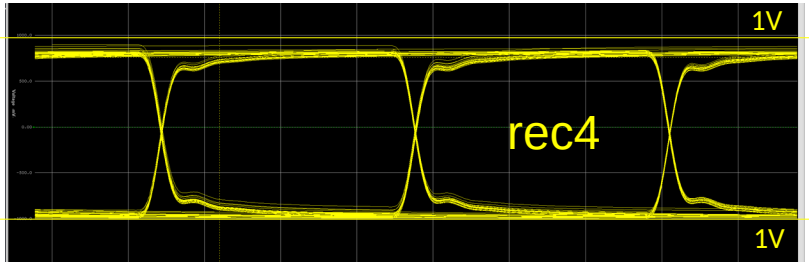
- Important features are:
  - Impedance matching
  - Rise time of signal edge
  - Signal loss over trace
- Simulation set to
  - 600 Mbps
  - 1V
  - differential

Some examples (arbitrary names):





Rec7 shows a lot of amplitude loss over a 10 cm trace, even though the eye still looks ok



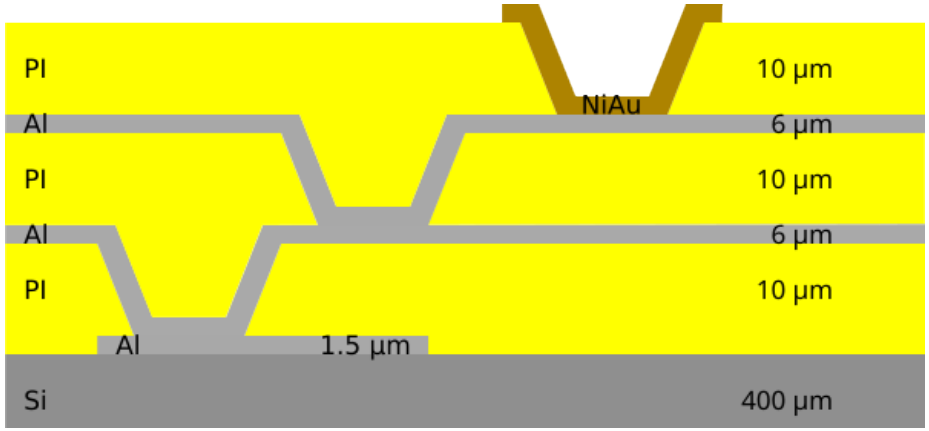
Rec4 shows a pretty nice example. A wide open eye with max and min voltage around 1V (input voltage).

MATERIAL BUDGET

The contributions to Material Budget:

- Main contribution Silicon:

400 µm	0.427% X_0
300 µm	0.32% X_0
100 µm	0.107% X_0



Assuming homogeneous distribution over whole ladder. As structuring leads to places with no/less Al, the material budget will be lower.

- RDL Contibutions:

Material	Thickness	X_0
Copper	3 µm	0.021% X_0
Aluminum	6 µm	0.0067% X_0
Polyimid	10 µm	0.0035% X_0
NiAu	100 nm	0% X_0

- RDL total:

Material	Thickness	X_0
Aluminum	2 x 6 µm	0.0135% X_0
Polyimid	2 x 10 µm	0.007% X_0
Total	32 µm	0.0205% X_0

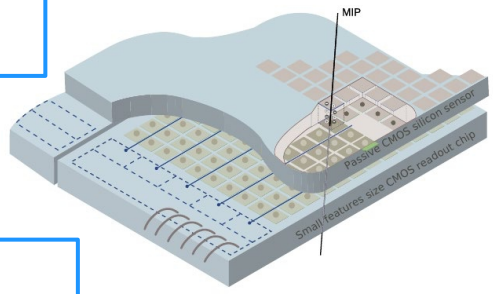
For Cu RDL: 0.0488% X_0 in total

ULTRA THIN HYBRIDS CONCEPT

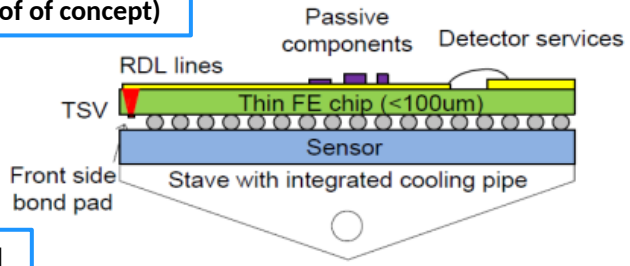
- Want to reduce mass, i.e. thickness of pixel detectors as much as possible while keeping the benefits of the hybrid approach:
  - Separate development and optimization of sensors and FE electronics allowing for best performance of FE electronic and sensor.
  - Fine pitch interconnection between FE and sensor pixel with a pitch down to ~20µm.
  - Thinning of FE and sensor parts to the minimum.
  - Can benefit from active CMOS sensor development by integrating some electronic already into the sensor

- Target is the development of ultra-thin hybrid pixel detectors based on:
  - 50 – 100 µm thick pixel sensor on 200 (300) mm CMOS wafers
  - ~20 µm thick pixel FE chip thickness on 200 (300) mm CMOS

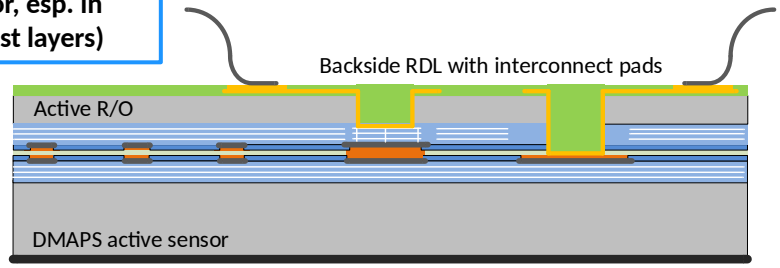
Standard hybrid pixel module:
150 µm FE & 150 µm sensor
2013 (ATLAS IBL & ITk)



TSV hybrid pixel module:
80 -100 µm FE & 150 µm sensor
2019 (AIDA 2020 proof of concept)

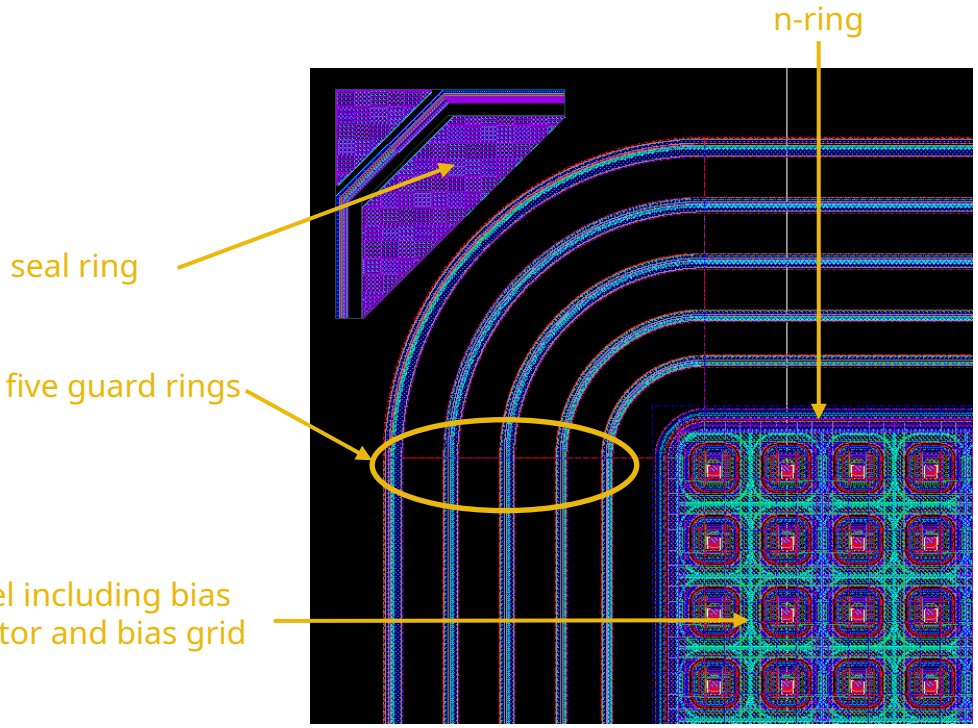


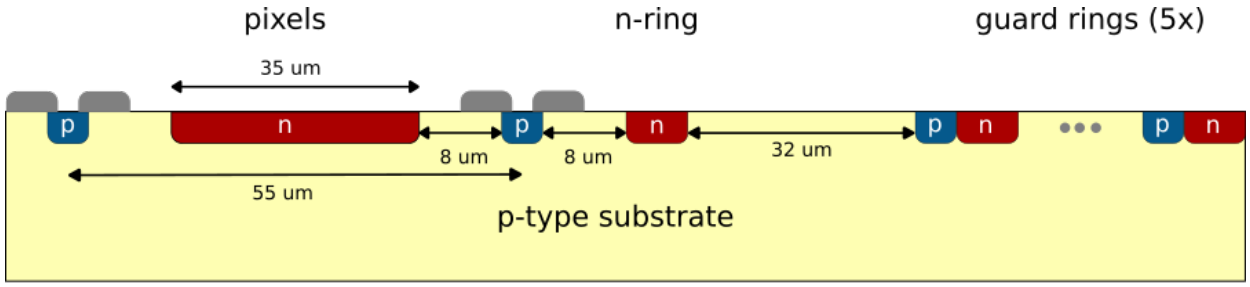
Ultra thin hybrid pixel module:
~20 µm FE &
50 -100 µm sensor
2025 (future tracking detector, esp. in innermost layers)



CMOS PIXEL SENSOR DESIGN

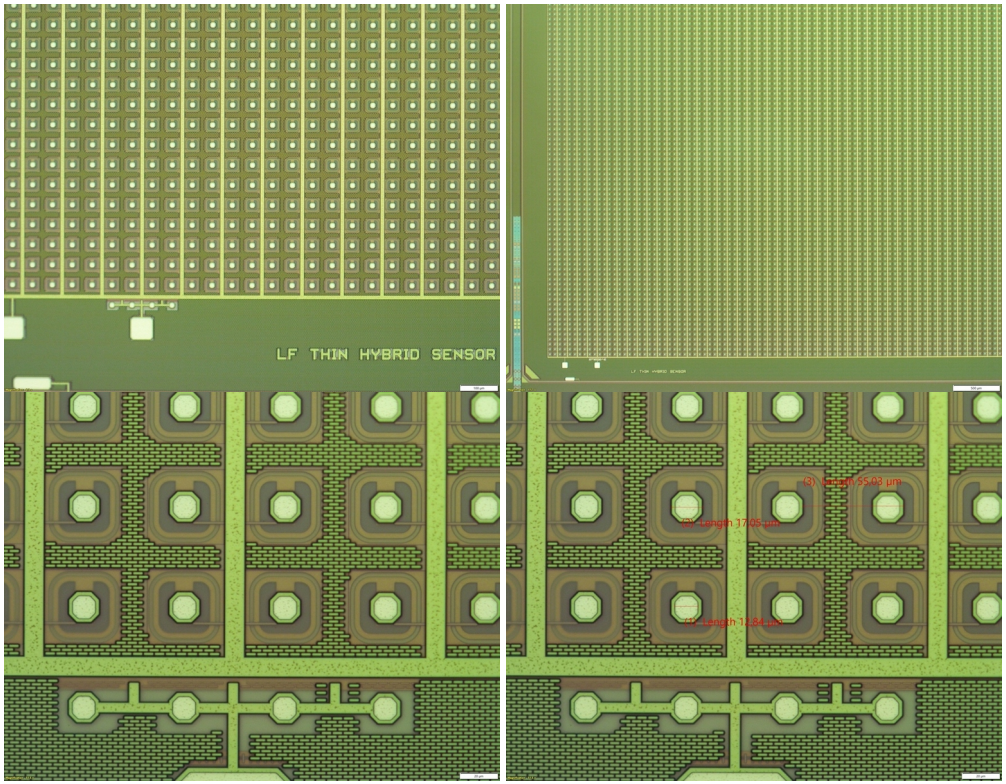
- Strategy: „copy“ layout from former passive CMOS submissions at LFoundry:
  - Match pixel size with TimePix3 pixel size → 55 µm pixels
  - Increase n-well size to 35 um → keep 8 µm spacing between n-well and p-stop
  - Poly-silicon bias resistor implemented (and bias grid)
  - N-ring surrounding the pixel matrix → 32 µm spacing between n-ring and p-well (from 1st guard ring)
  - Five n+p guard rings





CMOS PIXEL SENSOR FABRICATION

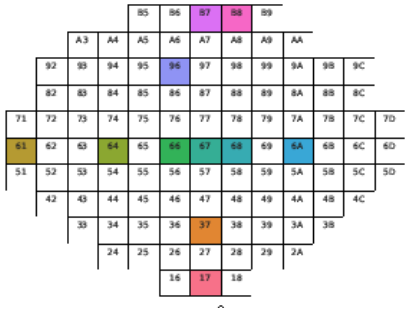
- Fabrication of sensor wafers done in 2024 at LFoundry with an engineering run
- 23 sensor wafers delivered in late 2024
- Wafers are now at IZM for postprocessing
  - 2 wafers have been processed with backside metallization and front side handling wafer removal
  - Visual inspection showed no obvious issues
  - Wafer are shipped to Bonn and Dortmund for sensor testing

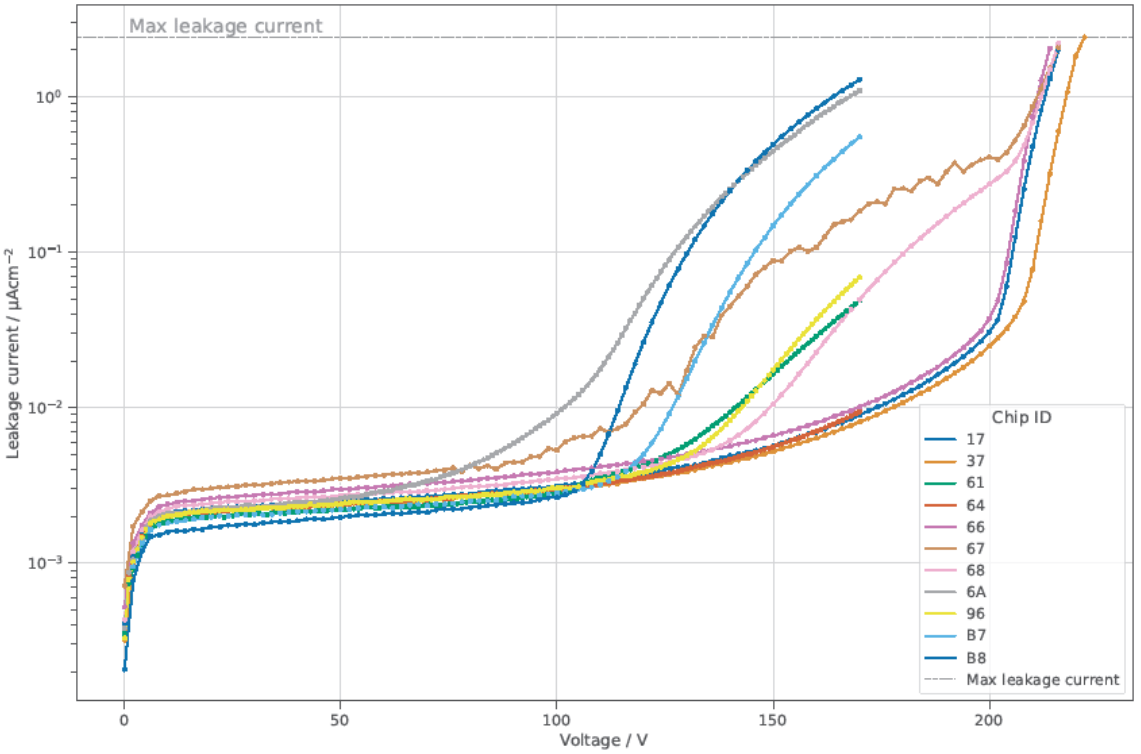


CMOS PIXEL SENSOR FIRST TEST

LF Thin Hybrids First wafer (???)

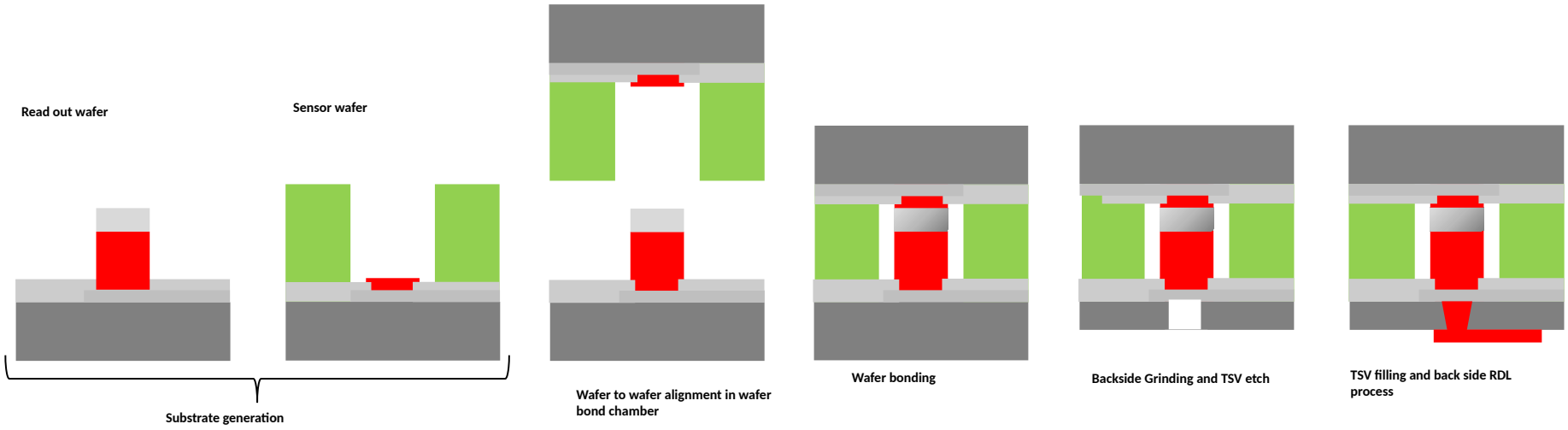
- The first measurements were carried out on 11 evenly distributed chips
  - The bias grid was grounded, and the N-ring remained floating
  - Contact with the chips was made manually - slow process!
  - Tested first up to a lower voltage
  - Breakdown occurs at ~ 200 V for chips tested up to 300 V
- **Sensors work as expected!**
  - More testing planned at Bonn & Dortmund





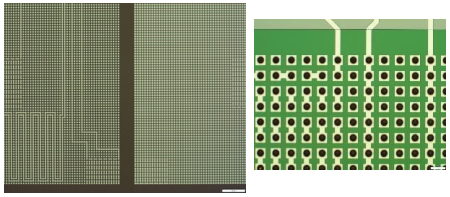
GENERAL PROCESS FLOW

- The Cu/Sn wafer bonding is a well established process
- The Cu/Sn bond will be supported by spin coated, photo-structured polymer layer which is joined simultaneously (polymer hybrid wafer bonding)
- Depending on total wafer stack thickness a mechanical support during TSV formation and backside RDL process will be required

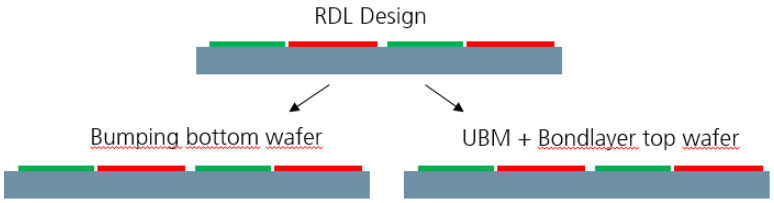


WAFER TO WAFER BONDING – PROCESS EVALUATION

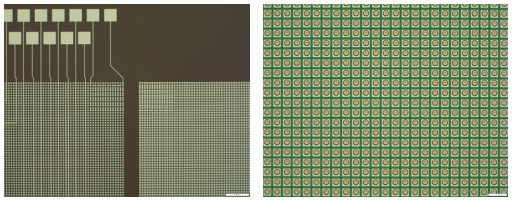
W2W bonding setup bottom wafer:



Bottom wafer with Cu-SnAg pillar



W2W bonding setup top wafer:



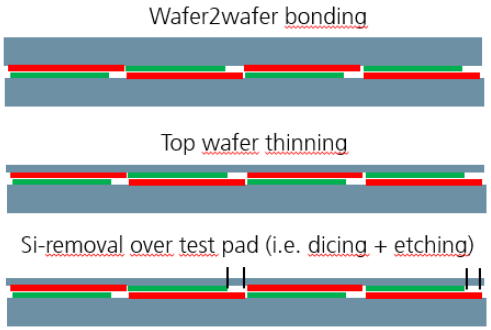
Top wafer with Cu-Pad and polymer layer

- Three wafer stacks for evaluation:

1) Planar Glass-Si wafer: optical bonding interface characterization (fast track)

2) Planar Si-wafer with UBM: polymer bonding with topography wafer

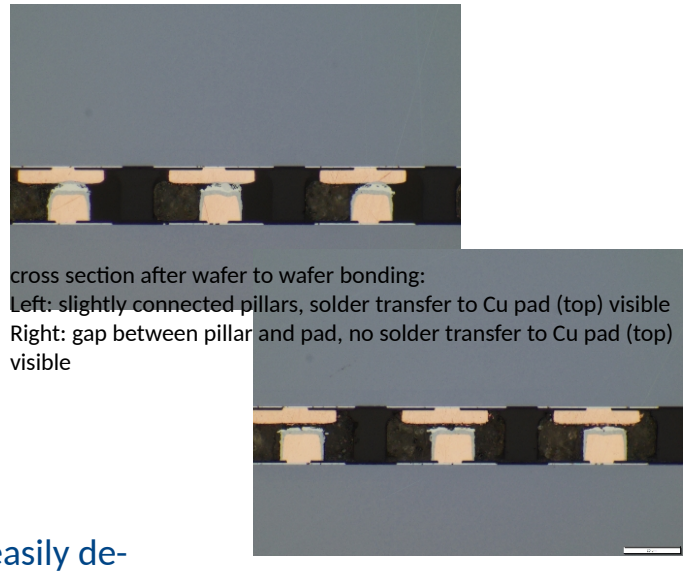
3) Daisy-chain-test wafer (silicon to silicon): bonding process evaluation with focus on polymer layer thickness – Pillar/UBM height tolerances



Process Development Goal:

Evaluation of a bonding material that enables the combination of a polymer glue bonding process with the Cu-SnAg pillar bonding process

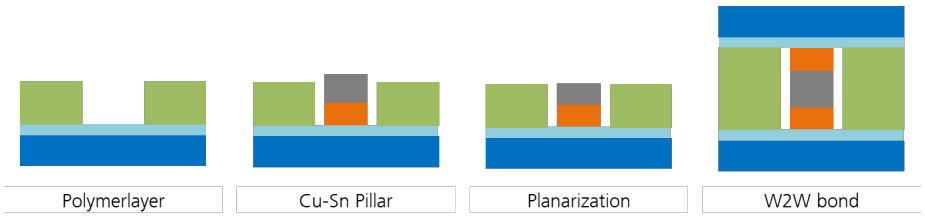
WAFER TO WAFER BONDING – PRELIMINARY RESULTS

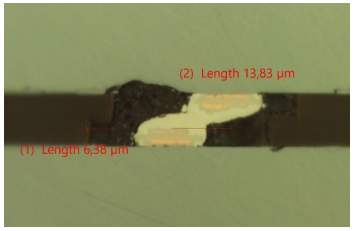


cross section after wafer to wafer bonding:
Left: slightly connected pillars, solder transfer to Cu pad (top) visible
Right: gap between pillar and pad, no solder transfer to Cu pad (top) visible

Preliminary Process Results:

- Process evaluated for 20µm polymer layer thickness, measured bond layer thickness: 21µm (+/- 0.5µm across the wafer)
- Pillar height: 13…15µm (as plated) (tolerances across the wafer)
  Cu pad height: 5.5µm (+/- 0.5µm across the wafer)
- Thinning of top wafer to 80µm thickness possible
- Dicing of wafer stack possible
- Low adhesion between top and bottom chip after dicing (chips can be easily de-bonded)
- Large area solder transfer from CuSnAg-pillar (bottom chip) to Cu pad (top chip) visible after top chip debonding but some pillars are not connected to Cu pads (see cross section)
- Bonding without additional pillar bumps planarization suffers from total height variations across the wafer
- → **Solution: Development of Pillar-Planarization Process**





cross section after W2W bond (1000x):
Top and bottom pillar shifted due to missing alignment marks on short loop test wafers but formation of interconnects are as expected

W2W BONDING – PROCESS EVALUATION SUMMARY

Conclusions:

- Lateral dimension (x, y) of bonding structures are sufficient to handle the W2W alignment tolerances (pad-, pillar-, polymer-via diameter)
- Very narrow tolerances in z-direction: pad – pillar – polymer thickness must and can be optimized by pillar-polymer layer planarization

Status and next steps for process definition and design of the final object:

- Adaption of process flow including TSV and RDL formation done
- Process step definition fixed
- Individual pixel side design finished (polymer bonding layer and pillar design for readout and sensor wafer)
- W2W bonding alignment mark configuration fixed
- Discussion on TSV and TMPX3 TSV and backside RDL ongoing (CERN, IZM, Bonn University)
- LFoundry DMAPS wafer (thickness 150 µm) in process:
  - Backside metallization on LF sensor wafer finished
  - Debonding of pixel side carrier wafer (from LF processing) ongoing
  - Next step: start of wafer processing for W2W bonding (backside carrier bonding, polymer layer, pillar formation and planarization)

SUMMARY

- All-Silicon Module approach viable for CMOS sensors with high yield
- Big reduction of material budget when air or contact cooled
- Relatively easy and somewhat cheap to produce
- Currently optimizing RDL layers for signals and power

- Thin Hybrid Modules combine advantages of low material budget and independent development of sensor and FE chip
- Possibility to combine concept with All-Silicon approach to reduce material even further
- Currently developing reliable wafer to wafer bonding process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