



Efinix Technology and Future Outlook

Fabian Kluge



- **Founded : 2012**
- **HQ in Cupertino, California, U.S.A.**
- **200+ Employees Worldwide**

A Silicon Valley Company with International Footprint



Leaderships



Ming Ng

COO & Sr. VP Service
30+ Years of Experience



Mark Oliver

VP, Americas Marketing & BD
35+ Years of Experience



Sammy Cheung

President & CEO
30+ Years of Experience



Tony Ngai

CTO & Sr. VP Engineering
35+ Years of Experience



Jay Schleicher

SVP, Software Engineering
30+ Years of Experience



Ikuo Nakanishi

VP, JAPI Sales & Biz Dev.
25+ Years of Experience



Harald Werner

VP & MD, EMEA Business
35+ Years of Experience



Jing Kuo

VP & GM, China Business 25+
Years of Experience

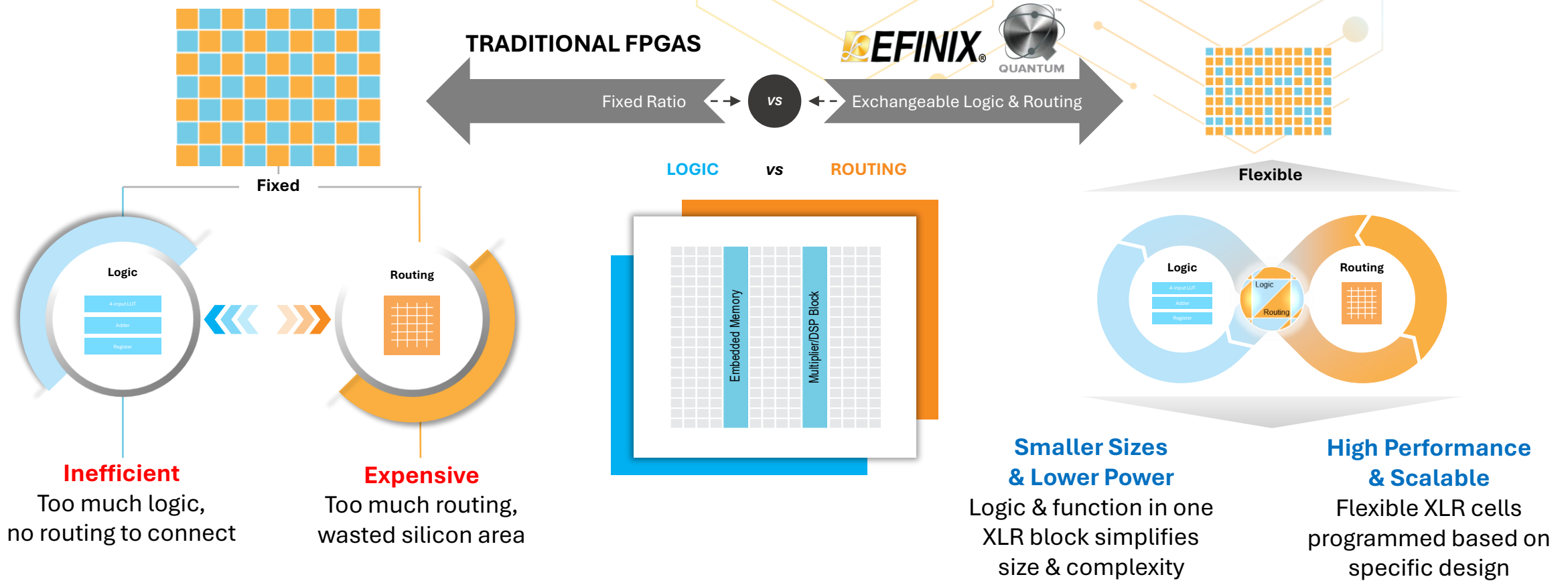


Ching Lun Yan

VP, Intelligent Solutions
15+ Years of Experience



Patented FPGA Architecture





Unique Differentiation

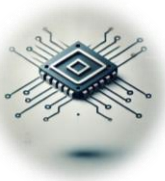
Advantages



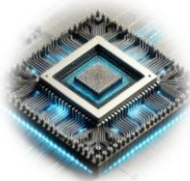
**Higher
Performance**



**Lower
Power**



**Smaller
Footprint**



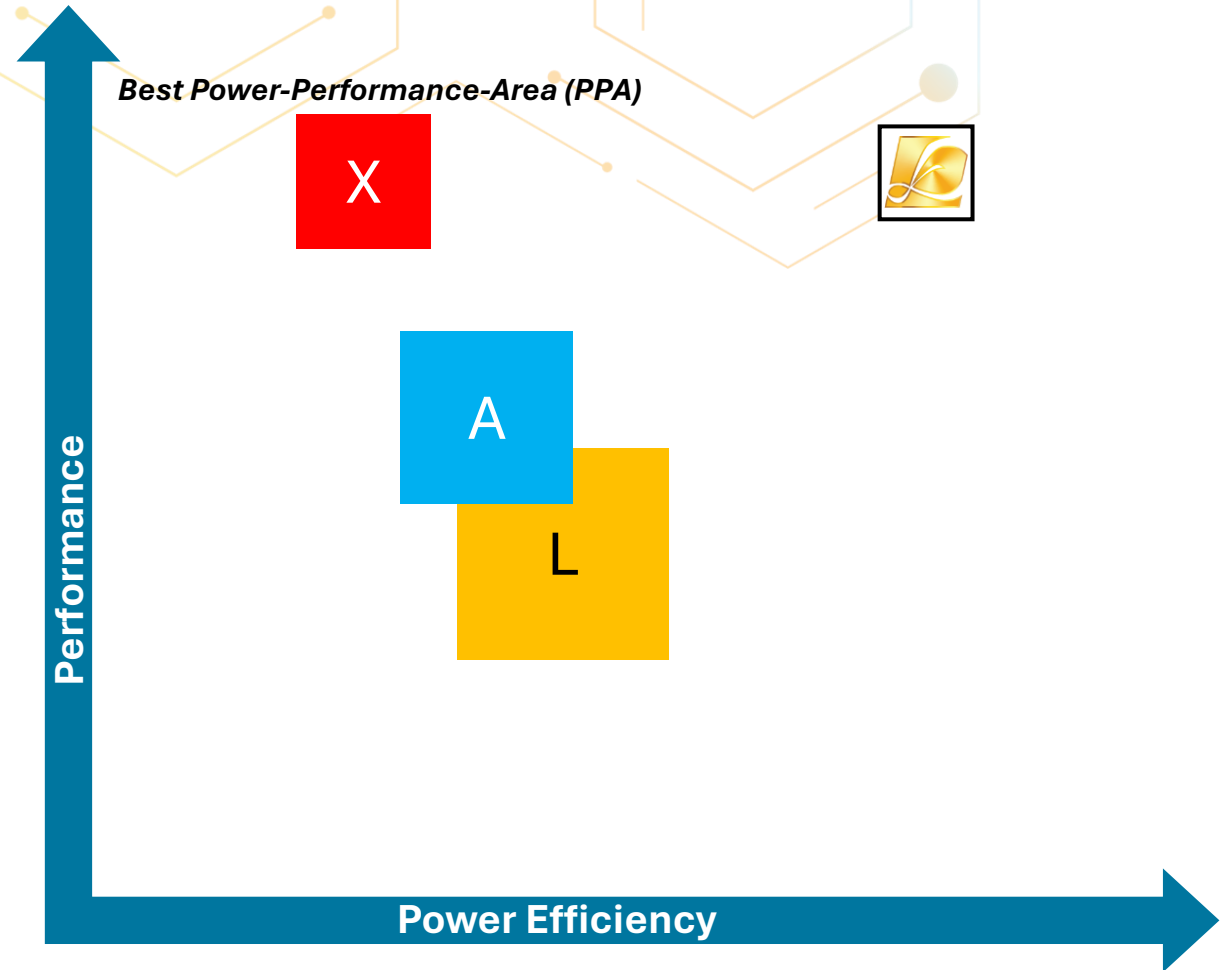
**Scalable
to High Density**



**Competitive
Price**



**Lowest
Development Cost**





A Complete Product Portfolio



General FPGA

IO Rich, Wide Range Selection, MIPI DPHY
CSI, DDR



Value for Mainstream Markets

Performance, Low Power, 12Gbps SerDes, LPDDR4 & MIPI
DPHY 2Gbps



High Performance & Low Power

Low Power, Size, 3.3Gbps LPDDR4/4x &
MIPI DPHY 2.5Gbps



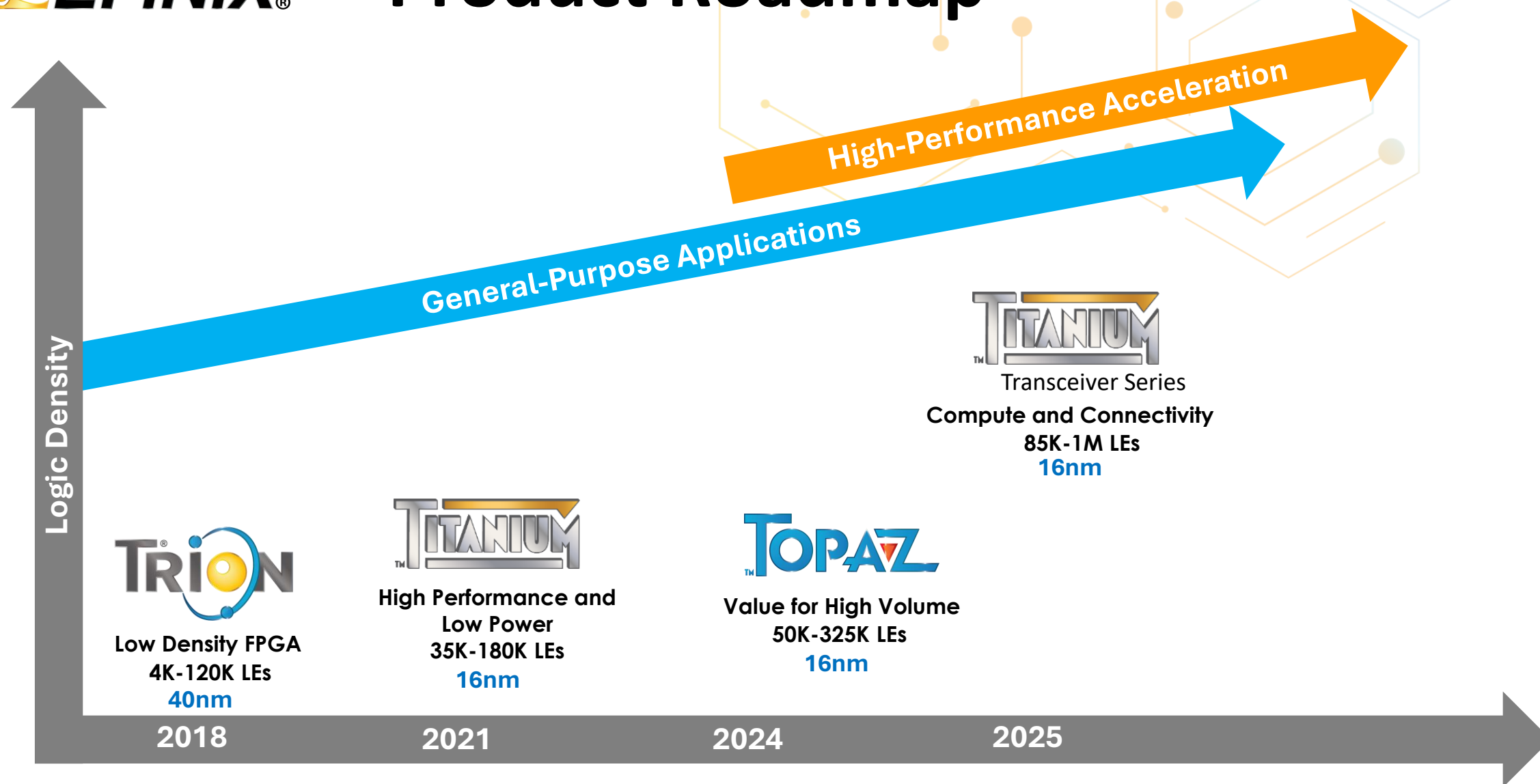
Serdes Series

Ultimate Compute & Connectivity

16/25Gbps Multi-Protocol SerDes, PCIe Gen4
Controller, Quad Core RISC-V CPU



Product Roadmap





Small form factor

Low power advantage enable Efinix lead in small form factor offering!

Ti60W64

3.5x3.4mm

**0.5mm ball pitch
WLCSP package**

Ti60F100S3F2

5.5x5.5mm

**0.5mm ball pitch
SIP 256Mb HyperRAM
+ 16Mb Flash**

Ti180J484D1

15x15mm

**0.65mm ball pitch
SIP 2Gb LPDDR4x
3000Mbps**

Ti135N567D2F4

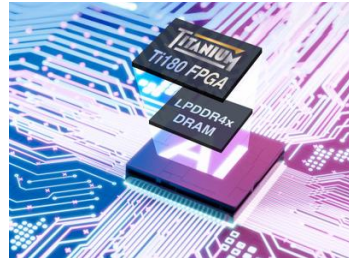
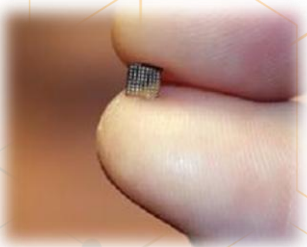
16x16 mm

**0.65mm ball pitch
8x 16 Gbps Serdes
PCIE Gen4
SIP 2Gb LPDDR4X
@3Gbps**

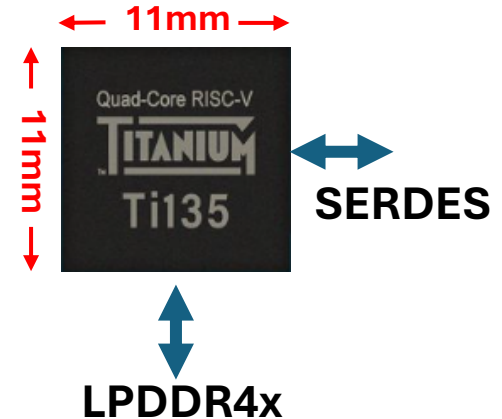
Ti135N441

11x11mm

**0.5mm ball pitch
8x 12.5Gbps Serdes
PCIE Gen3**



SERDES





Titanium Family Table



	Ti35	Ti60	Ti80**	Ti85	Ti90	Ti120	Ti125**	Ti135	Ti165	Ti180	Ti240	Ti375	Ti550	Ti750	Ti1000
LE (k)	36	62	79	83	92	123	123	134	162	176	237	370	550	750	1000
10K RAM (Mb)	1,53	2,62	3,70	6,18	7,34	9,80	5,90	9,95	12,10	13,11	19,37	27,53	39,65	55,80	74,40
DSP	93	160	288	300	359	478	288	486	590	640	946	1344	1936	2736	3648
PLLs	4	4	7	12	10	10	7	12	12	10	12	12	12	12	12
HVIO	34	34	35	133	80	80	35	133	181	80	181	181	200	200	200
HSIO	146	146	200	139	232	232	200	139	235	232	235	235	320	320	320
MIPI DPHY 1.5G, support CSI-2/DSI	Yes	Yes	-	Yes	Yes	Yes	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MIPI HSIO 2.5G, support CSI-2/DSI	-	-	Yes	-	-	-	Yes	-	-	-	-	-	Yes	Yes	Yes
MIPI DPHY x4 2.5Gbps Hard IP	-	-	-	X2	X4	X4	-	X2	X3	X4	X3	X3	X3	X3	X3
LPDDR4/X (> 3Gbps)	-	-	-	X32	X32	X32	-	X32	2 X32	X32	2 X32	2 X32	2x72	2x72	2x72
RISC-V hardwired	-	-	-	x	-	-	-	x	x	-	x	x	x	x	x
16 Gbps Serdes	-	-	-	X8	-	-	-	X8	X16	-	X16	X16	X16	X16	X16
25.8 Gbps Serdes	-	-	-	-	-	-	-	-	-	-	-	-	X8	X8	X8
PCIe Gen4 (16G) hard controller	-	-	-	1x PCIe Gen4x4	-	-	-	1x PCIe Gen4x4	2x PCIe Gen4x4	-	2x PCIe Gen4x4	2x PCIe Gen4x4	2x PCIe Gen4x8	2x PCIe Gen4x8	2x PCIe Gen4x8
Packages (HSIO/HVIO/LPDDR4/MIPI /SERDES)															
W64	0.4mm	3.5x3.4mm	-	34/0	-	-	-	-	-	-	-	-	-	-	-
F100 (SIP)	0.5mm	5.5x5.5mm	61/0	61/0	-	-	-	-	-	-	-	-	-	-	-
F100	0.5mm	5.5x5.5mm	61/0	61/0	-	-	-	-	-	-	-	-	-	-	-
F225	0.65mm	10x10mm	140/23	140/23	140/23	-	140/23	-	-	-	-	-	-	-	-
F169 (SIP)	0.65mm	9x9mm	-	-	83/27	-	83/27	-	-	-	-	-	-	-	-
F256	0.8mm	13x13mm	142/27	142/27	-	-	-	-	-	-	-	-	-	-	-
J361	0.65mm	13x13mm	-	-	-	110/20/16/2/0	110/20/16/2/0	-	-	110/20/16/2/0	-	-	-	-	-
G400	0.8mm	16x16mm	-	-	-	200/74/0/0/0	200/74/0/0/0	-	-	200/74/0/0/0	-	-	-	-	-
J484 (SIP)	0.65mm	15x15mm	-	-	-	-	-	-	-	190/54/0/2/0	-	-	-	-	-
J484	0.8mm	18x18mm	-	-	-	116/27/32/4/0	116/27/32/4/0	-	-	116/27/32/4/0	-	-	-	-	-
J324	0.8mm	15x15mm	-	-	202/30/0/0	-	202/30/0/0	-	-	-	-	-	-	-	-
G529	0.8mm	19x19mm	-	-	-	-	-	-	-	210/48/32/0/0	-	-	-	-	-
C529	0.8mm	19x19mm	-	-	-	-	-	-	176/50/32/0/0	-	176/50/32/0/0	176/50/32/0/0	-	-	-
N441	0.5mm	11x11mm	-	-	86/18/16/1/8	-	-	86/18/16/1/8	-	-	-	-	-	-	-
N576 SIP	0.65mm	16x16mm	-	-	116/50/0/2/8	-	-	116/50/0/2/8	-	-	-	-	-	-	-
N576	0.65mm	16x16mm	-	-	100/34/32/2/8	-	-	100/34/32/2/8	-	-	-	-	-	-	-
N676	0.8mm	22x22mm	-	-	139/84/32/2/8	-	-	139/84/32/2/8	-	-	-	-	-	-	-
N676**	0.65mm	18x18mm	-	-	-	-	-	-	140/84/32/2/8	-	130/63/32/2/12	130/63/32/2/12	-	-	-
N484	0.8mm	18x18mm	-	-	85/21/32/1/8	-	-	85/21/32/1/8	85/20/32/1/8	-	85/20/32/1/8	85/20/32/1/8	-	-	-
N900	0.8mm	25x25mm	-	-	-	-	-	-	168/50/32x2/2RX/16	-	168/50/32x2/2RX/16	168/50/32x2/2RX/16	-	-	-
N1156	1.0mm	35x35mm	-	-	-	-	-	-	234/103/32x2/3/16	-	234/103/32x2/3/16	234/103/32x2/3/16	x	x	x

** subject to change, just in the discussion

Availaible

F100 (SIP) :16 MbFlash + 256Mbit HyperRAM

Available soon (122025)

J484 (SIP) : 2Gb LPDDR4X x16

N576 SIP: 2Gb LPDDR4X x16, SPI flash

F169 (SIP): 2xHyperRam, SIP flash



Titanium Ti60 Highlight

Quantum™ compute fabric

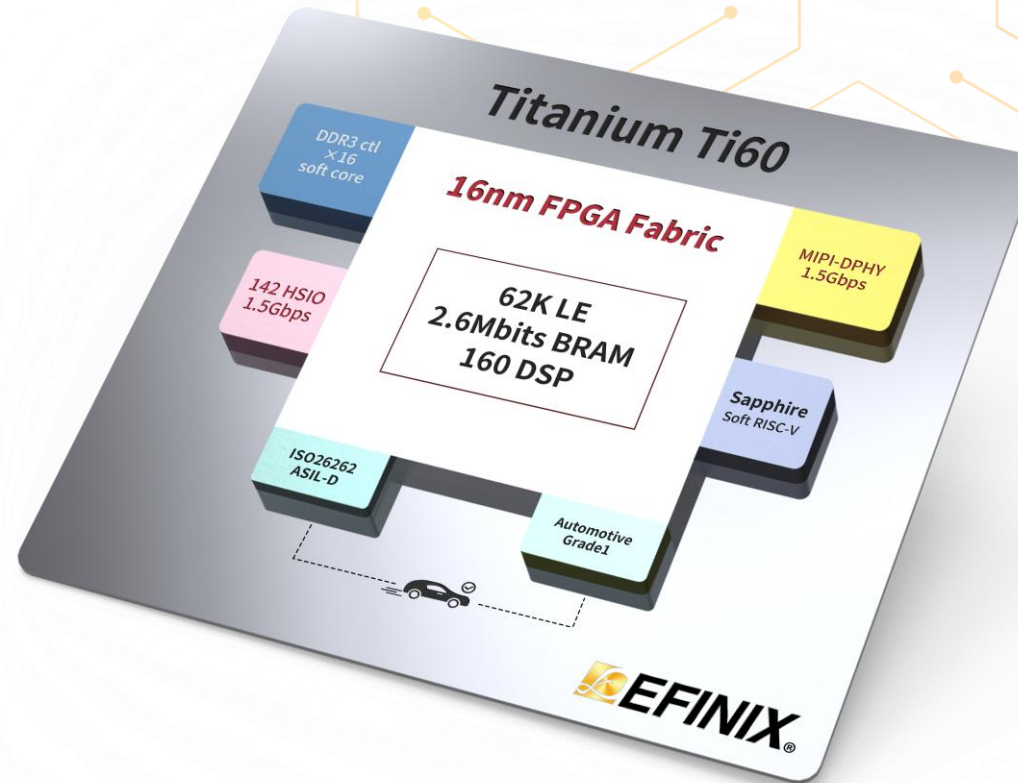
- TSMC 16nm process
- High performance, Low power fabric
- 0.95V and 0.85V (LP mode) support
- High DSP compute capability
- High Embedded Memory resource

Security

- AES-GCM Bitstream Encryption
- AES-GCM Symmetric Authentication
- RSA-4096 Asymmetric Authentication

Qualification

- AEC-Q100



High Voltage IO

- 3.3V, 2.5V, 1.8V capable

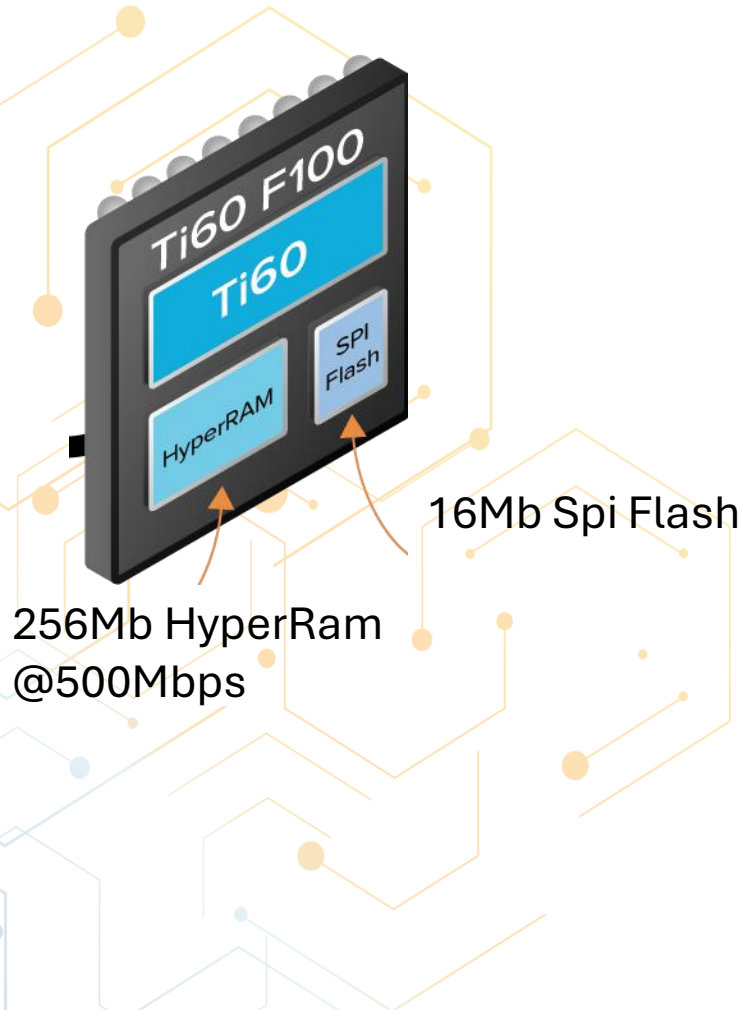
High Speed IO

- LVDS 1.5Gbps
- MIPI-DPHY 1.5Gbps

Sapphire Soft IP

- Up to 350MHz

Ti60F100 SIP



- FPGA with 60K LE, 2.6Mb Memory, 160 DSP Blocks
- BGA 100 Package (5.5x5.5mm, 0.5mm pitch)
- SPI flash 16Mb
- HyperRAM PSRAM up to 6.4Gbps (400Mbps x 16), (256Mb)
 - 500Mbps available soon !
- MIPI-CSI/DSI up to 1.5Gbps support.
 - 2x8 MIPI
 - 2x4 MIPI
- LVDS support up to 1.5Gbps
- VCC: 0.95/0.85V



Titanium Ti125 Highlight

Quantum™ compute fabric

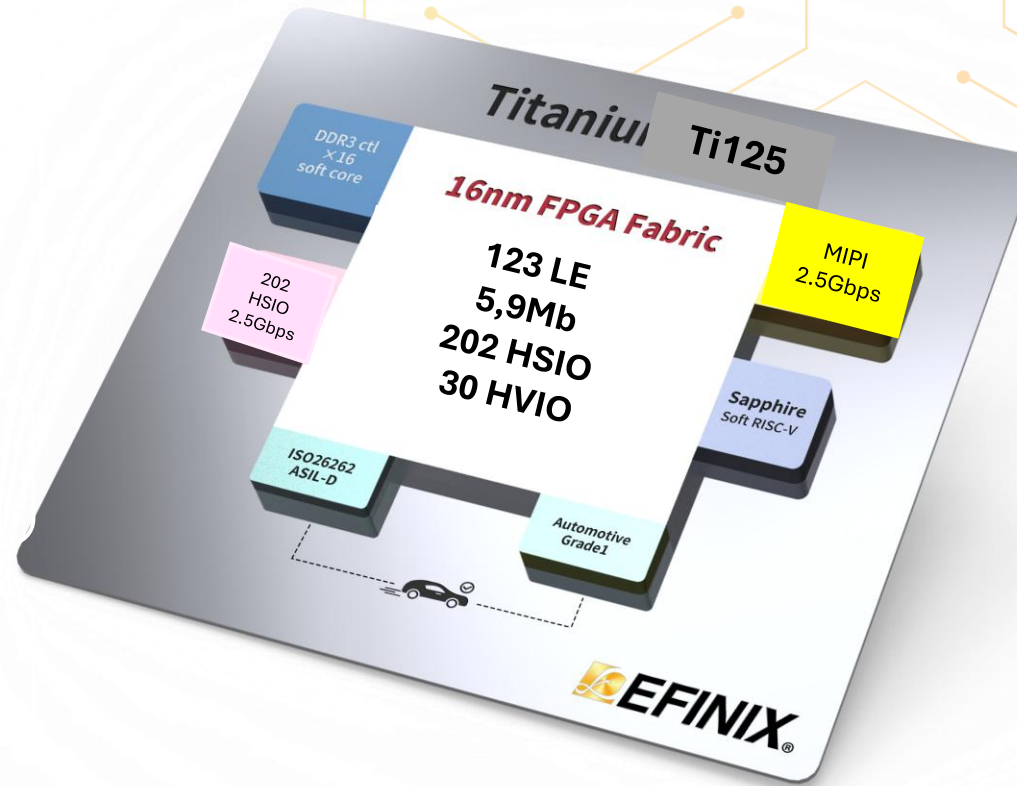
- TSMC 16nm process
- High performance, Low power fabric
- 0.95V and 0.85V (LP mode) support
- High DSP compute capability
- High Embedded Memory resource

Security

- AES-GCM Bitstream Encryption
- AES-GCM Symmetric Authentication
- RSA-4096 Asymmetric Authentication

Memory Controller Soft IP

- Up to 1333Mbps



High Voltage IO

- 3.3V, 2.5V, 1.8V capable

High Speed IO

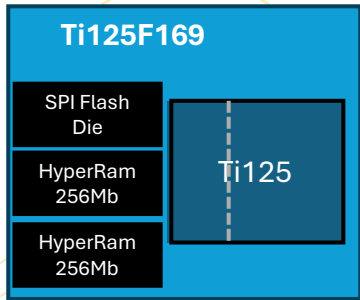
- LVDS 2.5Gbps
- MIPI-DPHY 2.5Gbps

Sapphire Soft IP

- Up to 350MHz



Ti125F169 SIP



- FPGA with 125K LE, 5.6Mb Memory, 288 DSP Blocks
- BGA 169 Package (8x8mm, 0.5mm pitch)
- SPI flash
- HyperRAM PSRAM up to 12.8Gbps (2x(400Mbps x 16)), (2x256Mb)
 - 500Mbps available soon !
- MIPI-CSI/DSI up to 2.5Gbps support.
 - x8 MIPI
 - x4 MIPI
- LVDS support up to 2.5Gbps
- DDR3 memory support up to 1333Mbps
- Samples expected end of the year !
- VCC: 0.95/0.85V



Titanium Serdes - Ti375 Highlight

Quantum™ compute fabric

- TSMC 16nm process
- High performance, Low power fabric
- 0.95V and 0.85V (LP mode) support
- High DSP compute capability
- High Embedded Memory resource

3300-LPDDR4/x Hard IP

- x32-bit LPDDR4/4x @ 3300Mbps
- LPDDR4x reduce I/O voltage by 50% for both memory & controller (1.1V to 0.6V)
- Harden DDR PHY and Controller IP, optimum performance and power

Security

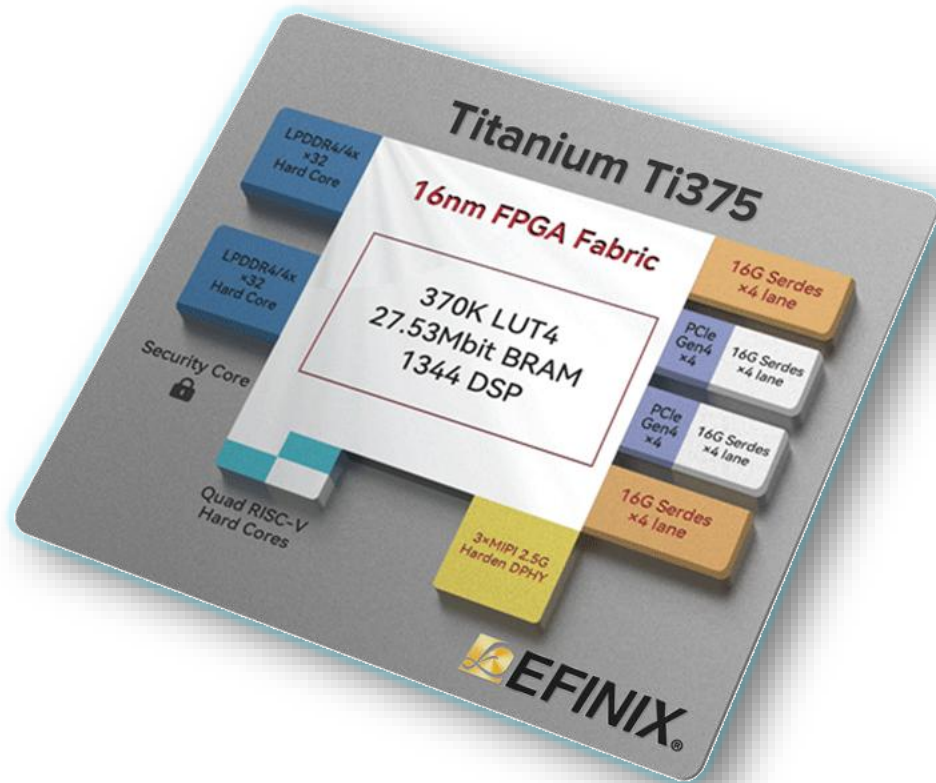
- AES-GCM Bitstream Encryption
- AES-GCM Symmetric Authentication
- RSA-4096 Asymmetric Authentication

Qualification

- AEC-Q100*

Quad Core Risc-V RV32 SoC

- Quad Core RV32-IMACFD
- MMU, FPU, Custom Instruction support



Quad 16Gbps High Speed Serdes

- Support x1, x2 and x4 configurations
- Support PCIe 4.0, 10G-KR, SGMII, PHY-only mode

PCIe Gen4x4 Controller Hard IP

- Compliant with PCIe 4.0, 3.2, 2.1, and 1.1 Spec
- Support x1, x2 and x4 configurations
- Configure as Root Port (RP), or End Point (EP)
- Single Root IO Virtualization (SRIOV)

2.5Gbps MIPI-DPHY Hard IP

- 3 MIPI-DPHY 2.5Gbps x4 lanes Hard IP instances (RX & TX)
- CSI-2, DSI soft IP

High Voltage IO

- 3.3V, 2.5V, 1.8V capable

High Speed IO

- LVDS 1.5Gbps
- MIPI-DPHY 1.5Gbps



Titanium Serdes – Ti135 Highlight

Quantum™ compute fabric

- TSMC 16nm process
- High performance, Low power fabric
- 0.95V and 0.85V (LP mode) support
- High DSP compute capability
- High Embedded Memory resource

3300-LPDDR4/x Hard IP

- x32-bit LPDDR4/4x @ 3300Mbps
- LPDDR4x reduce I/O voltage by 50% for both memory & controller (1.1V to 0.6V)
- Harden DDR PHY and Controller IP, optimum performance and power

Security

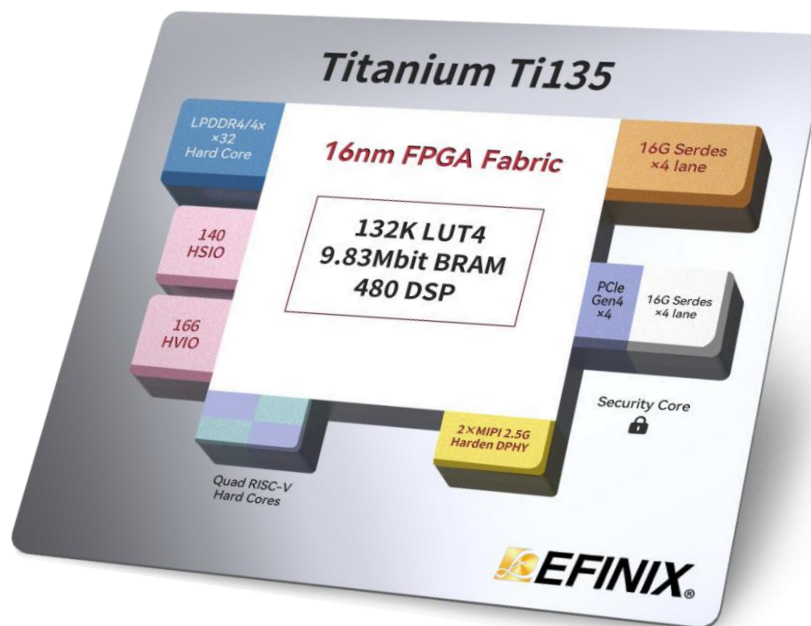
- AES-GCM Bitstream Encryption
- AES-GCM Symmetric Authentication
- RSA-4096 Asymmetric Authentication

Qualification

- AEC-Q100*

Quad Core Risc-V RV32 SoC

- Quad Core RV32-IMACFD
- MMU, FPU, Custom Instruction support



Quad 16Gbps High Speed Serdes

- Support x1, x2 and x4 configurations
- Support PCIe 4.0, 10G-KR, SGMII, PHY-only mode

PCIe Gen4x4 Controller Hard IP

- Compliant with PCIe 4.0, 3.2, 2.1, and 1.1 Spec
- Support x1, x2 and x4 configurations
- Configure as Root Port (RP), or End Point (EP)
- Single Root IO Virtualization (SRIOV)

2.5Gbps MIPI-DPHY Hard IP

- 2 MIPI-DPHY 2.5Gbps x4 lanes Hard IP instances (RX & TX)
- CSI-2, DSI soft IP

High Voltage IO

- 3.3V, 2.5V, 1.8V capable

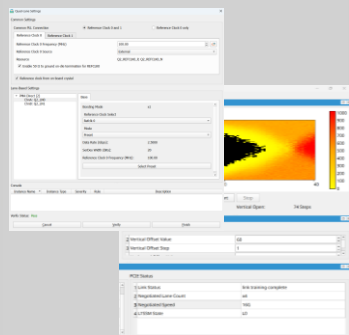
High Speed IO

- LVDS 1.5Gbps
- MIPI-DPHY 1.5Gbps



Transceiver Ecosystem

Efinity Support



Flexi rate, Mix Mode,
Multi-protocol Support

PCIE



PCIE EP Gen1/2/3/4

Ready!

1/2.5/5/10GE



Intel PHY
Realtek PHY
Marvel PHY

Ready!

SLVS-EC



Sony SLVS-EC
Gen1/2

Ready!

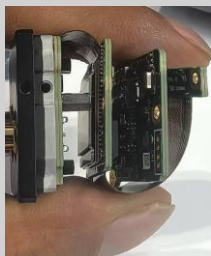
SDI



HD/3G-SDI
UHD/6G/12G-SDI

Ready!

CoaXPress



1.25/2.5/3.125/5/6.25
/10/12.5Gbps CXP

Ready!

JESD204B



JESD204B TX/RX
With TI ADC/DAC

Ready!

Aurora



Aurora 8b10b, 64b66b
With Xilinx Kintex7,
Virtex7 boards

Ready!

HDMI



HDMI 1.4/2.0 -> 4K60
HDMI 2.1 -> 8K60/4K120

Q3/25

Display Port



DP1.3 -> 4K60
DP1.4 -> 8K60/4K120

Q4/25



Continue Innovation

Sapphire SoC

- Soft Processor (Performance)
- RV32 with IMAFDC extension
- 100-400Mhz System Clock
- Quad Core
- Multi-way Instruction and Data Cache
- MMU, Linux Capable
- Hardware FPU
- Custom Instruction

Sapphire Lite

- Soft Processor (Area)
- RV32 with IM extension
- 100-200Mhz System Clock
- Single Core
- Instruction and Data Cache
- 4KLE resource consumption

Sapphire High Performance

Ti375, Ti240,
Ti165, Ti135, Ti85

- Hard Processor (High Performance)
- RV32 with IMAFDC extension
- >1GHz System Clock
- Quad Core
- Multi-way Instruction and Data Cache
- MMU, Linux Capable
- Hardware FPU
- Custom Instruction
- ~500mW CPU Hard IP power

Same Embedded Software Development, IDE, Tool Chain, Driver



Risc-V IDE



Debugger



Linux OS



RTOS



Zephyr OS

Ethernet
Linux/FreeRTOS
Solution Stack

SD Card Storage
Solution Stack

and more..

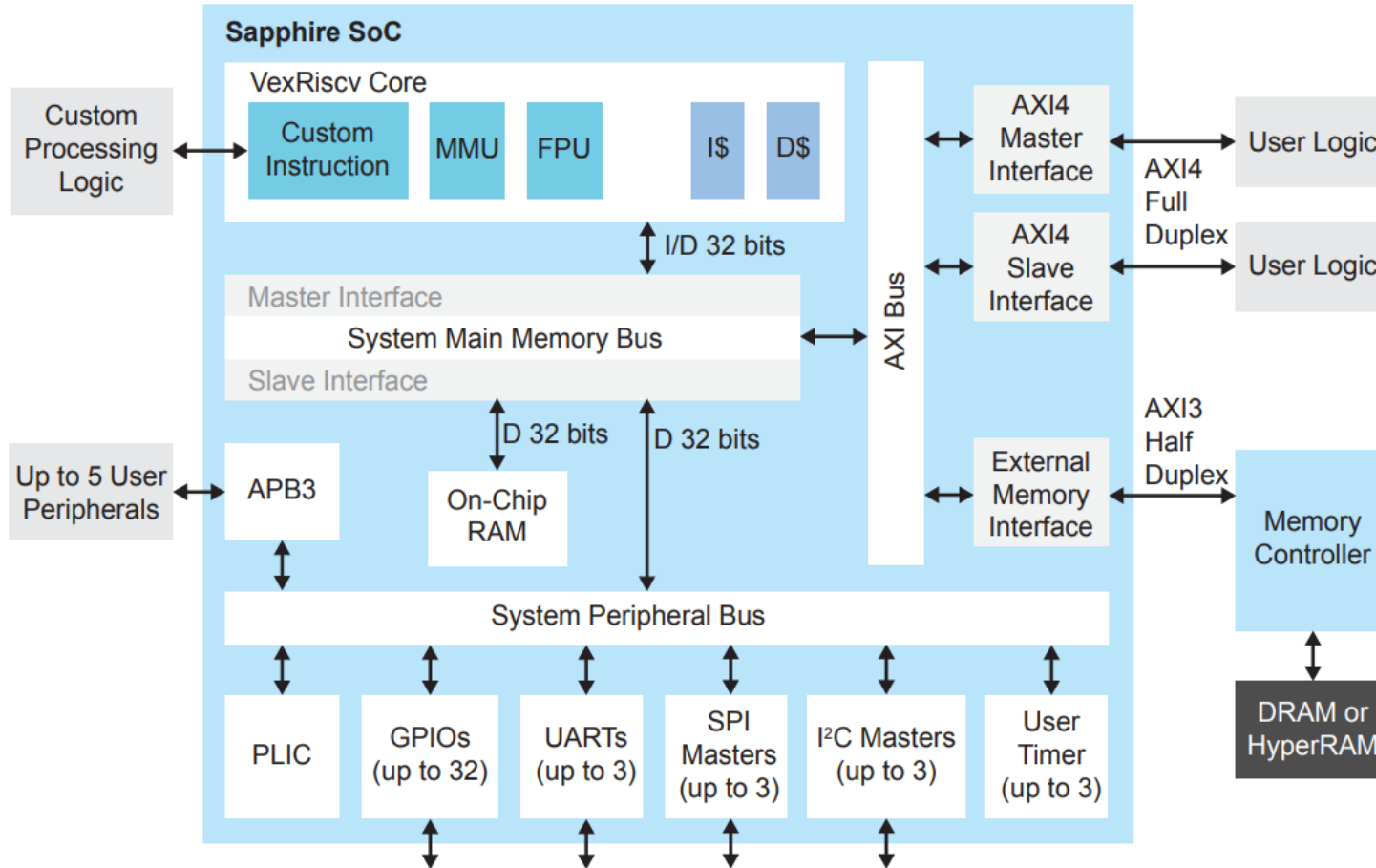
Comparison Hard VS Soft Sapphire

Hard Sapphire

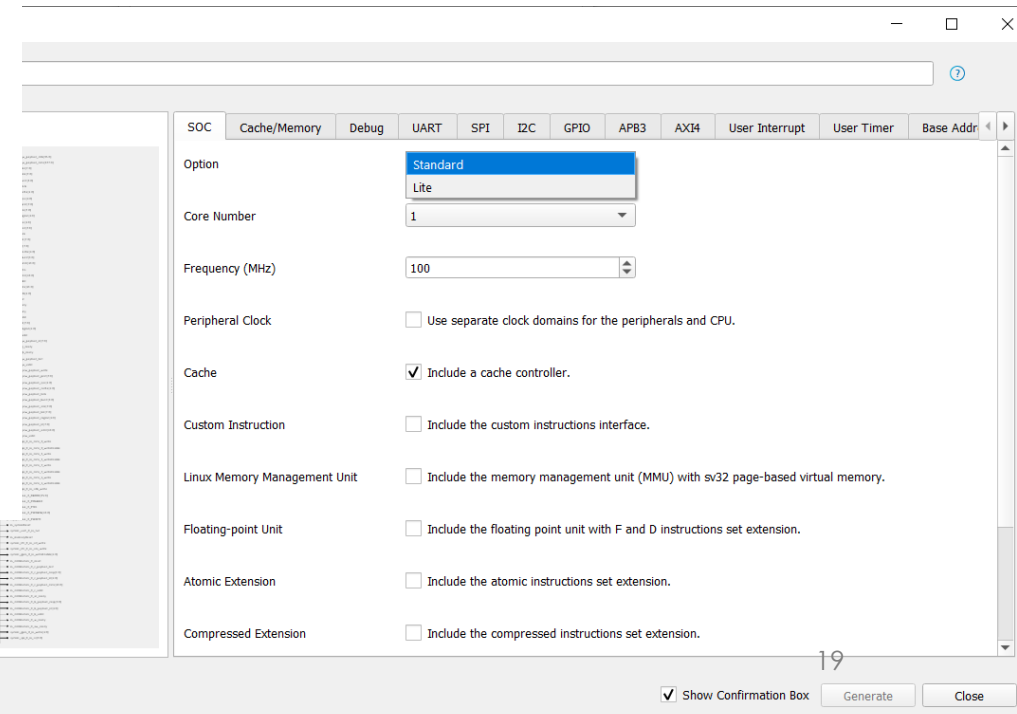
- 128-bit internal bus
- Improves data path latency between CPU and periphery
- Static branch predictor
- Unblocked operation for custom instruction
- Dedicated FPU for each core
- 8 Hardware breakpoints for debug module
- Data coherency between CPU and DMA channel (AXI Master)
- Additional write buffer to improve write performance to external memory

Soft Sapphire

- Max 64-bit internal bus
- Higher latency due to pipelining, trade-off for fmax
- No branch predictor
- Stall CPU pipeline until get the result from custom ALU
- Shared FPU for multi-core configuration
- Up to 4 hardware breakpoints
- No data coherency between CPU and DMA channel (AXI master)
- No write buffer introduced in SoC

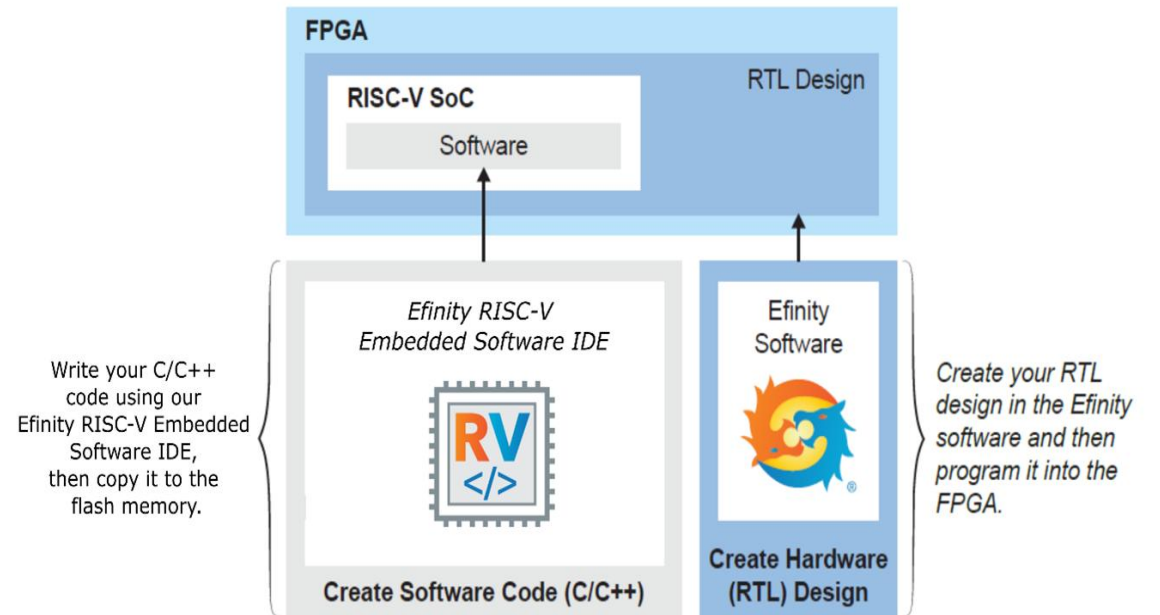


- New:
 - LINUX MMU
 - FPU
 - Custom Instructions



Required Software and Tools

- Efinity® software
- Pre-compiled, open-source SDK
- Eclipse IDE for managing projects and software with Ashling GUI
- RISC-V GCC compiler and GDB debugger
- OpenOCD debugger for debugging applications
 - Lauterbach Tracer support
- Windows build tools (Windows)
- Available from our web page
 - <https://www.efinixinc.com/products-riscv.html>





Soft IPs/SOC available in IP catalog

Additional examples e.g how to infer the different Memories like DP-RAM you can find under the support knowledgebase

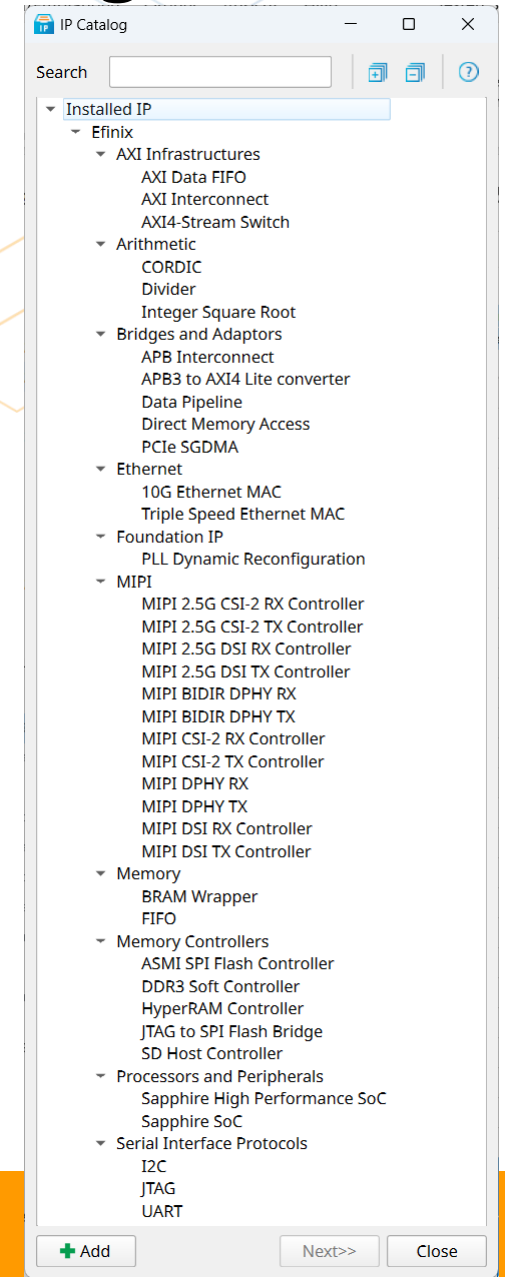
<https://www.efinixinc.com/support/kb/index.php>

Filter IP cores are available in Beta (FFT, FIR)

Open Source:

e.g.: <https://github.com/open-logic/open-logic>

I2C, SPI, AXI





Partner IP Cores : High Speed

- SLVS-EC available (Beta status), partner CIS, available from Efinix
- SDI 3/6 available (beta), partner CIS, available from Efinix
- SDI 12 in progress partner CIS, available from Efinix
- JESD204B available, partner Logic Fruit
- DP partner Logic Fruit
- HDMI partner Bitec
- Aurora partner ALSE
- CXP providing PMA settings, core in discussion
- Vx1 wrapper
- GigE-Vision/10GigE-Vision Imavix
- 40GE (4x10GE) Imavix



Free of charge Software Features



Projects

Project management to keep your design files organized



Dashboard

Easy-to-use dashboard to run the tool flow automatically or manually



Language Support

Verilog HDL, SystemVerilog, and VHDL



Interface Designer

Constrain logic and assign pins to blocks in the device periphery



IP Manager

Configure and add building blocks to your project



Floorplan Viewer

Browse through your design's logic and routing placement



Netlist Viewer

Displays and analyzes your design's netlist



Timing Browser

Browse timing and perform static timing analysis



Simulation

Supports simulation flows using the ModelSim, NCSim, Aldec, or free iVerilog simulators



BRAM Initial Content Updater

Update initial BRAM without performing a full compile



Python API

Use scripts to build your design's interface



Package Planner

Assign logic to package pins and view the pinout graphically



Hardware Debugger

Integrated hardware Debugger with Logic Analyzer and Virtual I/O debug cores



Programmer

GUI and command-line Programmer to configure your FPGA



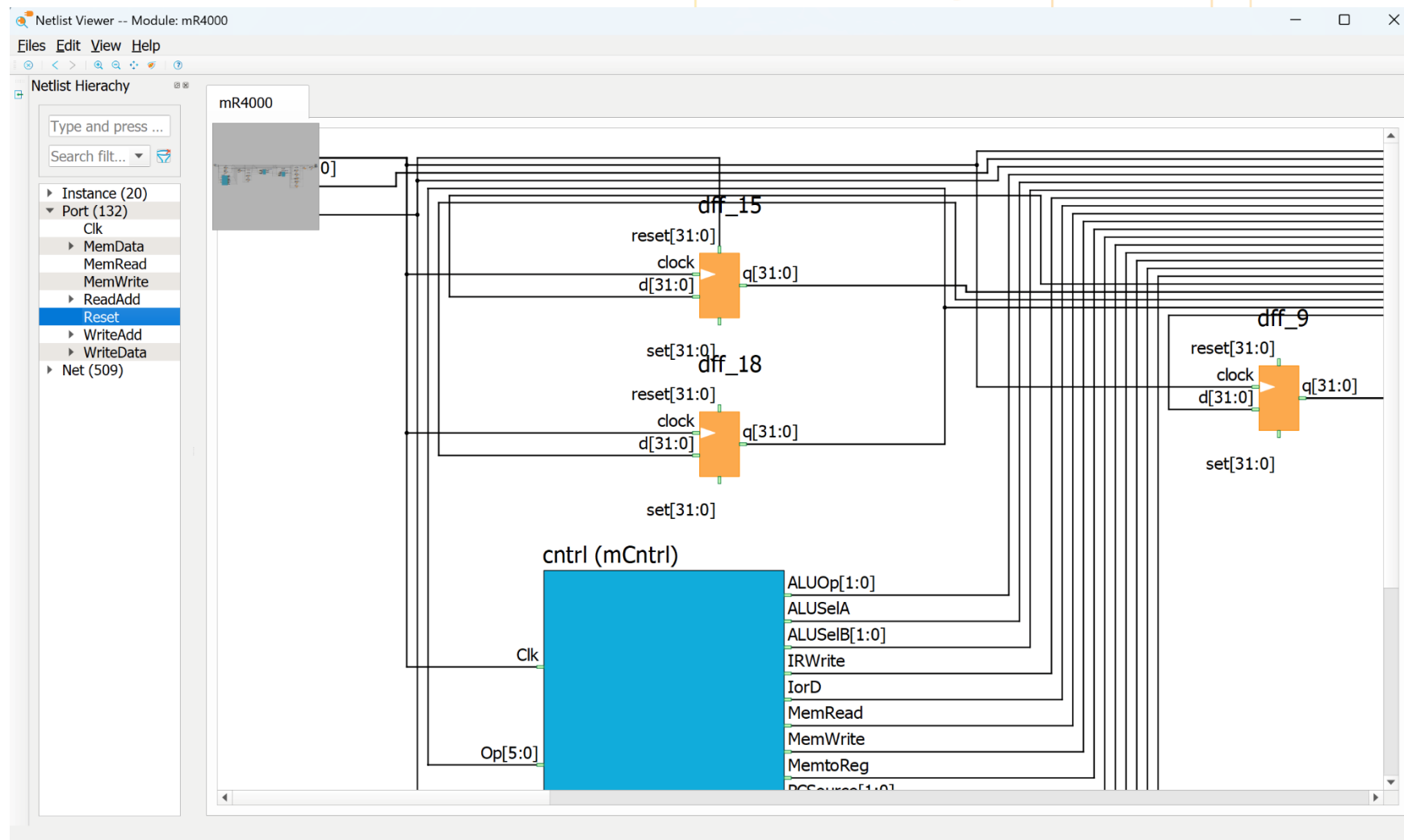
JTAG SVF Player

Sends JTAG command to an FPGA



Bitstream Authentication and Encryption

Sign and/or encrypt bitstreams



Floorplan Viewer



Floorplan

Cell Browser

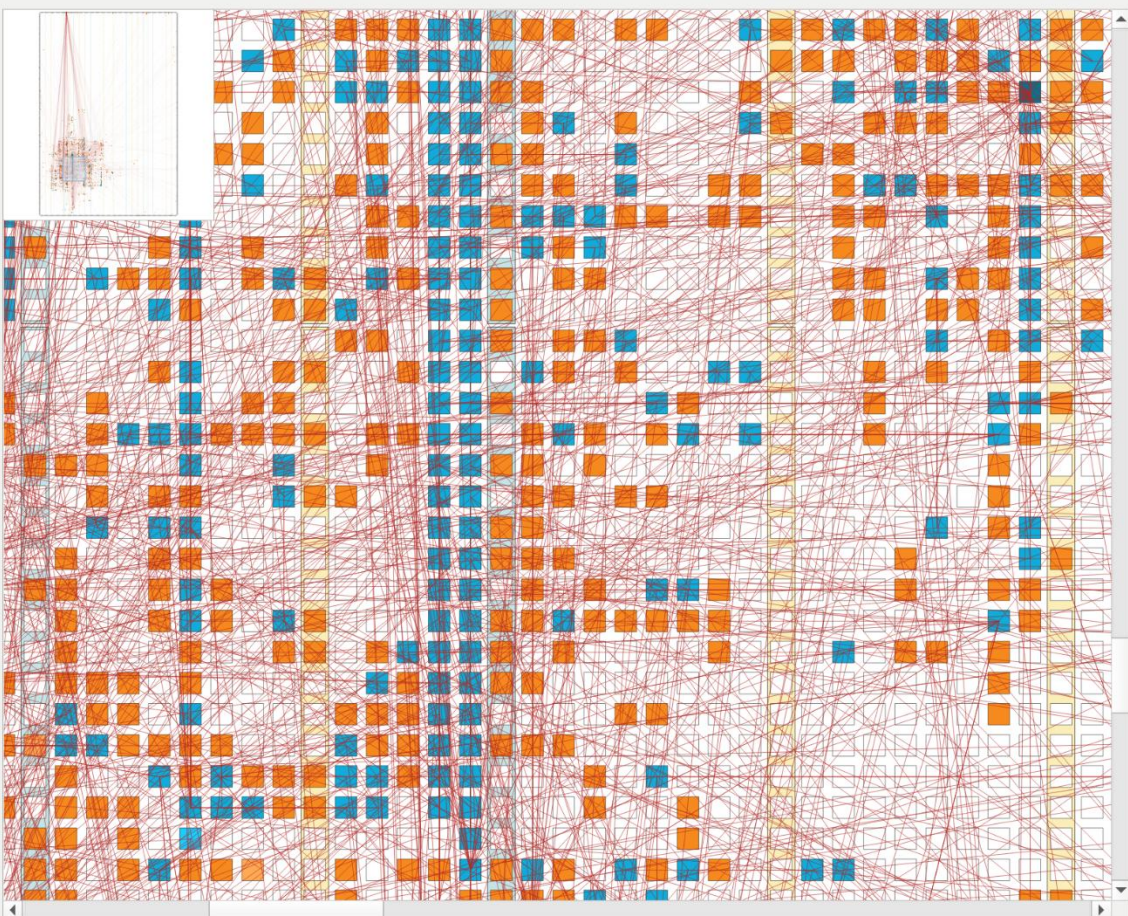
Type regex to filter... ☐ Regex

▼ Leaf Cells

- (37,70) ALUOp[0]~FF
- (32,62) ALUOp[1]~FF
- (37,61) ALUSelA~FF
- (32,67) ALUSelB[0]~FF
- (53,65) AUX_ADD_CI_alu/...
- (219,165) Clk
- (101,145) GND
- (71,89) Instruction[0]~FF**
- (82,47) Instruction[10]~FF
- (82,58) Instruction[11]~FF
- (19,61) Instruction[12]~FF
- (82,75) Instruction[13]~FF
- (68,119) Instruction[14]~FF
- (71,84) Instruction[15]~FF
- (31,114) Instruction[16]~FF
- (31,118) Instruction[17]~FF
- (71,105) Instruction[18]~FF
- (101,95) Instruction[19]~FF
- (37,60) Instruction[1]~FF

Inspector

Property	Value
1 Coordinate	(71, 89)
2 Name	Instruction[0]~FF
3 Type	eft
4 Route ...	2



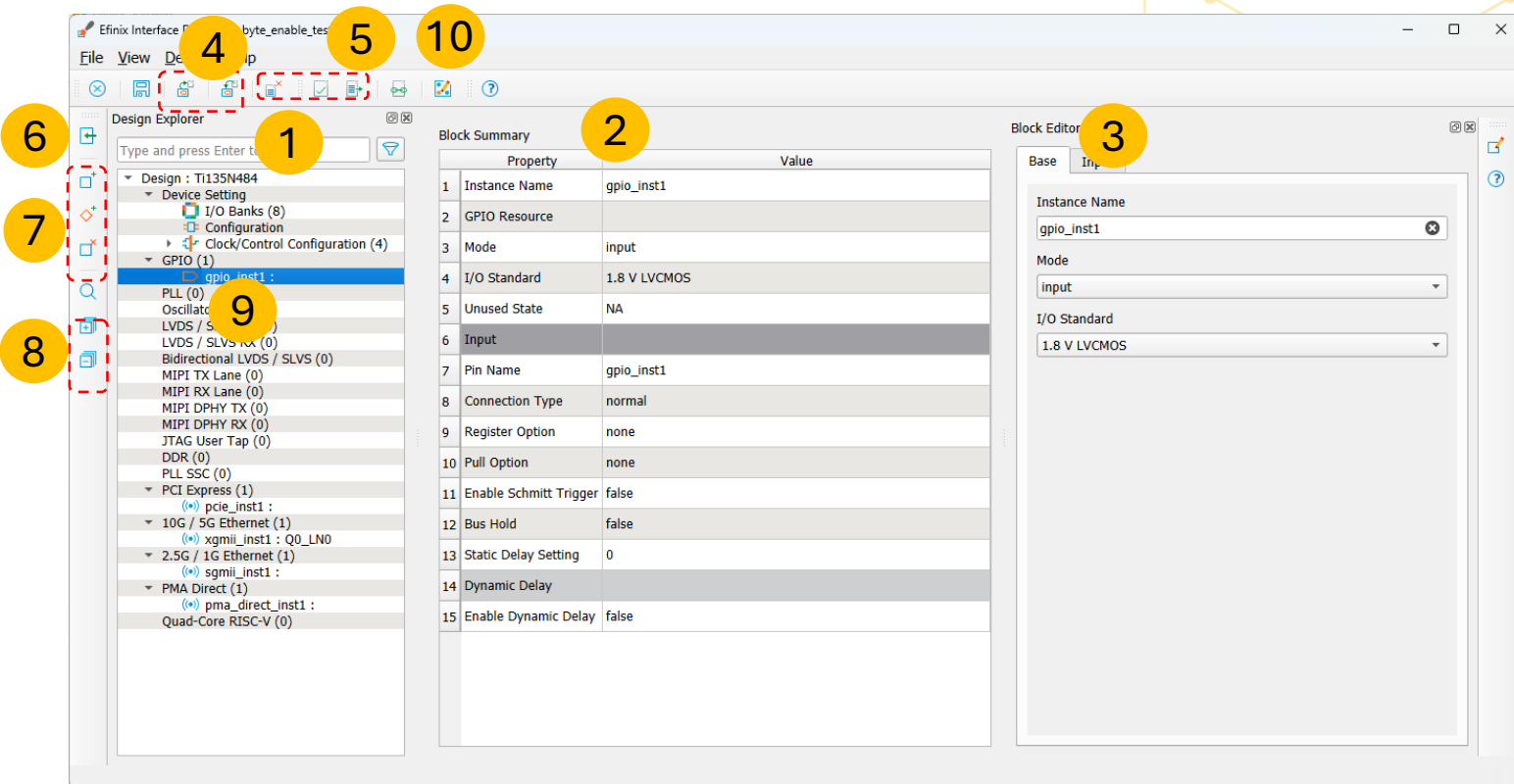
Type to search... Block: (71,89) type=eft routethru=2 name=Instruction[0]~FF

Legend

Filter

- ☒ Always Apply
- ☐ Block Name
- ☒ Block Type
- ☒ Routing
- ☒ Carry Chain

Interface Designer



1. The Design Explorer shows the interfaces in your Design
2. Block Summary shows settings for the selected Block
3. Block Editor add or change settings
4. Import/Export GPIO assignments
5. Project Management Tools for design check
6. Show/Hide Resource Assigner
7. Block Tools add/delete blocks
8. Expand/Collaps Design Explorer folder
9. Number of used blocks()
10. Package Planner



SERDES access: PCI-E

Efinix Interface Designer - byte_enable_test

File View Design Help

Design Explorer

Type and press Enter to search...

Design : T1135N484

- Device Setting
 - I/O Banks (8)
 - Configuration
 - Clock/Control Configuration (4)
 - GPIO (0)
 - PLL (0)
 - Oscillator (0)
 - LVDS / SLVS TX (0)
 - LVDS / SLVS RX (0)
 - Bidirectional LVDS / SLVS (0)
 - MIPI TX Lane (0)
 - MIPI RX Lane (0)
 - MIPI DPHY TX (0)
 - MIPI DPHY RX (0)
 - JTAG User Tap (0)
 - DDR (0)
 - PLL SSC (0)
 - PCI Express (1)
 - pcie_inst1 :
 - 10G / 5G Ethernet (1)
 - xgmii_inst1 :
 - 2.5G / 1G Ethernet (1)
 - sgmii_inst1 :
 - PMA Direct (1)
 - pma_direct_inst1 :
 - Quad-Core RISC-V (0)

Block Summary

Property	Value
1 Instance Name	pcie_inst1
2 PCIe Resource	
3 Base	
4 Generation	Gen3 (8.0 Gbps)
5 Link Width	x4
6 Maximum Payload Size	512 bytes
7 Mode	Endpoint
8 SRIS Enable	false
9 Reference Clock	
10 Reference Clock Frequency	100.000
11 Reference Clock Source	External
12 External Reference Clock	CMN_REFCLK0
13 Enable 50 Ω to ground on-die termination for REFCLK0	true
14 Reference clock from on-board crystal	true
15 Function	
16 Subsystem Vendor ID	0x1f7a
17 Total Physical Functions	4
18 Vendor ID	0x1f7a
19 Physical Function 0	
20 BAR0 Aperture	4 KB
21 BAR0 Control	32 bit non-prefetchable mem
22 BAR1 Control	Disabled
23 BAR2 Control	Disabled
24 BAR3 Control	Disabled

Block Editor

Base Reset Function Device Capability Pins

Instance Name

pcie_inst1

PCIe Resource

None

Mode

Endpoint

Link Width

x4

Generation

Gen3 (8.0 Gbps)

Maximum Payload Size

512 bytes

SRIS Enable

Reference Clock

Reference Clock Frequency

100,000

Reference Clock Source

External

External Clock

Clock

CMN_REFCLK0

Resource : Unknown

Enable 50 Ω to ground on-die termination for REFCLK0

Reference clock from on-board crystal

PCI Express Reset

Resource : Unknown

Instance : Unknown

Hot Reset Output Pin Name

pcie_inst1_HOT_RESET_OUT

Link Down Reset Pin Name

pcie_inst1_LINK_DOWN_RESET_OUT

Reset Acknowledge Pin Name

pcie_inst1_RESET_ACK

Reset Request Pin Name

pcie_inst1_RESET_REQ

Subsystem Vendor ID

0x1f7a

Vendor ID

0x1f7a

Total Physical Functions

4

Physical Function 0

Physical Function 1

BAR0 Aperture

4 KB

BAR0 Control

32 bit non-prefetchable memory

BAR1 Aperture

4 KB

BAR1 Control

Disabled

BAR2 Aperture

4 KB

BAR2 Control

Disabled

BAR3 Aperture

AXI

Interrupt

Message

Error Indication

APB

Function Level Reset

Status

Configuration Snoop

Enable AXI Master Interface

Enable AXI Slave Interface

AXI Clock Pin Name

Invert AXI Clock Pin

AXI Reset (Active-Low) Pin Name

pcie_inst1_USER_AXI_RESET_N

Master

Slave

Read Address Channel

Write Address Channel

Write Response Channel

Read Data Channel

Write Data Channel

Address ID [7:0] Bus Name

pcie_inst1_TARGET_AXI_ARID

Address Ready Pin Name

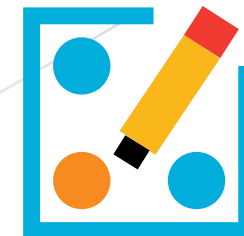
pcie_inst1_TARGET_AXI_ARREADY

Address Valid Pin Name

pcie_inst1_TARGET_AXI_ARVALID

Burst Length [7:0] Bus Name

pcie_inst1_TARGET_AXI_ARLEN



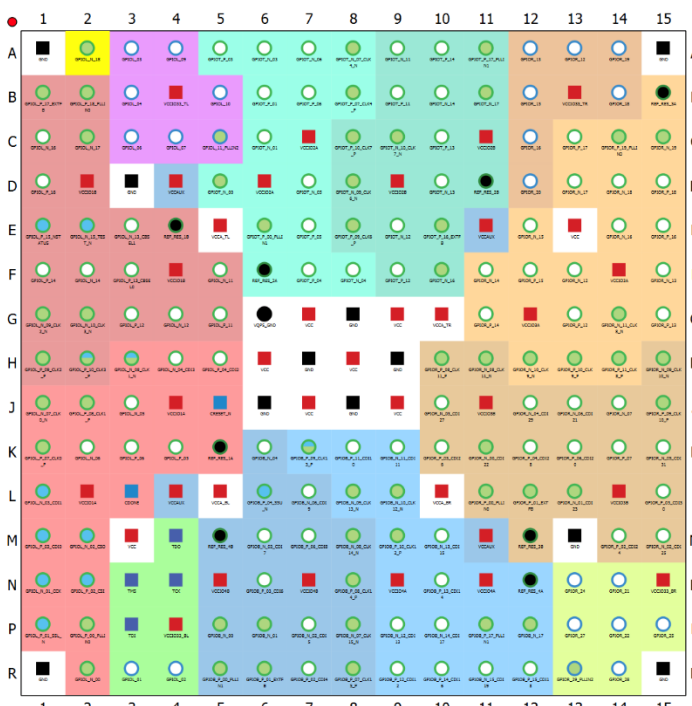
Package Planner - r4000

File View Help

Package View

225-ball FBGA Pinout Diagram

Top View Device Name: Ti60F225



View Configuration

Report Pin information

Pin Number: A2

Pin Name: GPIO_N_18

Pin Type: HSIO or Multi-Function

Signal Name: N/A

Direction: N/A

I/O Bank: 1B

I/O Bank Voltage: 1.8 V

I/O Standard: N/A

Pull Type: N/A

Block Type: HSIO

Block Instance: N/A

Resource Name: GPIO_PN_18, GPIO_N_18

MIPI Rx Group: I2

Function: User IO/ PLL_CLKIN



Hardware Debugger



efinity Debugger - unsaved profile

File Options Perspectives Help

Program

Configuration

USB Target: Titanium Ti60F225 Development Kit

USB Info: ID: 0403:6011

Bitstream: ning_for_new_customer/Tutorial_larger/outflow/Tutorial_larger.bit Ti60F225

Device Status: Last Updated: Thu Jun 13 24 16:07:18

Debugging: 0x10660a79 USER1

Core Status

Idle Waiting for Trigger Post-Trigger Full

Capture Status

Segment 0 of 1 Segment sample 0 of 1024 Total sample 0 of 1024

0% 0% 0%

Waveform Path: g\Flow_Training_for_new_customer\Tutorial_larger\la0_waveform.vcd Overwrite

Trigger Setup Capture Setup

Trigger Mode: Basic Only

Trigger Condition: Global 'AND'

Name	Operator	Radix	Value	Port
counter_ins...	==	Bin	XXXXXXXXXXXXXXXXXXXXXXXXXXXX0000000	probe0[31:0]

Console

GTKWave - C:\Users\HaraldWerner\OneDrive - Efinix Inc\EFINIX-EMEA\Training\Flow_Training_for_new_customer\Tutorial_larger\...\HARALD-T\AppData\Local\Temp\tmp1v1ajnh\tmp_continuous.vcd

File Edit Search Time Markers View Help

From: 0 sec To: 1023 ns Marker: 2 ns Cursor: 2 ns

Signals

```
stopn=1
resetsn=1
counter_inst/cnt[31:0]=8CC4AA02
counter_inst/cnt[31]=1
counter_inst/cnt[30]=0
counter_inst/cnt[29]=0
counter_inst/cnt[28]=0
counter_inst/cnt[27]=1
counter_inst/cnt[26]=1
counter_inst/cnt[25]=0
counter_inst/cnt[24]=0
counter_inst/cnt[23]=1
counter_inst/cnt[22]=1
counter_inst/cnt[21]=0
counter_inst/cnt[20]=0
counter_inst/cnt[19]=0
counter_inst/cnt[18]=1
counter_inst/cnt[17]=0
counter_inst/cnt[16]=0
counter_inst/cnt[15]=1
counter_inst/cnt[14]=0
counter_inst/cnt[13]=1
counter_inst/cnt[12]=0
counter_inst/cnt[11]=1
counter_inst/cnt[10]=0
counter_inst/cnt[9]=1
counter_inst/cnt[8]=0
counter_inst/cnt[7]=0
counter_inst/cnt[6]=0
```

Waves

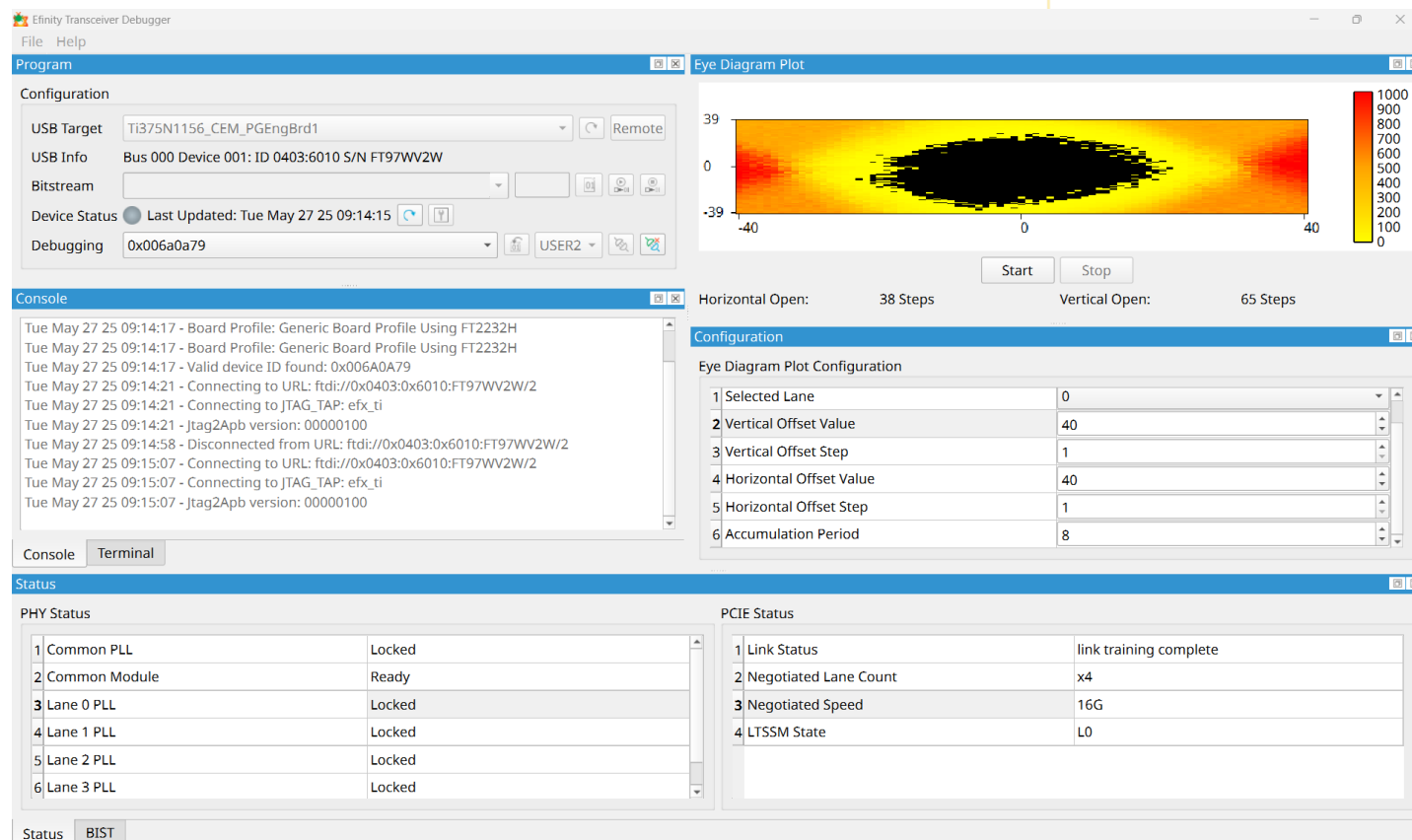
1 ns 2 ns 3 ns 4 ns 5 ns

8CC4AA00 8CC4AA01 8CC4AA02 8CC4AA03 8CC4AA04 8CC4AA05

September 2025



Serdes Debugger



➤ Eyesurf

➤ Build in Self Test(BIST)

➤ Internal Parallel Loopback

➤ Internal Serial Loopback

➤ External Serial Loopback

➤ Internal Register Read-write via APB



- Minimum requirements
 - Computer with a 64 bit operating system, dual-core processor, and 8 GB RAM
- Linux environments
 - Operating system: Ubuntu x86-64 v20.04 or later, Red Hat Enterprise x86-64 v8.8 or later
 - Linux X11 or Wayland windowing system (for Efinity® GUI)
 - Udev device manager for Efinix USB programming cable
 - Open-source Java 64-bit runtime environment (8 or higher); required for configuring the Sapphire RISC-V SoC in the IP Manager; available from: <https://developers.redhat.com/products/openjdk/download> (OpenJDK 8 or 11) – <http://jdk.java.net/16/> (OpenJDK 16)
- Windows environments
 - Windows 10 or later, 64 bit
 - Microsoft Visual C++ 2022 x64 runtime library (or latest version)
 - Open-source Java 64-bit runtime environment; required for configuring the Sapphire RISC-V SoC in the IP Manager; available from: – <https://www.java.com/en/download/manual.jsp> (Java 8)
- GTKwave 3.3.117 (GTKwave 3.3.100 for Windows)

Product	Model	Memory
Trion	T4, T8, T13, T20, T35	8 GB
	T55, T85, T120	12 GB
Titanium	Ti35, Ti60, Ti85, Ti90, Ti120, Ti135, Ti180	8 GB
	Ti165, Ti240, Ti375	12 GB
Topaz	Tz50, Tz75, Tz100, Tz110, Tz170	8 GB
	Tz200, Tz325	12 GB

Programming Hardware

Recommended hardware

- FT2232H Mini Module
- FT4232H Mini Module

(C232HM-DDHSL-0 FTDI cable still in use but no longer recommended)

Mini Modules are a bit more robust because of their VCC/GND plane. (noise)

Mini Modules and C232HM are for 3.3V JTAG interface only.

Other voltages are supported with EFINIX Download Cable II, designed by Centron, available e.g. at Digikey

