Efinix Technology and Future Outlook

Fabian Kluge

A Silicon Valley Company with International Footprint

- Founded : 2012
- HQ in Cupertino, California, U.S.A.
- 200+ Employees Worldwide

Leaderships

Ming Ng
COO & Sr. VP Service
30+ Years of Experience

LSI LOGIC · Microsemi · PMC-Sierra · Supertex inc. · TelCom Semiconductor Inc. · ZARLINK SEMICONDUCTOR

Mark Oliver
VP, Americas Marketing & BD
35+ Years of Experience

halo · HEWLETT PACKARD · MARVELL · XILINX · PANASAS

FOUNDER

Sammy Cheung
President & CEO
30+ Years of Experience

ALTERA · CYPRESS EMBEDDED IN TOMORROW

FOUNDER

Tony Ngai
CTO & Sr. VP Engineering
35+ Years of Experience

ALTERA · AT&T · IBM · LATTICE SEMICONDUCTOR · XILINX

Jay Schleicher
SVP, Software Engineering
30+ Years of Experience

ALTERA

Ikuo Nakanishi
VP, JAPI Sales & Biz Dev.
25+ Years of Experience

QuickLogic · XILINX

Harald Werner
VP & MD, EMEA Business
35+ Years of Experience

Actel · LATTICE SEMICONDUCTOR · VIEWlogic · SIEMENS

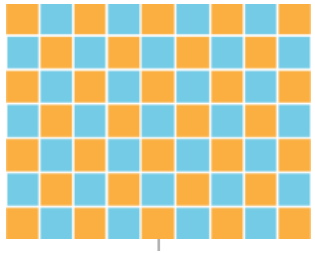
Jing Kuo
VP & GM, China Business 25+ Years of Experience

ALTERA

Ching Lun Yan
VP, Intelligent Solutions
15+ Years of Experience

ALTERA

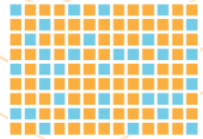
Patented FPGA Architecture



TRADITIONAL FPGAS

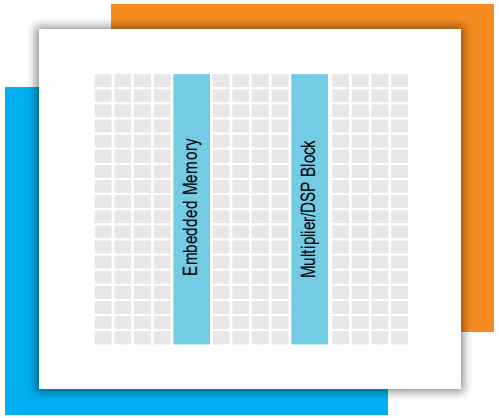
Fixed Ratio — *vs* — Exchangeable Logic & Routing

EFINIX® QUANTUM™

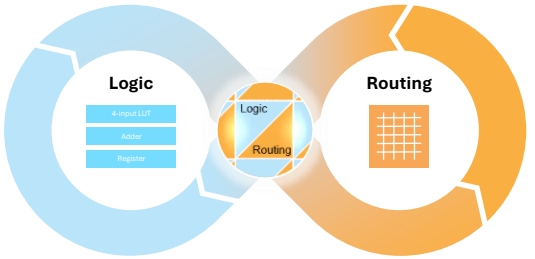


Fixed

LOGIC *vs* ROUTING



Flexible



Inefficient
Too much logic, no routing to connect

Expensive
Too much routing, wasted silicon area

Smaller Sizes & Lower Power
Logic & function in one XLR block simplifies size & complexity

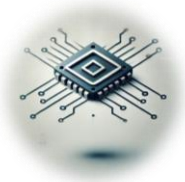
High Performance & Scalable
Flexible XLR cells programmed based on specific design

Unique Differentiation

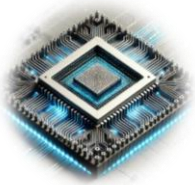
Advantages

Higher Performance

Lower Power



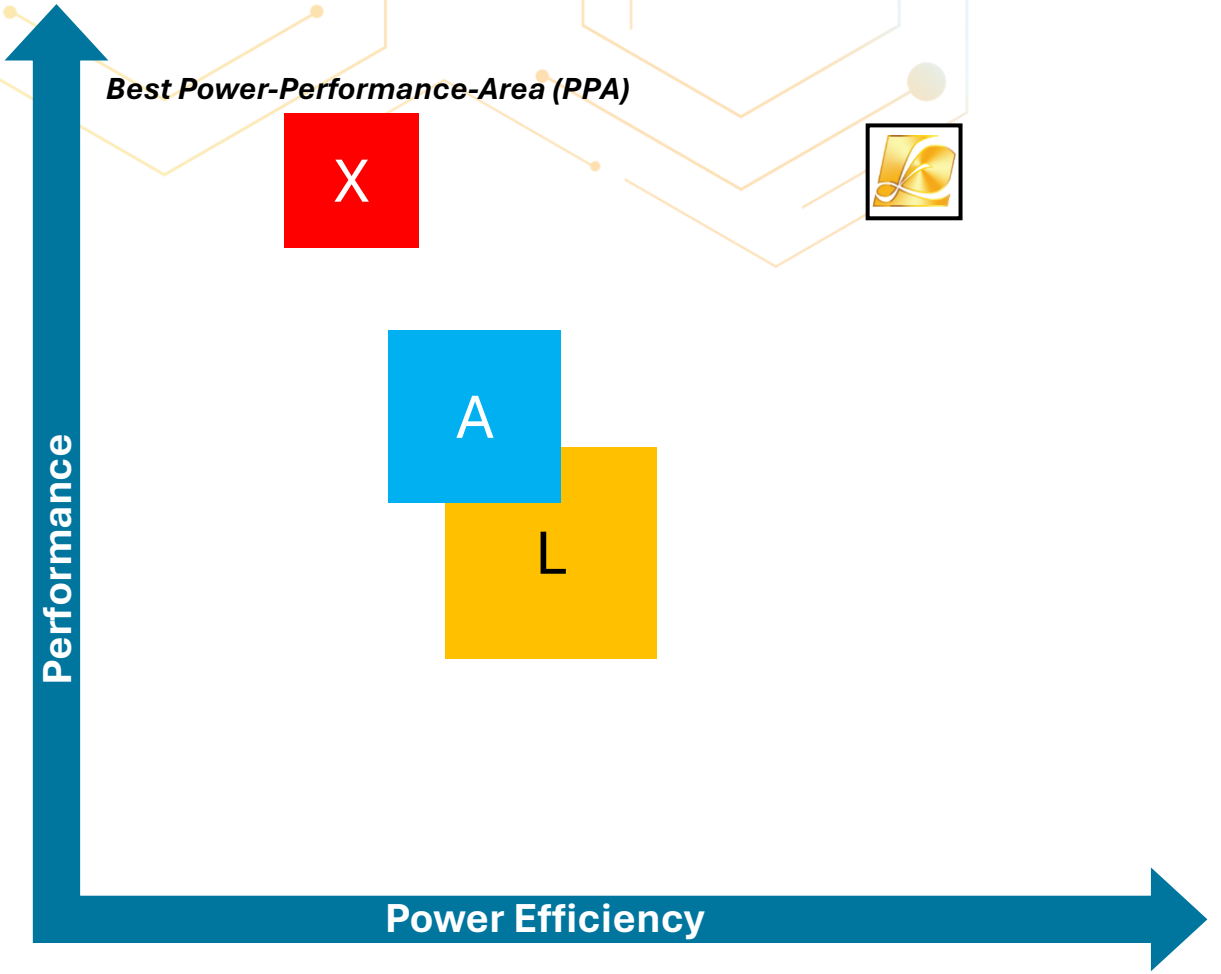
Smaller Footprint



Scalable to High Density

Competitive Price

Lowest Development Cost



A Complete Product Portfolio

General FPGA

IO Rich, Wide Range Selection, MIPI DPHY CSI, DDR

Value for Mainstream Markets

Performance, Low Power,12Gbps SerDes, LPDDR4 & MIPI DPHY 2Gbps

High Performance & Low Power

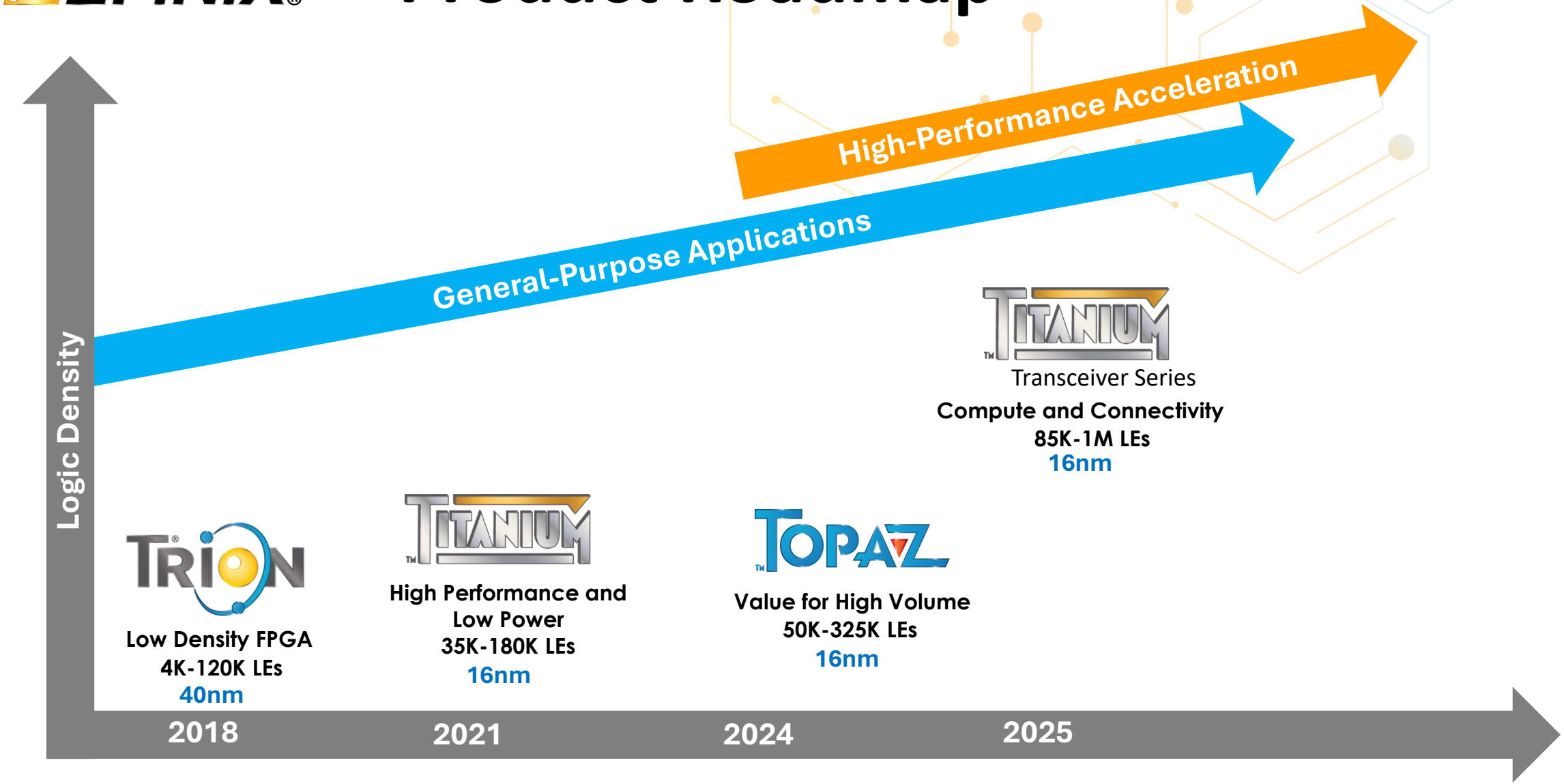
Low Power, Size, 3.3Gbps LPDDR4/4x & MIPI DPHY 2.5Gbps

Ultimate Compute & Connectivity

Serdes Series

16/25Gbps Multi-Protocol SerDes, PCIE Gen4 Controller, Quad Core RISC-V CPU

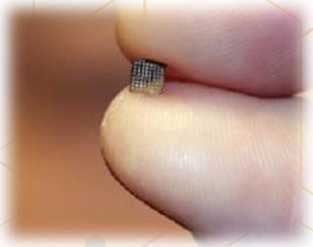
Product Roadmap



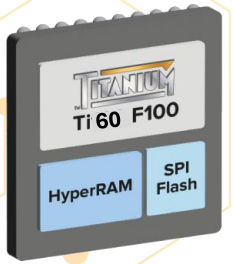
Small form factor

Low power advantage enable Efinix lead in small form factor offering!

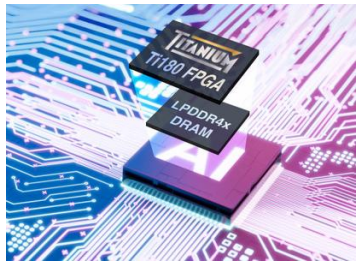
Ti60W64
3.5x3.4mm
0.5mm ball pitch
WLCSP package



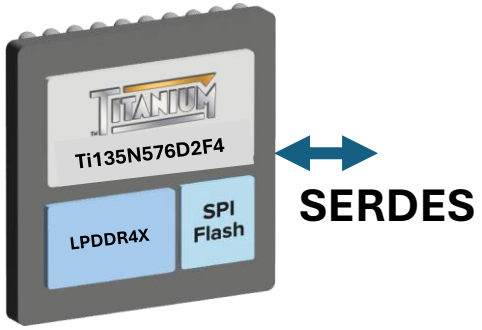
Ti60F100S3F2
5.5x5.5mm
0.5mm ball pitch
SIP 256Mb HyperRAM
+ 16Mb Flash



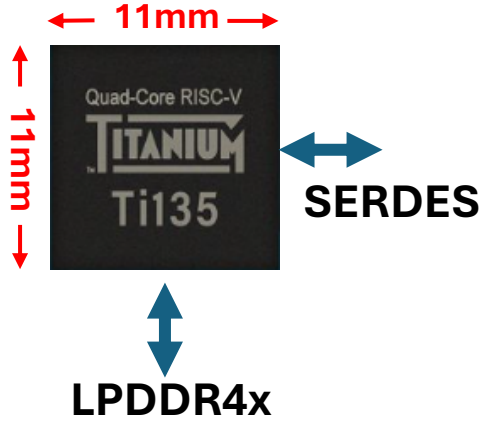
Ti180J484D1
15x15mm
0.65mm ball pitch
SIP 2Gb LPDDR4x
3000Mbps



Ti135N567D2F4
16x16 mm
0.65mm ball pitch
8x 16 Gbps Serdes
PCIE Gen4
SIP 2Gb LPDDR4X
@3Gbps



Ti135N441
11x11mm
0.5mm ball pitch
8x 12.5Gbps Serdes
PCIE Gen3



Titanium Family Table

	Ti35	Ti60	Ti80**	Ti85	Ti90	Ti120	Ti125**	Ti135	Ti165	Ti180	Ti240	Ti375	Ti550	Ti750	Ti1000
LE (k)	36	62	79	83	92	123	123	134	162	176	237	370	550	750	1000
10K RAM (Mb)	1,53	2,62	3,70	6,18	7,34	9,80	5,90	9,95	12,10	13,11	19,37	27,53	39,65	55,80	74,40
DSP	93	160	288	300	359	478	288	486	590	640	946	1344	1936	2736	3648
PLLs	4	4	7	12	10	10	7	12	12	10	12	12	12	12	12
HVIO	34	34	35	133	80	80	35	133	181	80	181	181	200	200	200
HSIO	146	146	200	139	232	232	200	139	235	232	235	235	320	320	320
MIPI DPHY 1.5G, support CSI-2/DSI	Yes	Yes	-	Yes	Yes	Yes	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MIPI HSIO 2.5G, support CSI-2/DSI	-	-	Yes	-	-	-	Yes	-	-	-	-	-	Yes	Yes	Yes
MIPI DPHY x4 2.5Gbps Hard IP	-	-	-	X2	X4	X4	-	X2	X3	X4	X3	X3	X3	X3	X3
LPDDR4/X (> 3Gbps)	-	-	-	X32	X32	X32	-	X32	2 X32	X32	2 X32	2 X32	2x72	2x72	2x72
RISC-V hardwired			-	x			-	x	x		x	x	x	x	x
16 Gbps Serdes	-	-	-	X8	-	-	-	X8	X16	-	X16	X16	X16	X16	X16
25.8 Gbps Serdes	-	-	-	-	-	-	-	-	-	-	-	-	X8	X8	X8
PCIE Gen4 (16G) hard controller	-	-		1x PCIE Gen4x4				1x PCIE Gen4x4	2x PCIE Gen4x4		2x PCIE Gen4x4	2x PCIE Gen4x4	2x PCIE Gen4x8	2x PCIE Gen4x8	2x PCIE Gen4x8
Packages (HSIO/HVIO/LPDDR4/MIPI /SERDES)															
W64	0.4mm	3.5x3.4mm	-	34/0						-	-	-	-		-	-
F100 (SIP)	0.5mm	5.5x5.5mm	61/0	61/0						-	-	-	-		-	-
F100	0.5mm	5.5x5.5mm	61/0	61/0						-	-	-	-		-	-
F225	0.65mm	10x10mm	140/23	140/23	140/23				140/23		-	-	-		-	-
F169 (SIP)	0.65mm	9x9mm			83/27				83/27		-	-	-		-	-
F256	0.8mm	13x13mm	142/27	142/27							-	-	-		-	-
J361	0.65mm	13x13mm	-	-			110/20/16/2/0	110/20/16/2/0			-	-	-		-	-
G400	0.8mm	16x16mm					200/74/0/0/0	200/74/0/0/0								
J484 (SIP)	0.65mm	15x15mm	-	-			-	-			-	-	-		-	-
J484	0.8mm	18x18mm	-	-			116/27/32/4/0	116/27/32/4/0			-	-	-		-	-
J324	0.8mm	15x15mm	-	-	202/30/0/0				202/30/0/0		-	-	-		-	-
G529	0.8mm	19x19mm	-	-							-	-	-			
C529	0.8mm	19x19mm	-	-			-	-			176/50/32/0/0	-	176/50/32/0/0	176/50/32/0/0			
N441	0.5mm	11x11mm				86/18/16/1/8				86/18/16/1/8							
N576 SIP	0.65mm	16x16mm				116/50/0/2/8				116/50/0/2/8							
N576	0.65mm	16x16mm				100/34/32/2/8				100/34/32/2/8							
N676	0.8mm	22x22mm	-	-		139/84/32/2/8	-	-		139/84/32/2/8	-	-	-	-			
N676**	0.65mm	18x18mm				-	-	-		-	140/84/32/2/8	-	130/63/32/2/12	130/63/32/2/12			
N484	0.8mm	18x18mm	-	-		85/21/32/1/8	-	-		85/21/32/1/8	85/20/32/1/8	-	85/20/32/1/8	85/20/32/1/8			
N900	0.8mm	25x25mm	-	-			-	-			168/50/32x2/2RX/16	-	168/50/32x2/2RX/16	168/50/32x2/2RX/16			
N1156	1.0mm	35x35mm	-	-			-	-			234/103/32x2/3/16	-	234/103/32x2/3/16	234/103/32x2/3/16	x	x	x

** subject to change, just in the discussion — Avaialble

F100 (SIP) :16 MbFlash + 256Mbit HyperRAM — Available soon (122025)

J484 (SIP) : 2Gb LPDDR4X x16

N576 SIP: 2Gb LPDDR4X x16, SPI flash

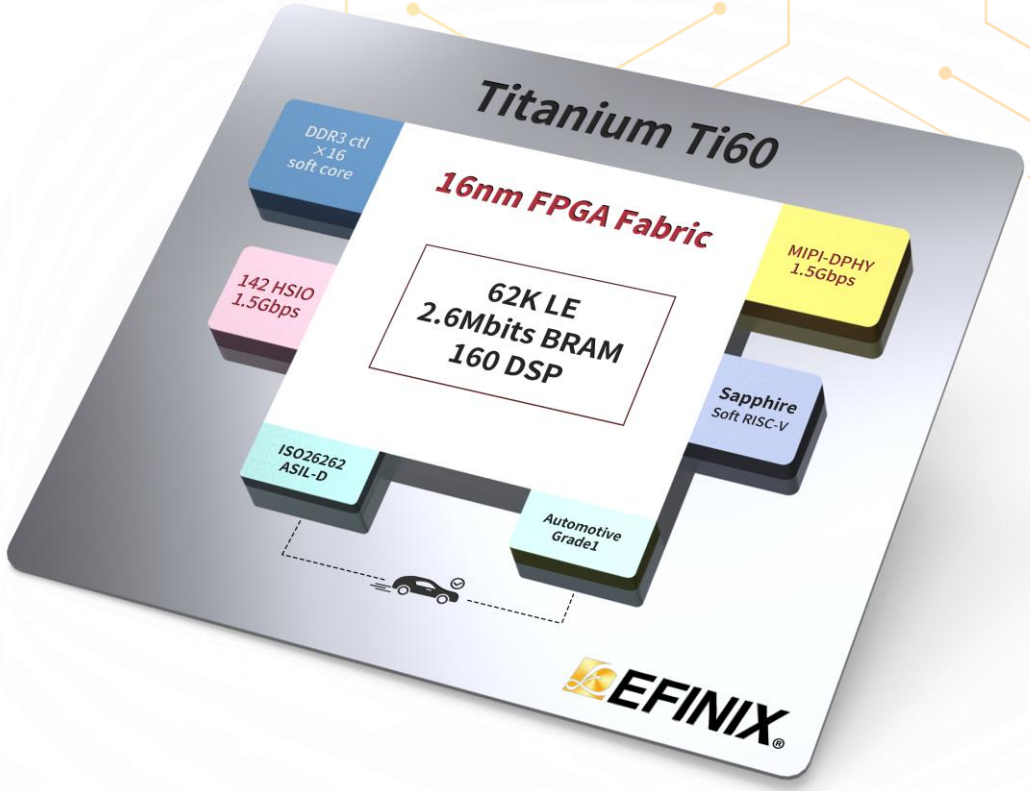
F169 (SIP): 2xHyperRam, SIP flash

Titanium Ti60 Highlight

Quantum™ compute fabric
- TSMC 16nm process
- High performance, Low power fabric
- 0.95V and 0.85V (LP mode) support
- High DSP compute capability
- High Embedded Memory resource

Security
- AES-GCM Bitstream Encryption
- AES-GCM Symmetric Authentication
- RSA-4096 Asymmetric Authentication

Qualification
- AEC-Q100

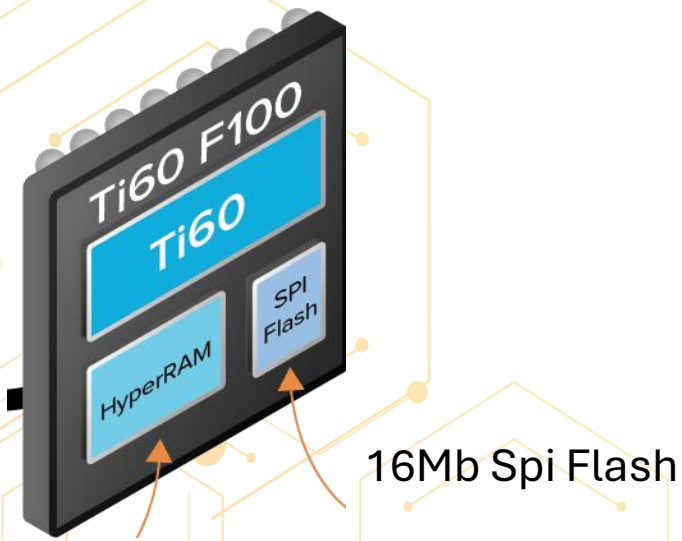


High Voltage IO
- 3.3V, 2.5V, 1.8V capable

High Speed IO
- LVDS 1.5Gbps
- MIPI-DPHY 1.5Gbps

Sapphire Soft IP
- Up to 350MHz

Ti60F100 SIP



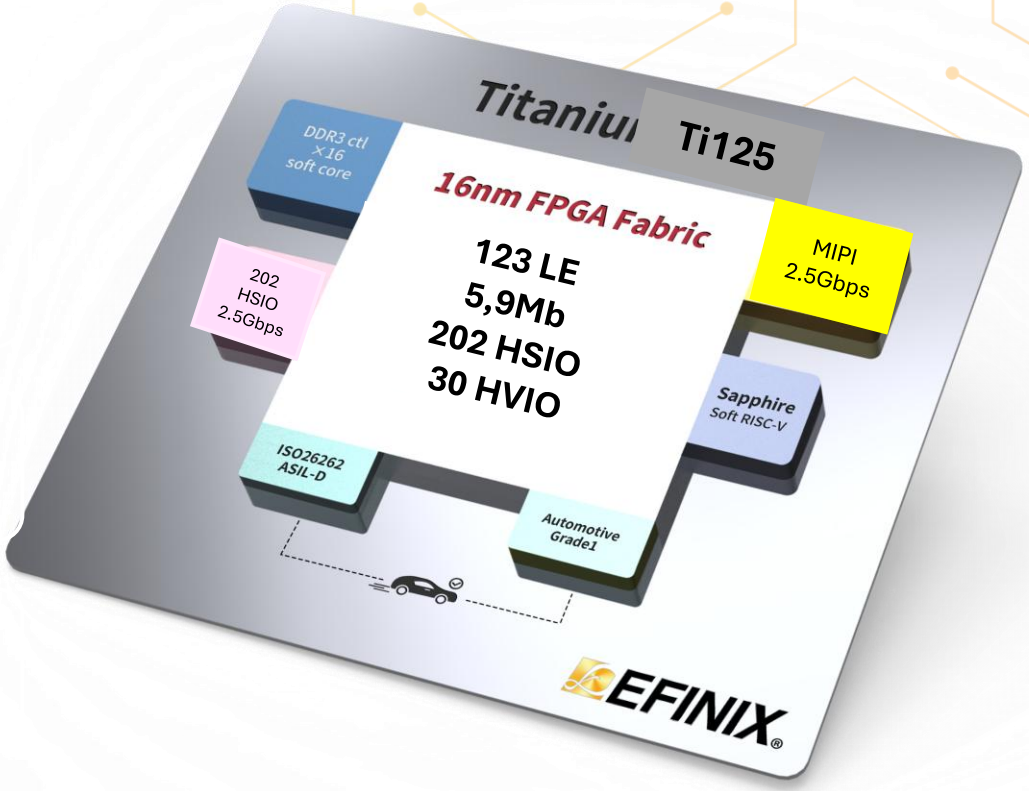
- FPGA with 60K LE, 2.6Mb Memory, 160 DSP Blocks
- BGA 100 Package (5.5x5.5mm, 0.5mm pitch)
- SPI flash 16Mb
- HyperRAM PSRAM up to 6.4Gbps (400Mbps x 16), (256Mb)
  - 500Mbps available soon !
- MIPI-CSI/DSI up to 1.5Gbps support.
  - 2x8 MIPI
  - 2x4 MIPI
- LVDS support up to 1.5Gbps
- VCC: 0.95/0.85V

Titanium Ti125 Highlight

Quantum™ compute fabric
- TSMC 16nm process
- High performance, Low power fabric
- 0.95V and 0.85V (LP mode) support
- High DSP compute capability
- High Embedded Memory resource

Security
- AES-GCM Bitstream Encryption
- AES-GCM Symmetric Authentication
- RSA-4096 Asymmetric Authentication

Memory Controller Soft IP
- Up to 1333Mbps

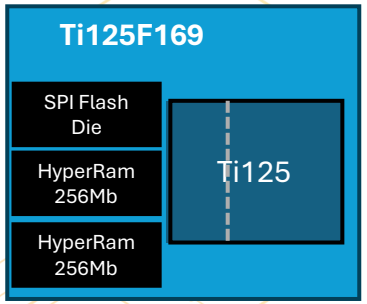


High Voltage IO
- 3.3V, 2.5V, 1.8V capable

High Speed IO
- LVDS 2.5Gbps
- MIPI-DPHY 2.5Gbps

Sapphire Soft IP
- Up to 350MHz

Ti125F169 SIP



- FPGA with 125K LE, 5.6Mb Memory, 288 DSP Blocks
- BGA 169 Package (8x8mm, 0.5mm pitch)
- SPI flash
- HyperRAM PSRAM up to 12.8Gbps (2x(400Mbps x 16)), (2x256Mb)
  - 500Mbps available soon !
- MIPI-CSI/DSI up to 2.5Gbps support.
  - x8 MIPI
  - x4 MIPI
- LVDS support up to 2.5Gbps
- DDR3 memory support up to 1333Mbps
- Samples expected end of the year !

- VCC: 0.95/0.85V

Titanium Serdes - Ti375 Highlight

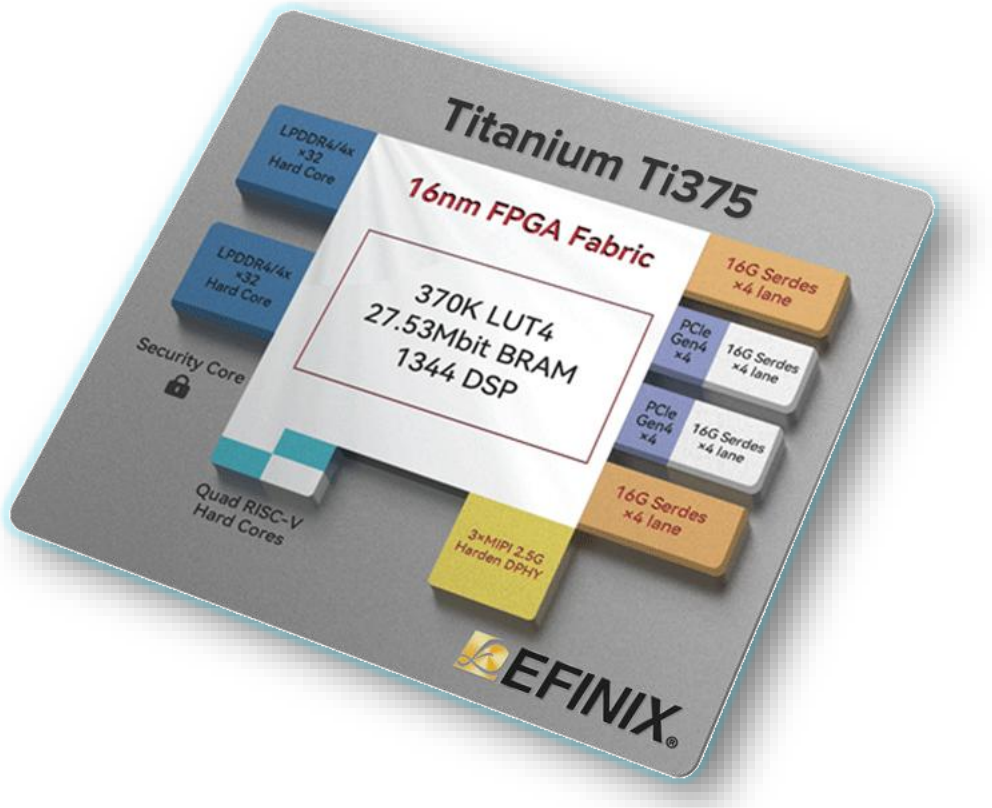
Quantum™ compute fabric
- TSMC 16nm process
- High performance, Low power fabric
- 0.95V and 0.85V (LP mode) support
- High DSP compute capability
- High Embedded Memory resource

3300-LPDDR4/x Hard IP
- x32-bit LPDDR4/4x @ 3300Mbps
- LPDDR4x reduce I/O voltage by 50% for both memory & controller (1.1V to 0.6V)
- Harden DDR PHY and Controller IP, optimum performance and power

Security
- AES-GCM Bitstream Encryption
- AES-GCM Symmetric Authentication
- RSA-4096 Asymmetric Authentication

Qualification
- AEC-Q100*

Quad Core Risc-V RV32 SoC
- Quad Core RV32-IMACFD
- MMU, FPU, Custom Instruction support



Quad 16Gbps High Speed Serdes
- Support x1, x2 and x4 configurations
- Support PCIe 4.0, 10G-KR, SGMII, PHY-only mode

PCIE Gen4x4 Controller Hard IP
- Compliant with PCIe 4.0, 3.2, 2.1, and 1.1 Spec
- Support x1, x2 and x4 configurations
- Configure as Root Port (RP), or End Point (EP)
- Single Root IO Virtualization (SRIOV)

2.5Gbps MIPI-DPHY Hard IP
- 3 MIPI-DPHY 2.5Gbps x4 lanes Hard IP instances (RX & TX)
- CSI-2, DSI soft IP

High Voltage IO
- 3.3V, 2.5V, 1.8V capable

High Speed IO
- LVDS 1.5Gbps
- MIPI-DPHY 1.5Gbps

*: planned

Titanium Serdes – Ti135 Highlight

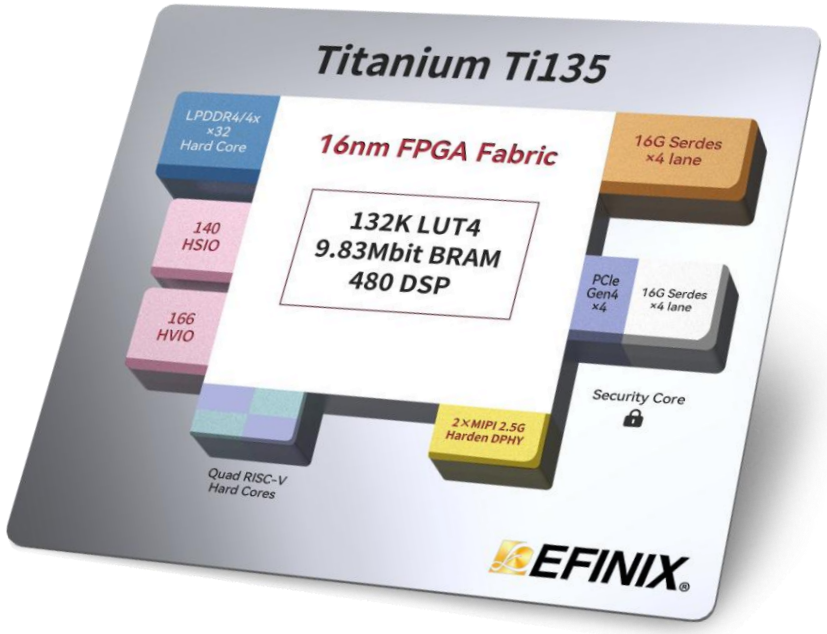
Quantum™ compute fabric
- TSMC 16nm process
- High performance, Low power fabric
- 0.95V and 0.85V (LP mode) support
- High DSP compute capability
- High Embedded Memory resource

3300-LPDDR4/x Hard IP
- x32-bit LPDDR4/4x @ 3300Mbps
- LPDDR4x reduce I/O voltage by 50% for both memory & controller (1.1V to 0.6V)
- Harden DDR PHY and Controller IP, optimum performance and power

Security
- AES-GCM Bitstream Encryption
- AES-GCM Symmetric Authentication
- RSA-4096 Asymmetric Authentication

Qualification
- AEC-Q100*

Quad Core Risc-V RV32 SoC
- Quad Core RV32-IMACFD
- MMU, FPU, Custom Instruction support



Quad 16Gbps High Speed Serdes
- Support x1, x2 and x4 configurations
- Support PCIe 4.0, 10G-KR, SGMII, PHY-only mode

PCIE Gen4x4 Controller Hard IP
- Compliant with PCIe 4.0, 3.2, 2.1, and 1.1 Spec
- Support x1, x2 and x4 configurations
- Configure as Root Port (RP), or End Point (EP)
- Single Root IO Virtualization (SRIOV)

2.5Gbps MIPI-DPHY Hard IP
- 2 MIPI-DPHY 2.5Gbps x4 lanes Hard IP instances (RX & TX)
- CSI-2, DSI soft IP

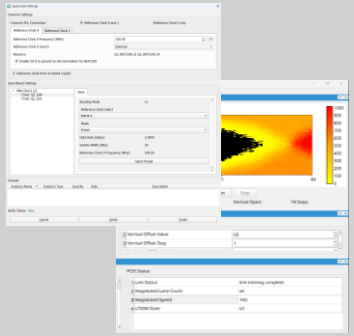
High Voltage IO
- 3.3V, 2.5V, 1.8V capable

High Speed IO
- LVDS 1.5Gbps
- MIPI-DPHY 1.5Gbps

*: planned

Transceiver Ecosystem

Efinity Support



Flexi rate, Mix Mode,
Multi-protocol Support

PCIE

PCIE EP Gen1/2/3/4

Ready!

1/2.5/5/10GE

Intel PHY
Realtek PHY
Marvel PHY

Ready!

SLVS-EC

Sony SLVS-EC
Gen1/2

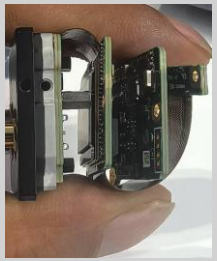
Ready!

SDI

HD/3G-SDI
UHD/6G/12G-SDI

Ready!

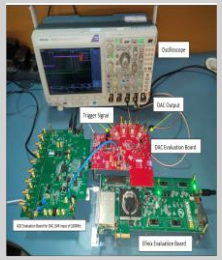
CoaXPress



1.25/2.5/3.125/5/6.25
/10/12.5Gbps CXP

Ready!

JESD204B



JESD204B TX/RX
With TI ADC/DAC

Ready!

Aurora

Aurora 8b10b, 64b66b
With Xilinx Kintex7,
Virtex7 boards

Ready!

HDMI

HDMI 1.4/2.0 -> 4K60
HDMI 2.1 -> 8K60/4K120

Q3/25

Display Port

DP1.3 -> 4K60
DP1.4 -> 8K60/4K120

Q4/25

September 2025

Continue Innovation

Sapphire SoC

- Soft Processor (Performance)
- RV32 with IMAFDC extension
- 100-400Mhz System Clock
- Quad Core
- Multi-way Instruction and Data Cache
- MMU, Linux Capable
- Hardware FPU
- Custom Instruction

Sapphire Lite

- Soft Processor (Area)
- RV32 with IM extension
- 100-200Mhz System Clock
- Single Core
- Instruction and Data Cache
- 4KLE resource consumption

Sapphire High Performance

Ti375, Ti240, Ti165,Ti135,Ti85

- Hard Processor (High Performance)
- RV32 with IMAFDC extension
- >1GHz System Clock
- Quad Core
- Multi-way Instruction and Data Cache
- MMU, Linux Capable
- Hardware FPU
- Custom Instruction
- ~500mW CPU Hard IP power

Same Embedded Software Development, IDE, Tool Chain, Driver

Risc-V IDE | **Debugger** | **Linux OS** | **RTOS** | **Zephyr OS**

Ethernet Linux/FreeRTOS Solution Stack

SD Card Storage Solution Stack

and more..

Comparison Hard VS Soft Sapphire

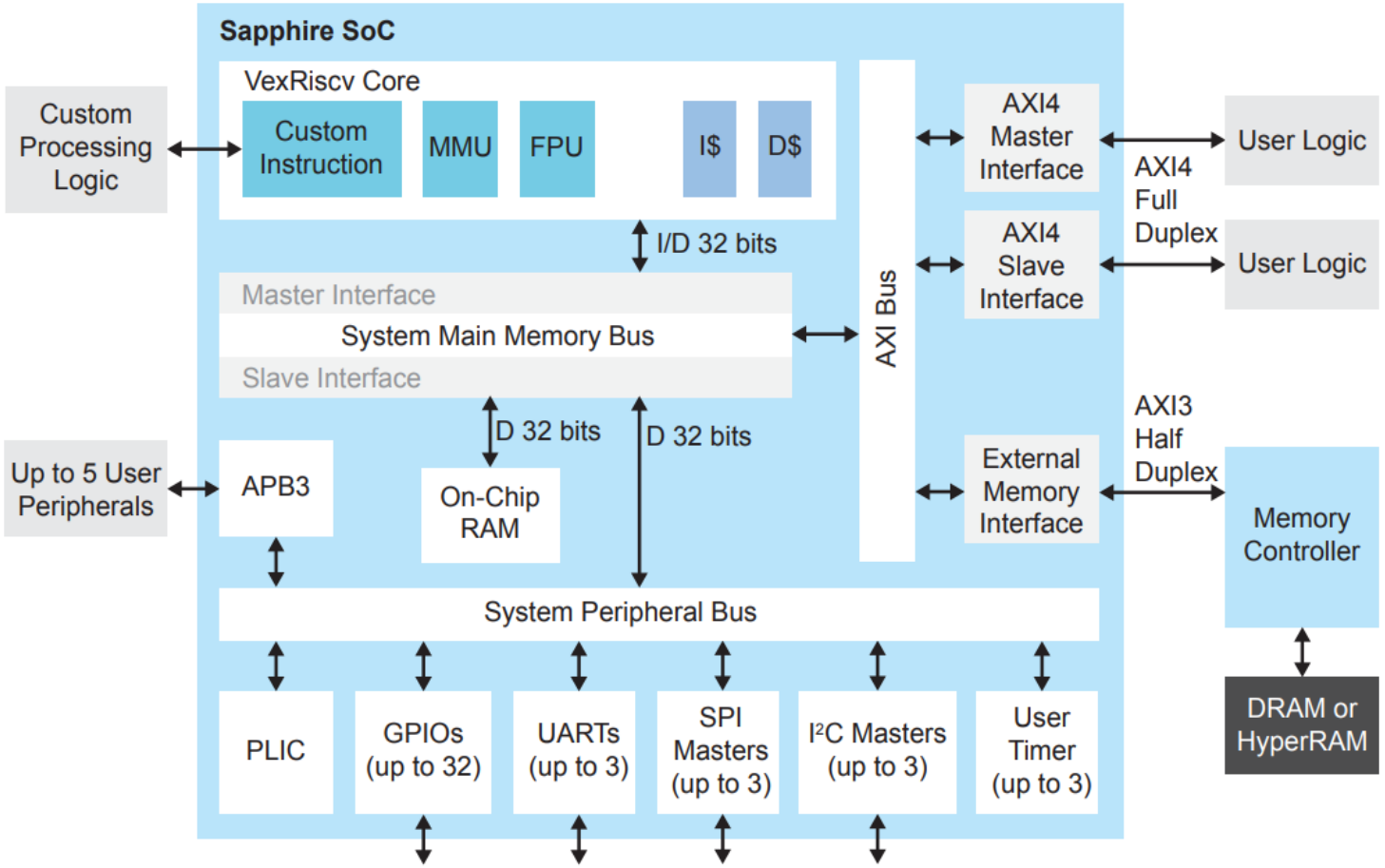
Hard Sapphire

- 128-bit internal bus
- Improves data path latency between CPU and periphery
- Static branch predictor
- Unblocked operation for custom instruction
- Dedicated FPU for each core
- 8 Hardware breakpoints for debug module
- Data coherency between CPU and DMA channel (AXI Master)
- Additional write buffer to improve write performance to external memory

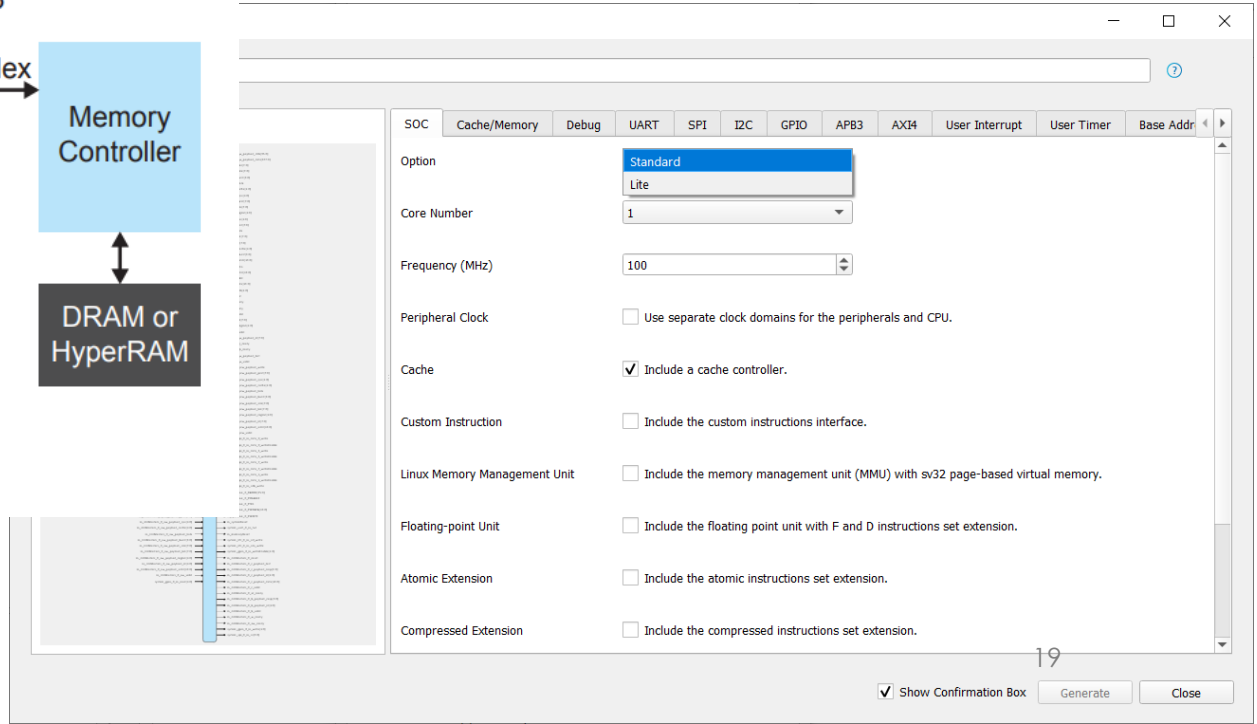
Soft Sapphire

- Max 64-bit internal bus
- Higher latency due to pipelining, trade-off for fmax
- No branch predictor
- Stall CPU pipeline until get the result from custom ALU
- Shared FPU for multi-core configuration
- Up to 4 hardware breakpoints
- No data coherency between CPU and DMA channel (AXI master)
- No write buffer introduced in SoC

Sapphire

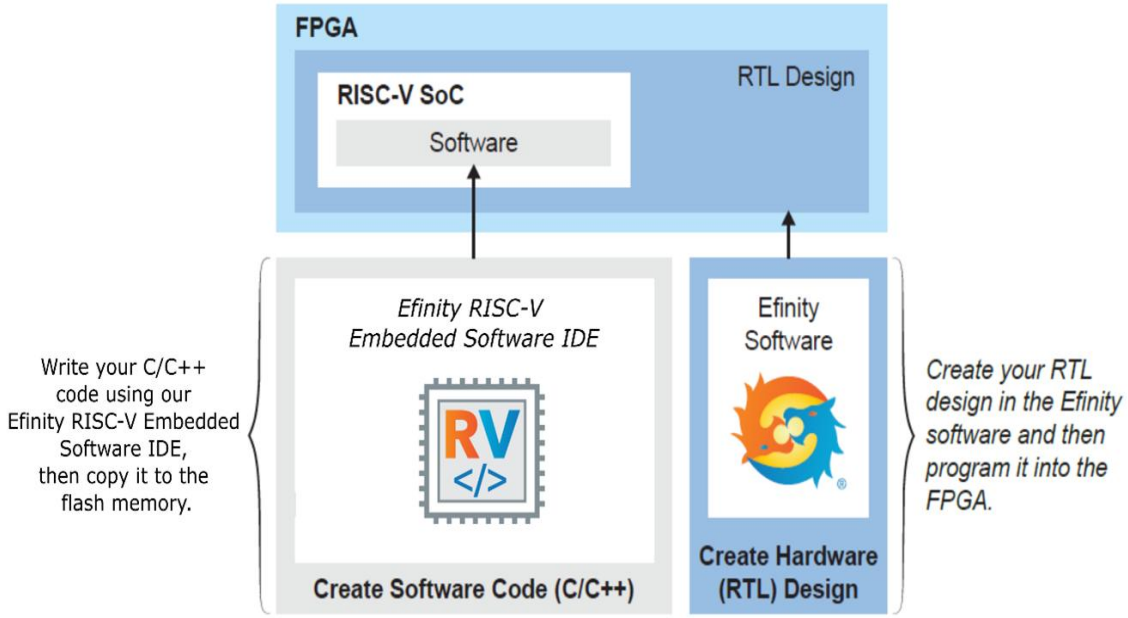


- New:
  - LINUX MMU
  - FPU
  - Custom Instructions



Required Software and Tools

- Efinity® software
- Pre-compiled, open-source SDK
- Eclipse IDE for managing projects and software with Ashling GUI
- RISC-V GCC compiler and GDB debugger
- OpenOCD debugger for debugging applications
  - Lauterbach Tracer support
- Windows build tools (Windows)
- Available from our web page
  - https://www.efinixinc.com/products-riscv.html



Soft IPs/SOC available in IP catalog

Additional examples e.g how to infere the different Memories like DP-RAM you can find under the support knowledgebase

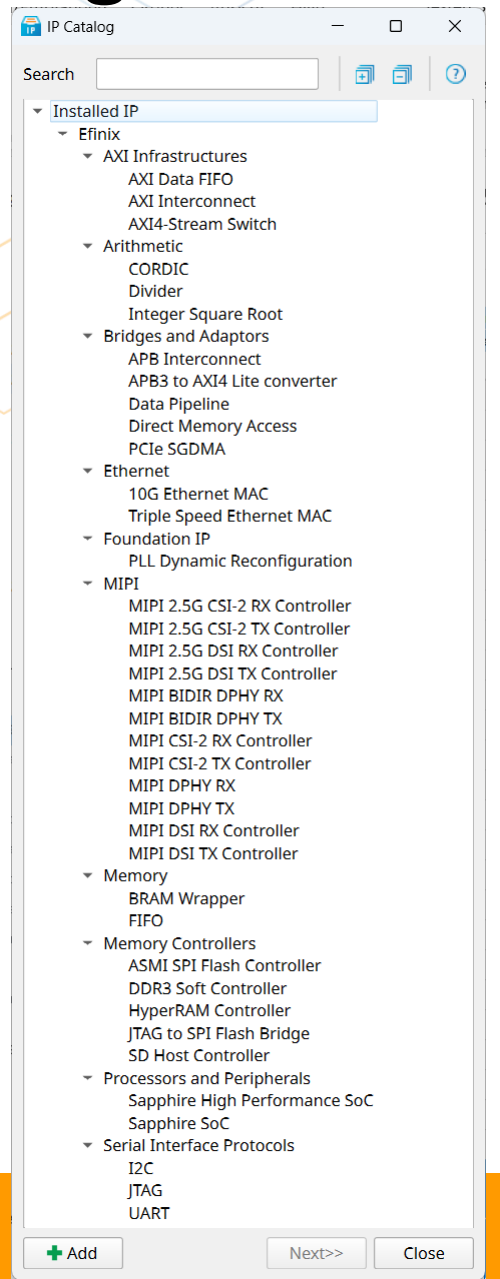
https://www.efinixinc.com/support/kb/index.php

Filter IP cores are available in Beta (FFT, FIR)

Open Source:

e.g.: https://github.com/open-logic/open-logic

I2C, SPI, AXI



Partner IP Cores : High Speed

- SLVS-EC available (Beta status), partner CIS, available from Efinix
- SDI 3/6 available (beta), partner CIS, available from Efinix
- SDI 12 in progress partner CIS, available from Efinix
- JESD204B available, partner Logic Fruit
- DP partner Logic Fruit
- HDMI partner Bitec
- Aurora partner ALSE
- CXP providing PMA settings, core in discussion
- Vx1 wrapper
- GigE-Vision/10GigE-Vison Imavix
- 40GE (4x10GE) Imavix

Free of charge Software Features

Projects
Project management to keep your design files organized

Dashboard
Easy-to-use dashboard to run the tool flow automatically or manually

Language Support
Verilog HDL, SystemVerilog, and VHDL

Interface Designer
Constrain logic and assign pins to blocks in the device periphery

IP Manager
Configure and add buildling blocks to your project

Floorplan Viewer
Browse through your design's logic and routing placement

Netlist Viewer
Displays and analyzes your design's netlist

Timing Browser
Browse timing and perform static timing analysis

Simulation
Supports simulation flows using the ModelSim, NCSim, Aldec, or free iVerilog simulators

BRAM Initial Content Updater
Update initial BRAM without performing a full compile

Python API
Use scripts to build your design's interface

Package Planner
Assign logic to package pins and view the pinout graphically

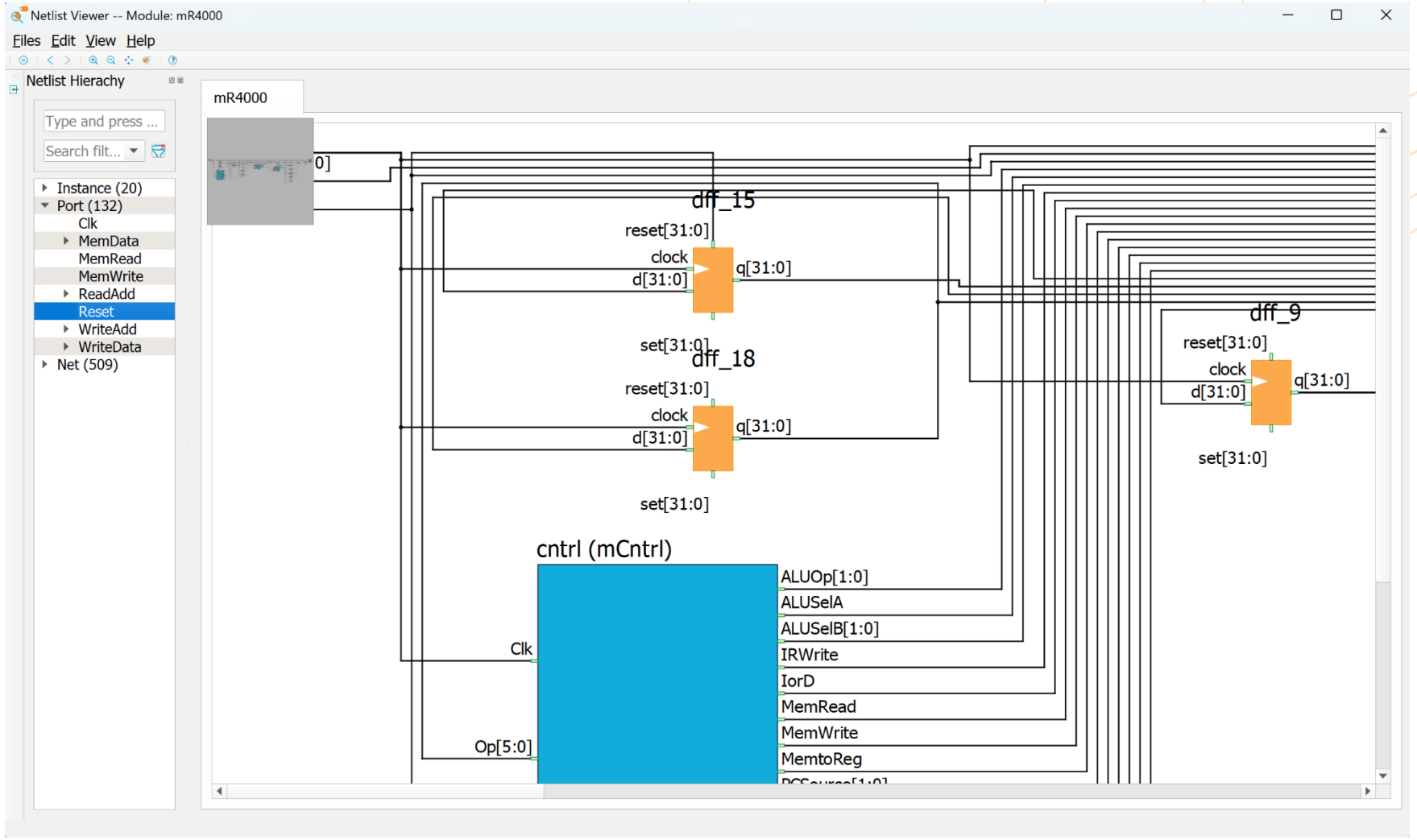
Hardware Debugger
Integrated hardware Debugger with Logic Analyzer and Virtual I/O debug cores

Programmer
GUI and command-line Programmer to configure your FPGA

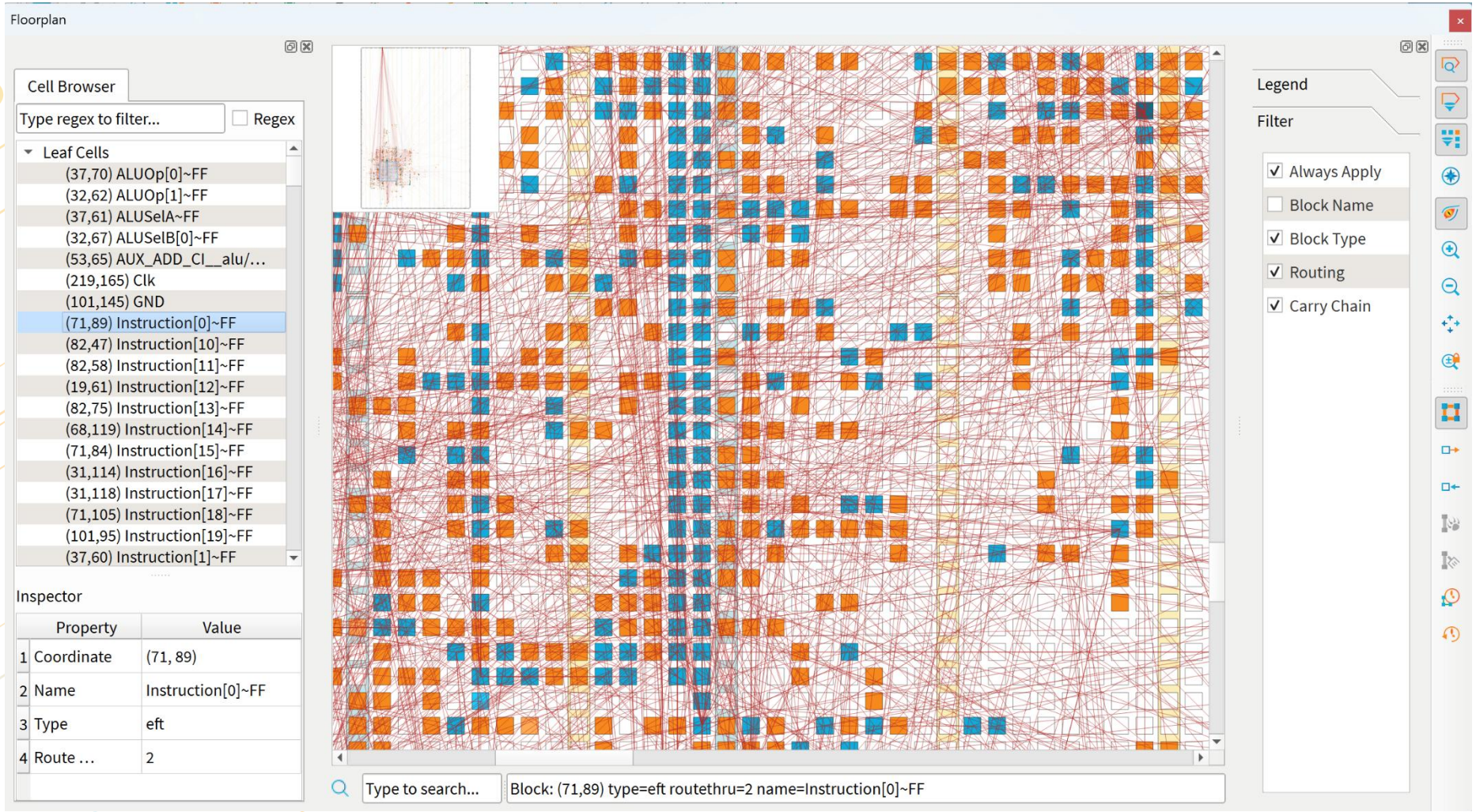
JTAG SVF Player
Sends JTAG command to an FPGA

Bitstream Authentication and Encryption
Sign and/or encrypt bitstreams

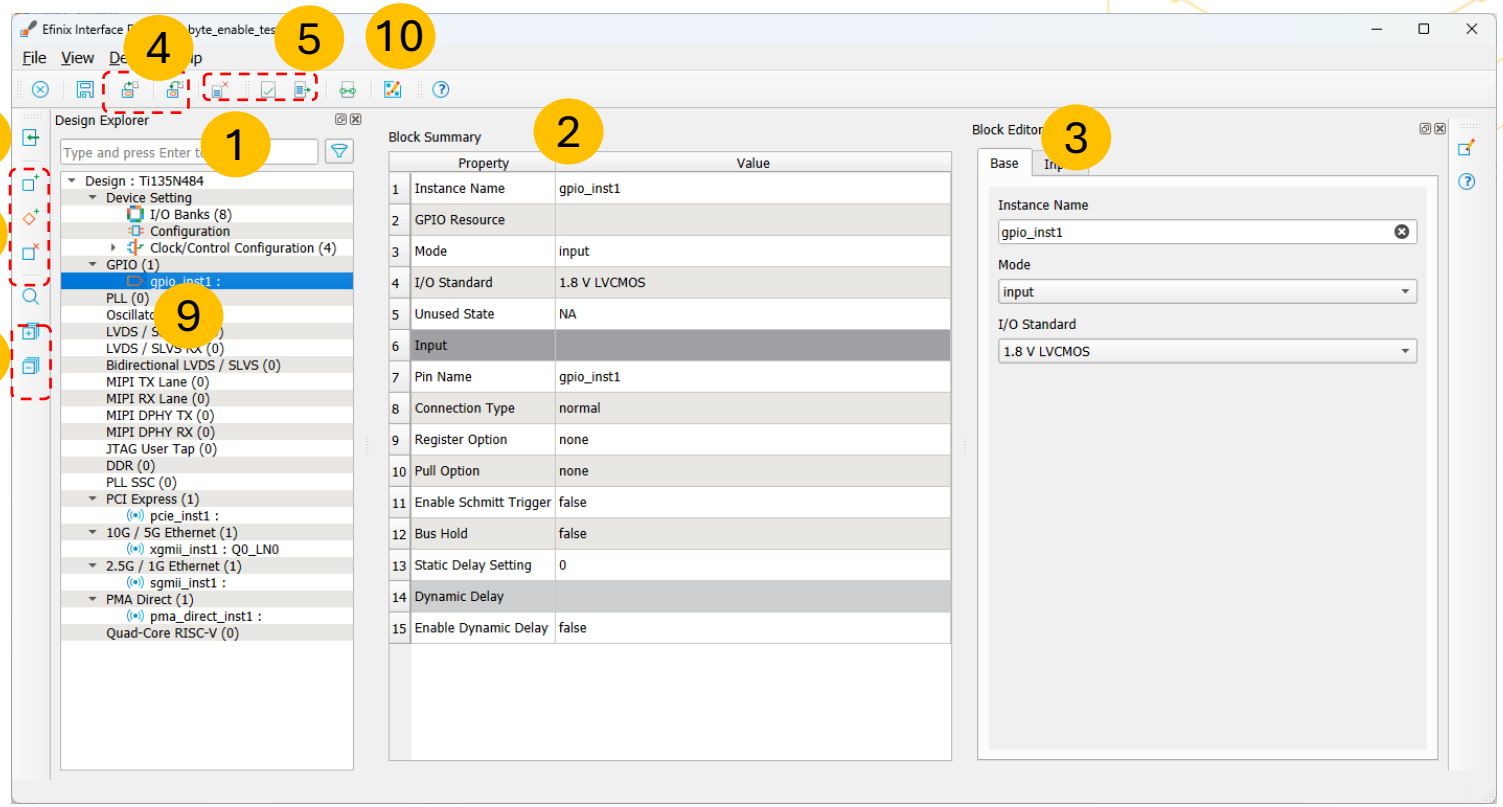
RTL Viewer


Netlist Viewer -- Module: mR4000
Files Edit View Help
Netlist Hierachy
Type and press ...
Search filt...
Instance (20)
Port (132)
Clk
MemData
MemRead
MemWrite
ReadAdd
Reset
WriteAdd
WriteData
Net (509)
mR4000
dff_15
reset[31:0]
clock
d[31:0]
q[31:0]
set[31:0]
dff_18
reset[31:0]
clock
d[31:0]
q[31:0]
set[31:0]
dff_9
reset[31:0]
clock
d[31:0]
q[31:0]
set[31:0]
cntrl (mCntrl)
Clk
Op[5:0]
ALUOp[1:0]
ALUSelA
ALUSelB[1:0]
IRWrite
IorD
MemRead
MemWrite
MemtoReg

Floorplan Viewer

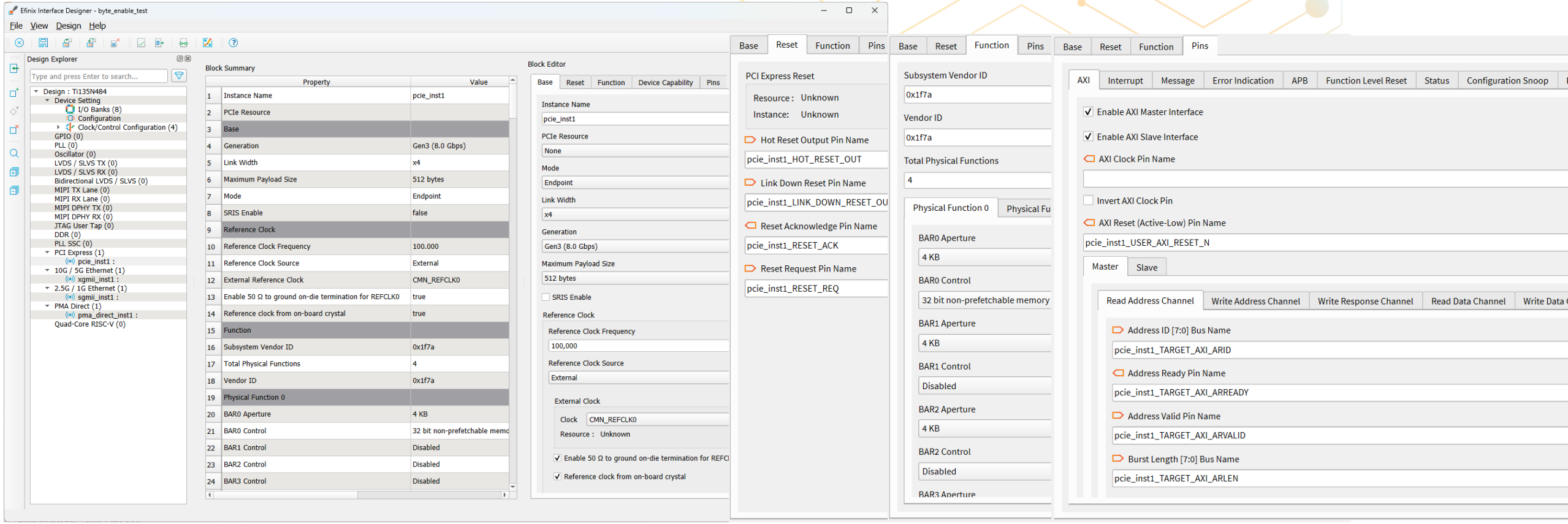


Interface Designer

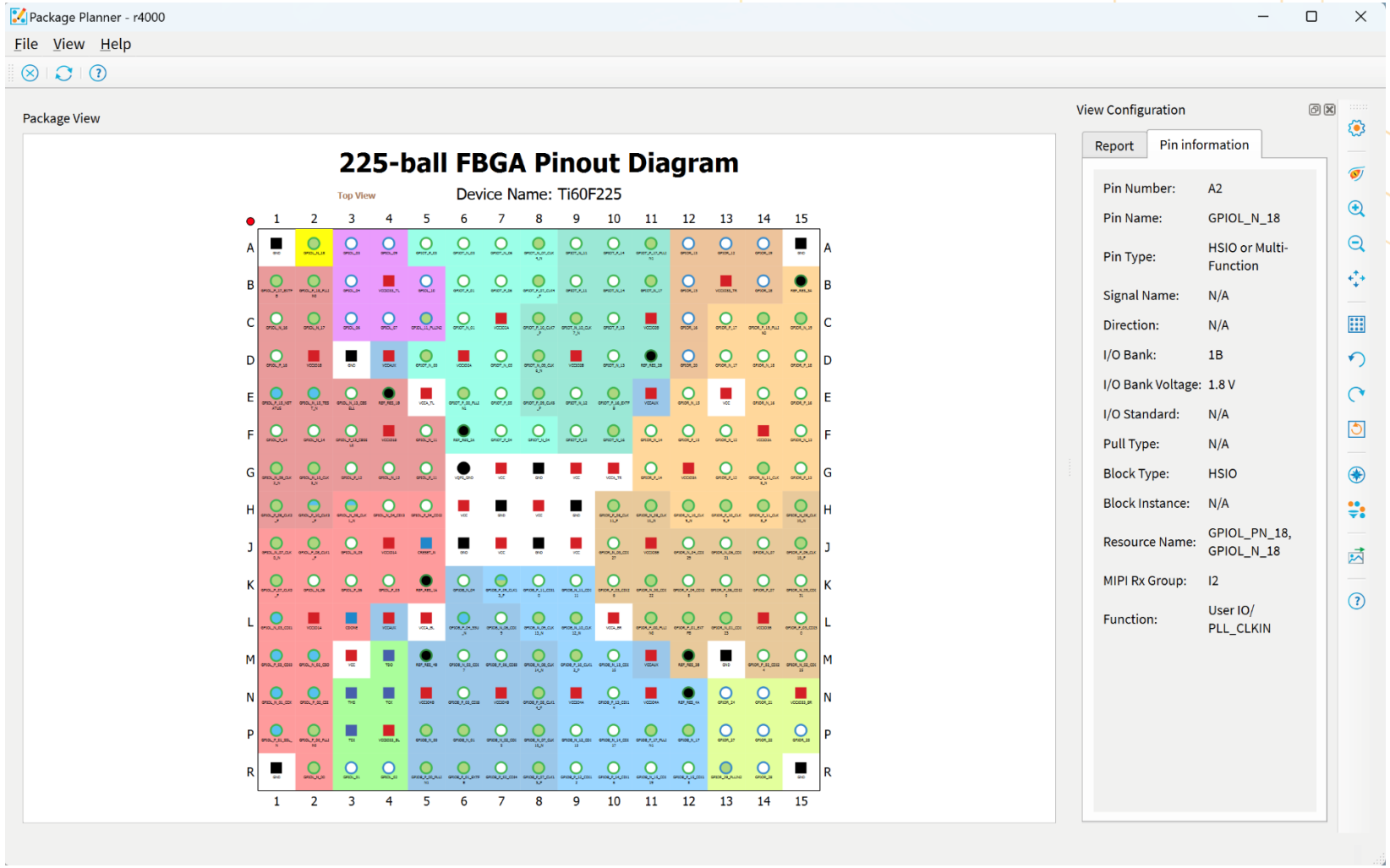


1. The Design Explorer shows the interfaces in your Design
2. Block Summary shows settings for the selected Block
3. Block Editor add or change settings
4. Import/Export GPIO assignments
5. Project Management Tools for design check
6. Show/Hide Resource Assigner
7. Block Tools add/delete blocks
8. Expand/Collaps Design Explorer folder
9. Number of used blocks()
10. Package Planner

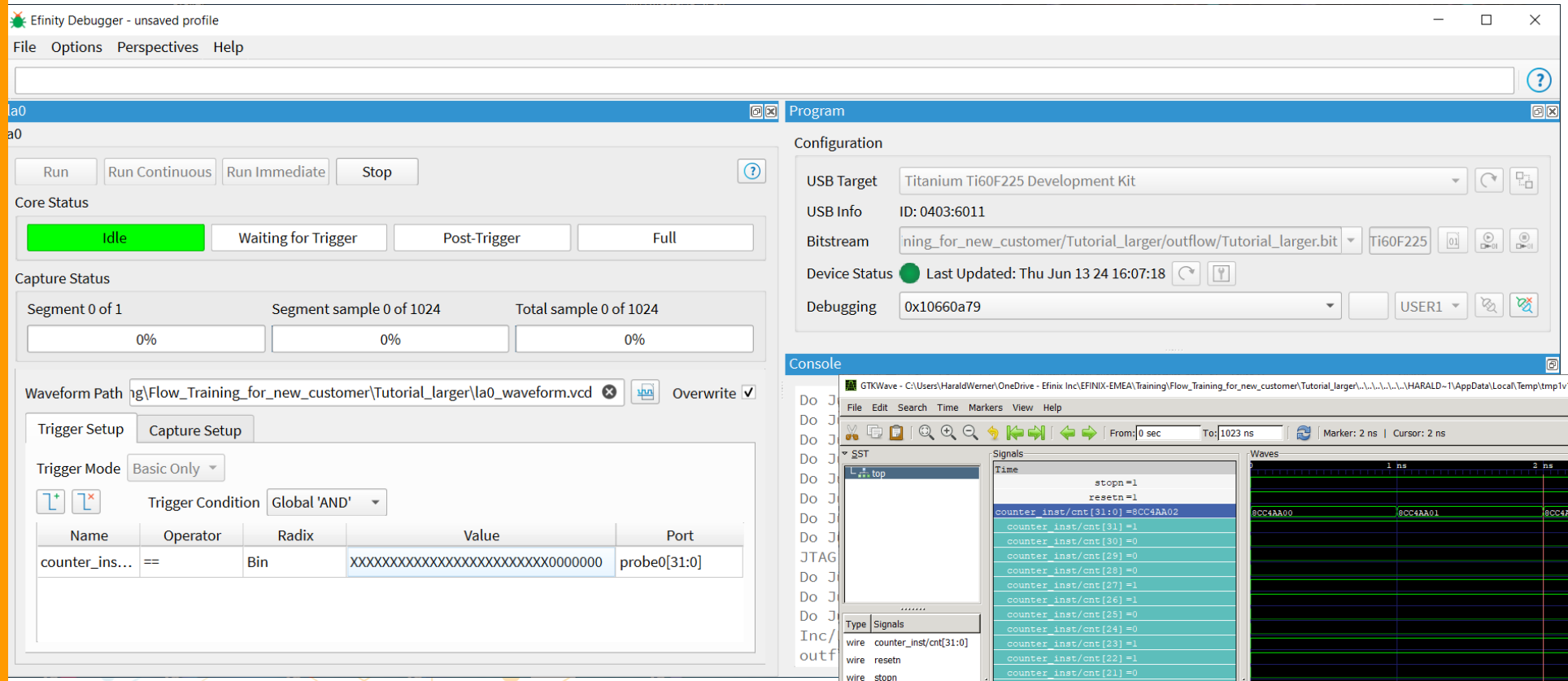
SERDES access: PCI-E



Package Planner

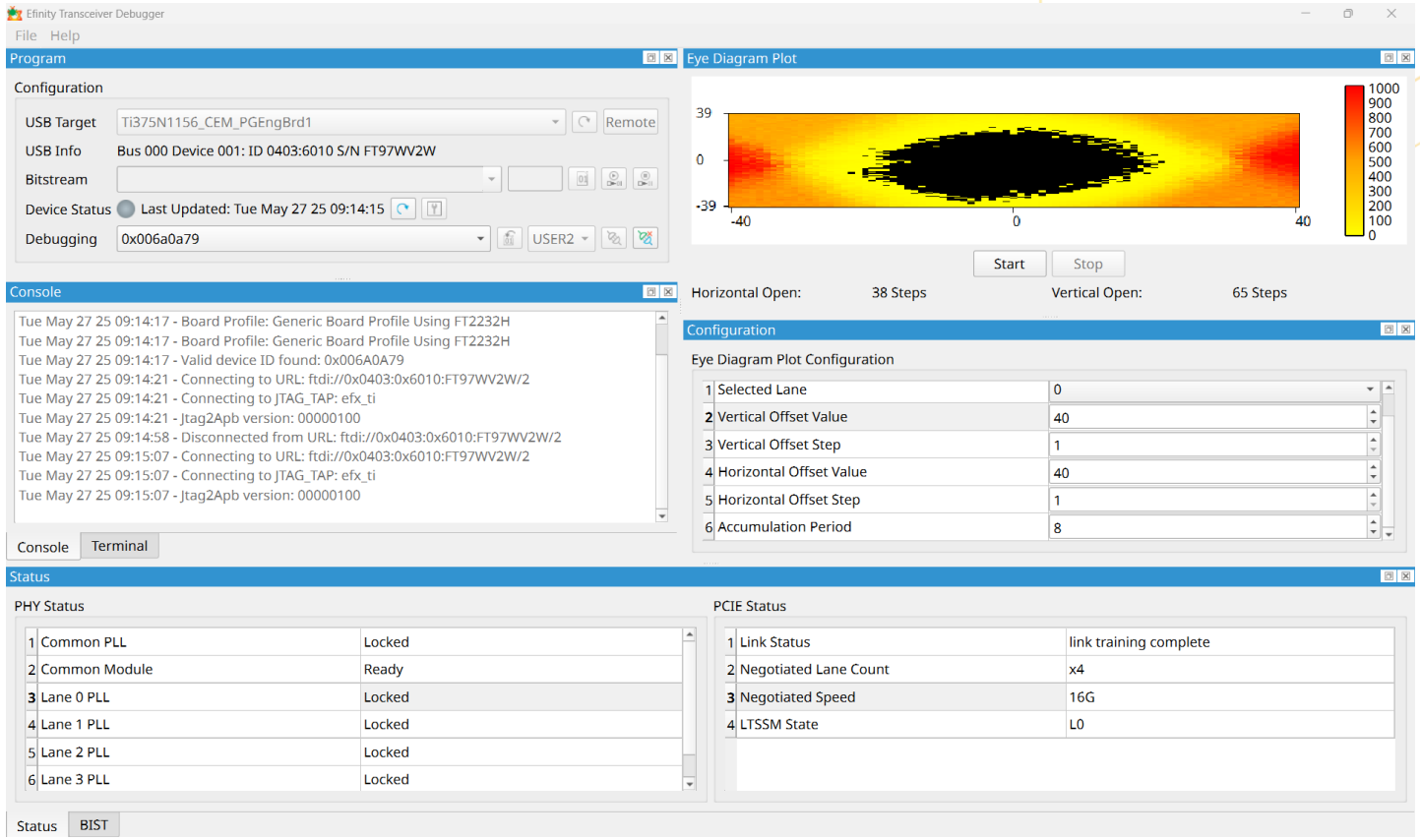


Hardware Debugger



September 2025

Serdes Debugger



- Eyesurf
- Build in Self Test(BIST)
  - Internal Parallel Loopback
  - Internal Serial Loopback
  - External Serial Loopback
- Internal Register Read-write via APB

Product	Model	Memory
Trion	T4, T8, T13, T20, T35	8 GB
	T55, T85, T120	12 GB
Titanium	Ti35, Ti60, Ti85, Ti90, Ti120, Ti135, Ti180	8 GB
	Ti165, Ti240, Ti375	12 GB
Topaz	Tz50, Tz75, Tz100, Tz110, Tz170	8 GB
	Tz200, Tz325	12 GB

- Minimum requirements
  - Computer with a 64 bit operating system, dual-core processor, and 8 GB RAM
- Linux environments
  - Operating system: Ubuntu x86-64 v20.04 or later, Red Hat Enterprise x86-64 v8.8 or later
  - Linux X11 or Wayland windowing system (for Efinity® GUI)
  - Udev device manager for Efinix USB programming cable
  - Open-source Java 64-bit runtime environment (8 or higher); required for configuring the Sapphire RISC-V SoC in the IP Manager; available from: https://developers.redhat.com/products/openjdk/download (OpenJDK 8 or 11) – http://jdk.java.net/16/ (OpenJDK 16)
- Windows environments
  - Windows 10 or later, 64 bit
  - Microsoft Visual C++ 2022 x64 runtime library (or latest version)
  - Open-source Java 64-bit runtime environment; required for configuring the Sapphire RISC-V SoC in the IP Manager; available from: – https://www.java.com/en/download/manual.jsp (Java 8)
- GTKwave 3.3.117 (GTKwave 3.3.100 for Windows)

Programming Hardware

Recommended hardware

- FT2232H Mini Module
- FT4232H Mini Module

(C232HM-DDHSL-0 FTDI cable still in use but no longer recommended)

Mini Modules are a bit more robust because of their VCC/GND plane. (noise)

Mini Modules and C232HM are for 3.3V JTAG interface only.

Other voltages are supported with EFINIX Download Cable II, designed by Centron, available e.g. at Digikey