FBK Platform for Flexible PCB Manufacturing

MICRO NANO FACILITY

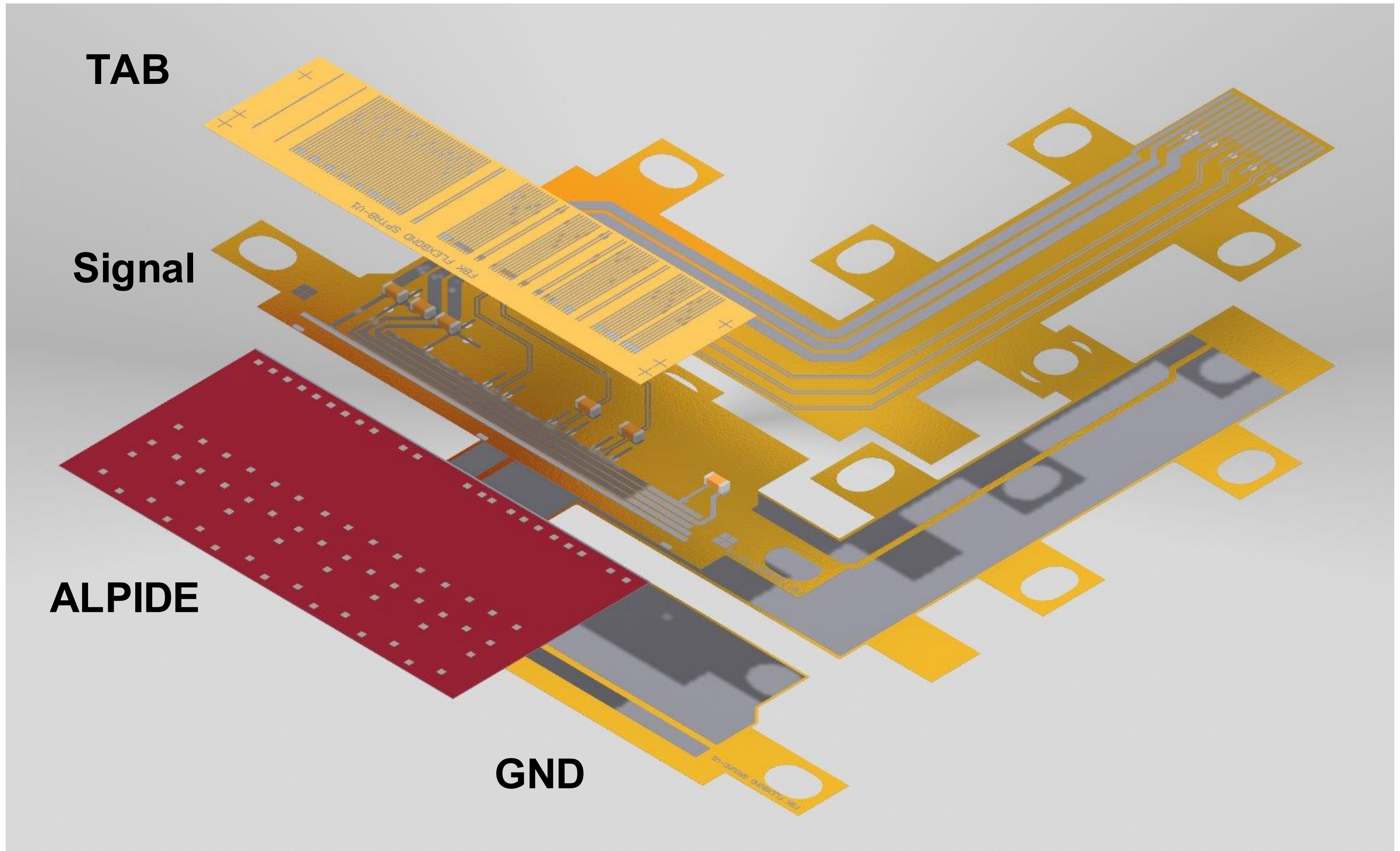
02/09/2025 @ **KIT**

ECFA DRD 7.6b Workshop on Future Detector Technologies

David Novel, Alessandro Lega, Maurizio Boscardin
novel@fbk.eu alega@fbk.eu boscardi@fbk.eu

with the contribution of several colleagues of the Sensor and Devices Center

Low mass Aluminium Flex Platform
ALPIDE integration with TAB



!! Design inspired from ITS3 tests with bent ALPIDE [1] and adapted for spTAB !!

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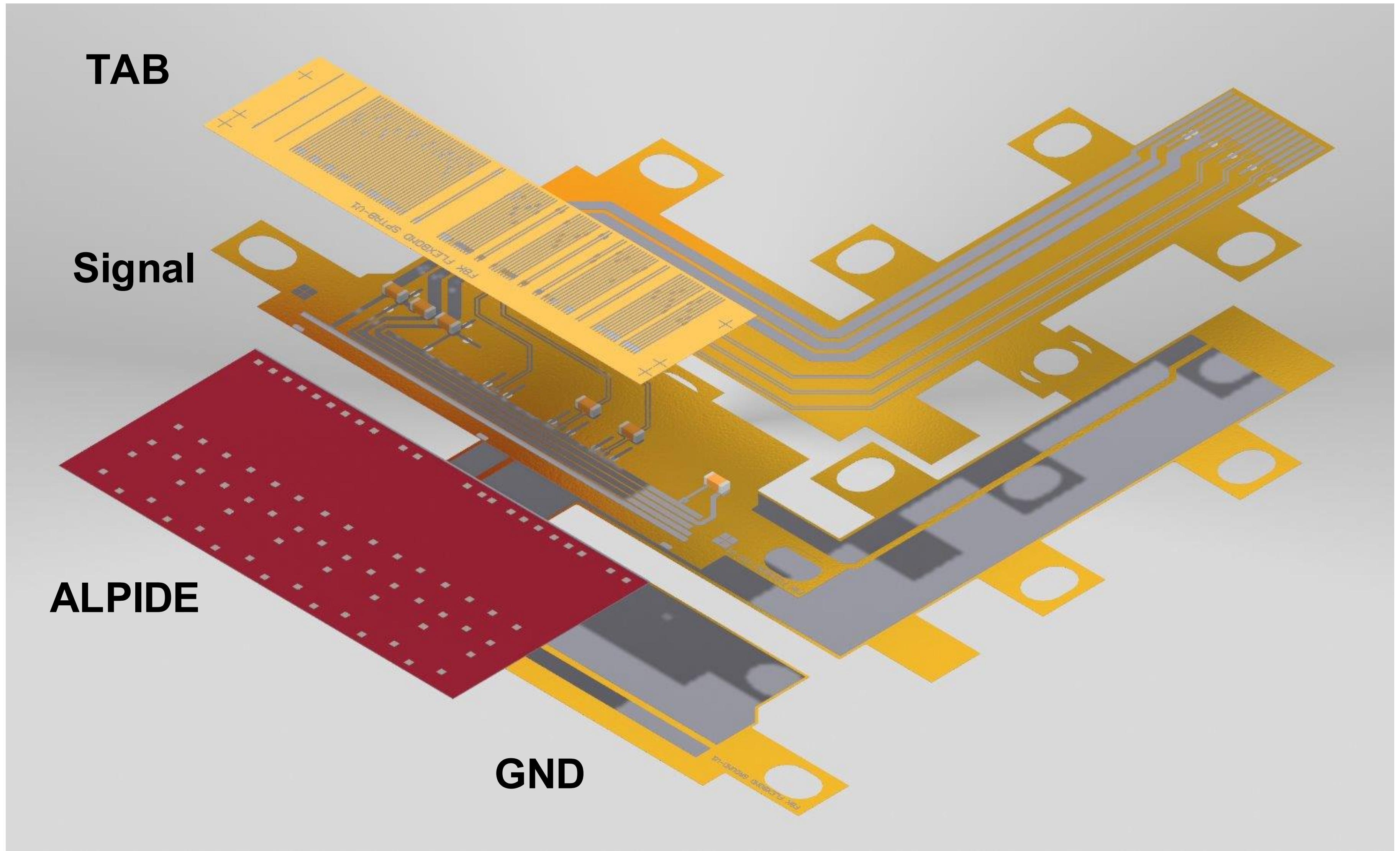

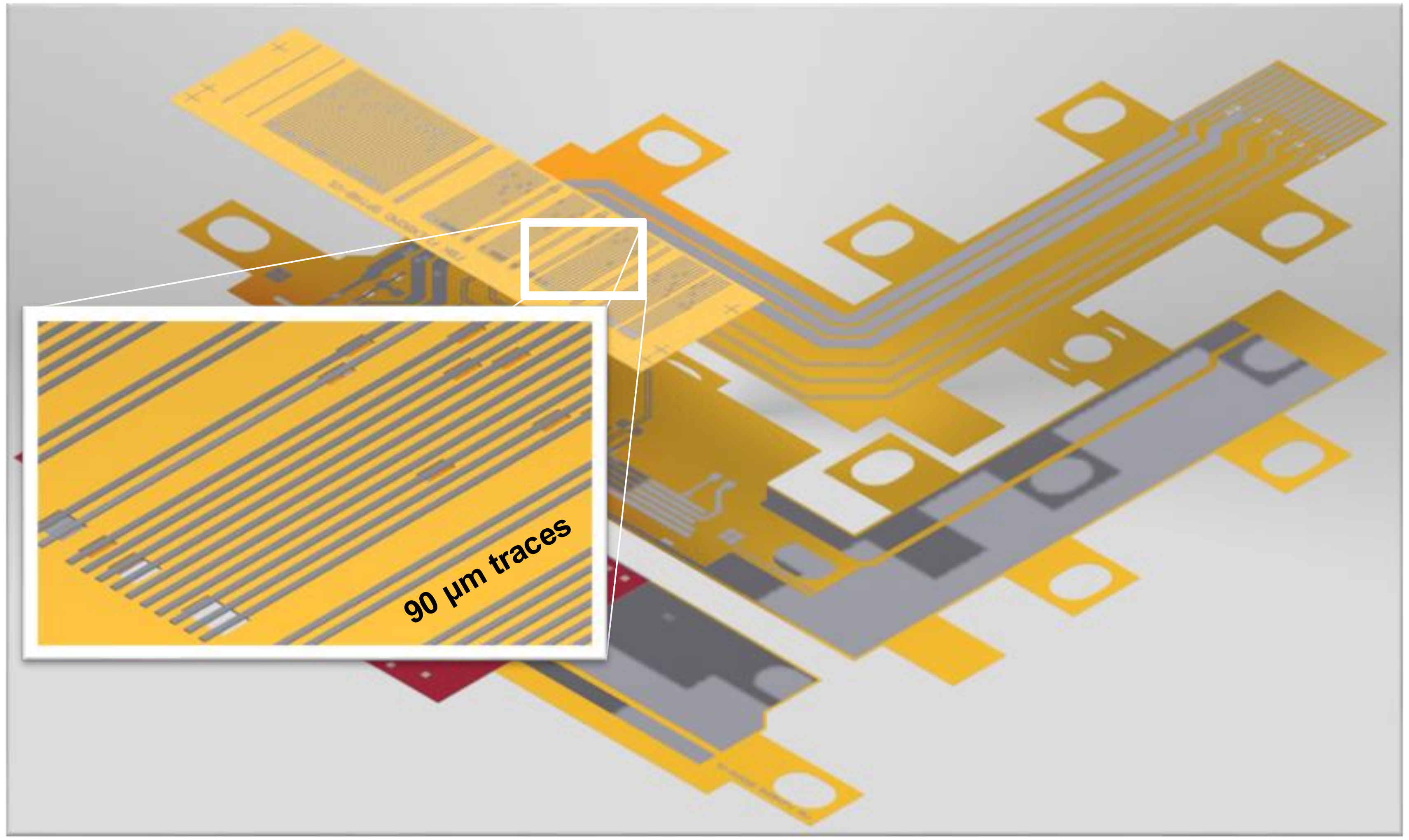

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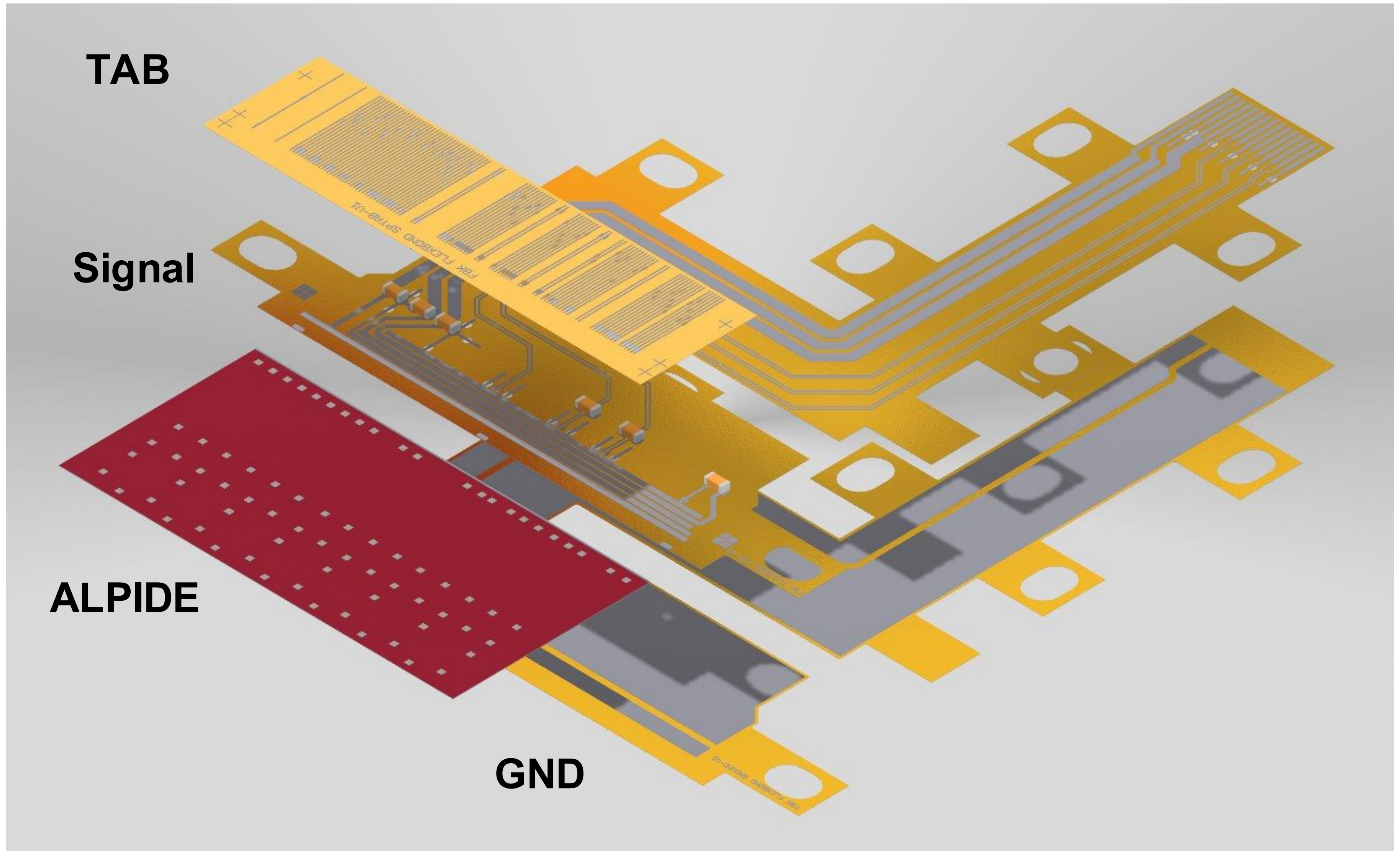

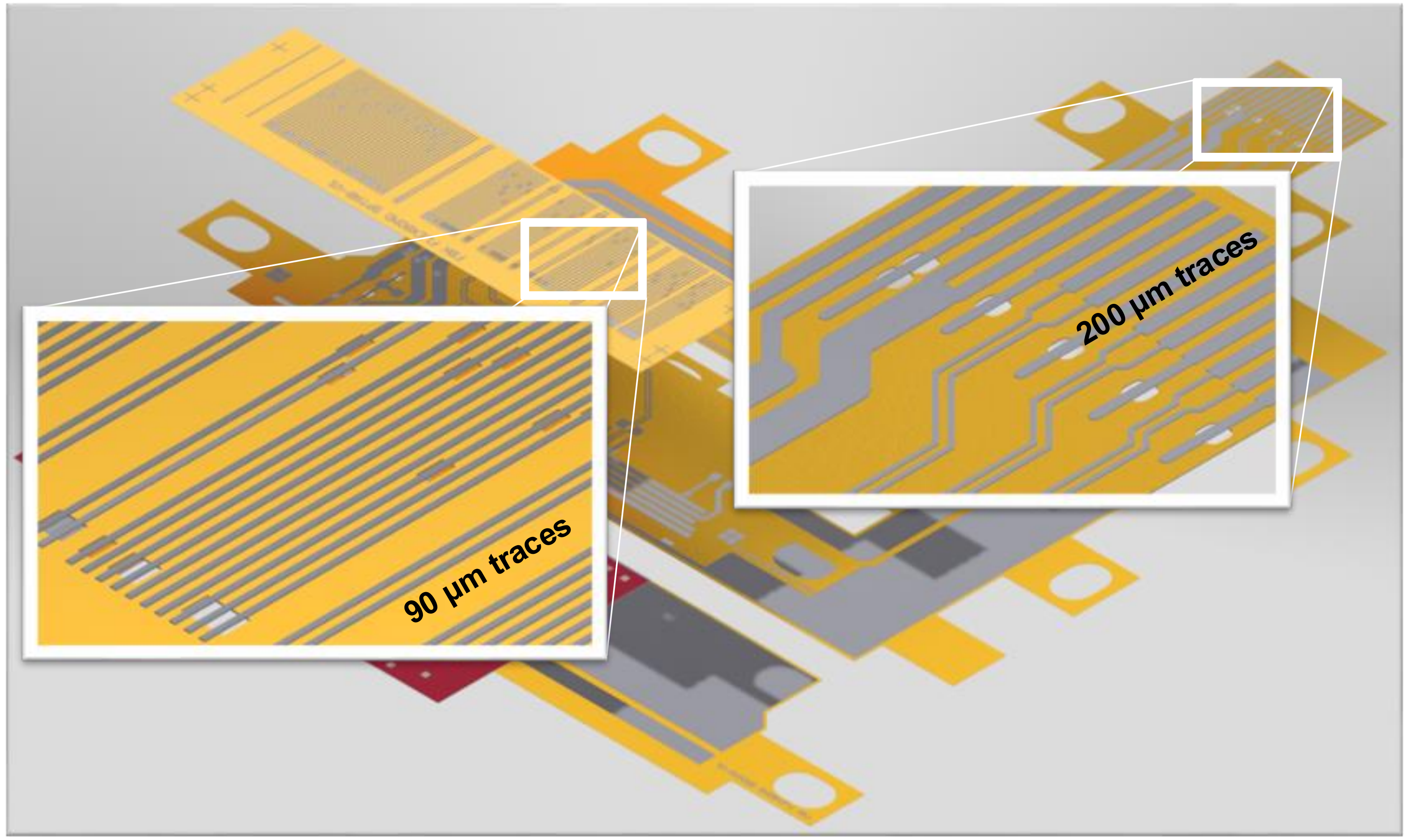

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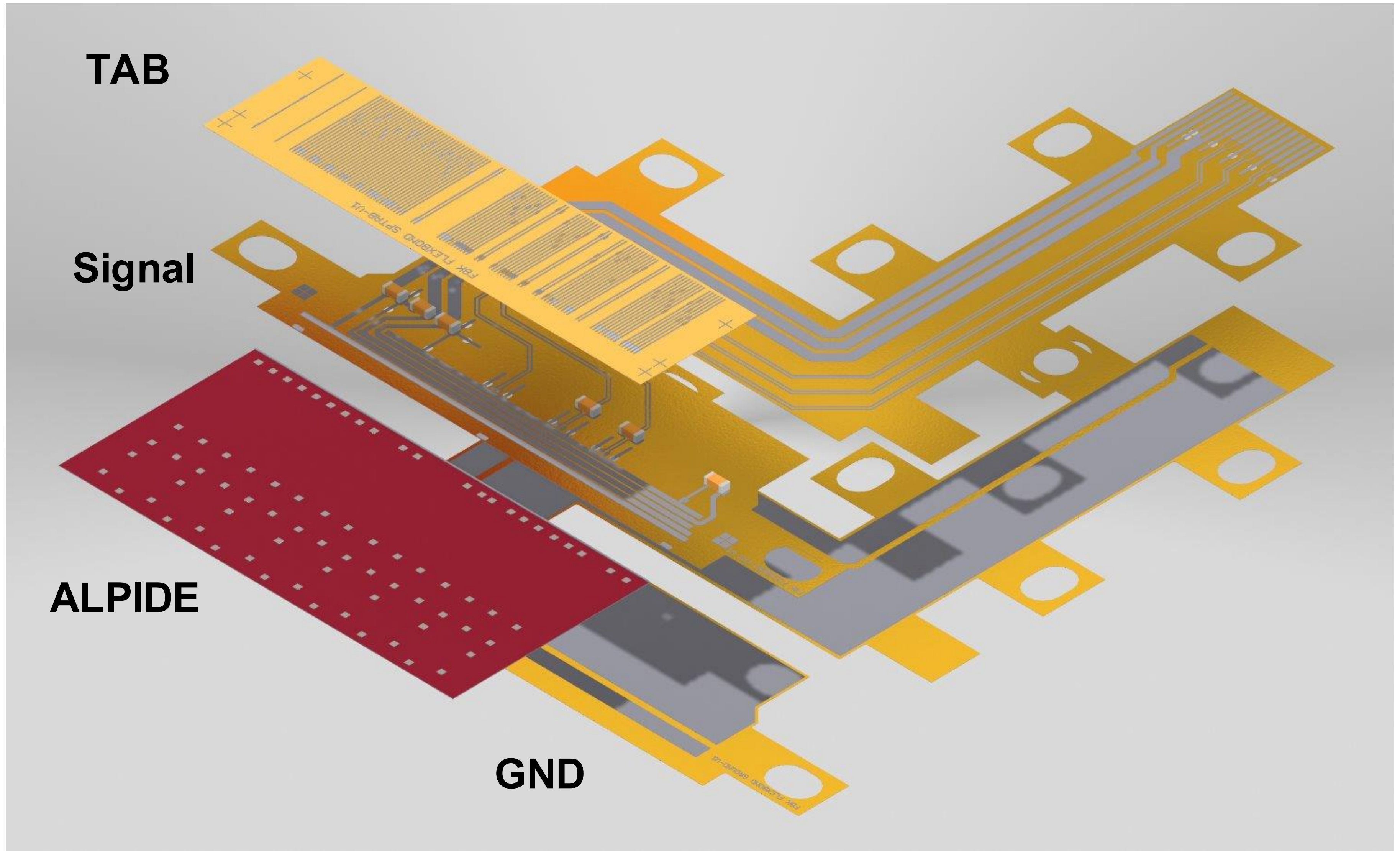

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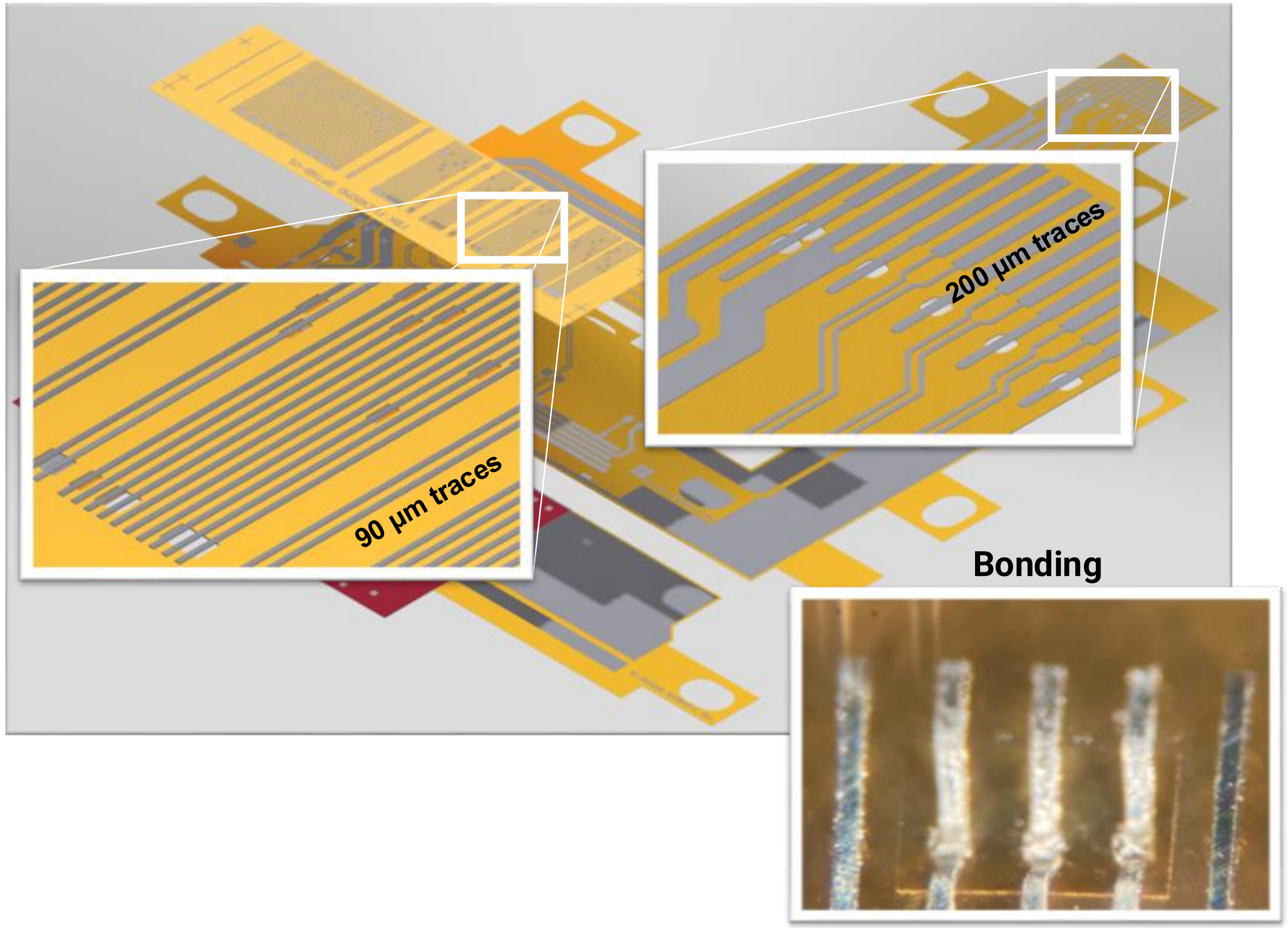

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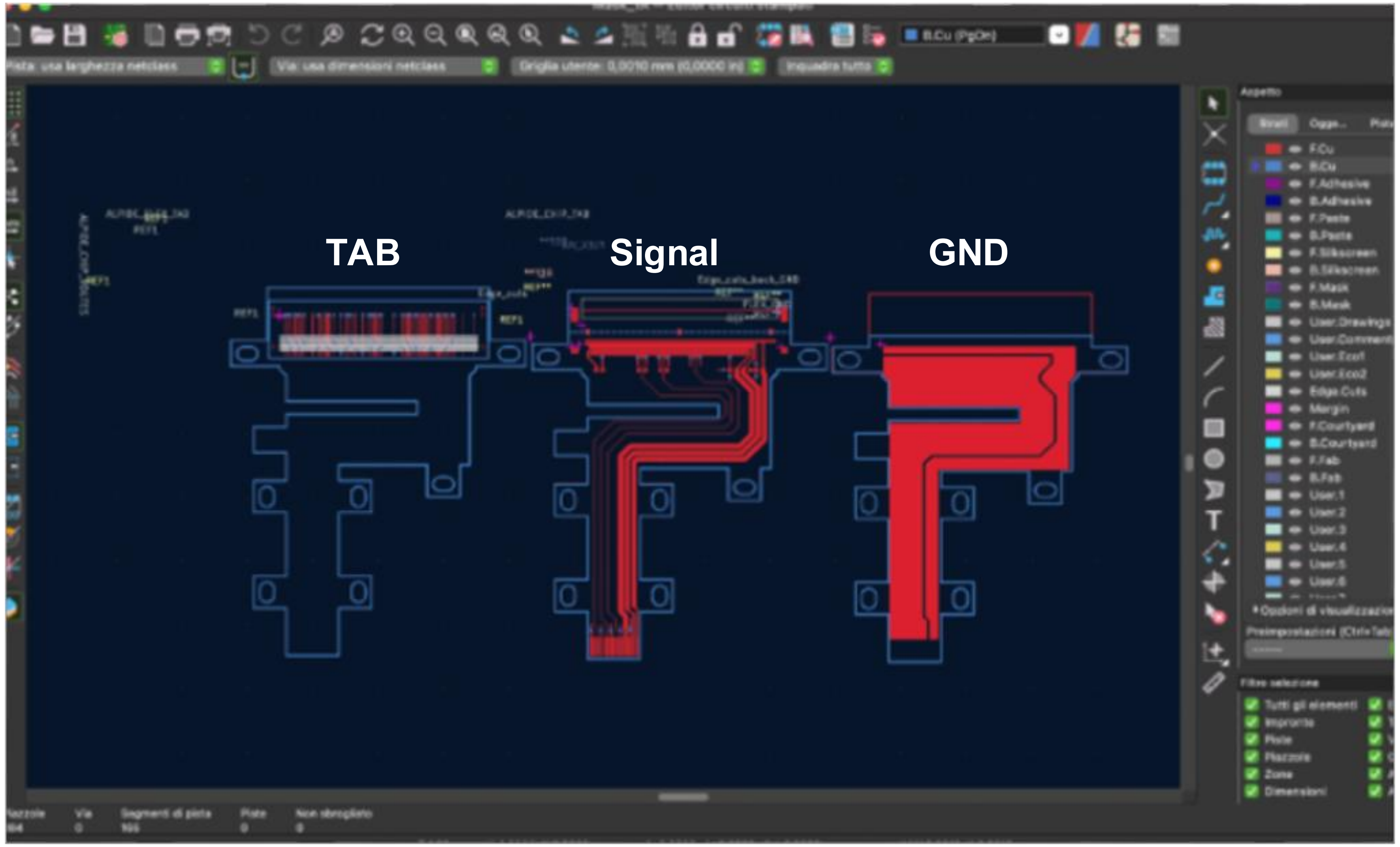
Low mass Aluminium Flex Platform
From KiCAD to KLayout design



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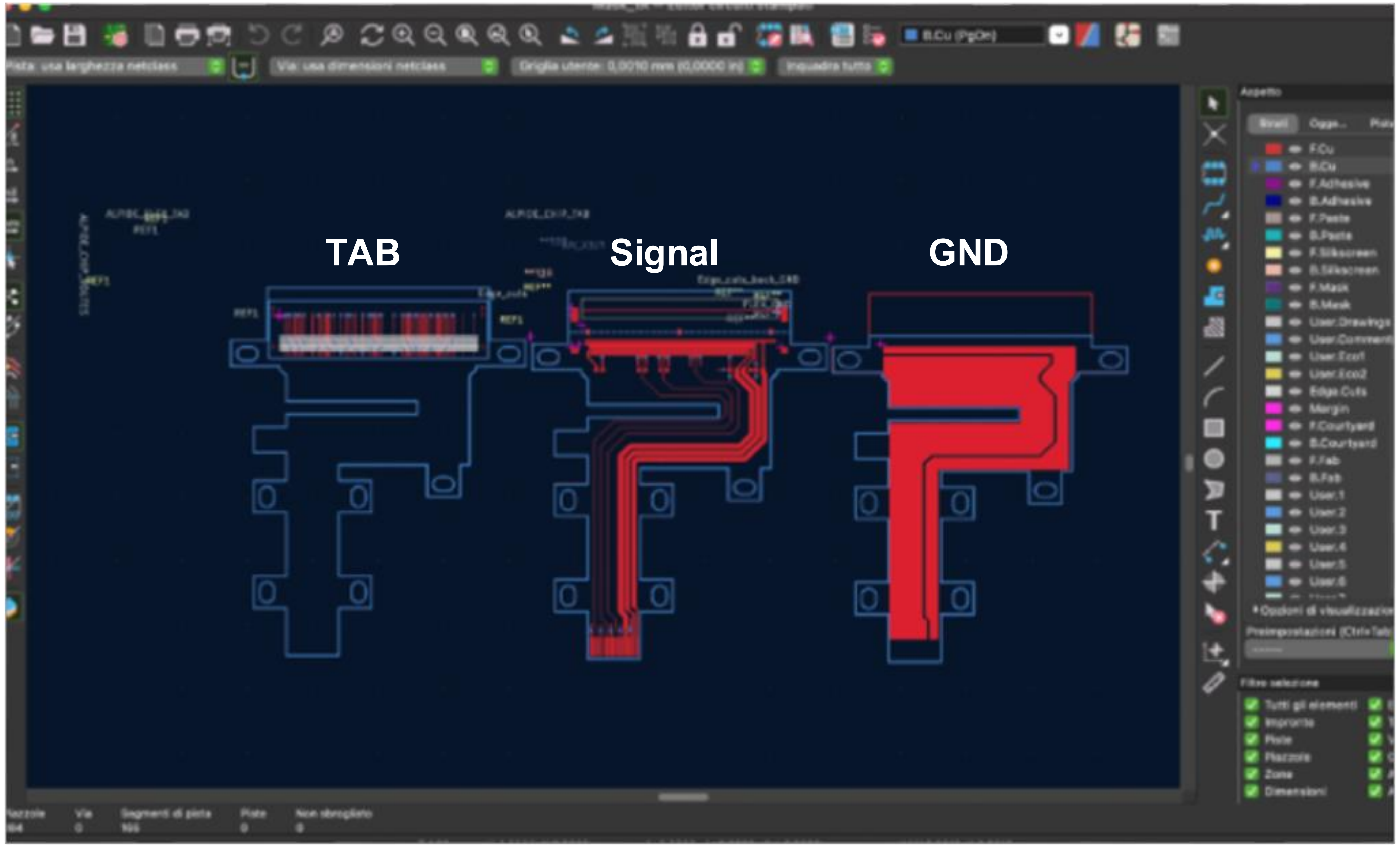
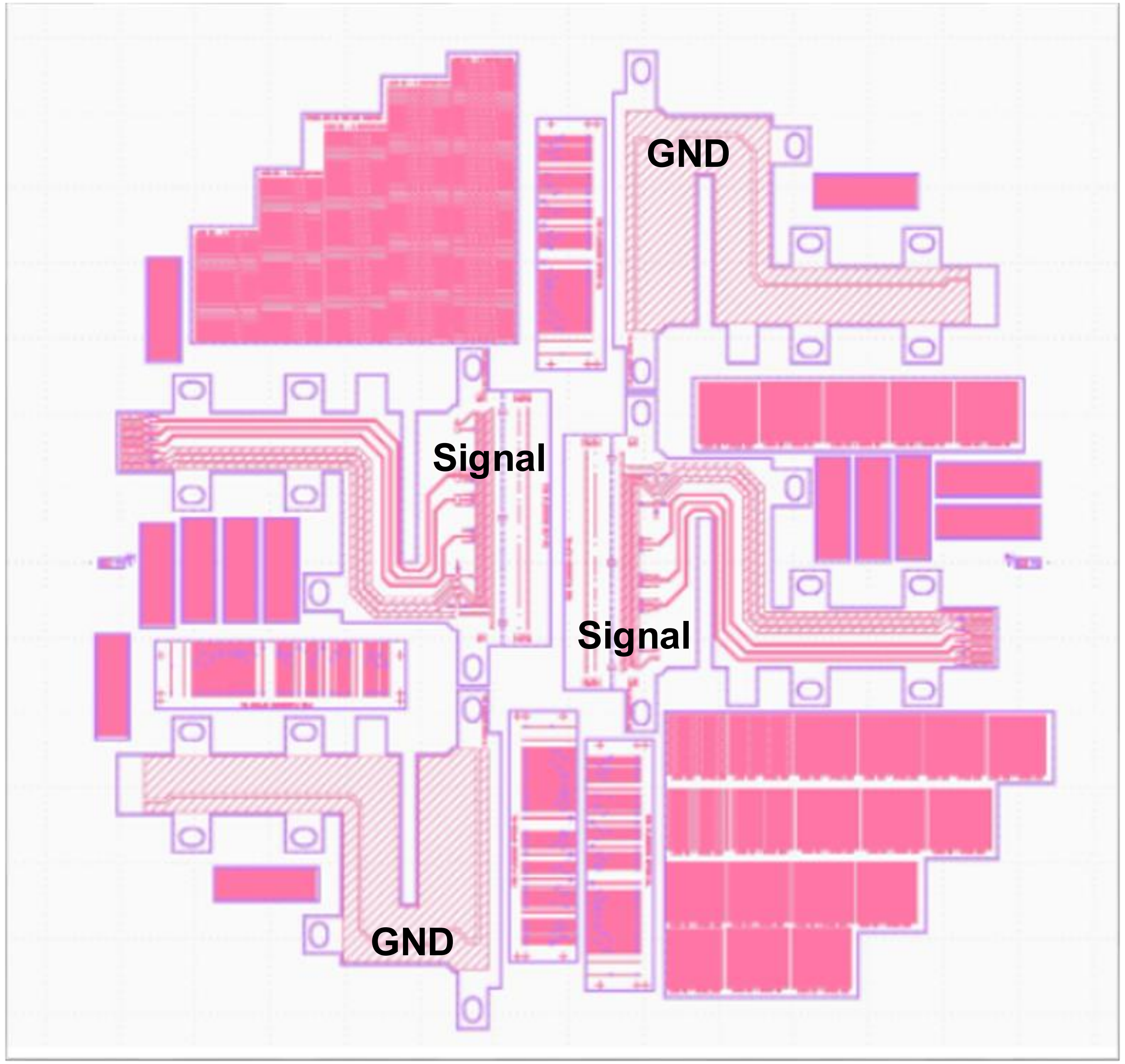
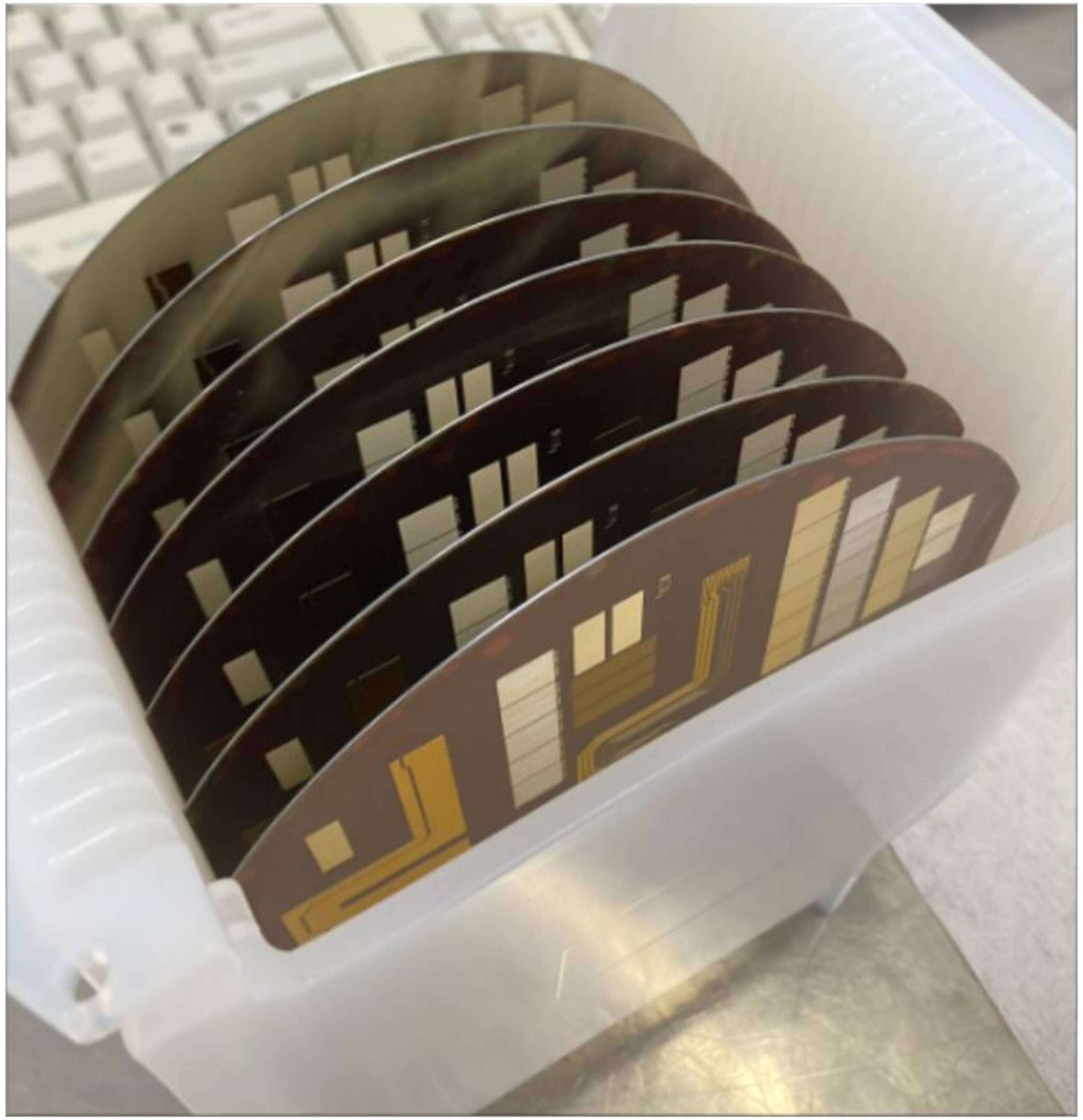




Low mass Aluminium Flex Platform
Wafer-level manufacturing



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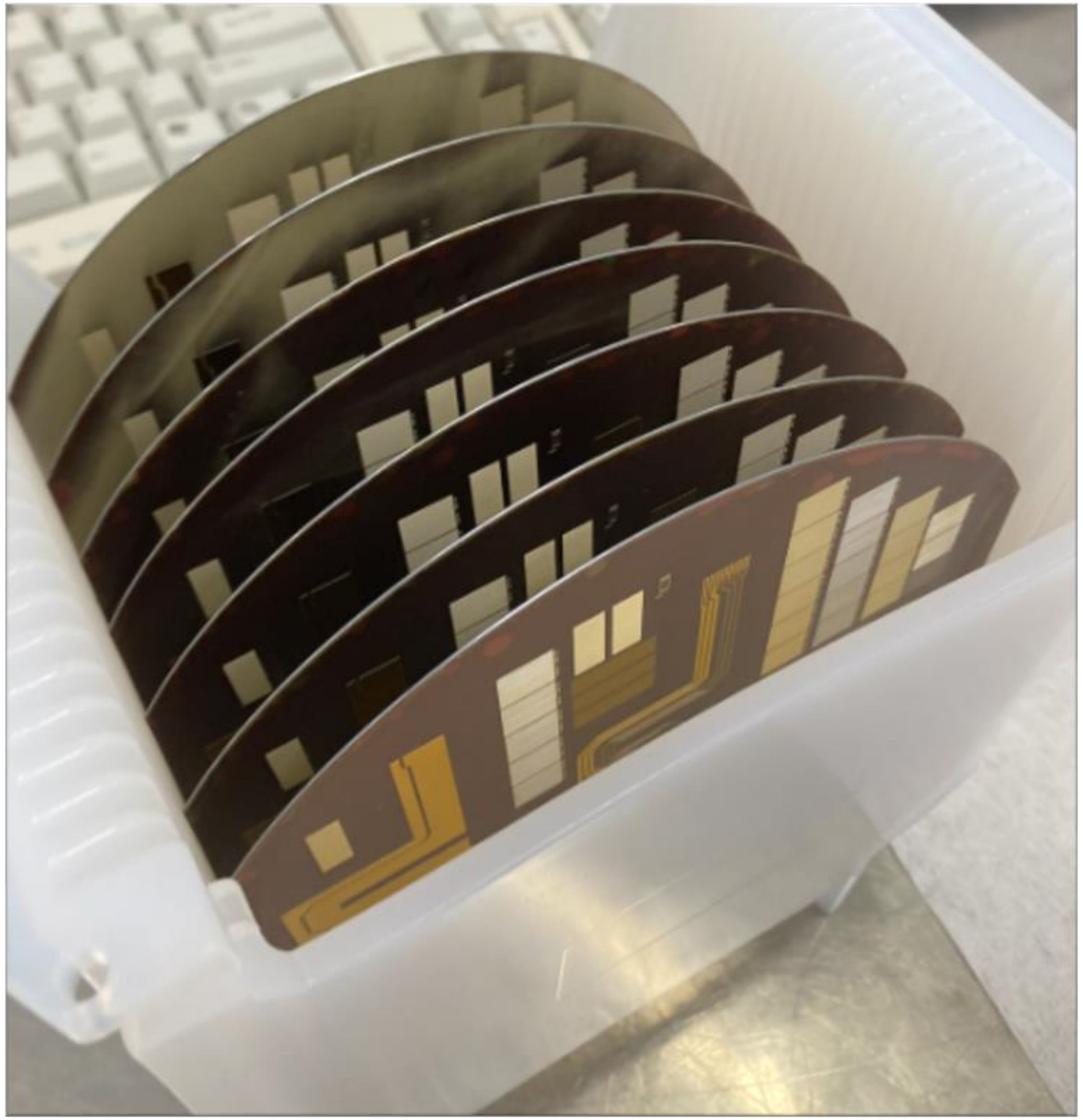
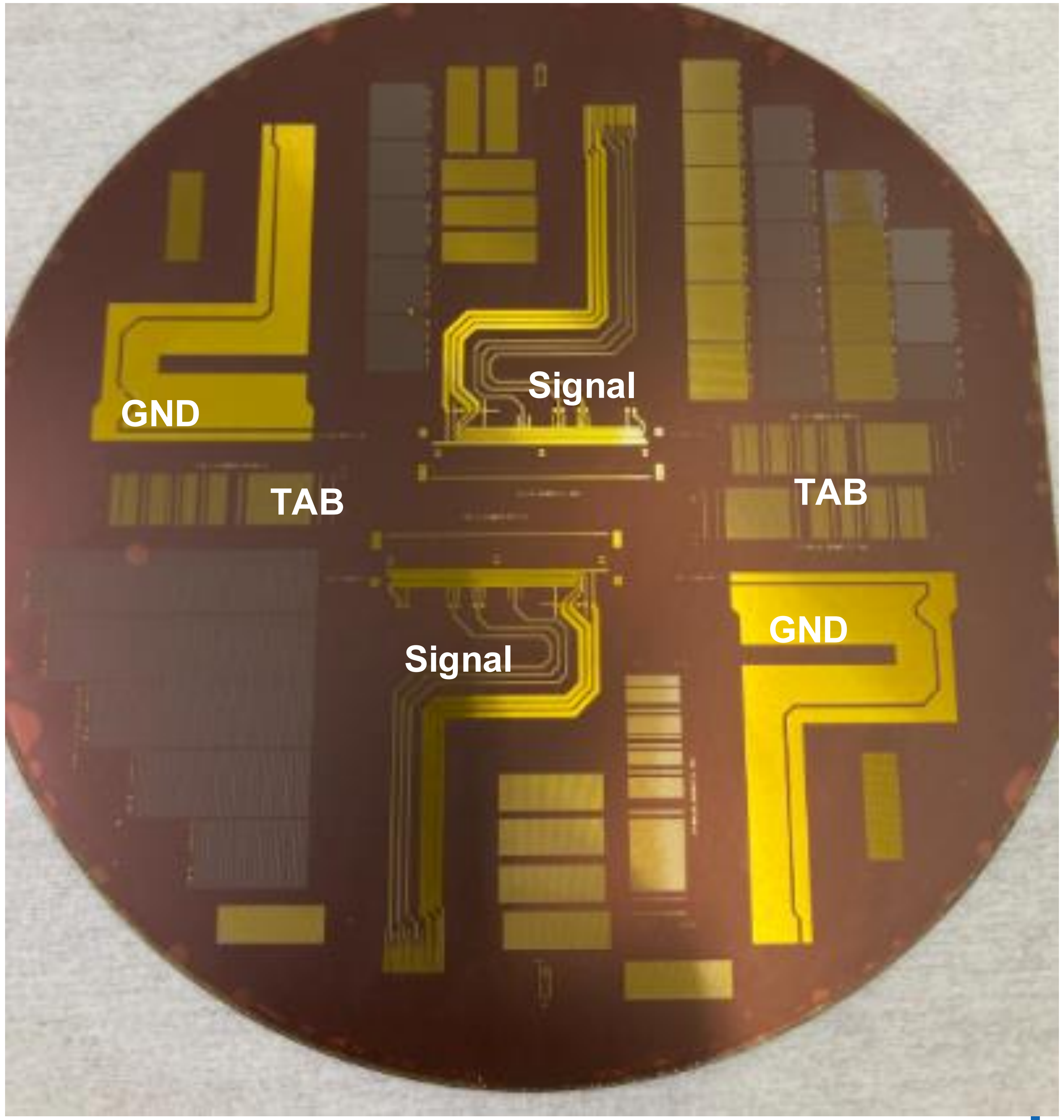
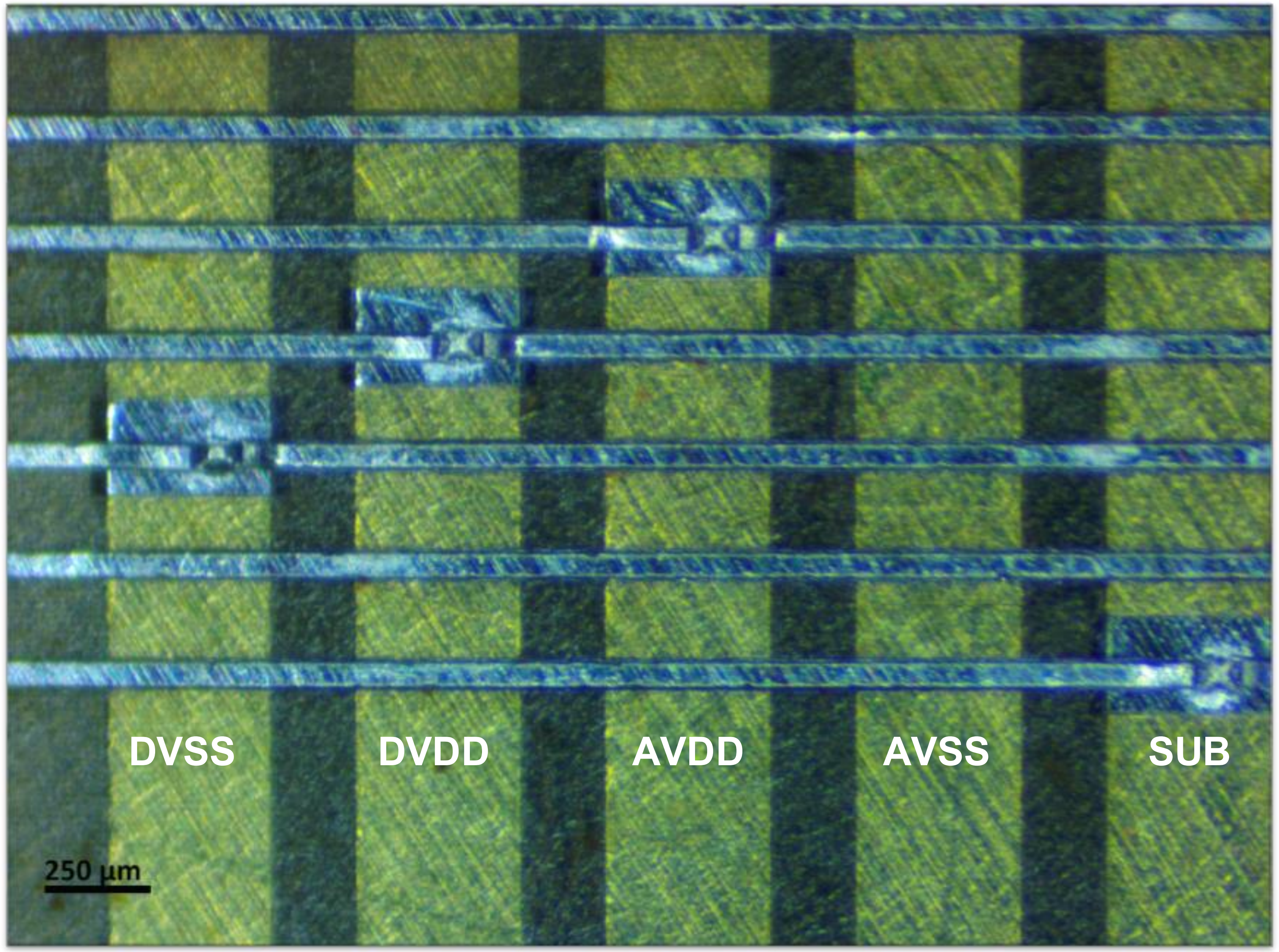
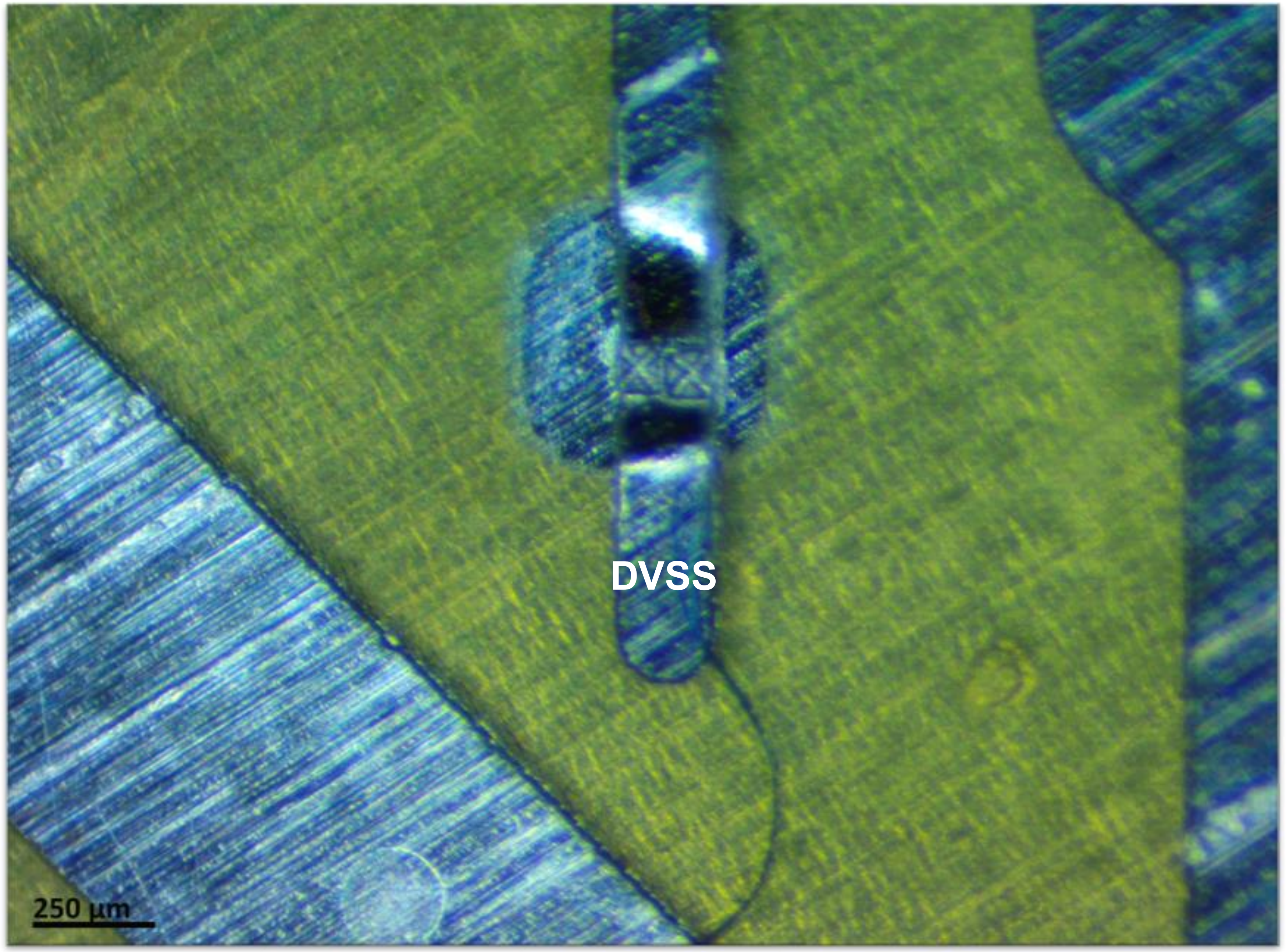


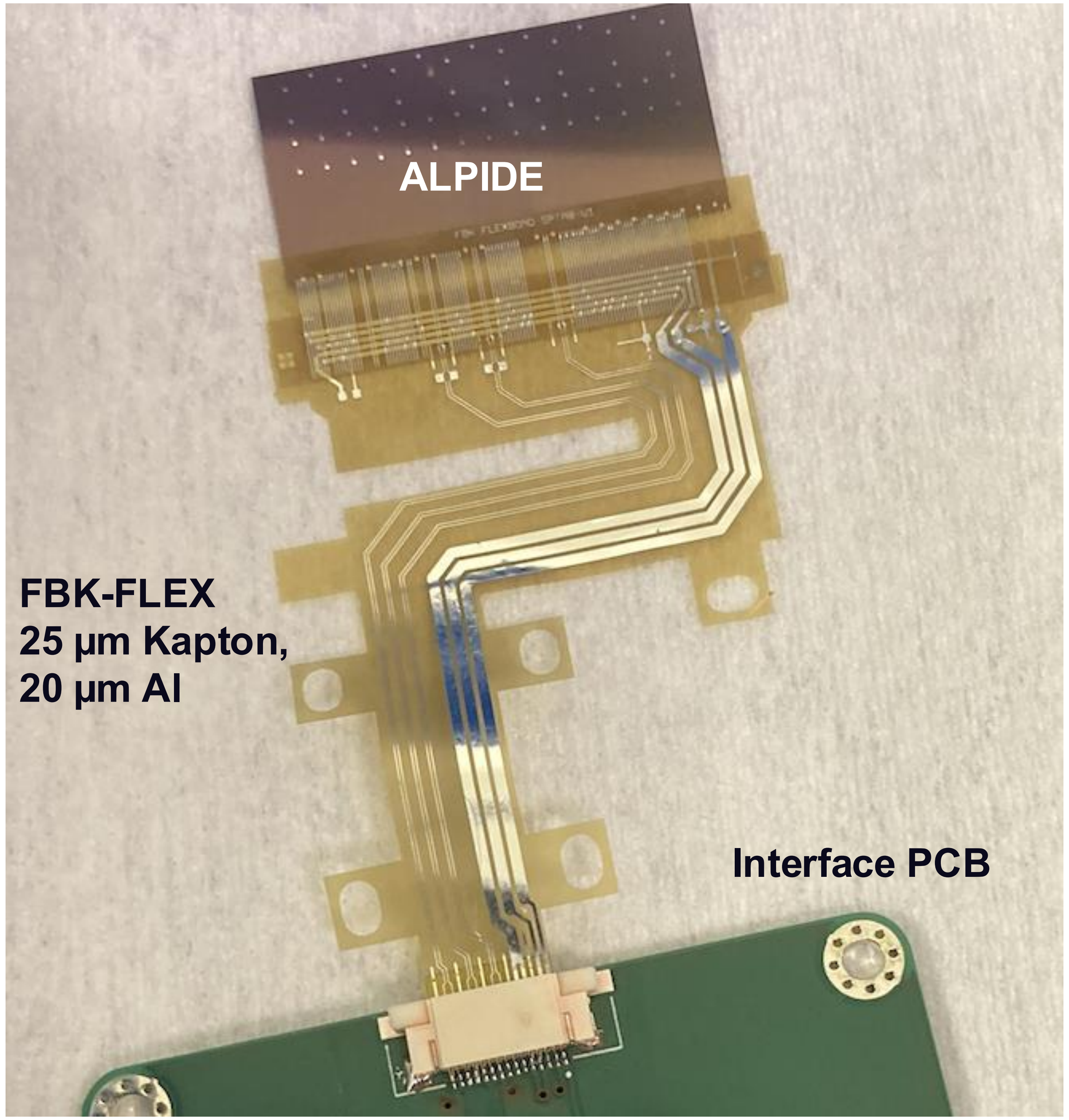


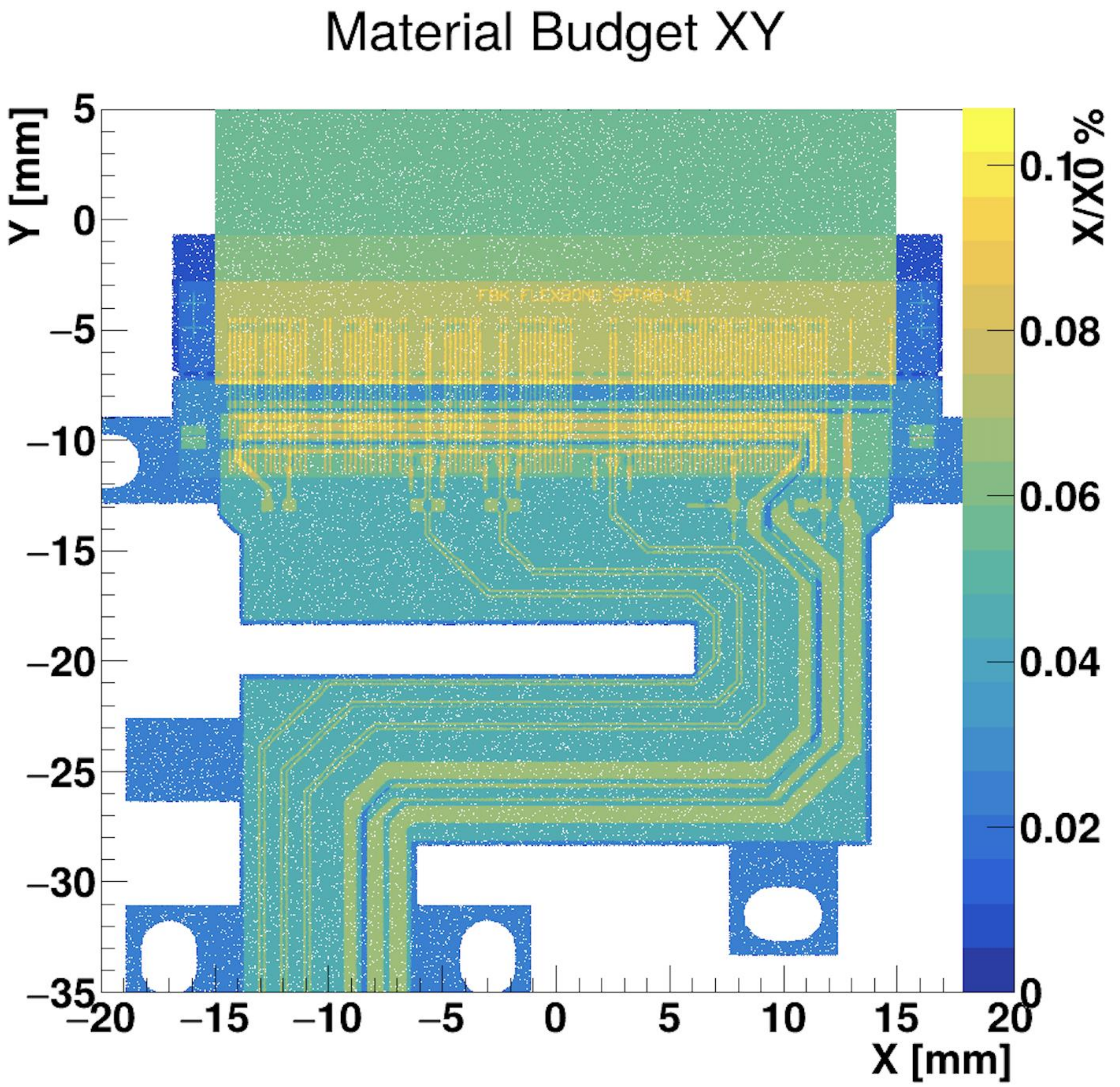
Low mass Aluminium Flex Platform
Single Point Tape Automated Bonding



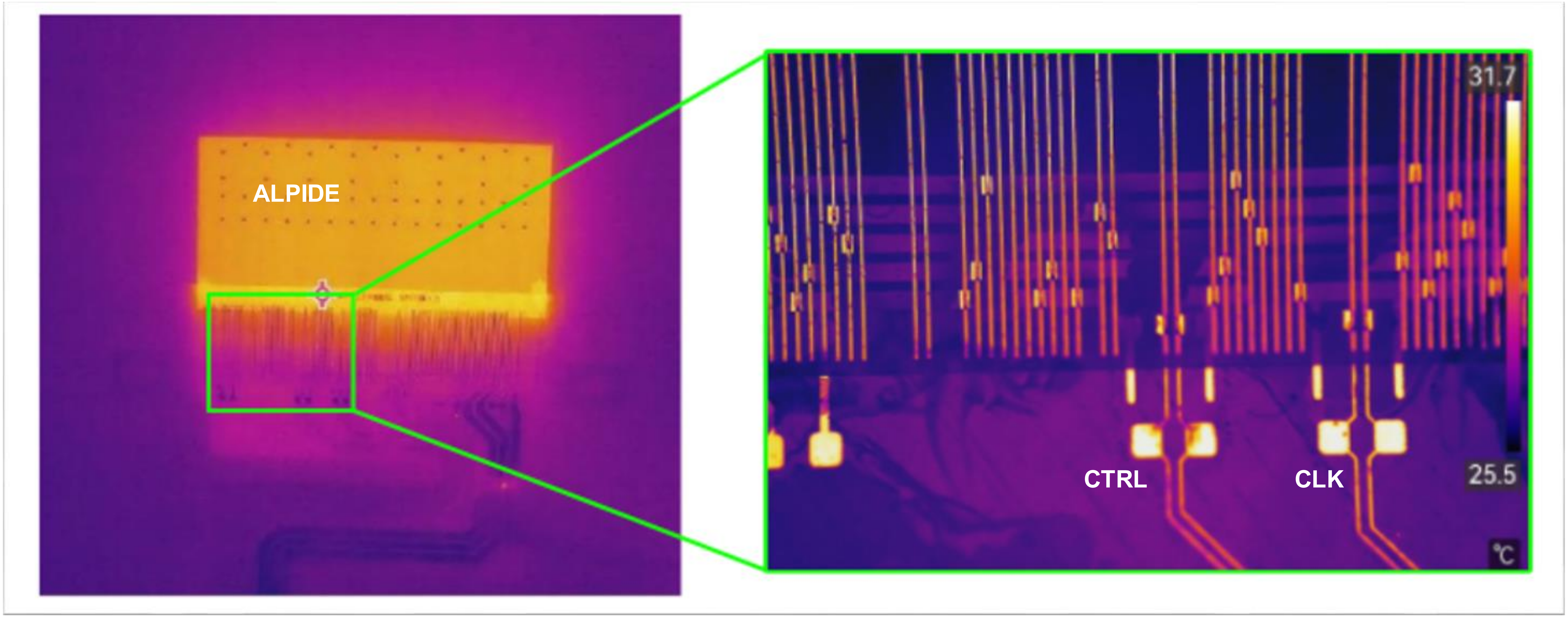


Low mass Aluminium Flex Platform
Final PCB and Material Budget





Low mass Aluminium Flex Platform
Electrical/thermal testing on ~50 samples



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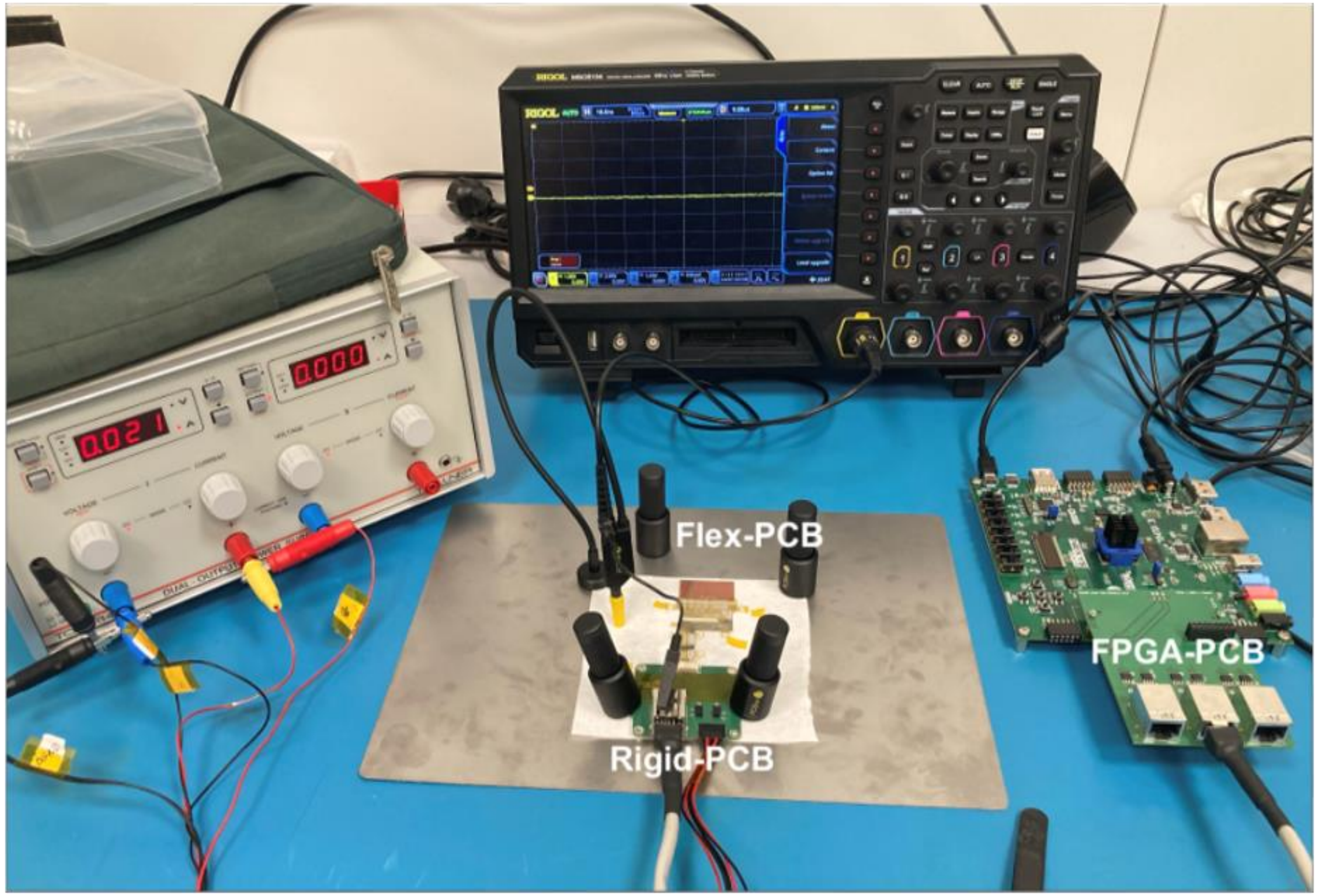
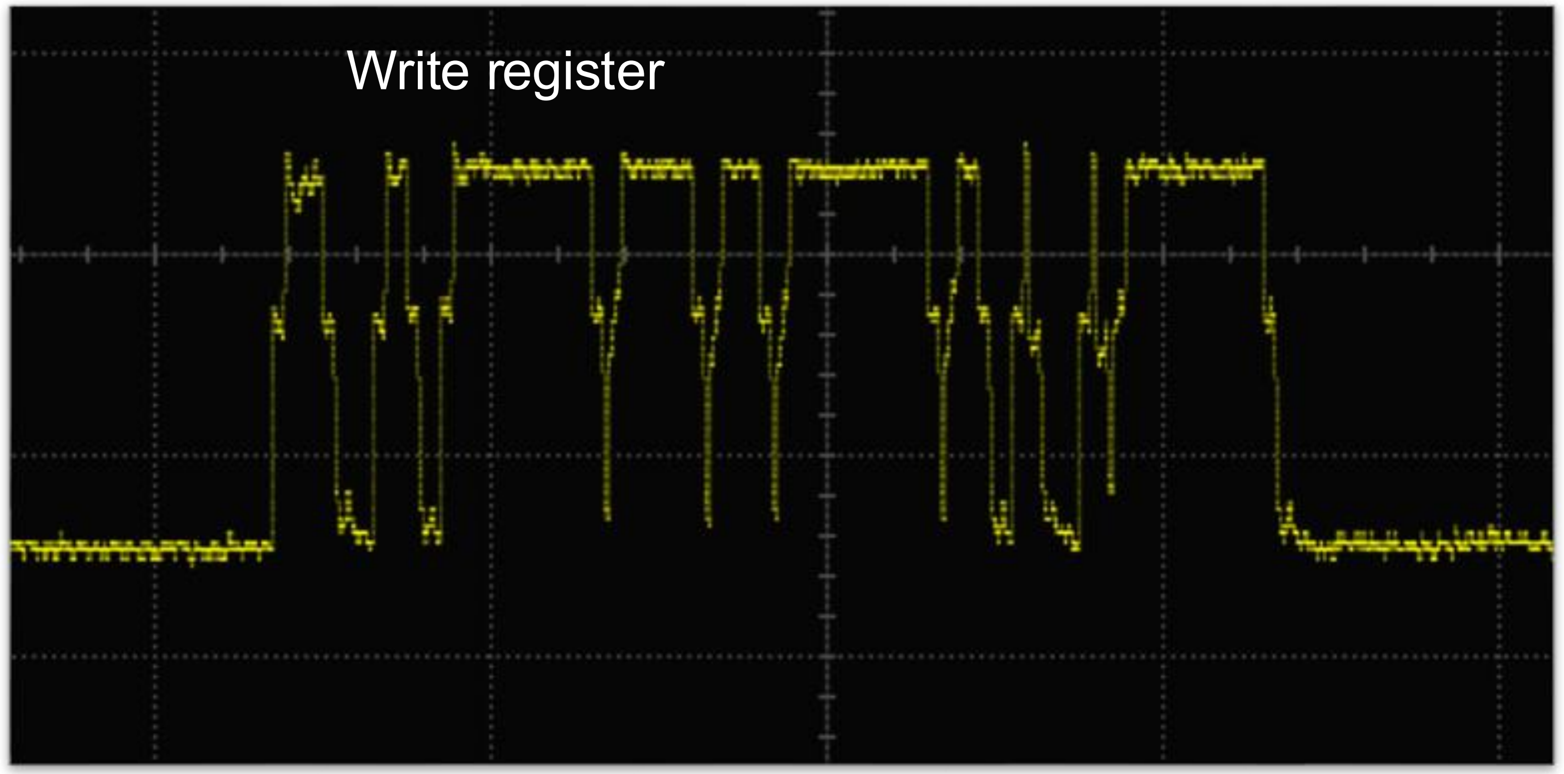
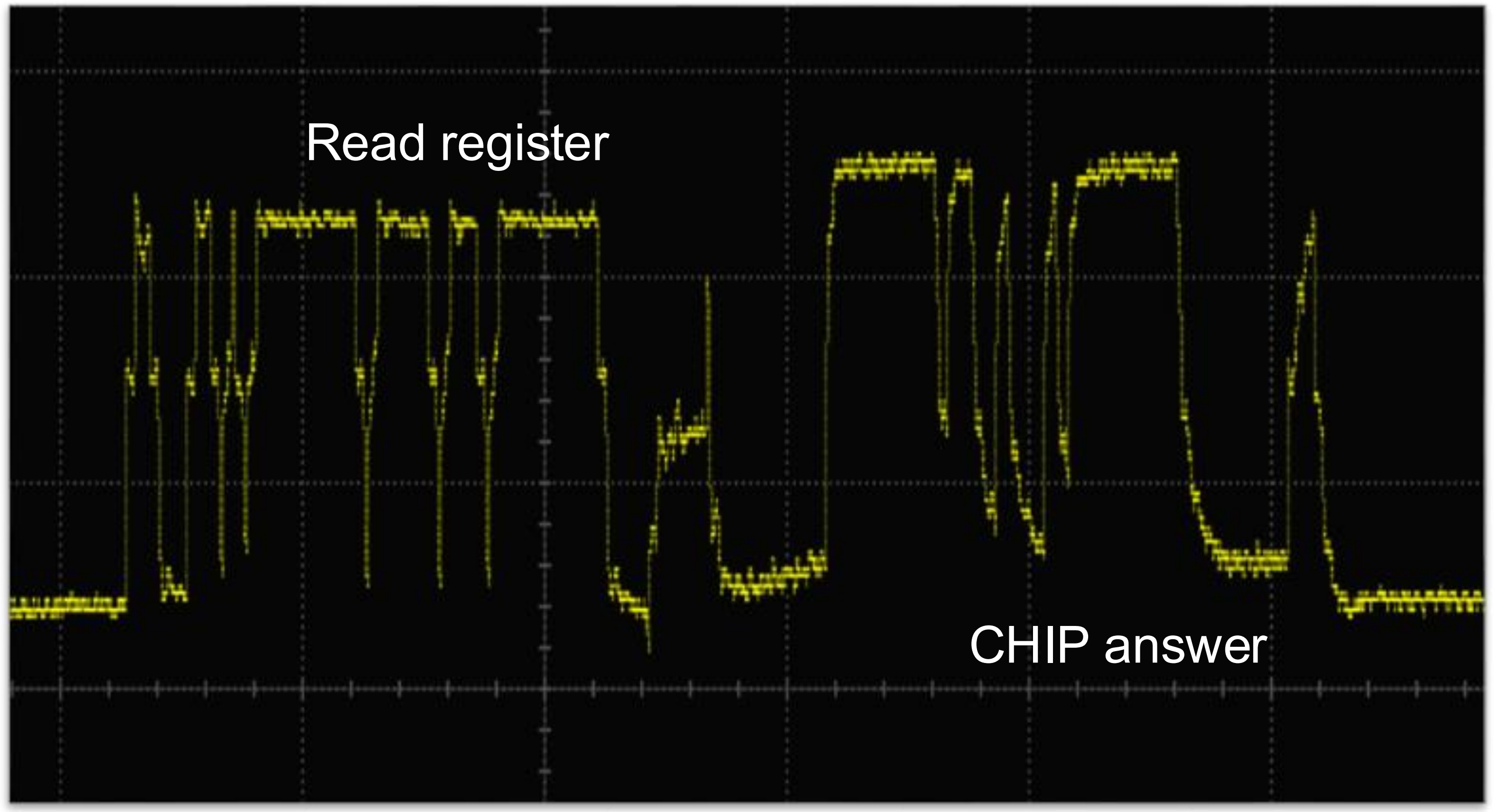
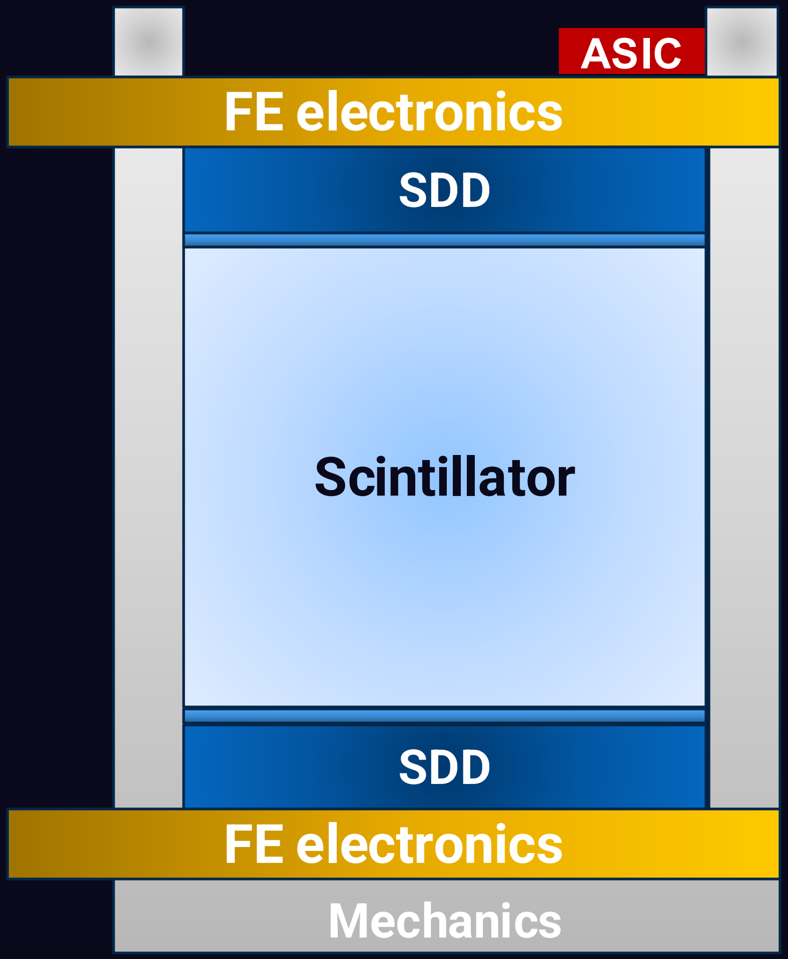


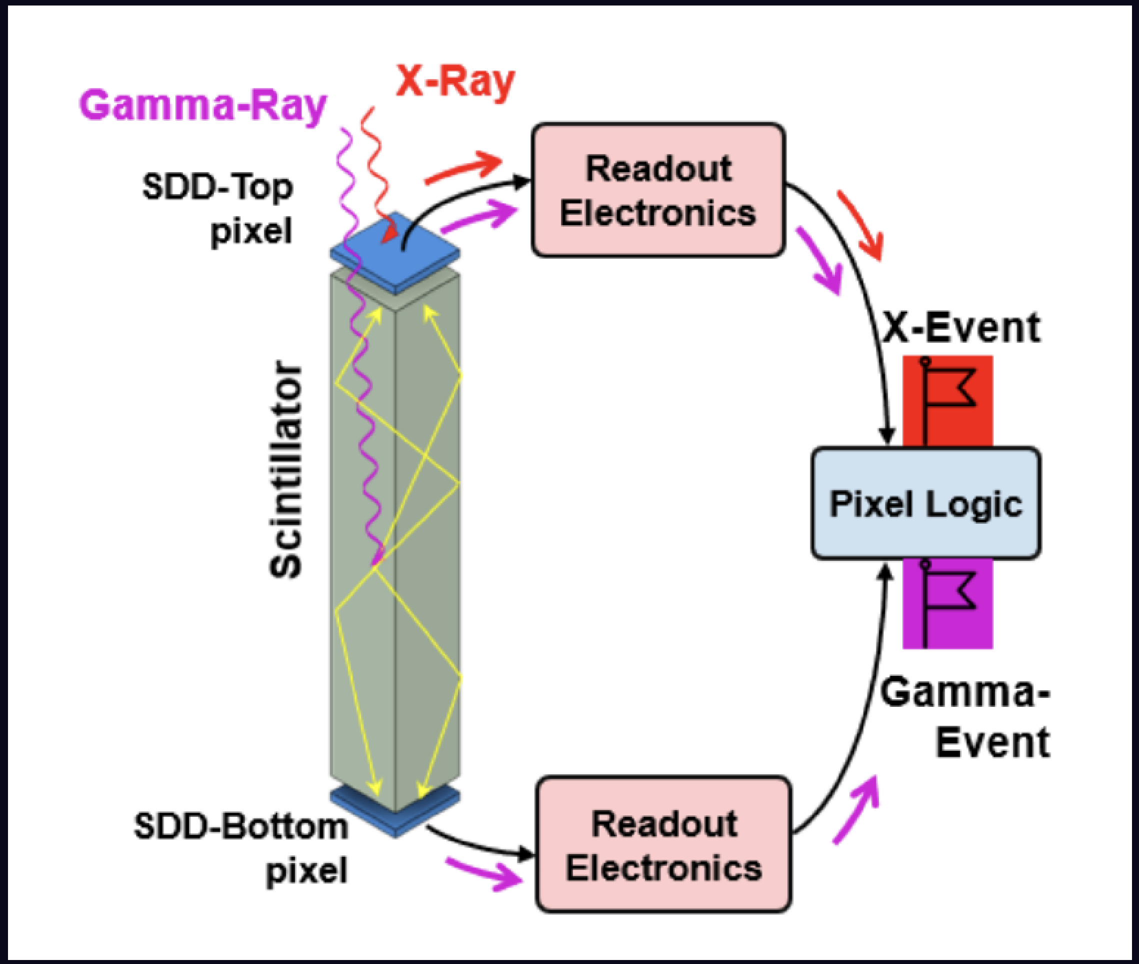


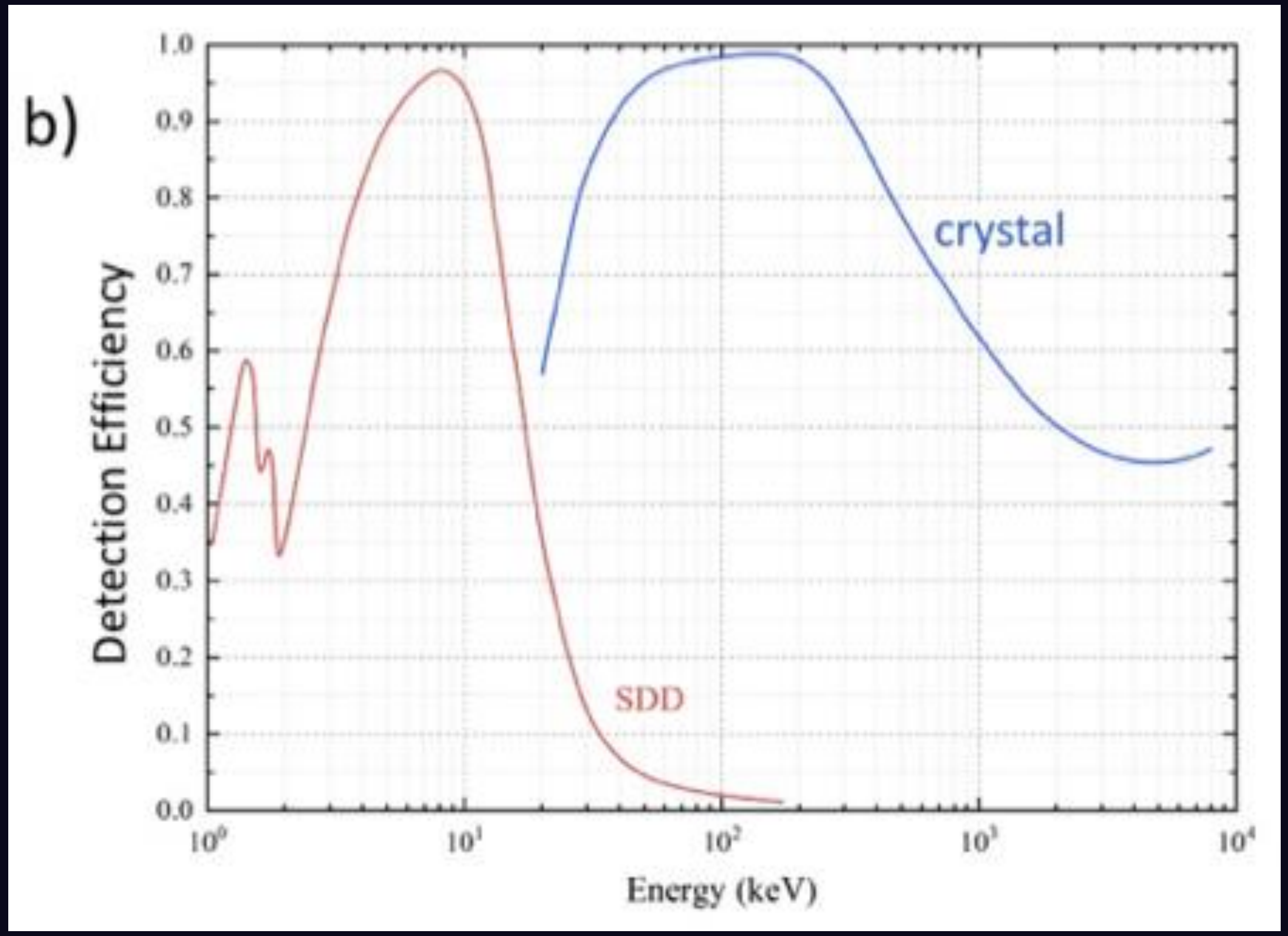


2x2 detector system for X-ray and γ detection

Developed by the REDSOX Collaboration [1]







[1] Front. Detect. Sci. Technol 3:1551757. doi: 10.3389/fdest.2025.1551757
[2] S. Srivastava et al 2024 JINST 19 C02005

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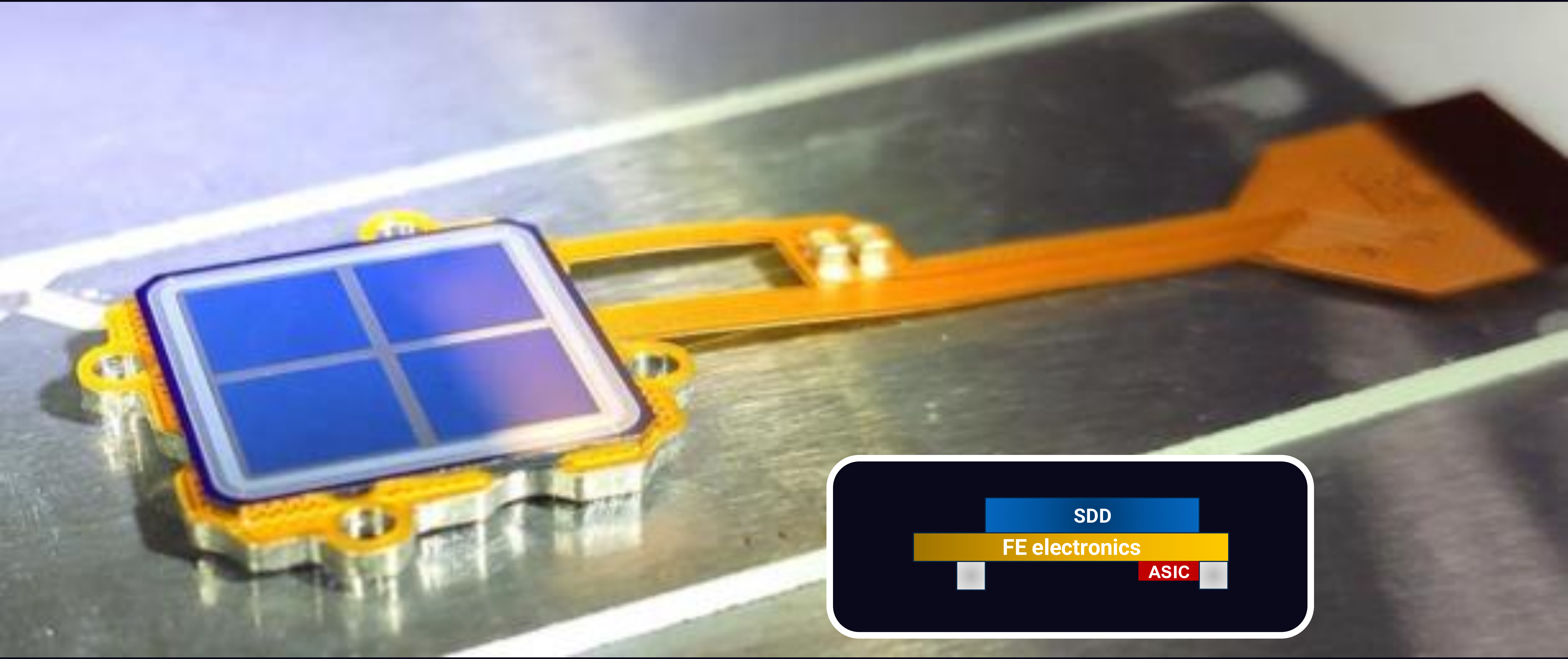
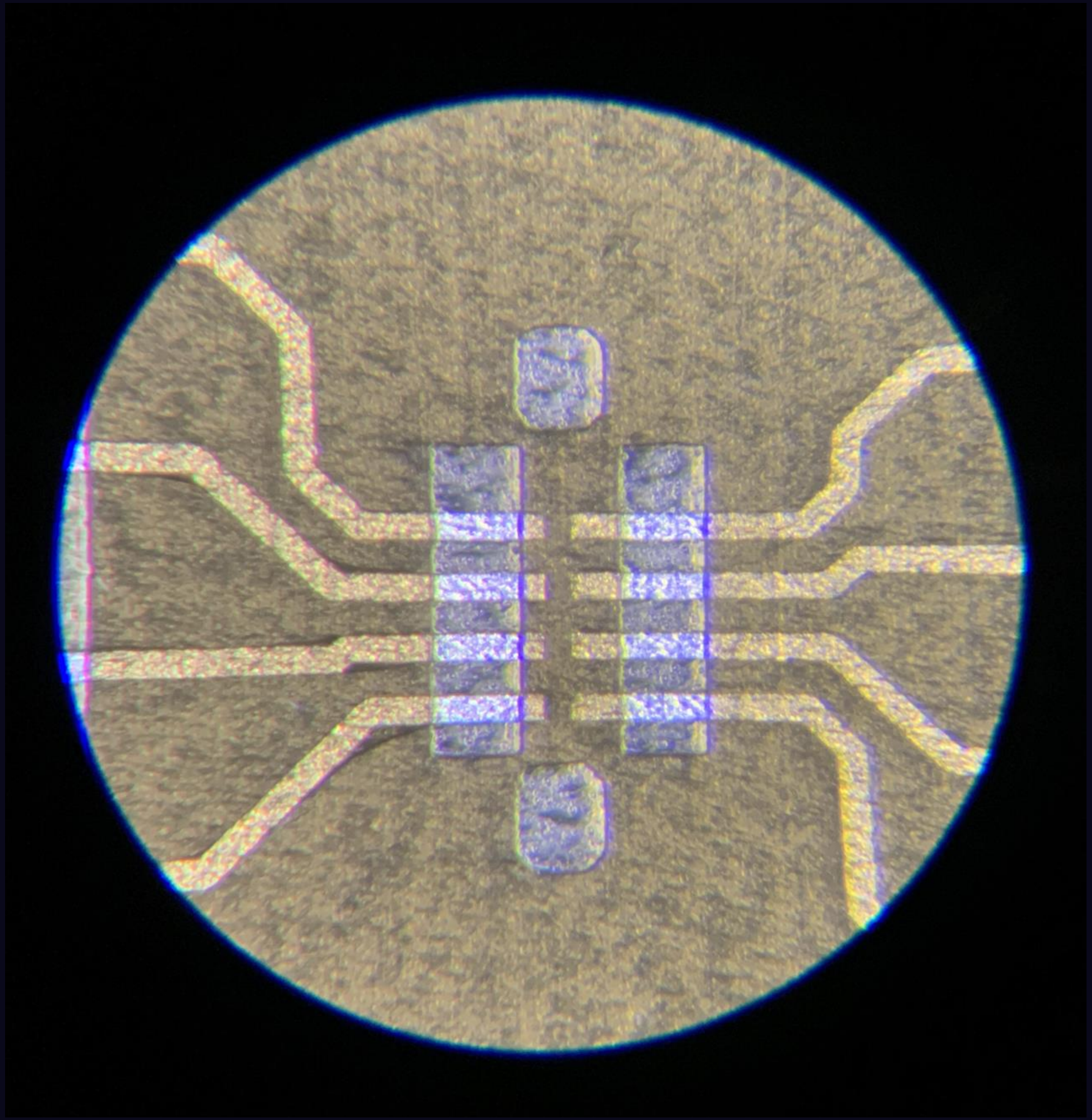
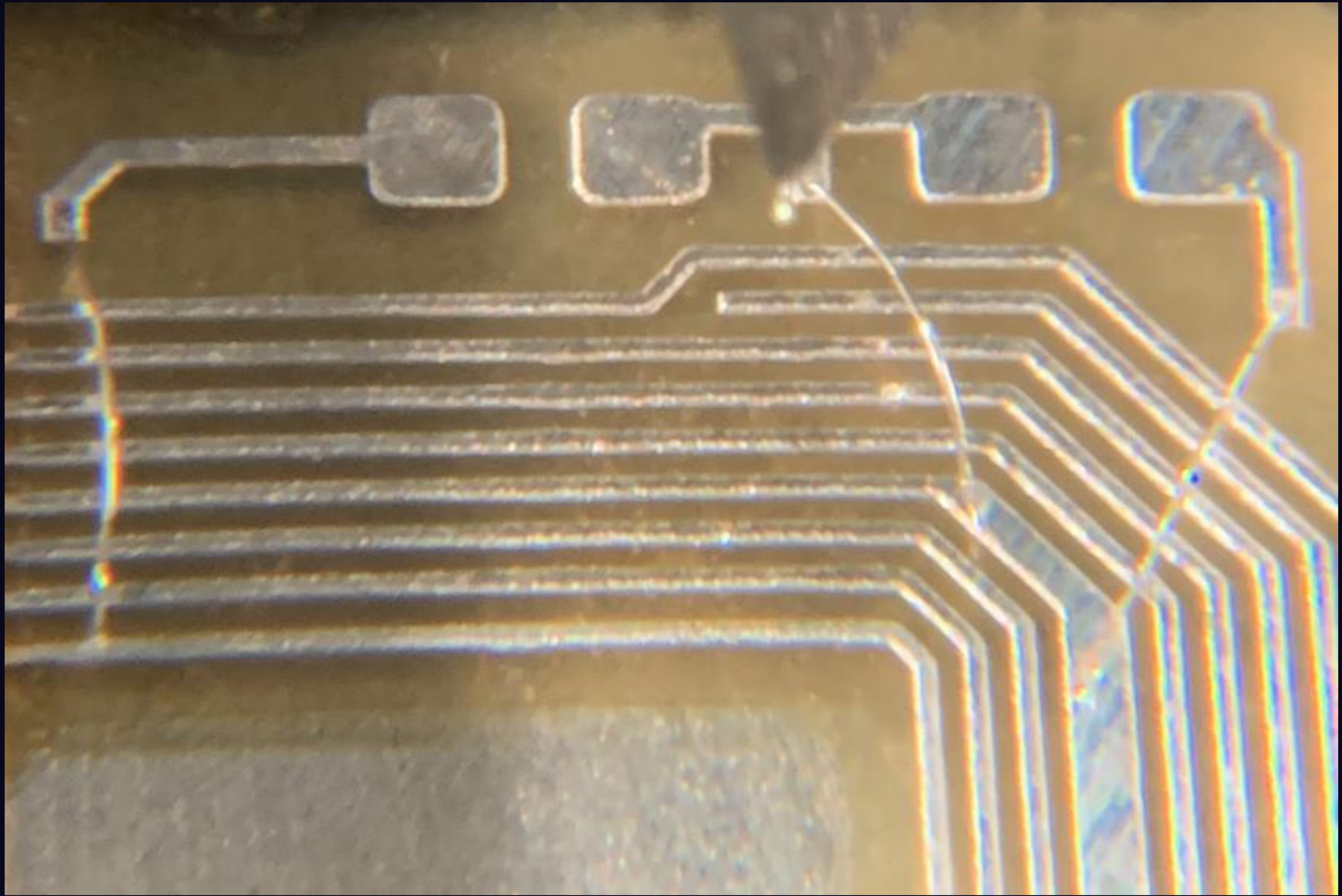


Courtesy of E. Demenev

spTAB?

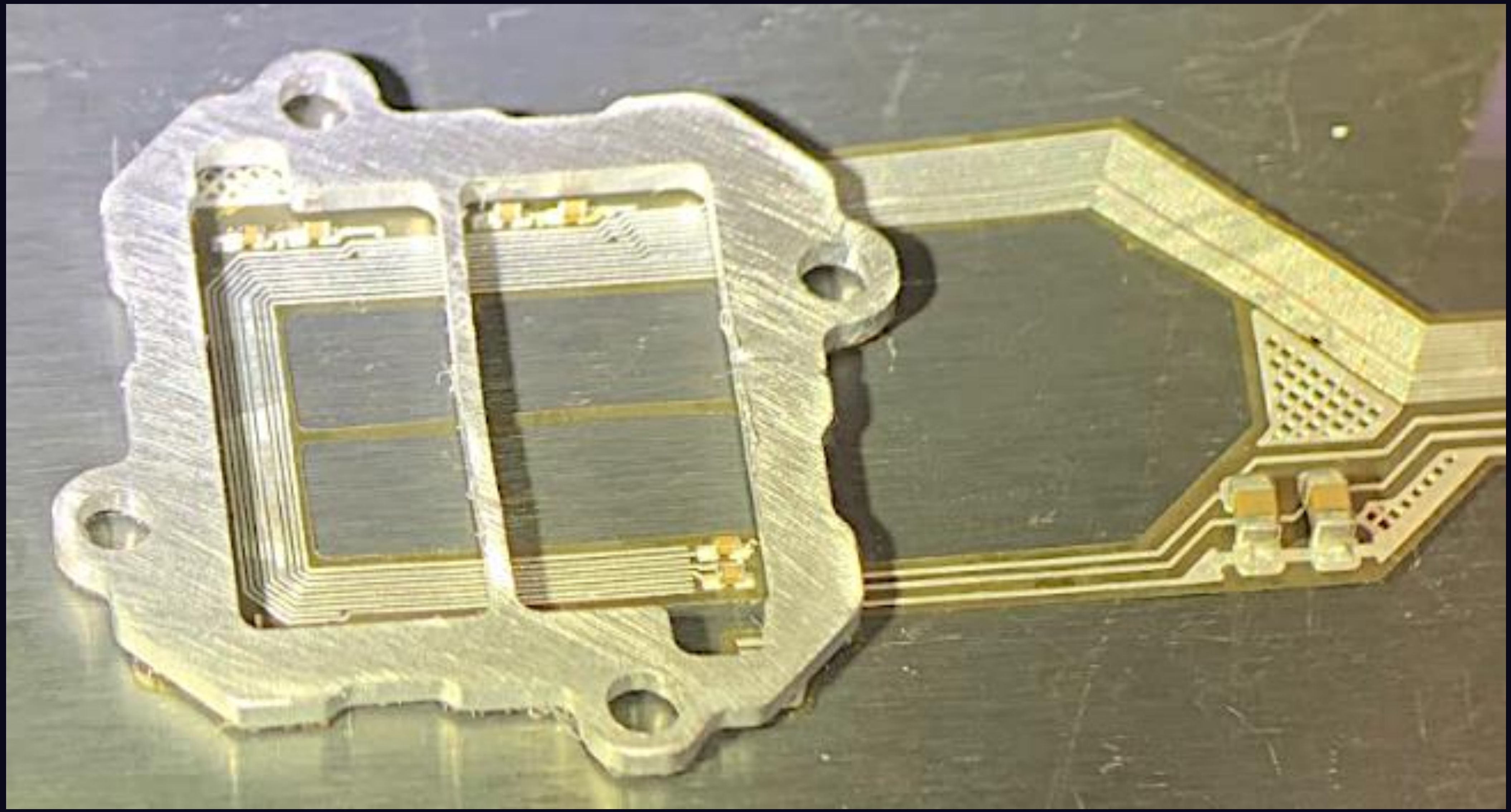


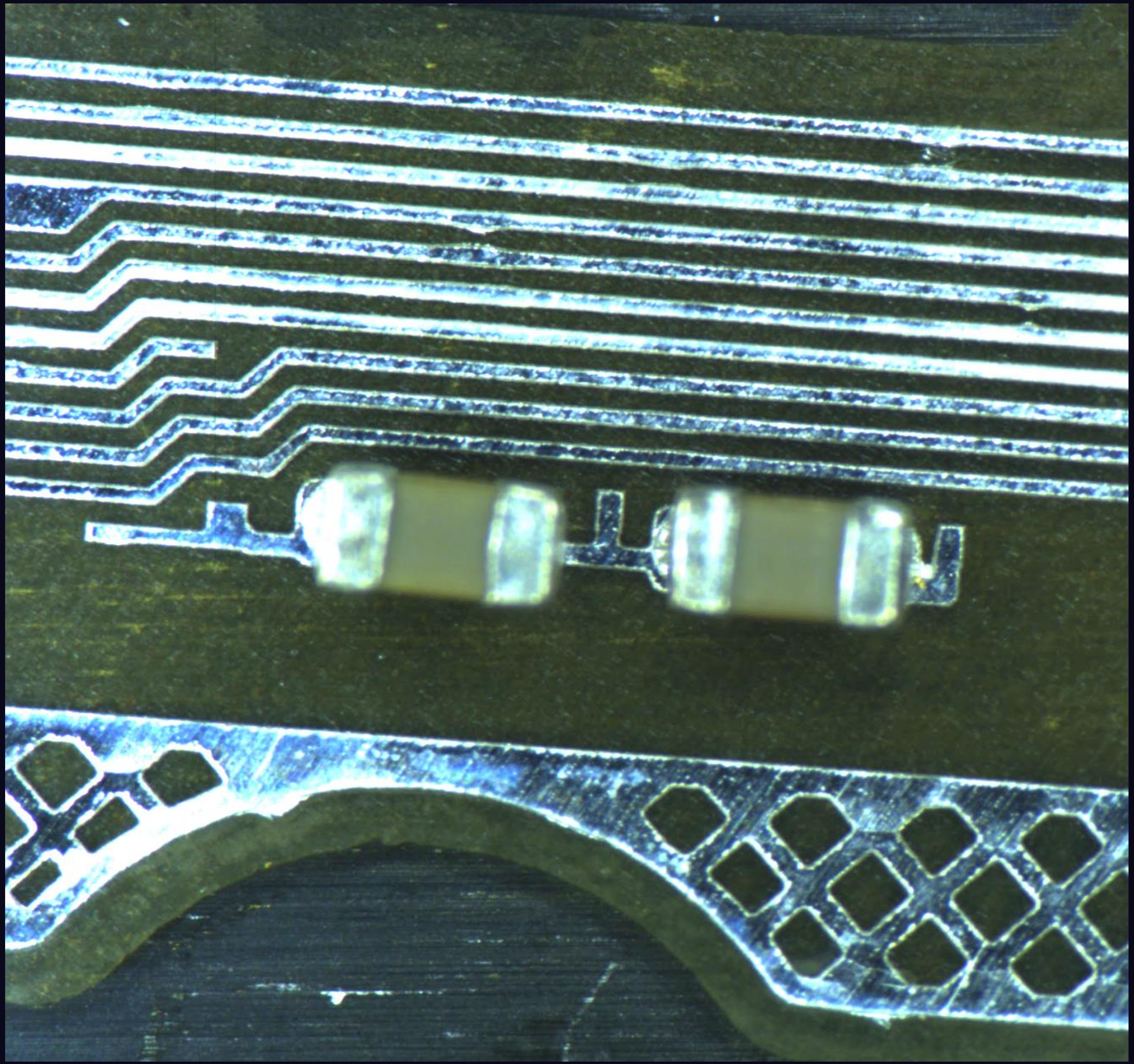
Wire bonding?



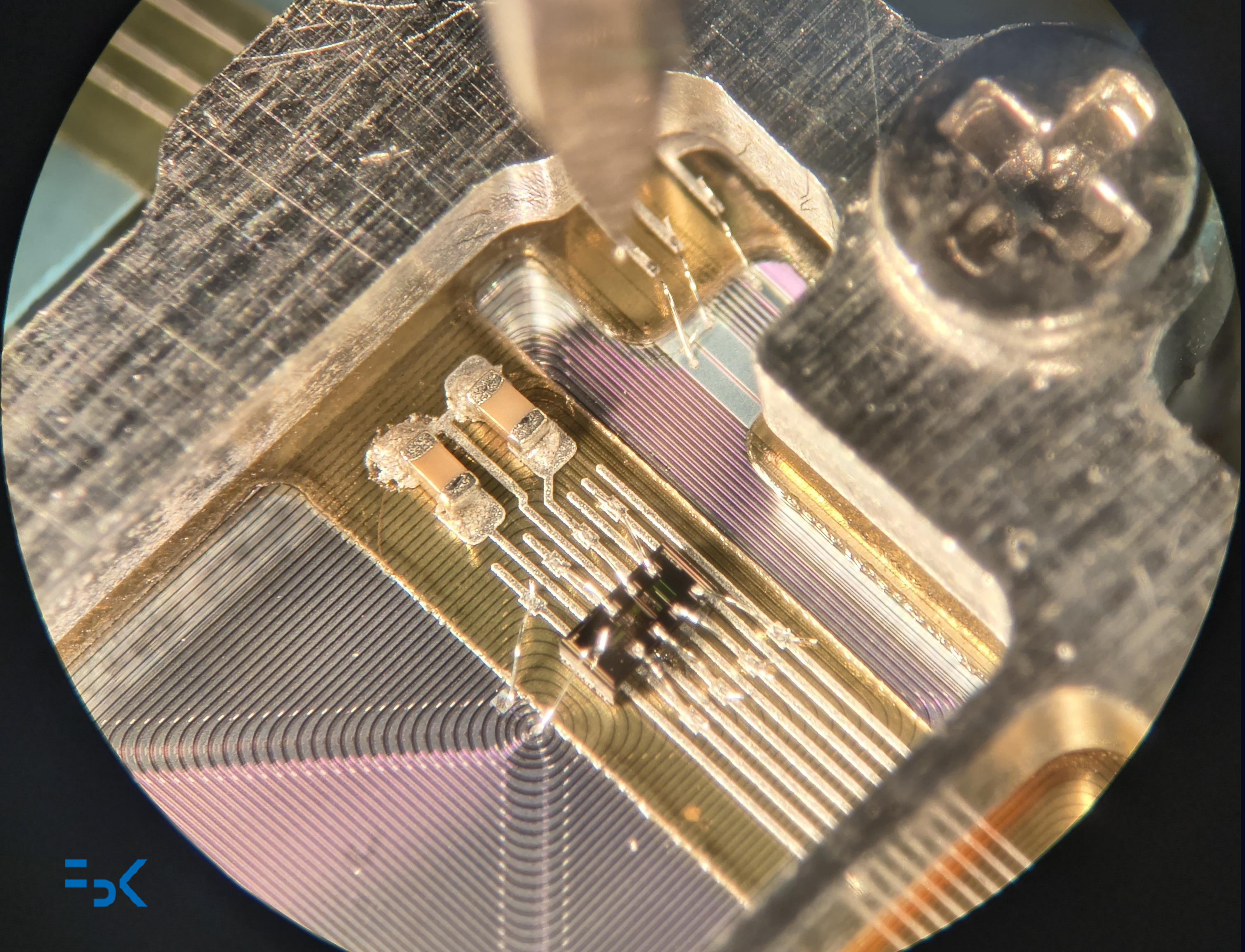
Both are compatible with FBK Low X/X_0 Flex Tech

Can SMDs be mounted?





Yes



A compact self-standing detector system

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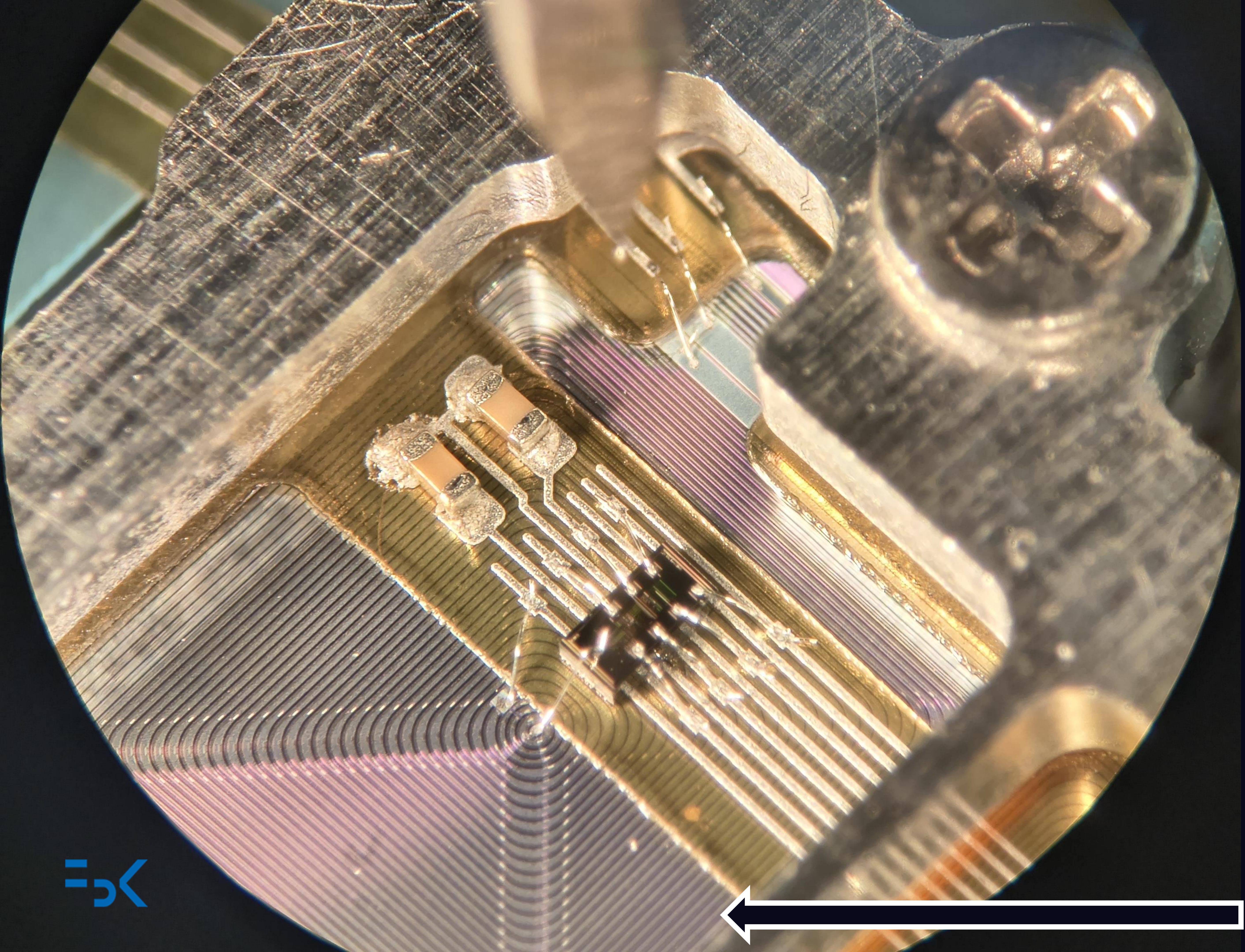
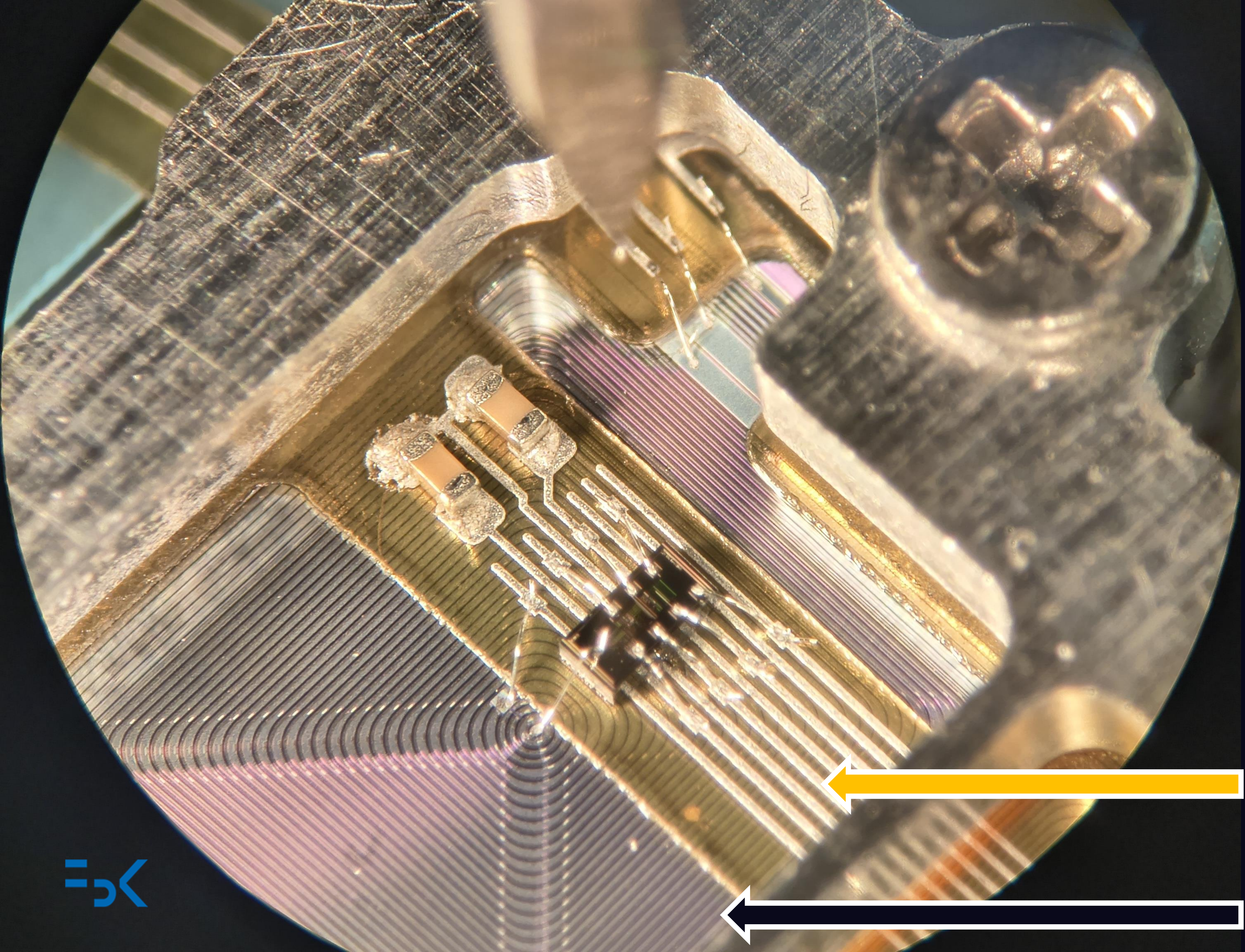


SDD

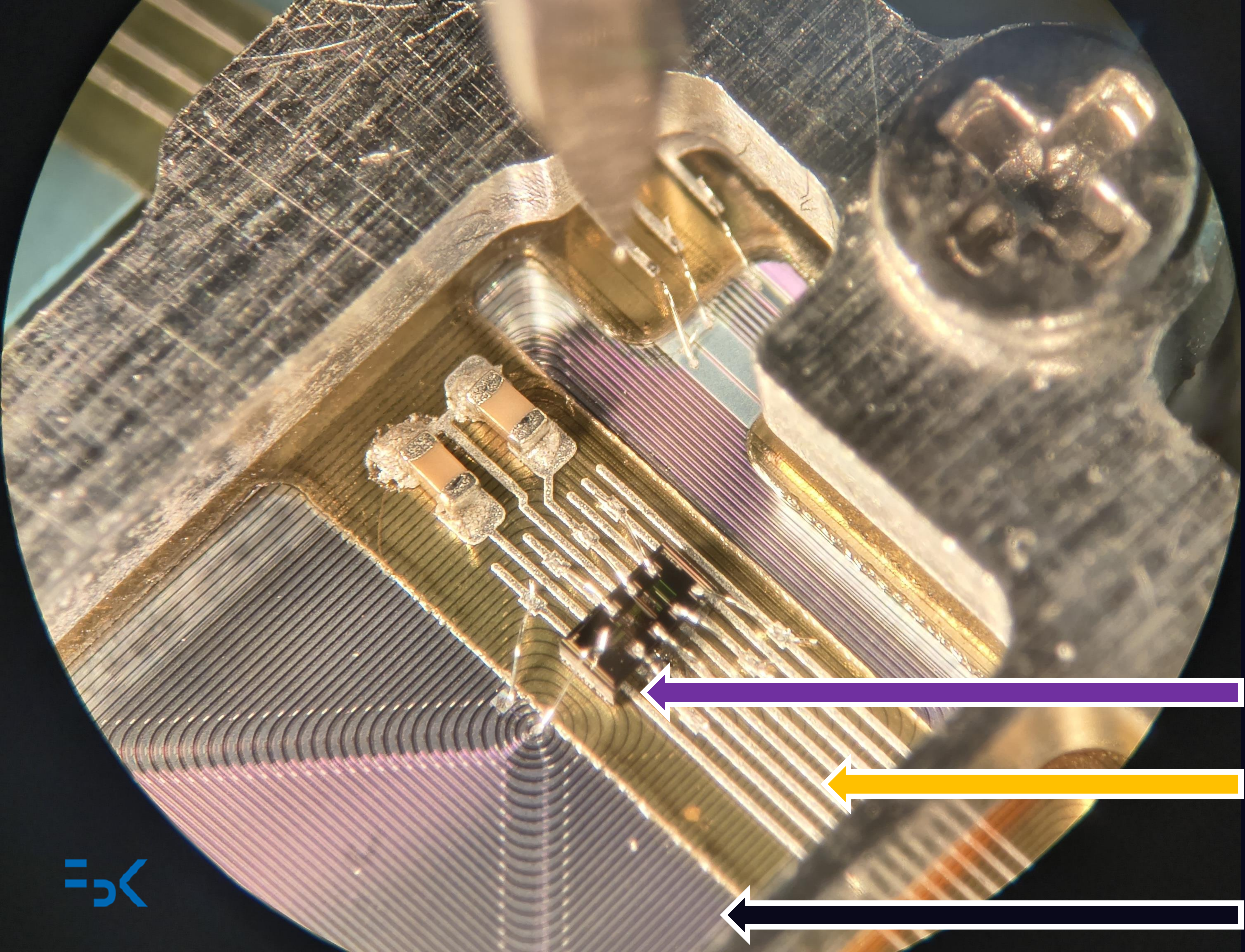
A compact self-standing detector system



Aluminum Flex

SDD

A compact self-standing detector system



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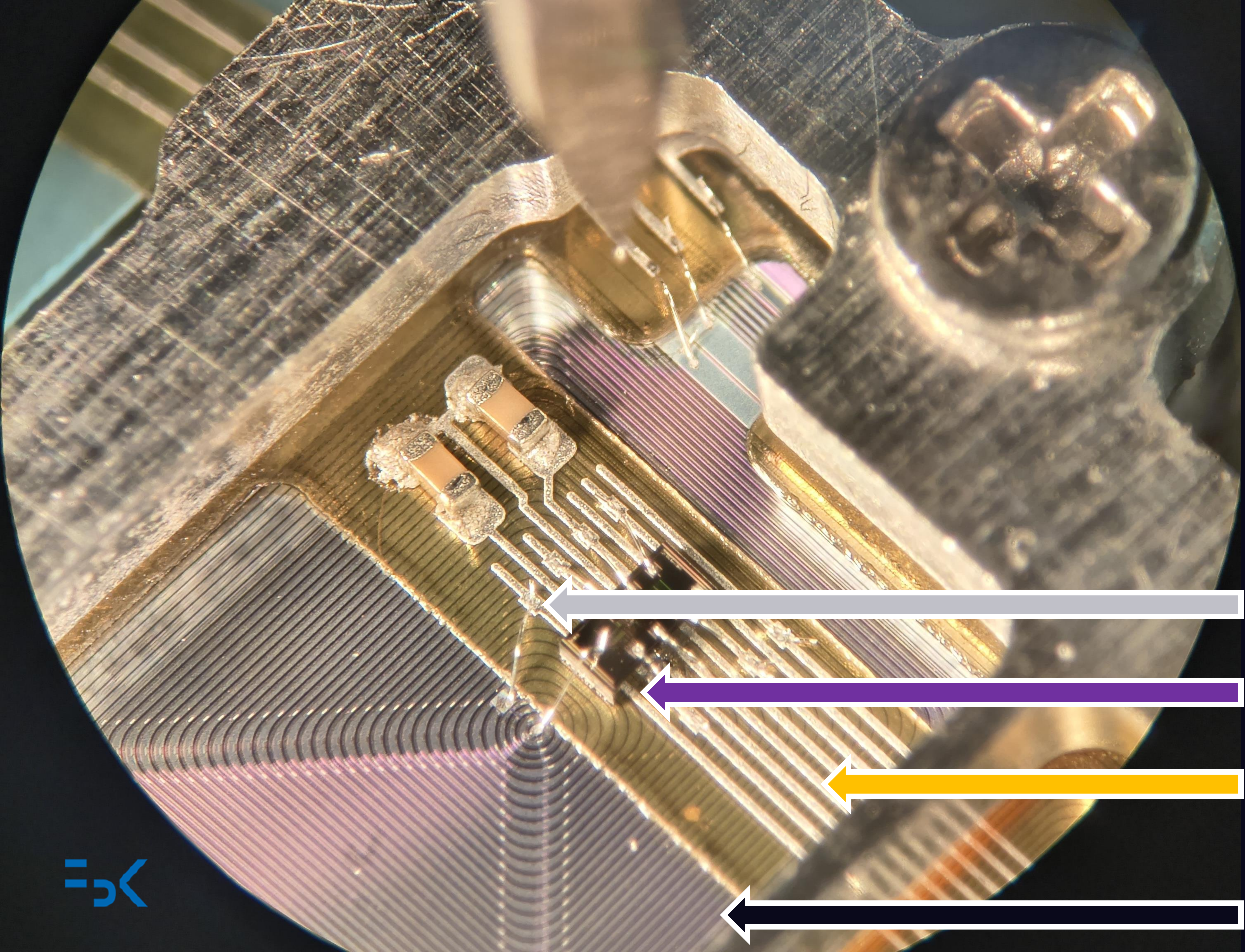

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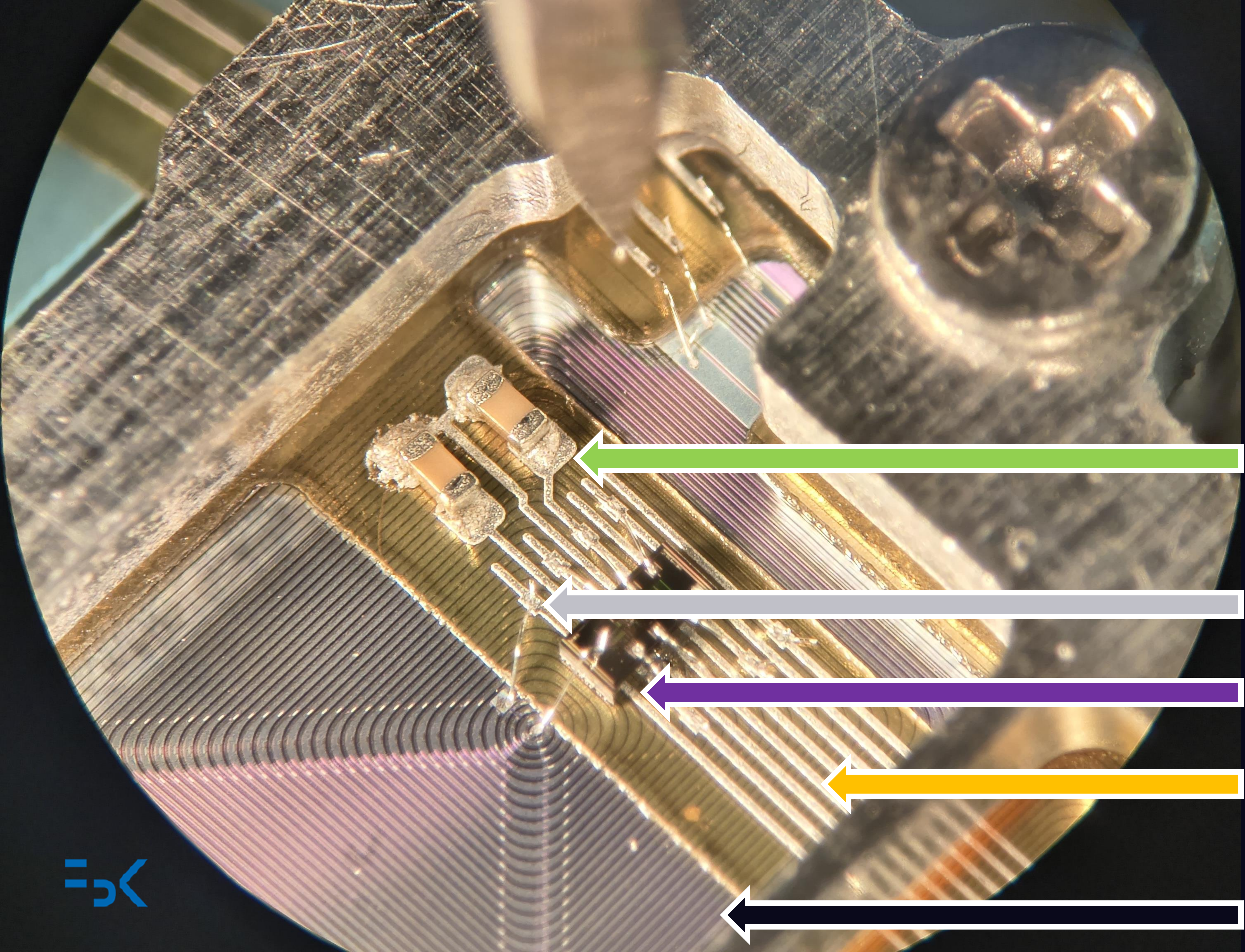

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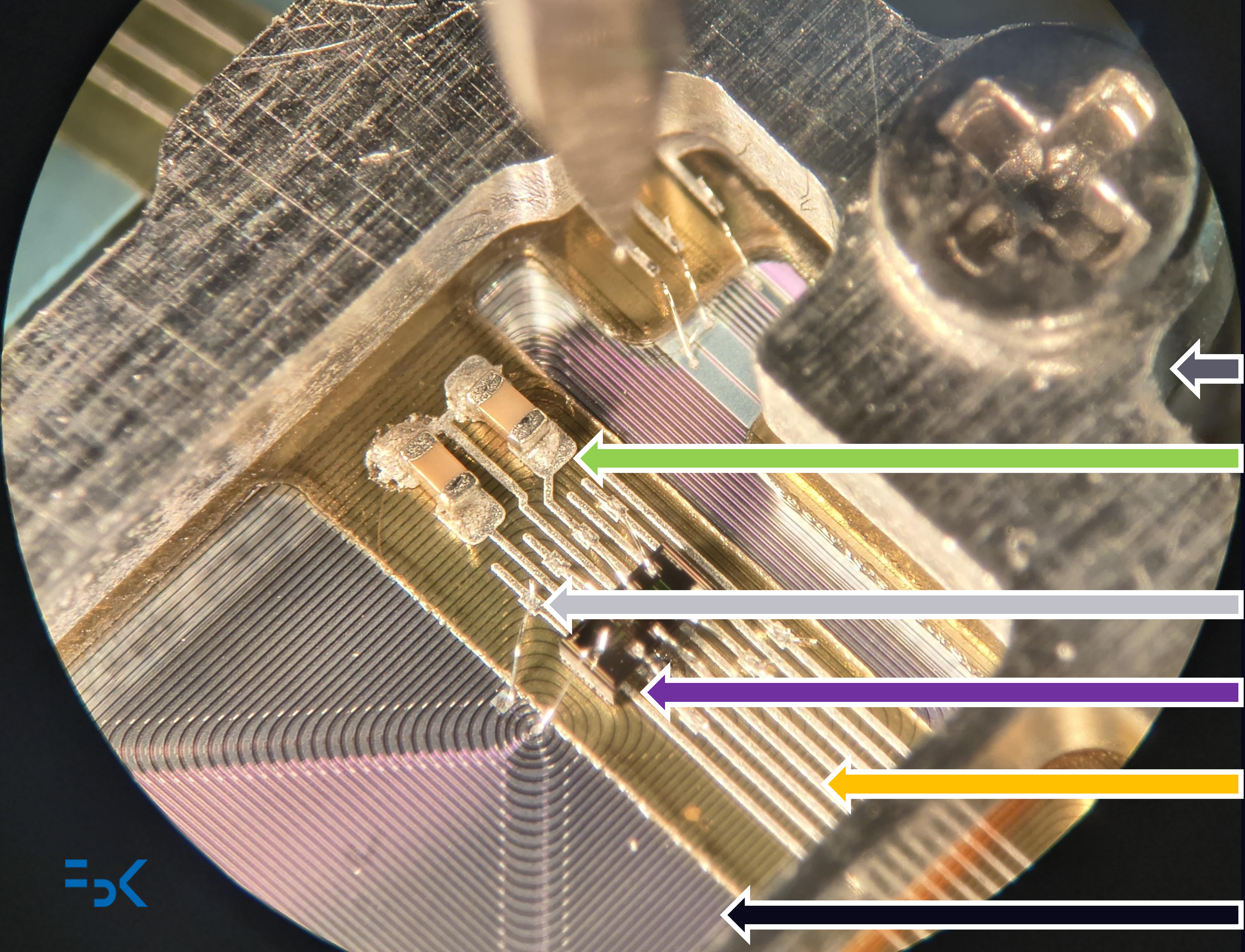


Support Mechanics

SMDs

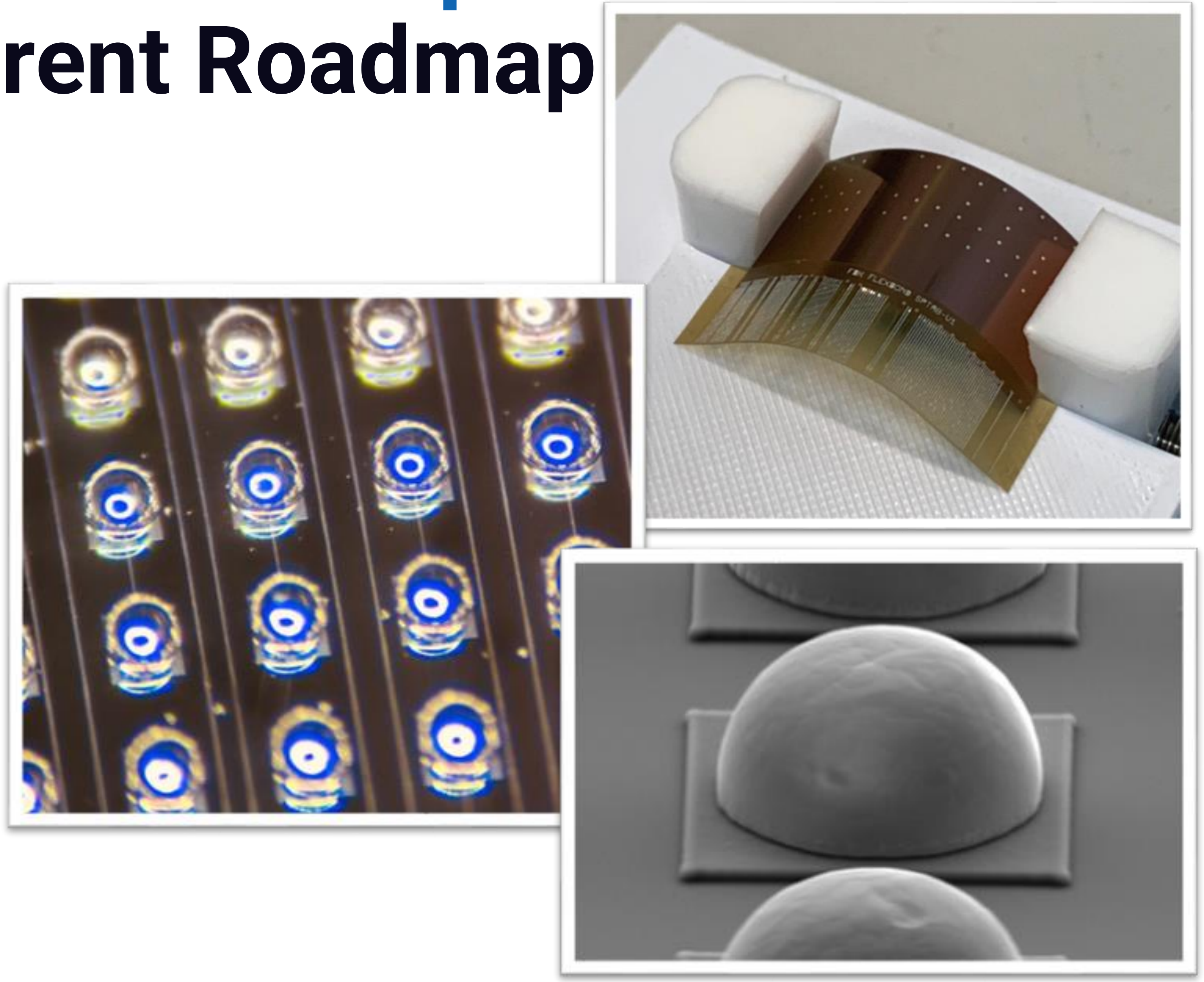
Wire Bonding

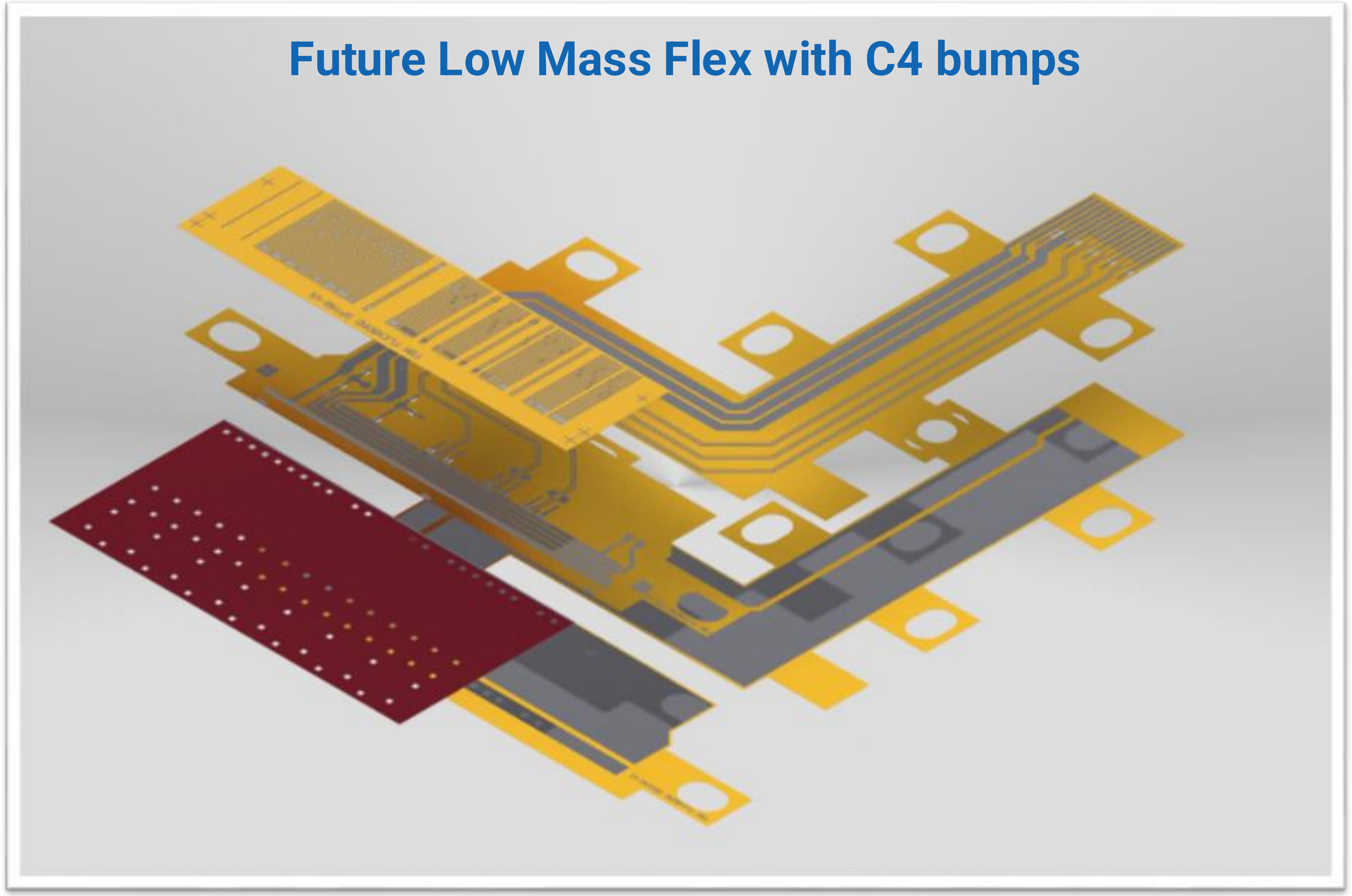
FE ASIC

Aluminum Flex

SDD

Future Developments
Current Roadmap





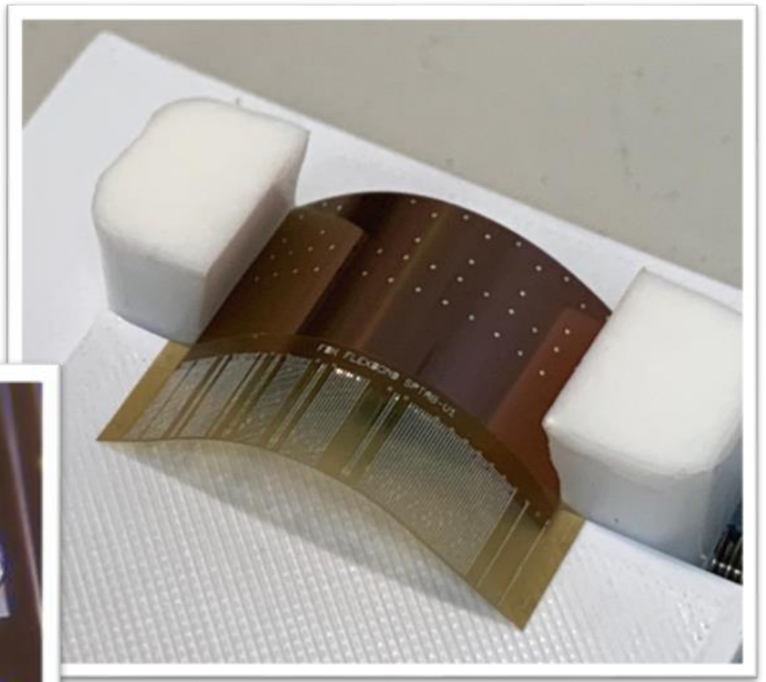
Current Tech Roadmap priorities

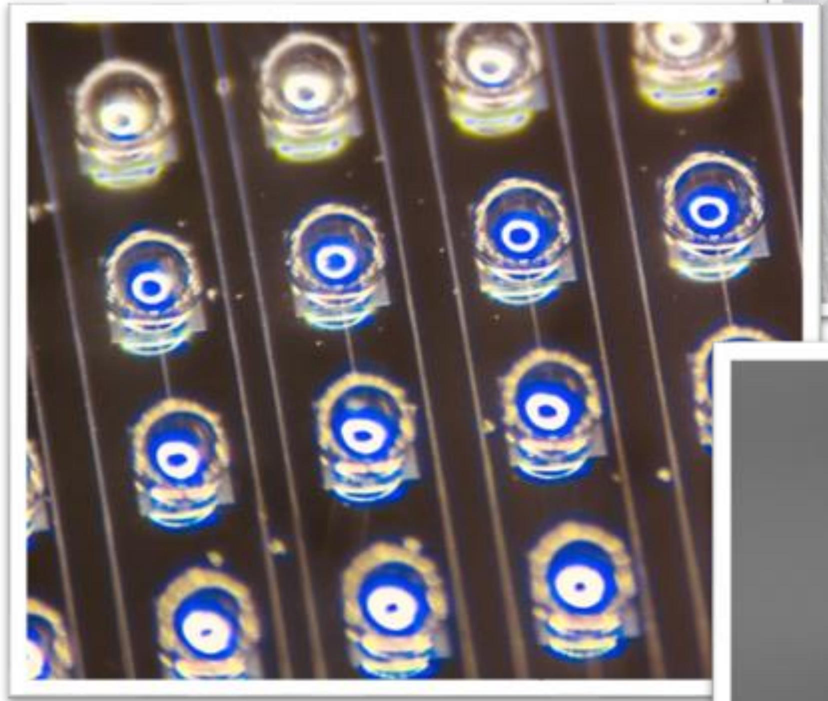
- Stacking
- Plating (Ni, ENIG)

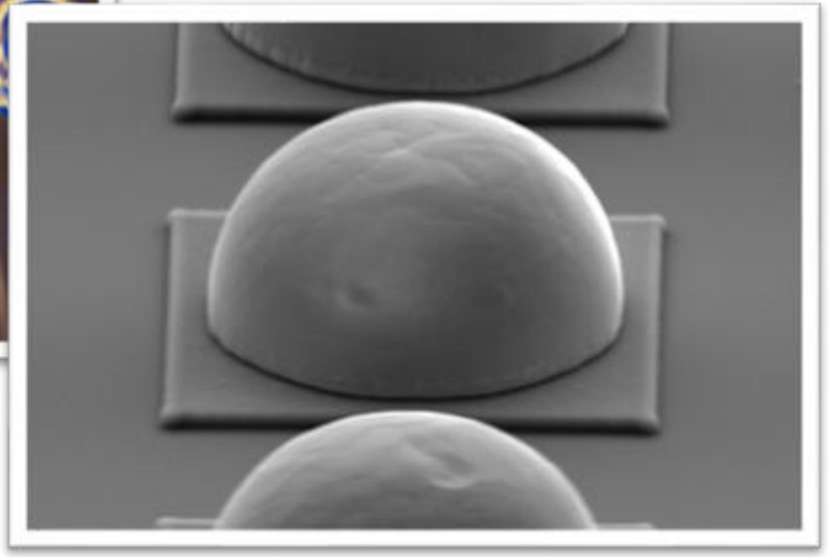
- Space qualification
- Low X/X_0 Flip-Chip on Flex
- Signal integrity

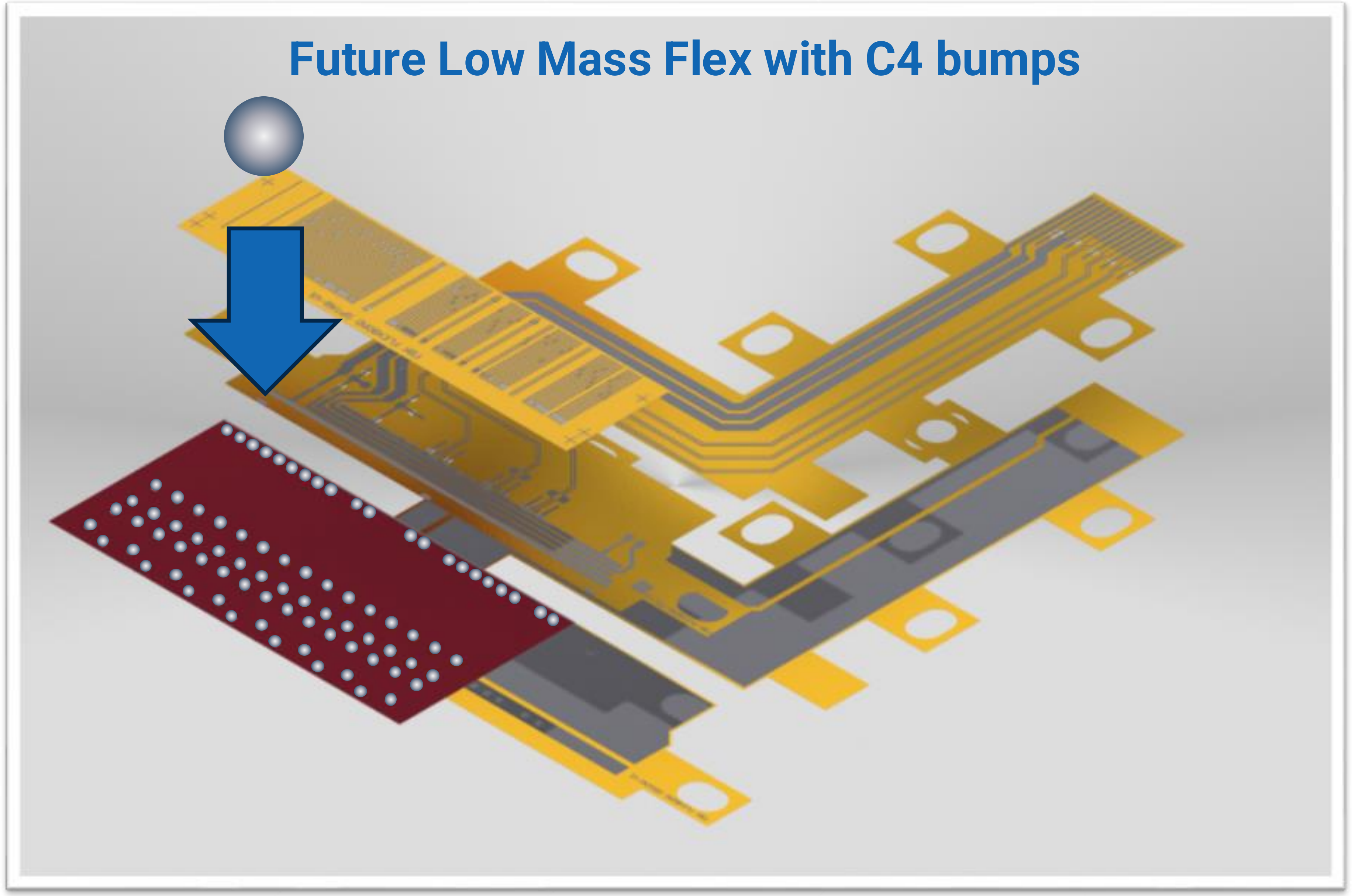
- High data rates (few GHz)
- Multi-chip modules

Future Developments
Current Roadmap









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FBK status update

Anze Sitar

Giovanni Paternoster

David Novel

Internal upgrades on

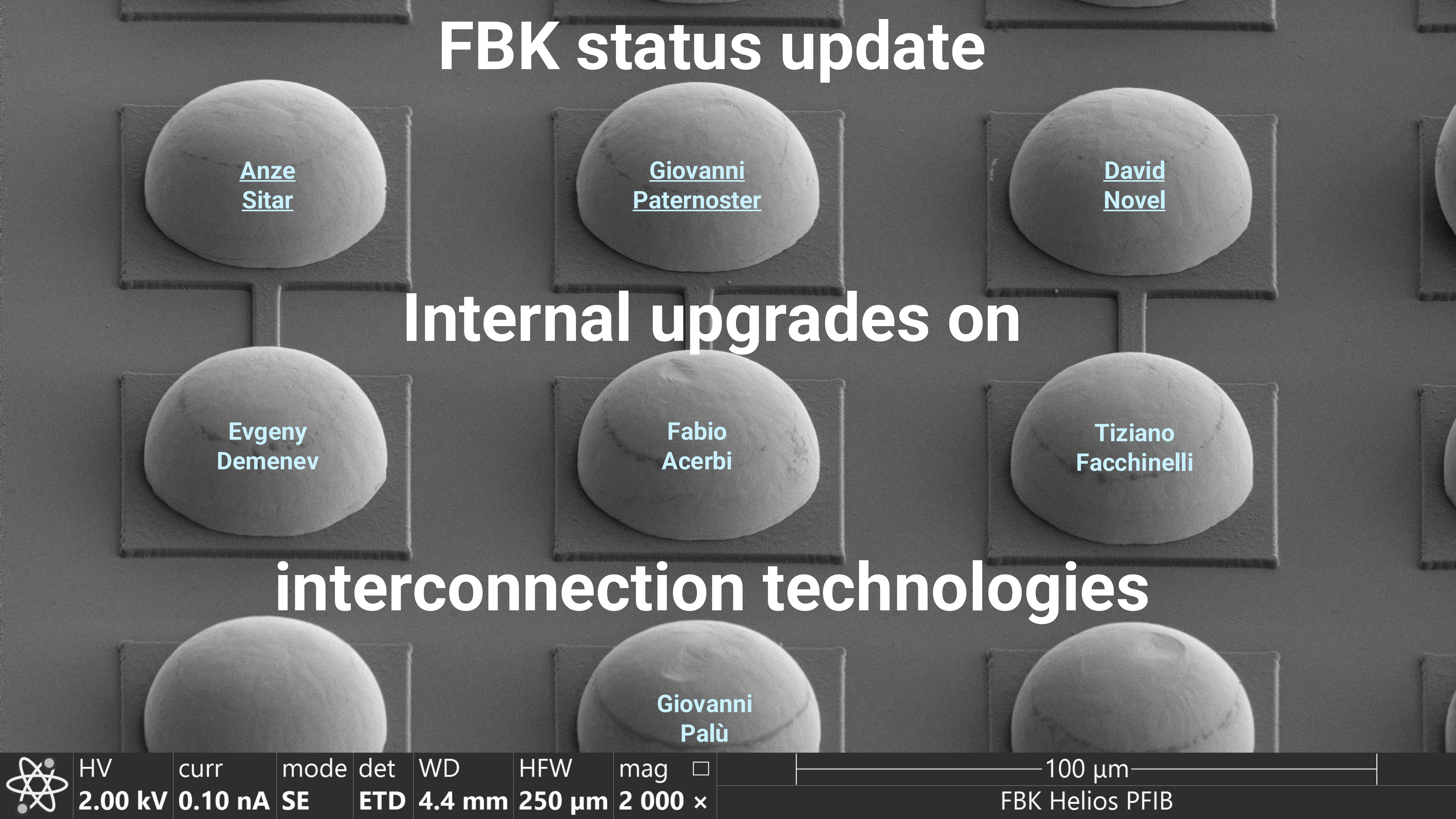
Evgeny Demenev

Fabio Acerbi

Tiziano Facchinelli

interconnection technologies

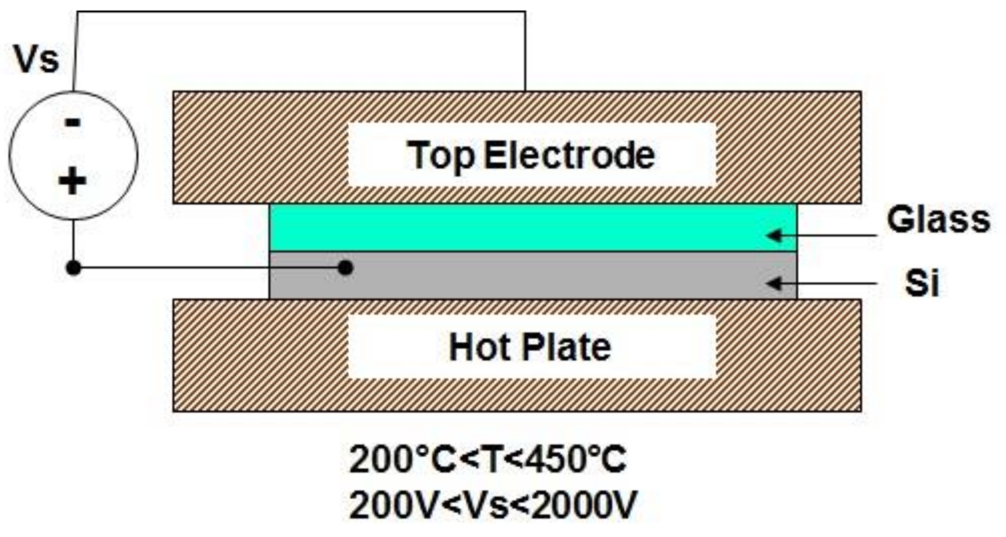
Giovanni Palù



FBK 3D integration
Current capabilities

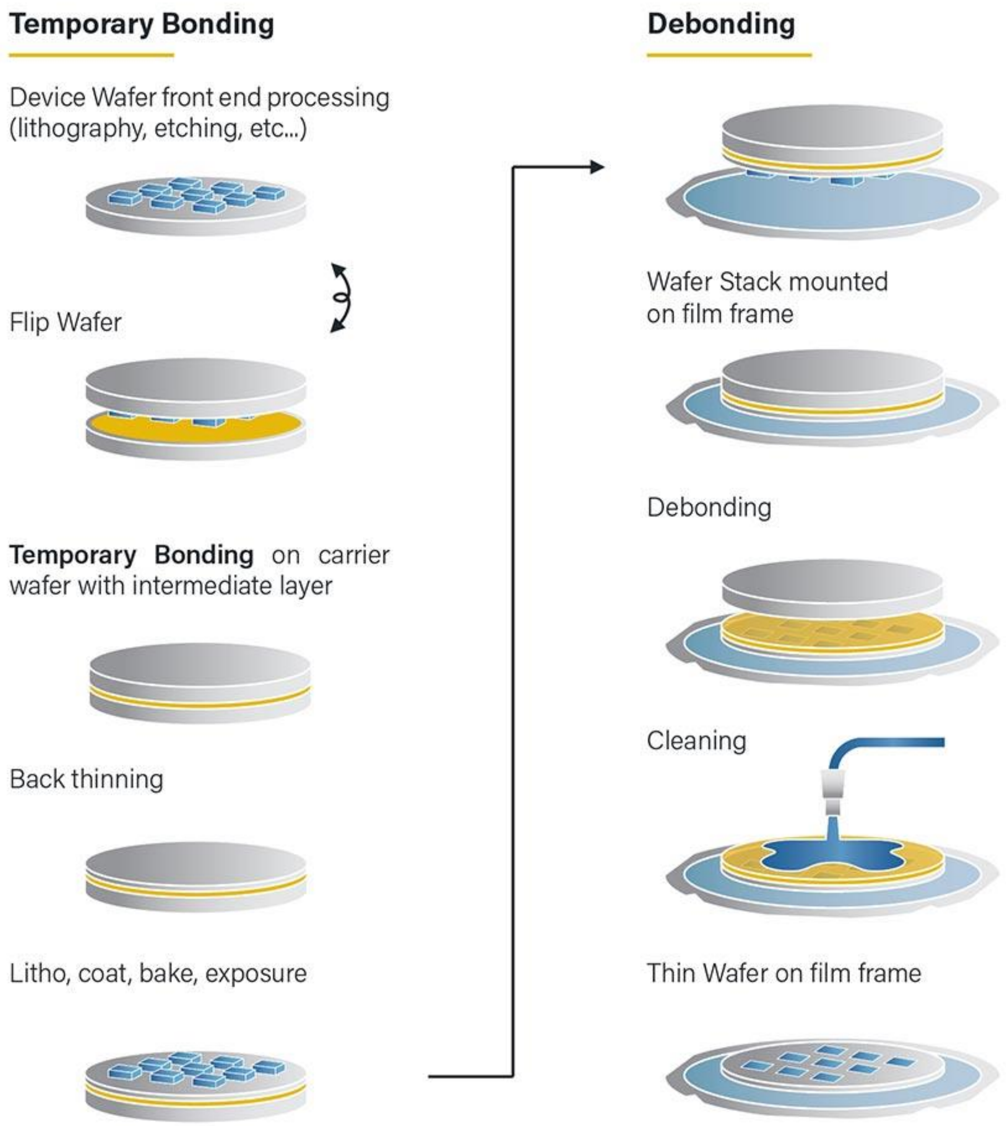
1. Sputtering system (various metal layers, under bump metal – UBM)
2. Evaporators (various metal layers, under bump metal – UBM)
3. Electrodeposition of Au
4. Anodic bonding of wafers
5. Adhesive bonding and debonding of wafers
6. Grinding & polishing down to micron thickness
7. Semi-automatic Wirebonding

Anodic bonding



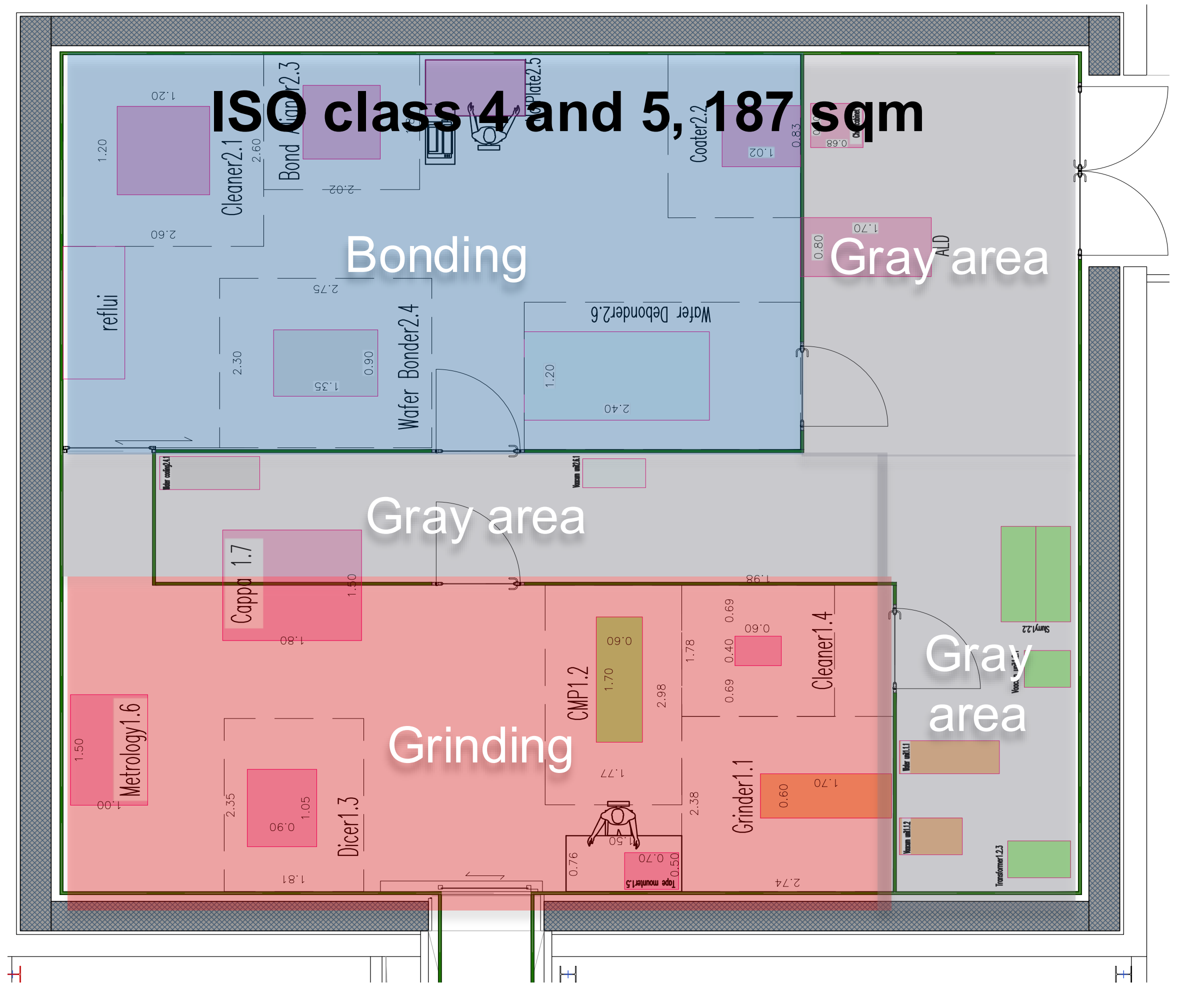
Wire bonding

Temporary (de)bonding



FBK 3D integration
New Cleanroom – operational

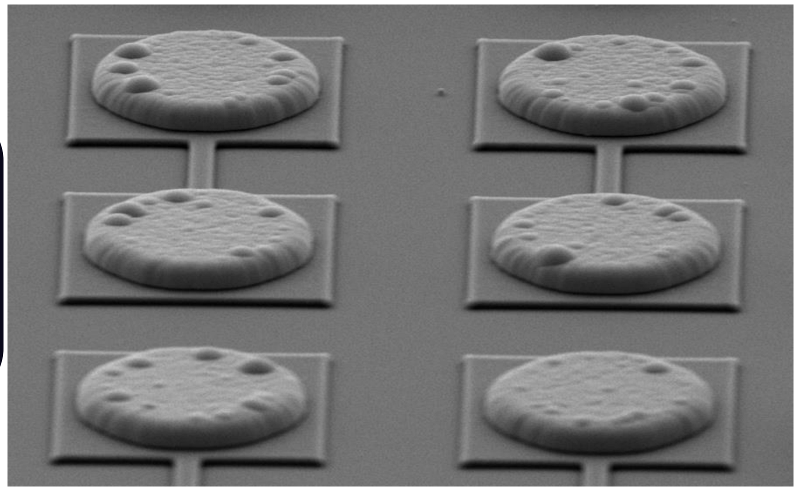
- Wafer Temporary Bonding/Debonding
- Metal and Fusion Direct Bonding
- Grinding and Polishing
- Metrology for 3D stacked wafers
- ALD

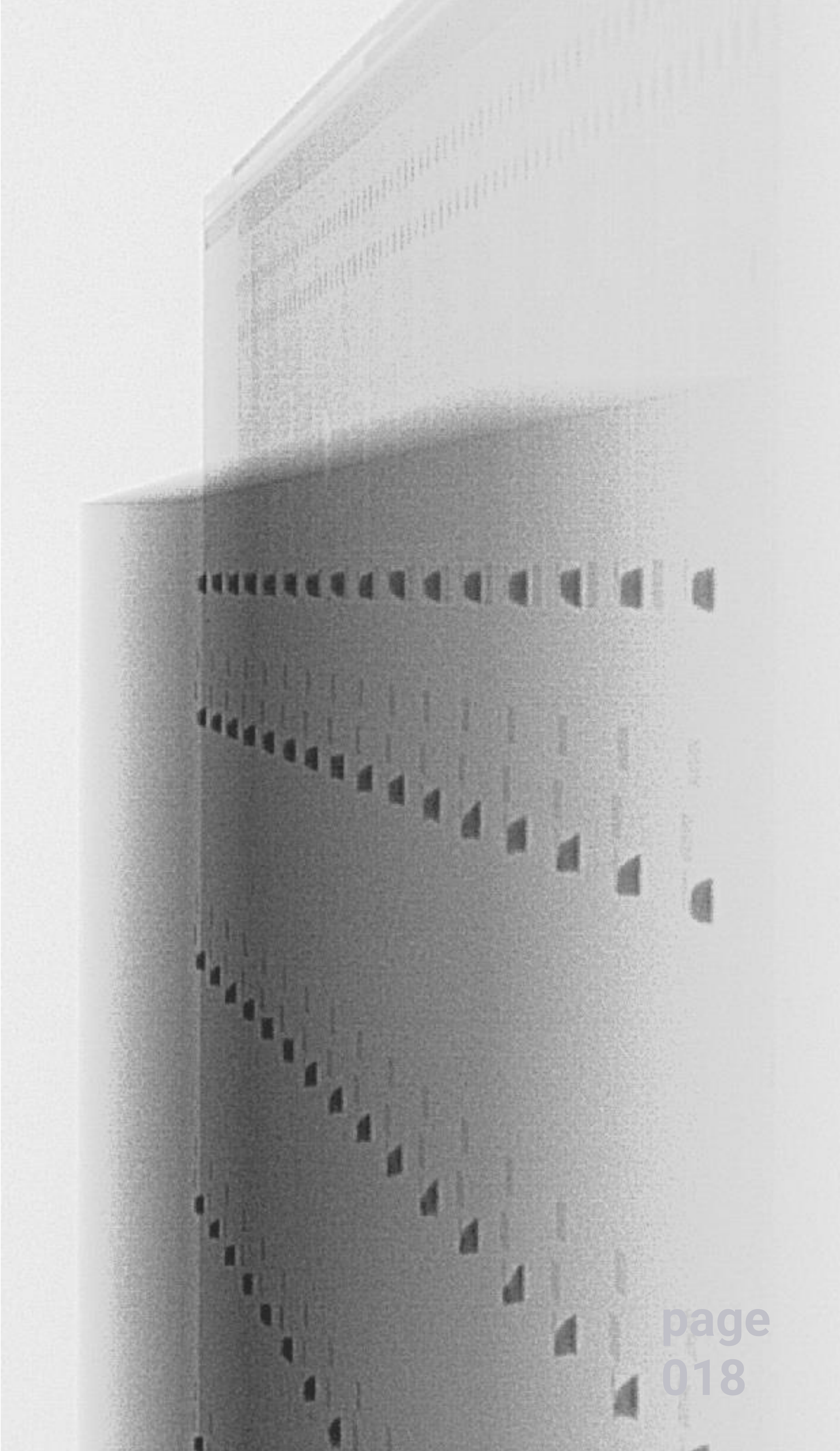


FBK 3D integration
Proposed pipeline

Pitch (> 70 µm)
Chips, wafers, PCBs, Flex

Electroless plating UBM
Nickel, (Palladium), Gold





New installations are planned in FBK, starting from 2026

FBK 3D integration
Proposed pipeline

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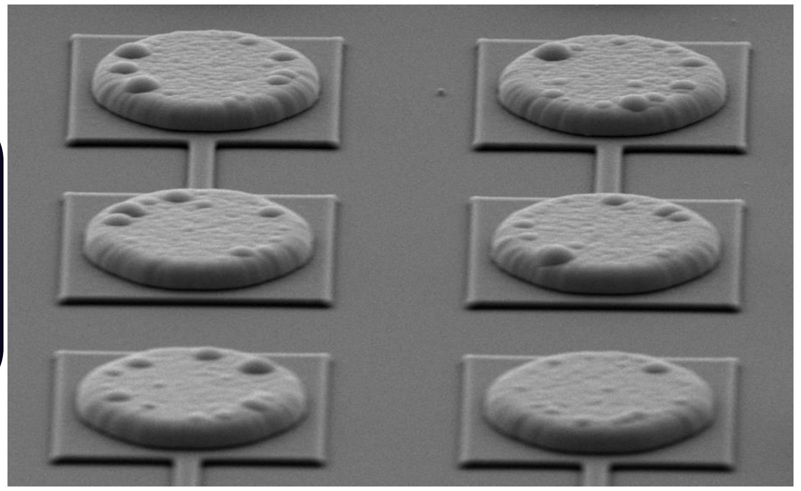
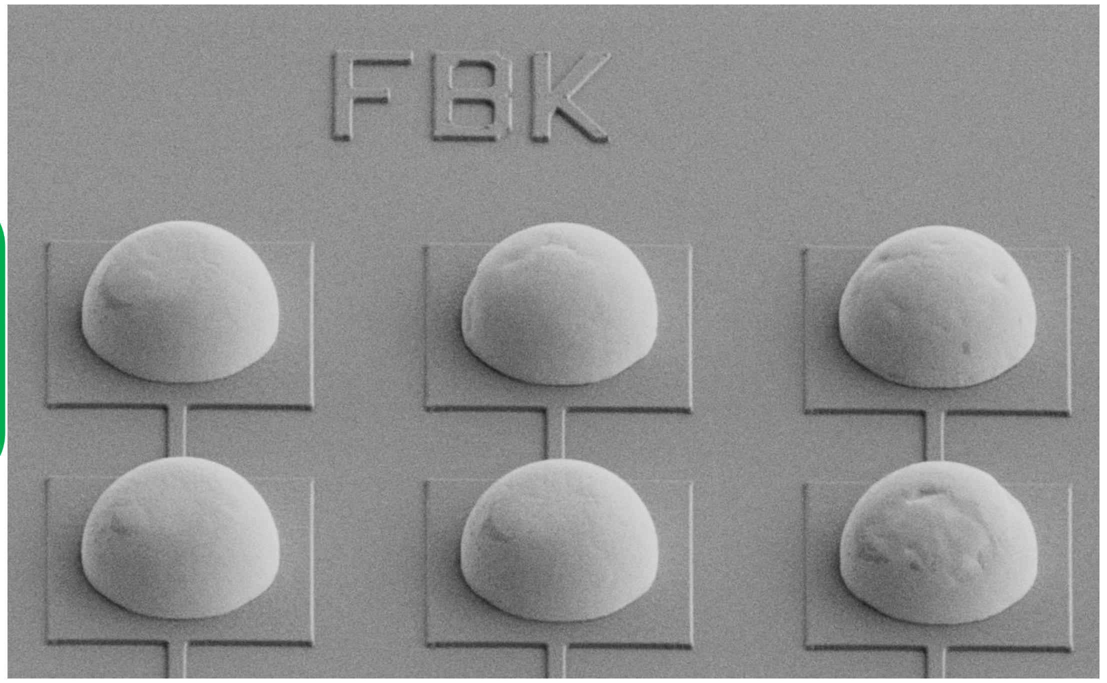


Chips, wafers, PCBs, Flex

Solder ball deposition
(30) 40-250 µm

Already installed in FBK



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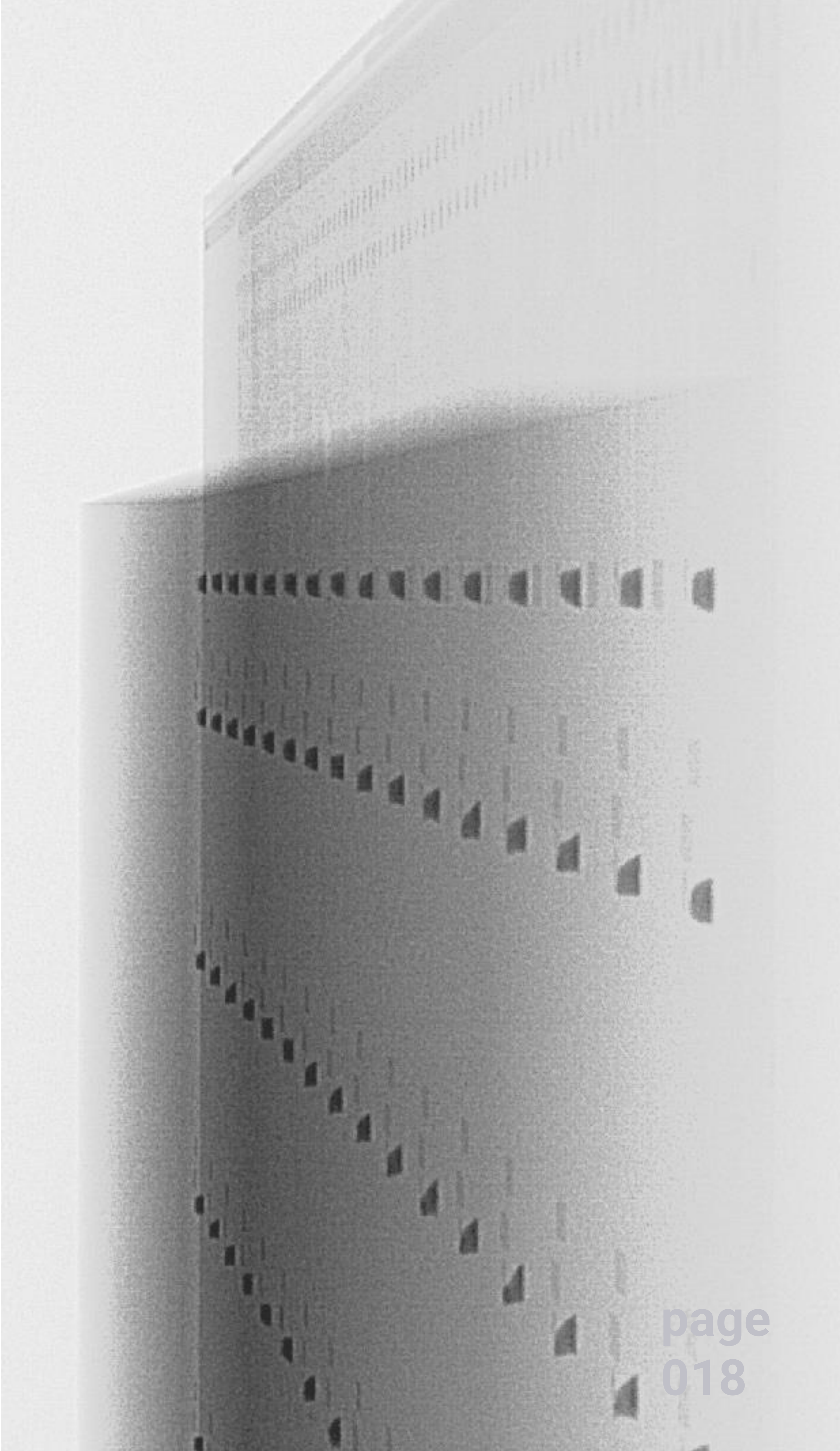
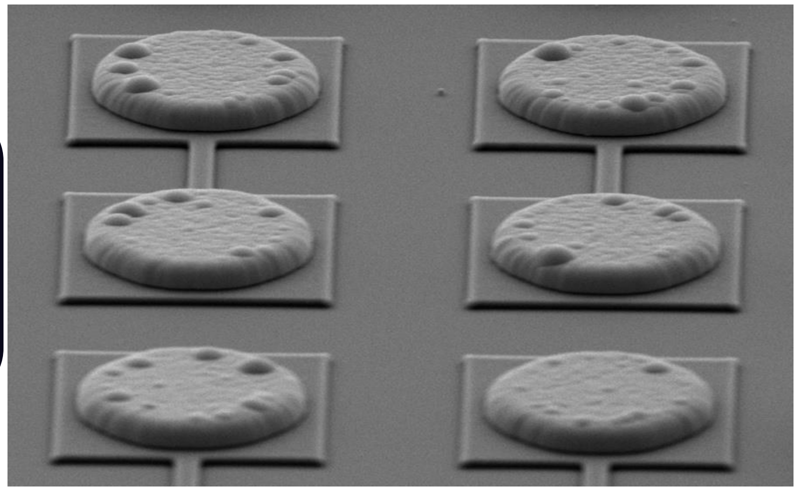


FBK 3D integration
Proposed pipeline

Pitch (> 70 µm) Chips, wafers, PCBs, Flex	**Electroless plating** **UBM** Nickel, (Palladium), Gold



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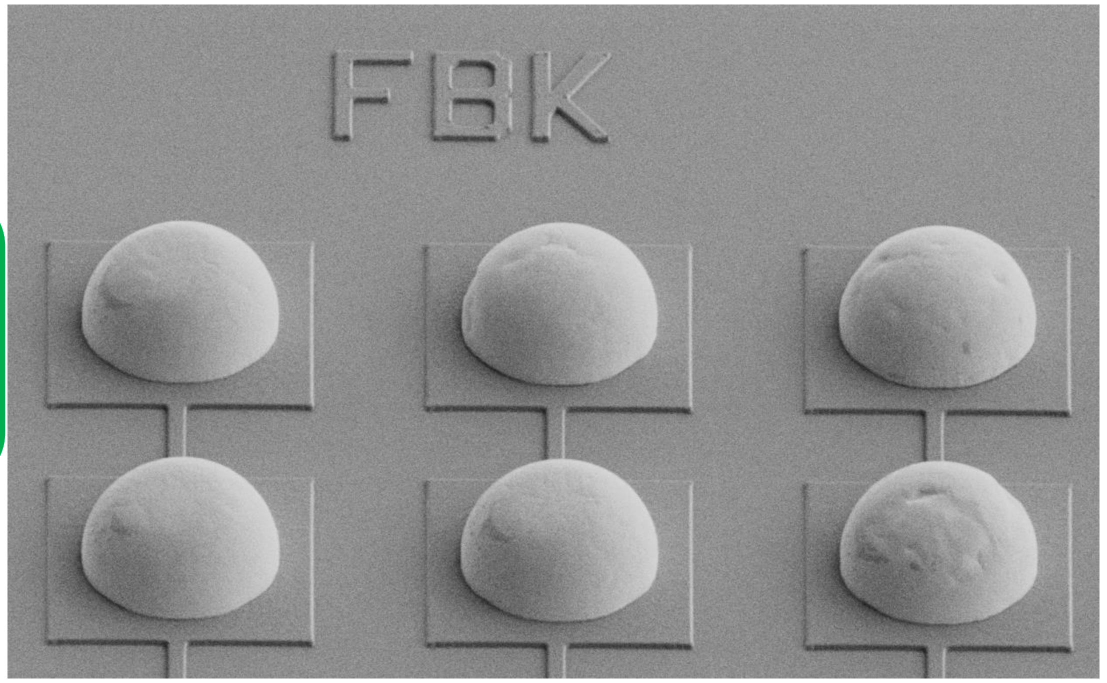
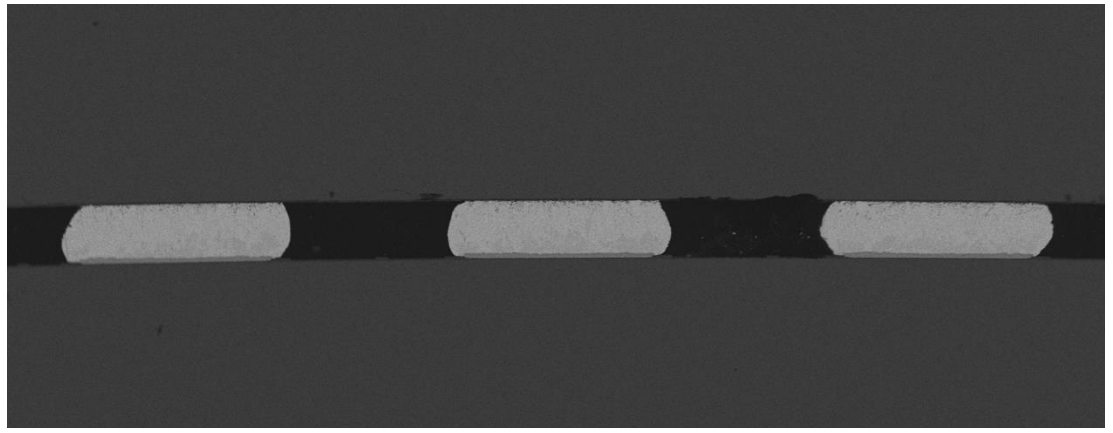


Chip to chip Chip to wafer Chip to PCBs	**Flip-Chip**



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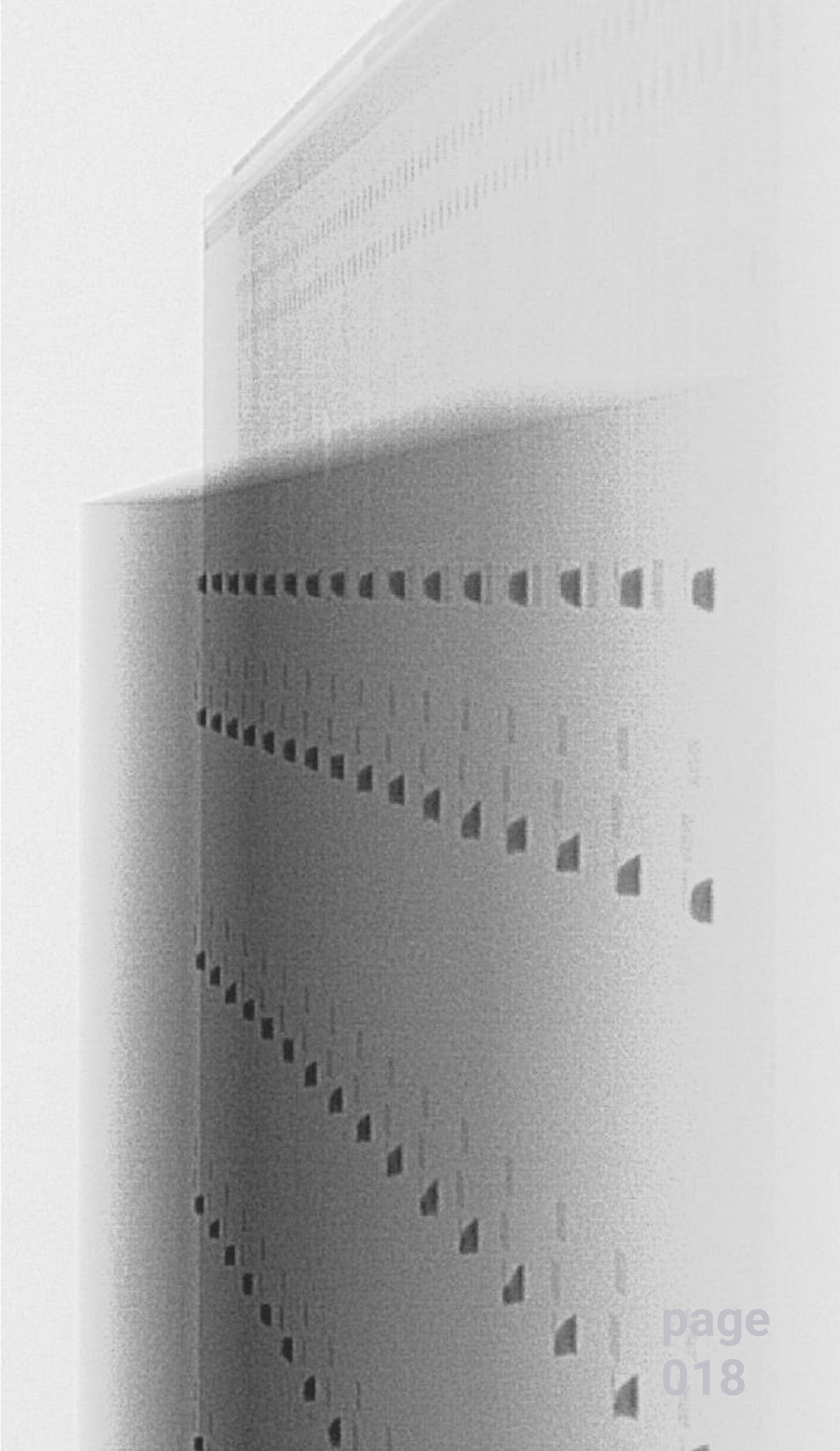
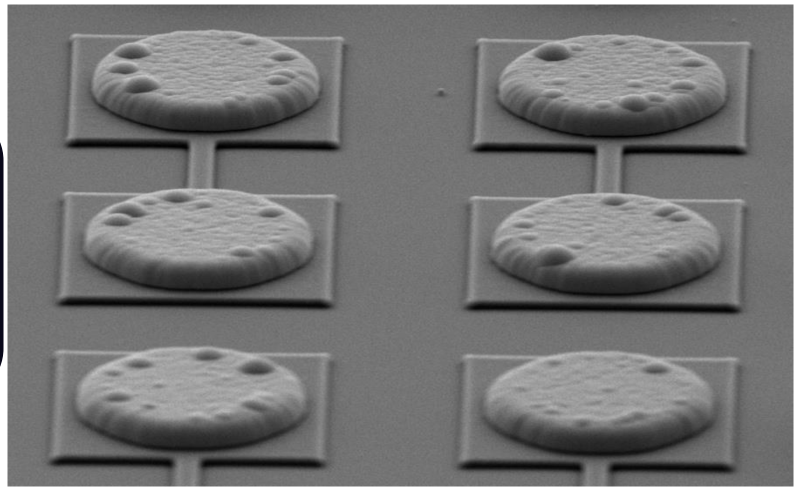


FBK 3D integration
Proposed pipeline

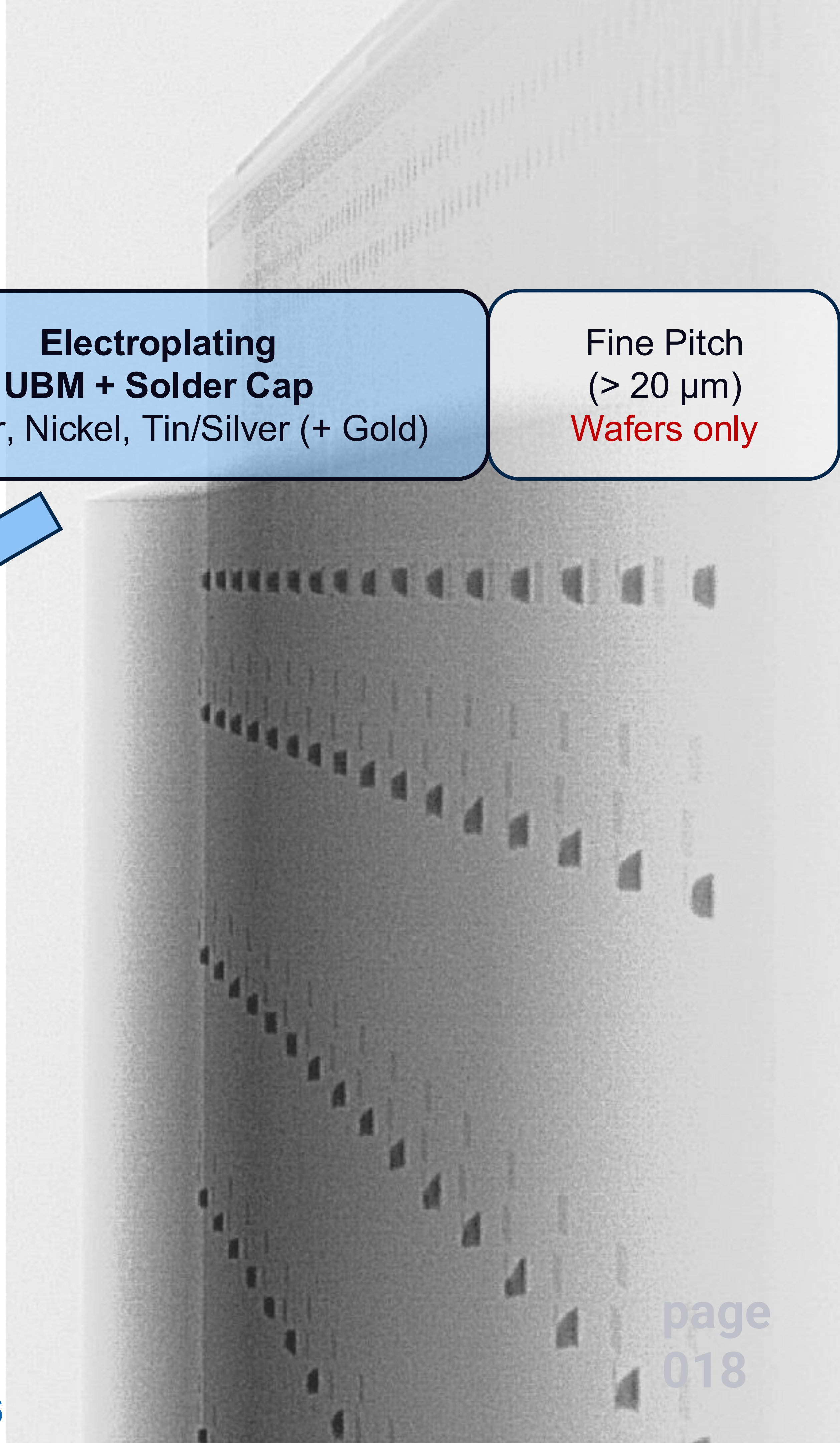
Pitch (> 70 µm)
Chips, wafers, PCBs, Flex

Electroless plating
UBM
Nickel, (Palladium), Gold



Electroplating
UBM + Solder Cap
Copper, Nickel, Tin/Silver (+ Gold)

Fine Pitch
(> 20 µm)
Wafers only



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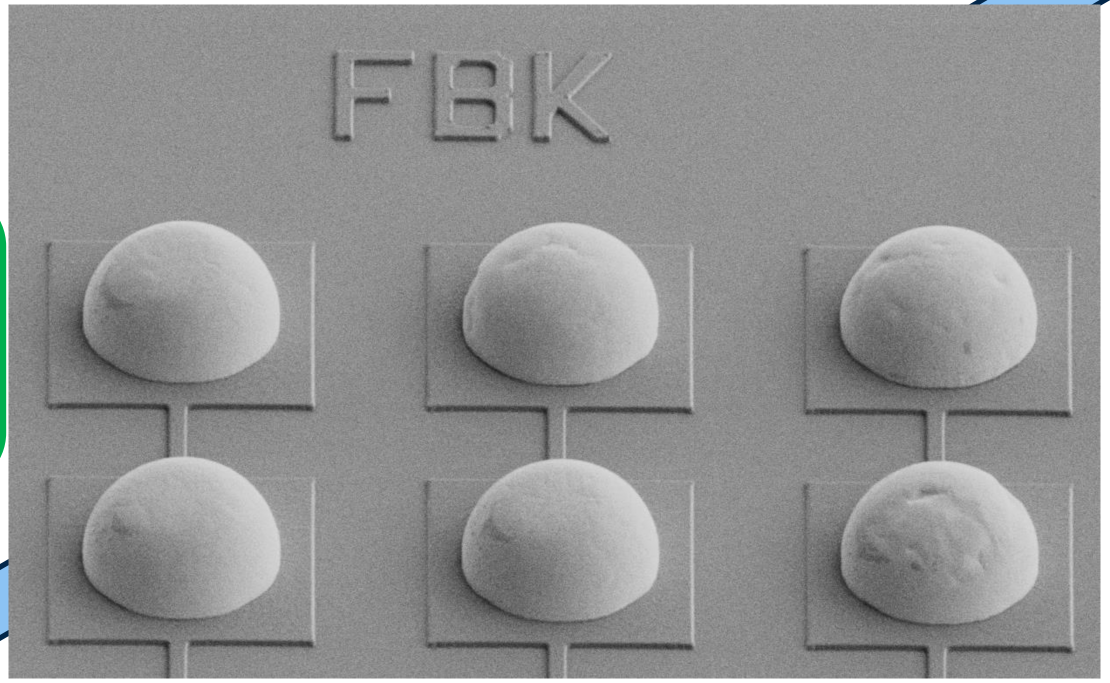
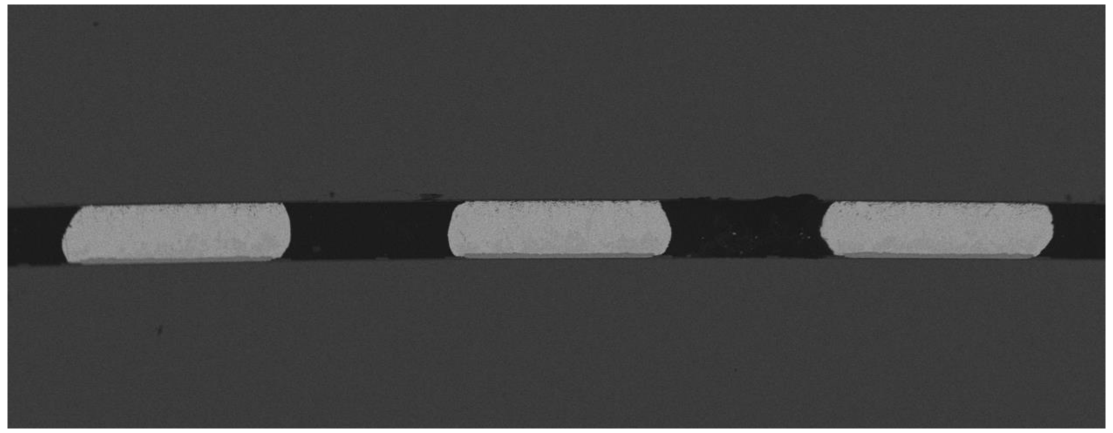


Chip to chip
Chip to wafer
Chip to PCBs

Flip-Chip



New installations are planned in FBK, starting from 2026

FBK & DRD3

FBK contact: David Novel

DRD3

HV-CMOS Pixel Detector Demonstrator with Serial Powering and Innovative Interconnections

3rd DRD3 Week on Solid State Detectors R&D
Amsterdam, 2-6 June 2025

Attilio Andreazza — Università di Milano and INFN
Yanyan Gao — University of Edinburgh

CCF Project Proposal by

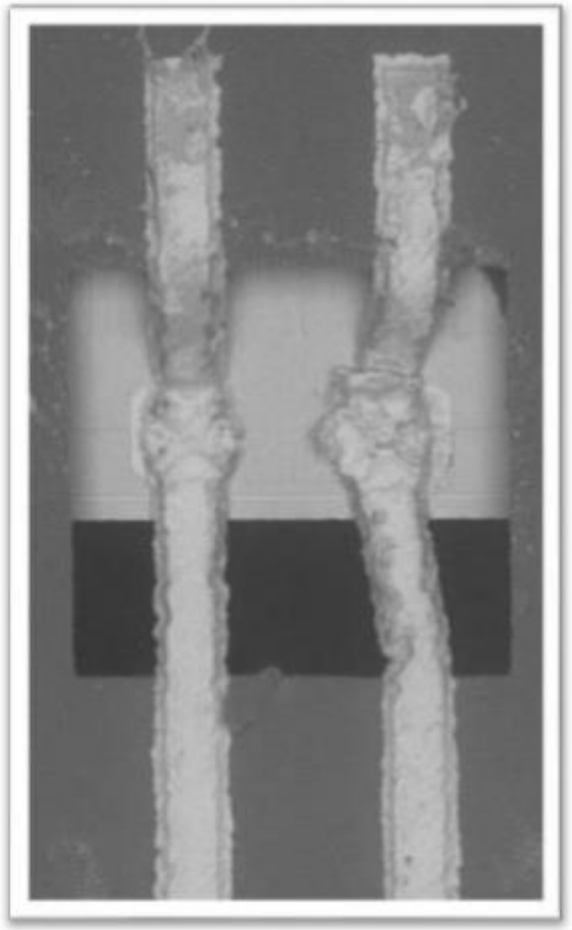
Birmingham, Bristol, Edinburgh, FBK, Heidelberg, Hochschule RheinMain, IHEP, KIT, Lancaster, Milano, Pisa, Torino, Trento

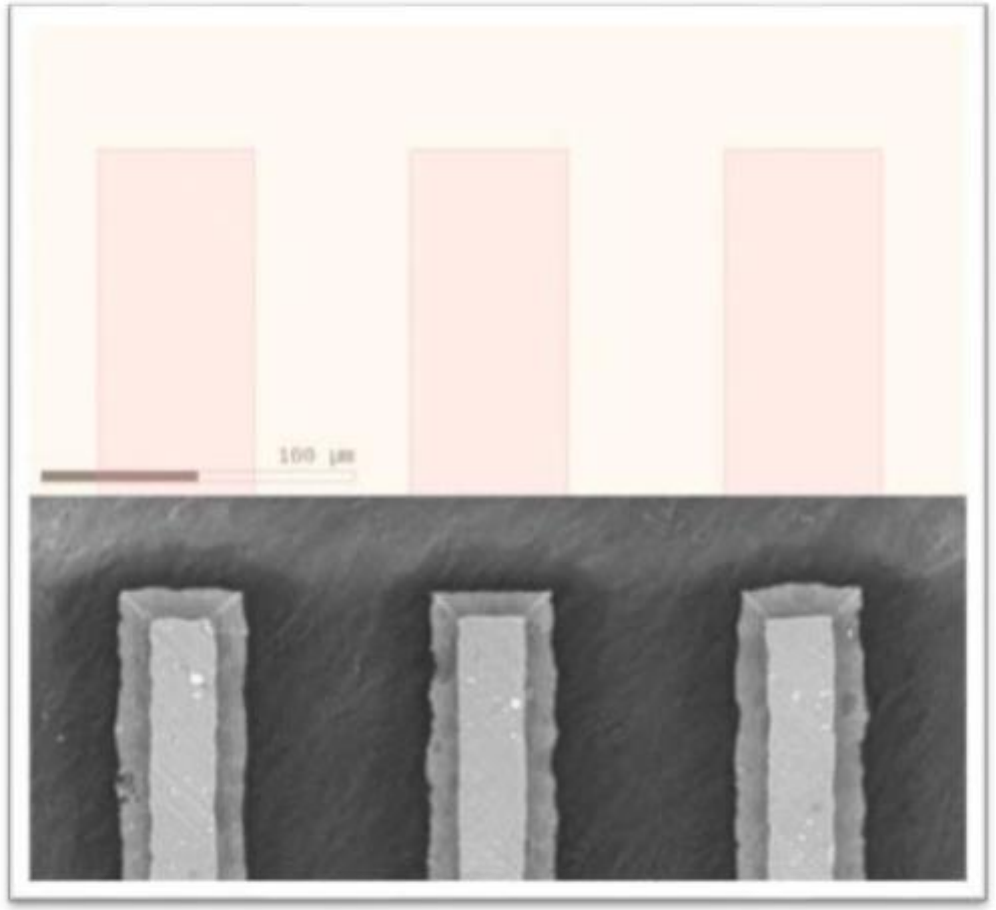
INFN MILANO

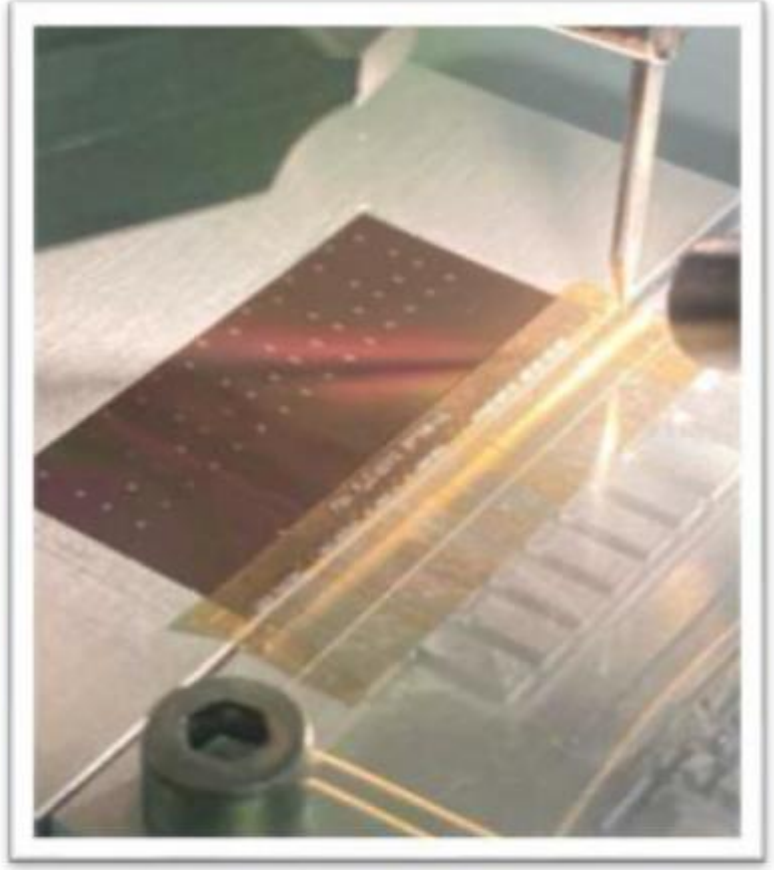
UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

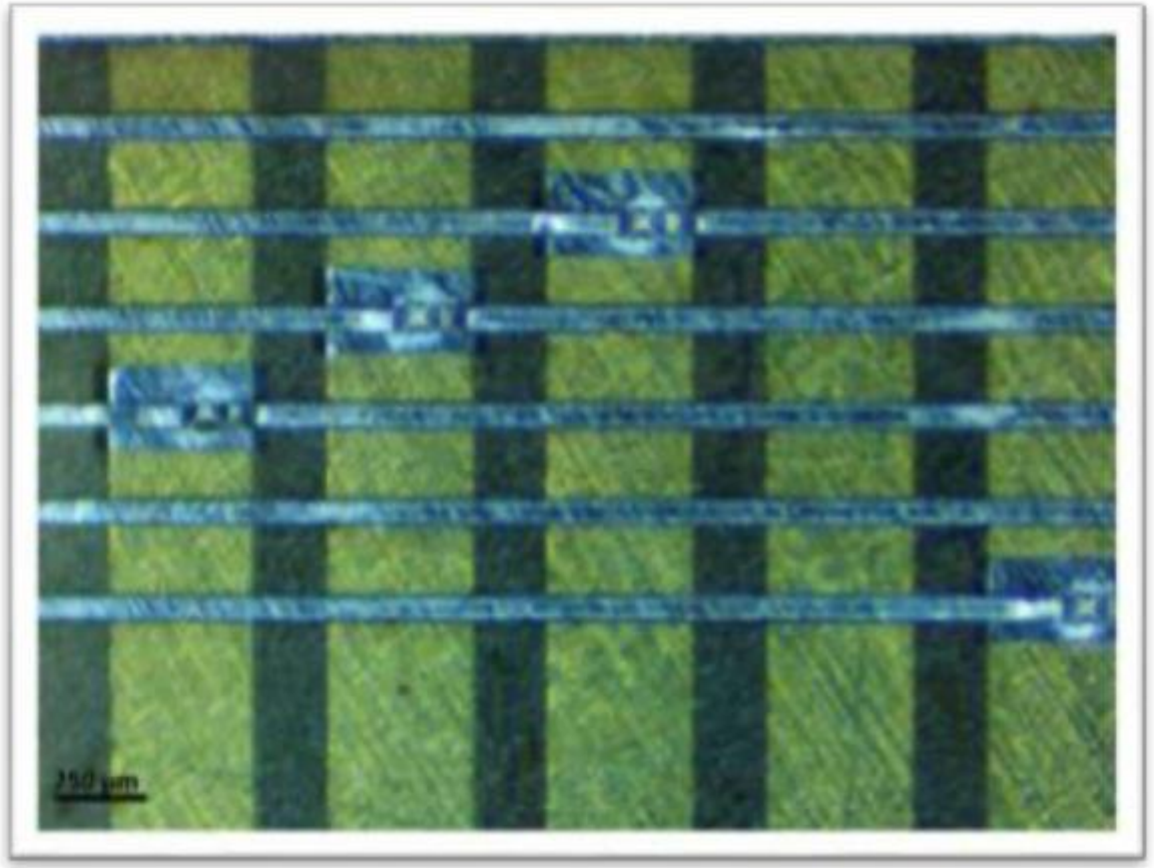
Stage 2: FBK technology

- Fabrication process inspired from the state-of-art LTU-Kharkiv [DOI: 10.15407/fm24.01.143]
- Processing inside FBK cleanrooms
- Kapton-Al PCBs
  - 20 μm Al thickness
  - 25 Kapton thickness
  - **Wafer level manufacturing (6" wafers)**
- Feature size
  - minimal size is 2 × Al thickness = 40 μm
  - very high line density (90 μm pitch)
- Interconnection
  - spTAB 75 × 75 μm tool tip
  - flex-to-chip TAB
  - flex-to-flex TAB:
    - use TAB as vias to reduce overall material
    - connection to additional flexible PCB









3rd DRD3 week on solid state detectors R&D

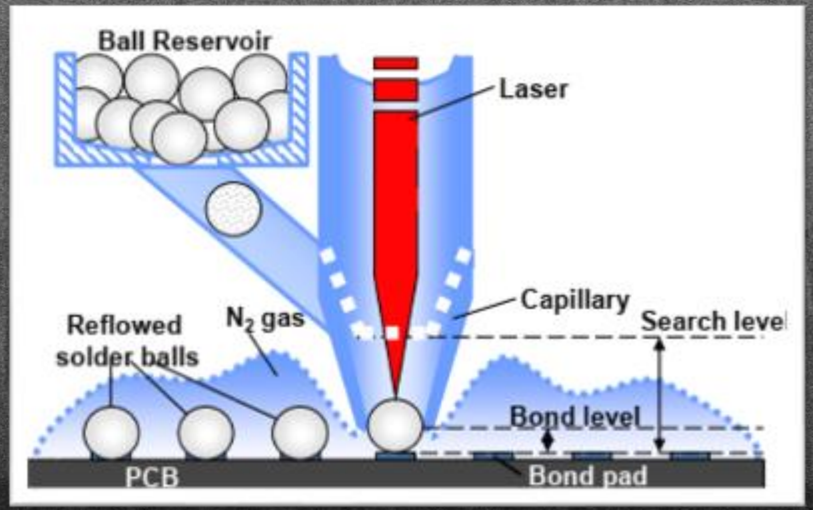
FBK contact: Maurizio Boscardin

DRD3

In-house plating, hybridisation and module-integration technologies for pixel detectors

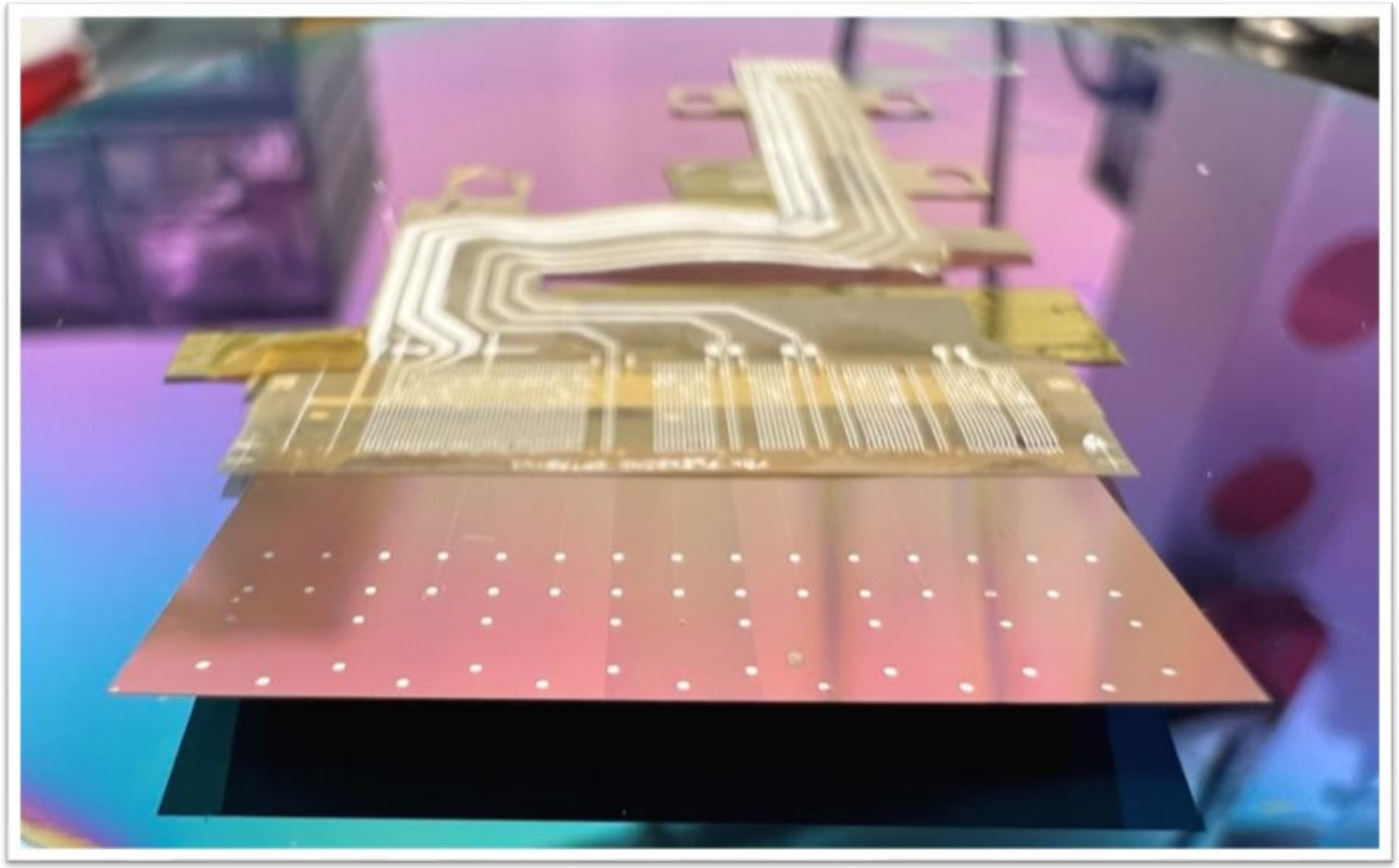
WG7 Interconnect
Dominik Dannheim

LPNHE, CERN, FBK, UNIGE



Thank you!

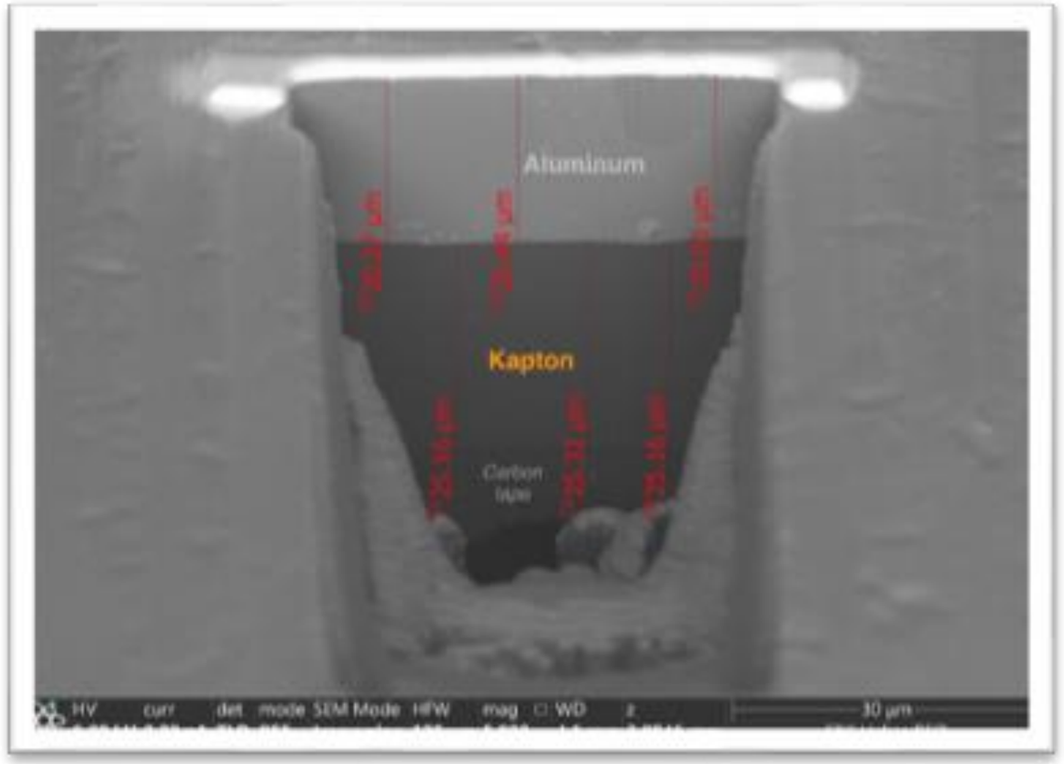
Low mass Aluminium Flex Platform
The recipe



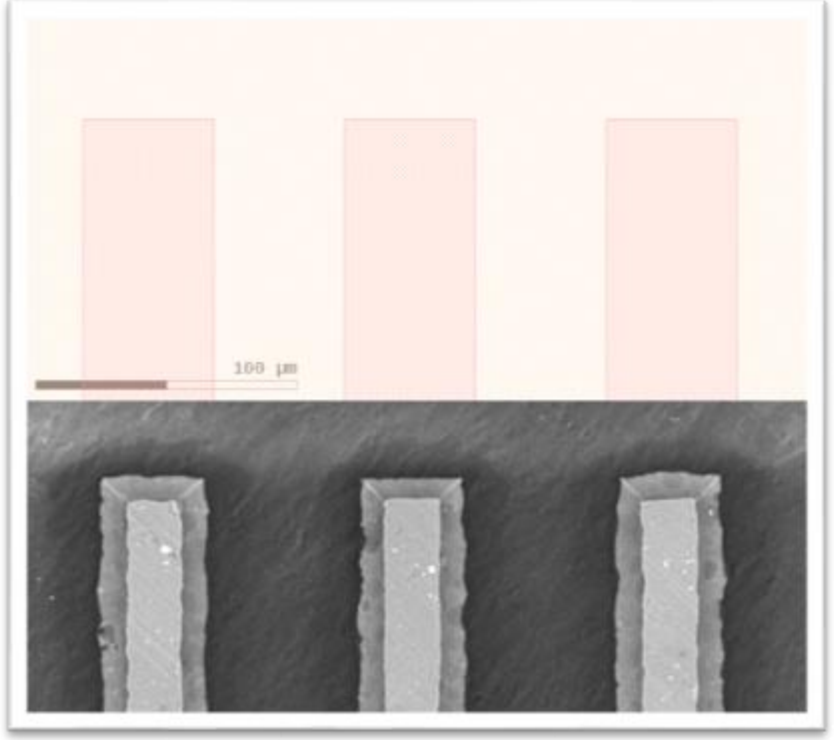
50 µm ALPIDE chip + 90 µm Aluminium-Kapton flex PCB double layer

- ❑ **Flex cable with Aluminium**
  - (X_{0Al} = 8.9 cm, X_{0Cu} = 1.4 cm)
- ❑ **Minimal thickness**
  - 20 µm Al /layer
  - 25 µm Kapton /layer
  - 0.03% X/X0 /layer
- ❑ **Tape Automated Bonding**
  - Single point Tape Automated Bonding (spTAB)
  - Cross-imaged bonding tip

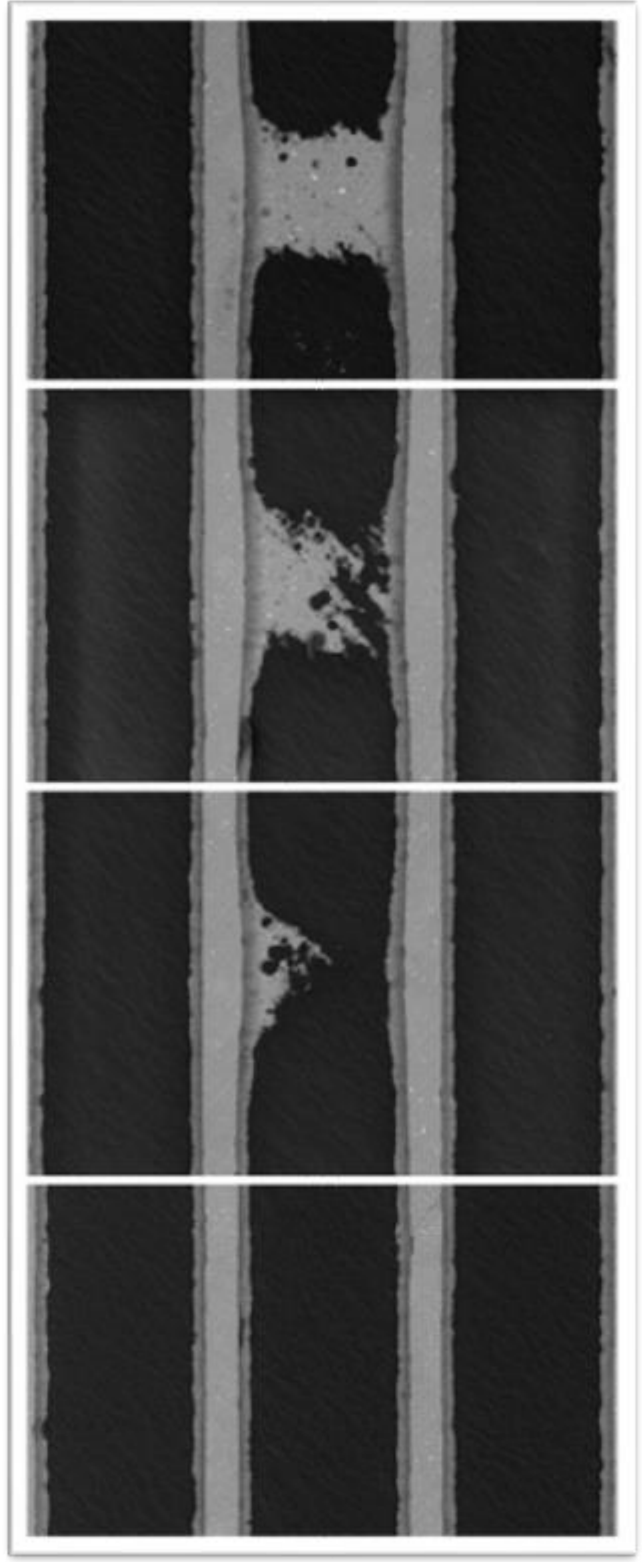
Low mass Aluminium Flex Platform
Aluminium patterning with wet etching



Cross section of the PI-aluminium (20-25 µm) substrate



Analysis to correlate nominal and final patterned dimensions



Aluminium etching optimization

- ❑ **High patterning control**
  - Aluminium thickness of 20 µm is our standard
  - Minimum trace width and spacing = 40 µm for this aluminium thickness (can be decreased with thinner Aluminium)

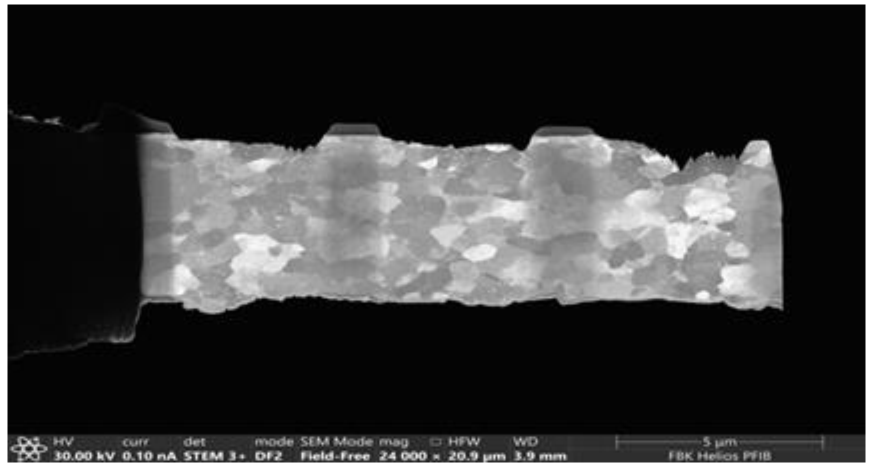
Thickness (µm)	Measured Resistivity (µΩ cm)
20	3.02

Preliminary measurements on resistivity of the aluminium

Device & Material characterization
Examples

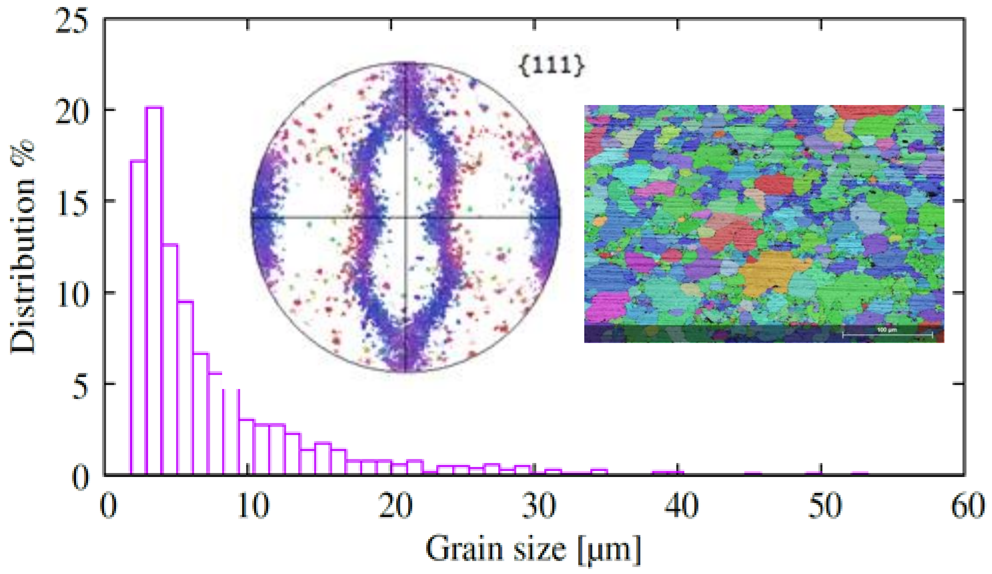
MATERIALS

DEVICES



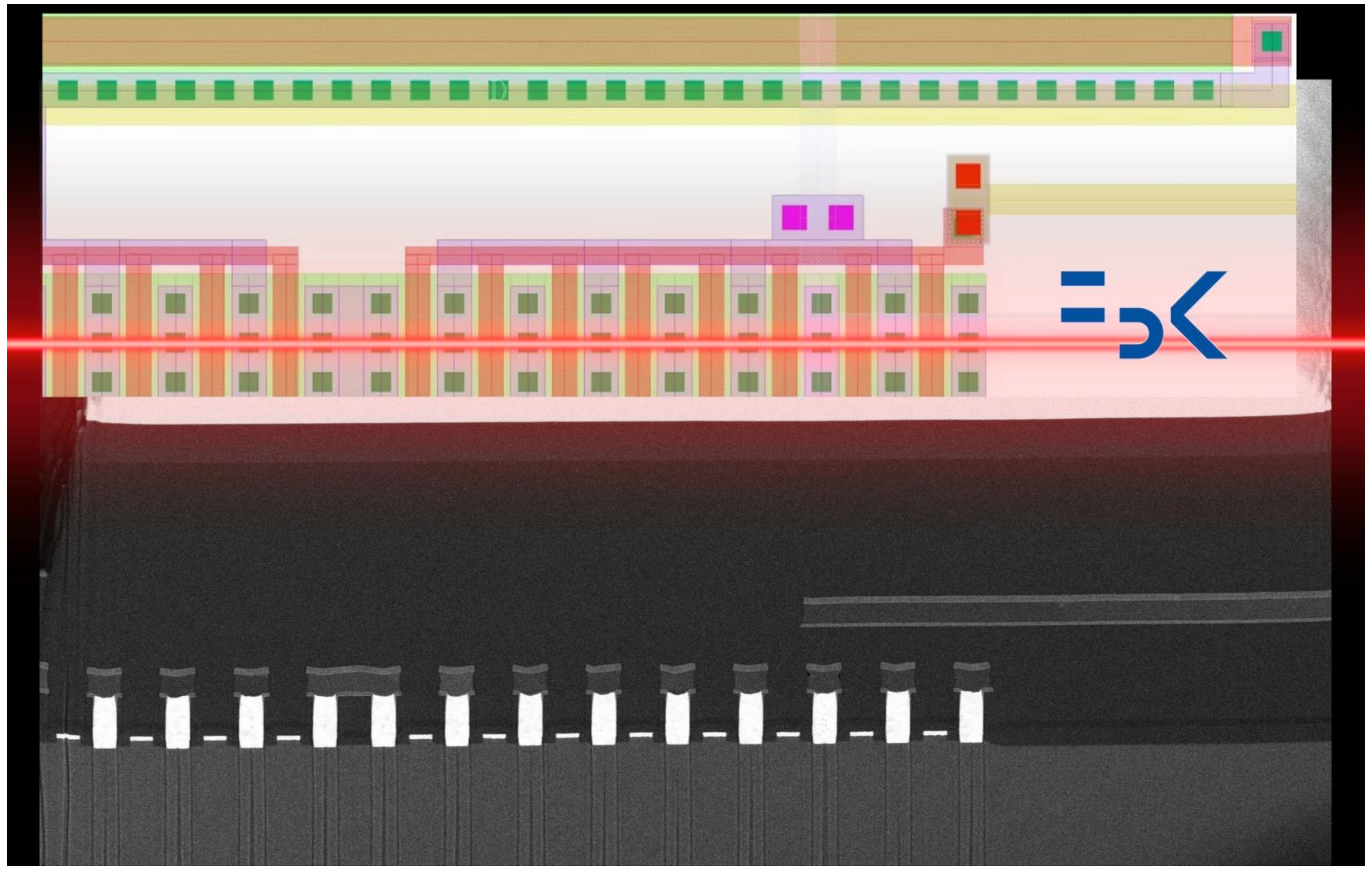
TEM lamellas

Characterization of grain size and crystallographic orientation



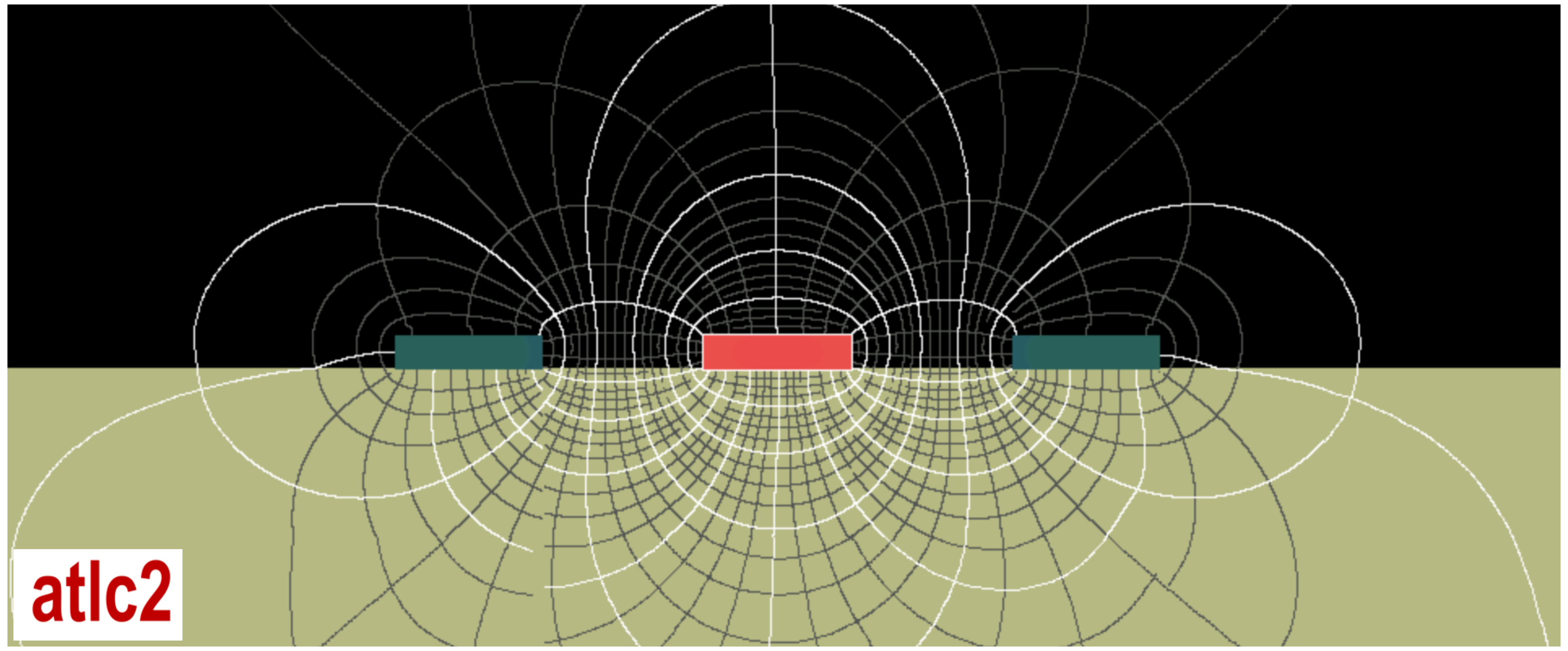
Top view ASIC layout

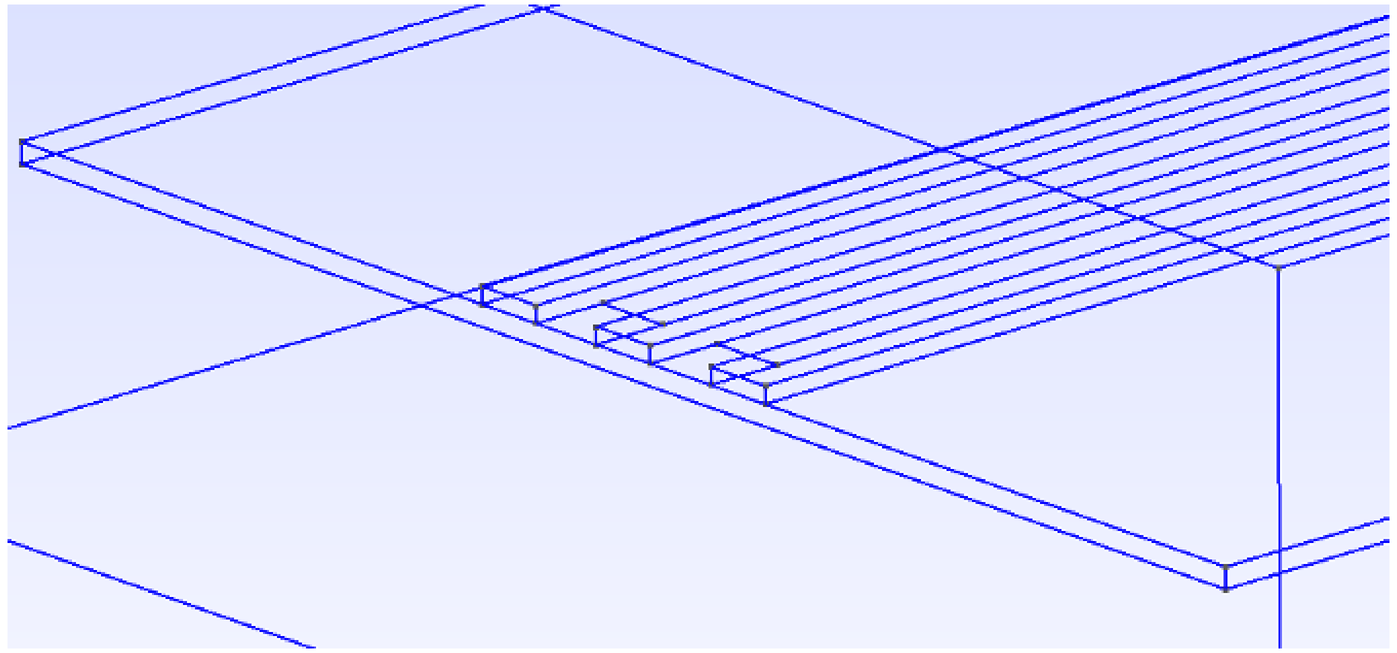
Lateral view Cross-section of the chip

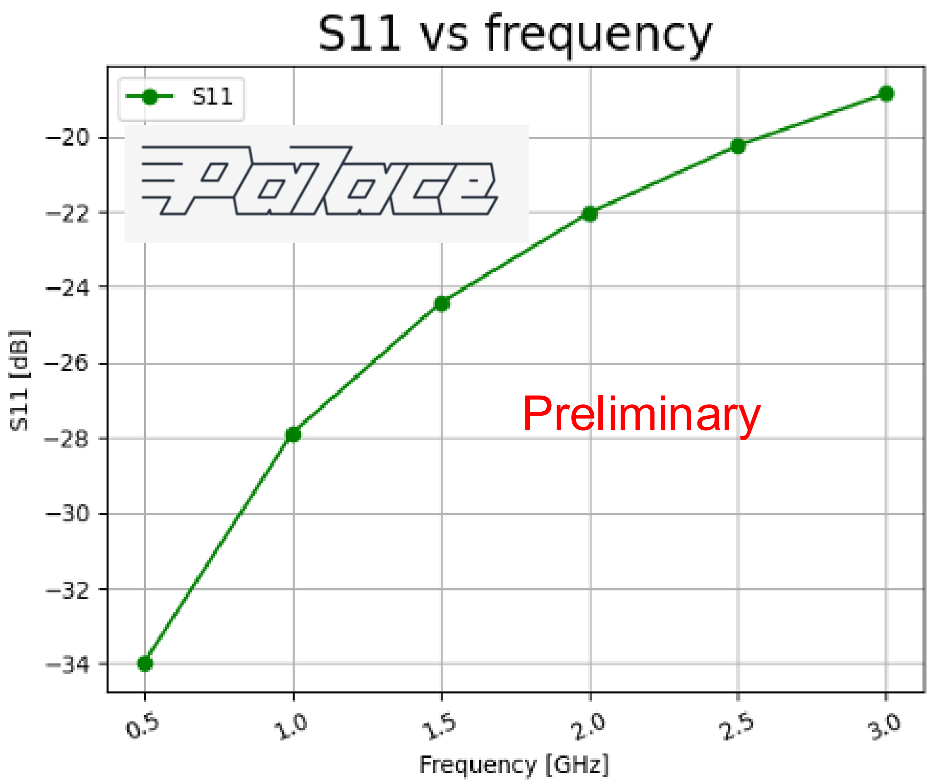


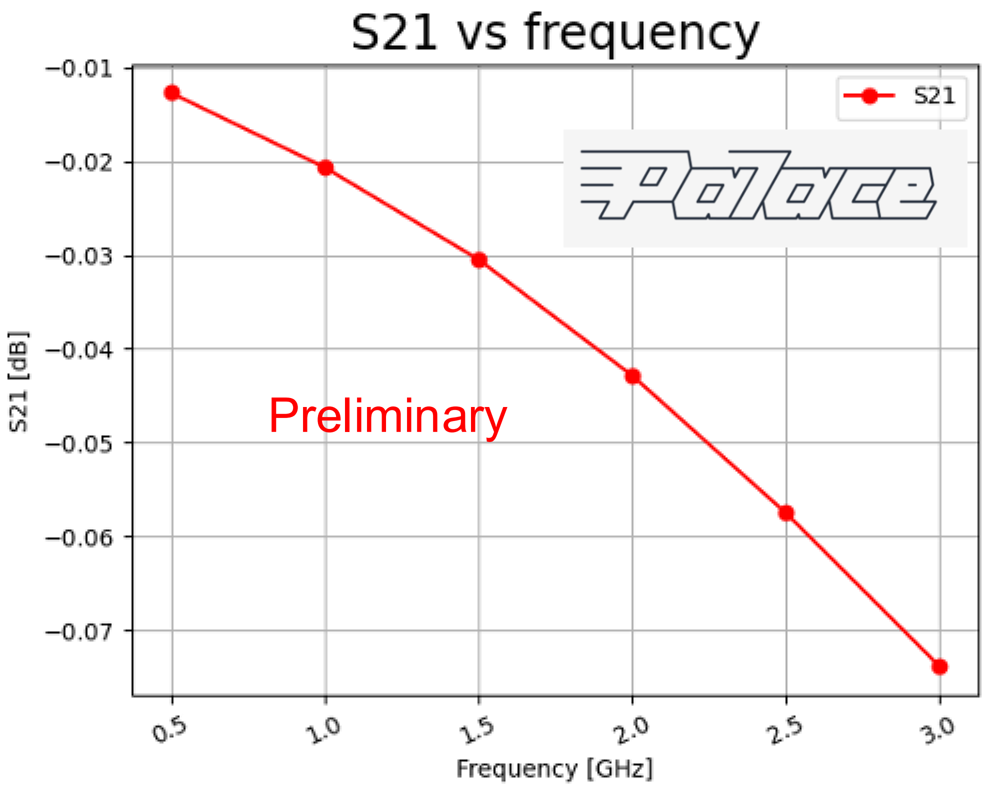
ASIC defect correction

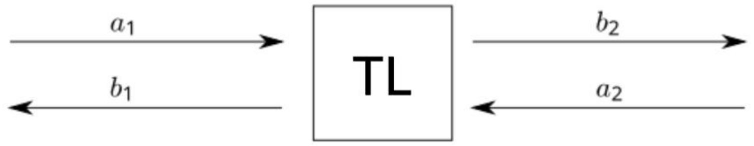
Ongoing R&D
FEM simulations











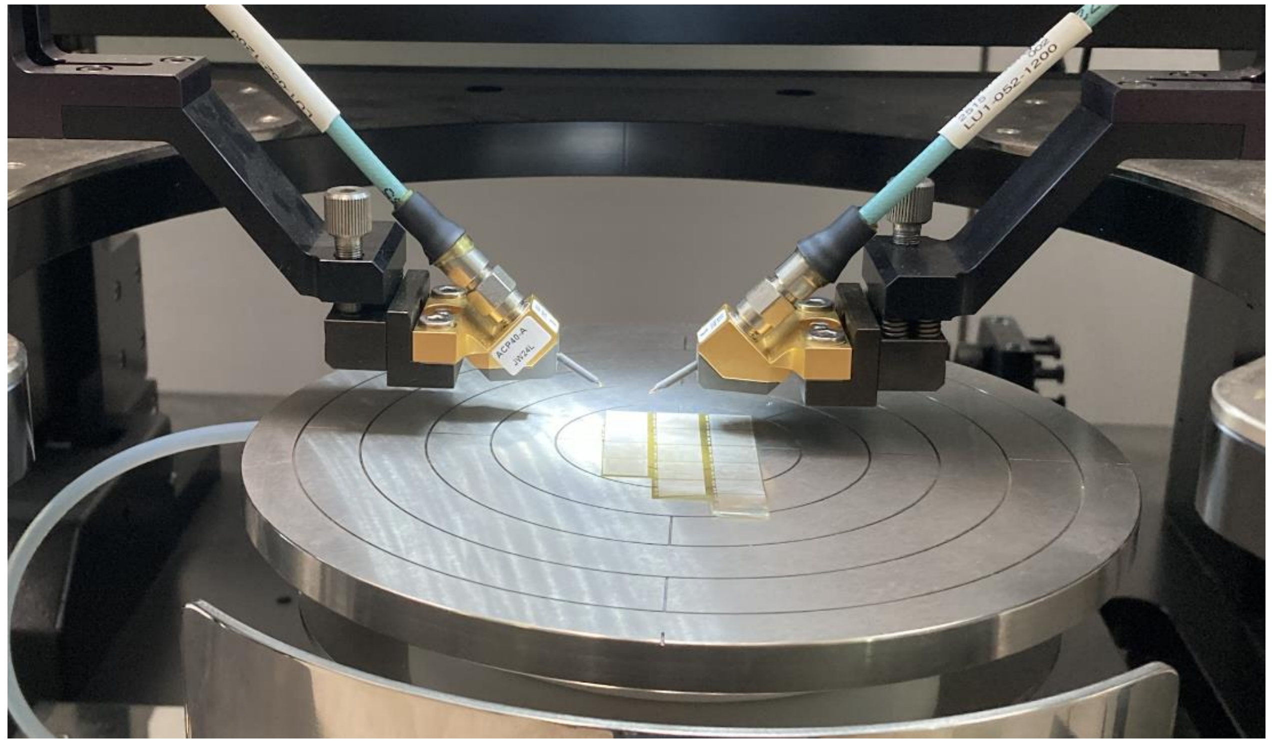
$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$

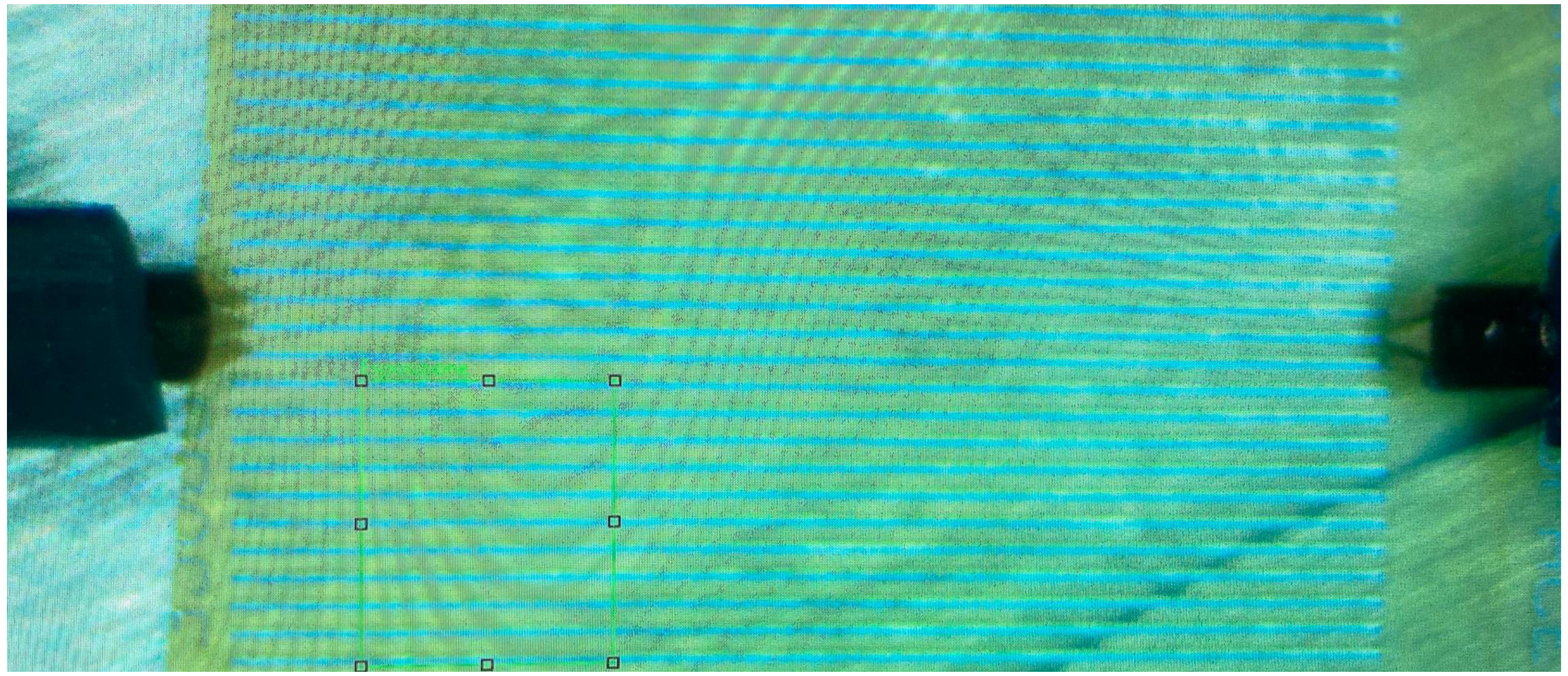
$$S_{11} = \frac{b_1}{a_1} = \frac{V_1^-}{V_1^+}$$

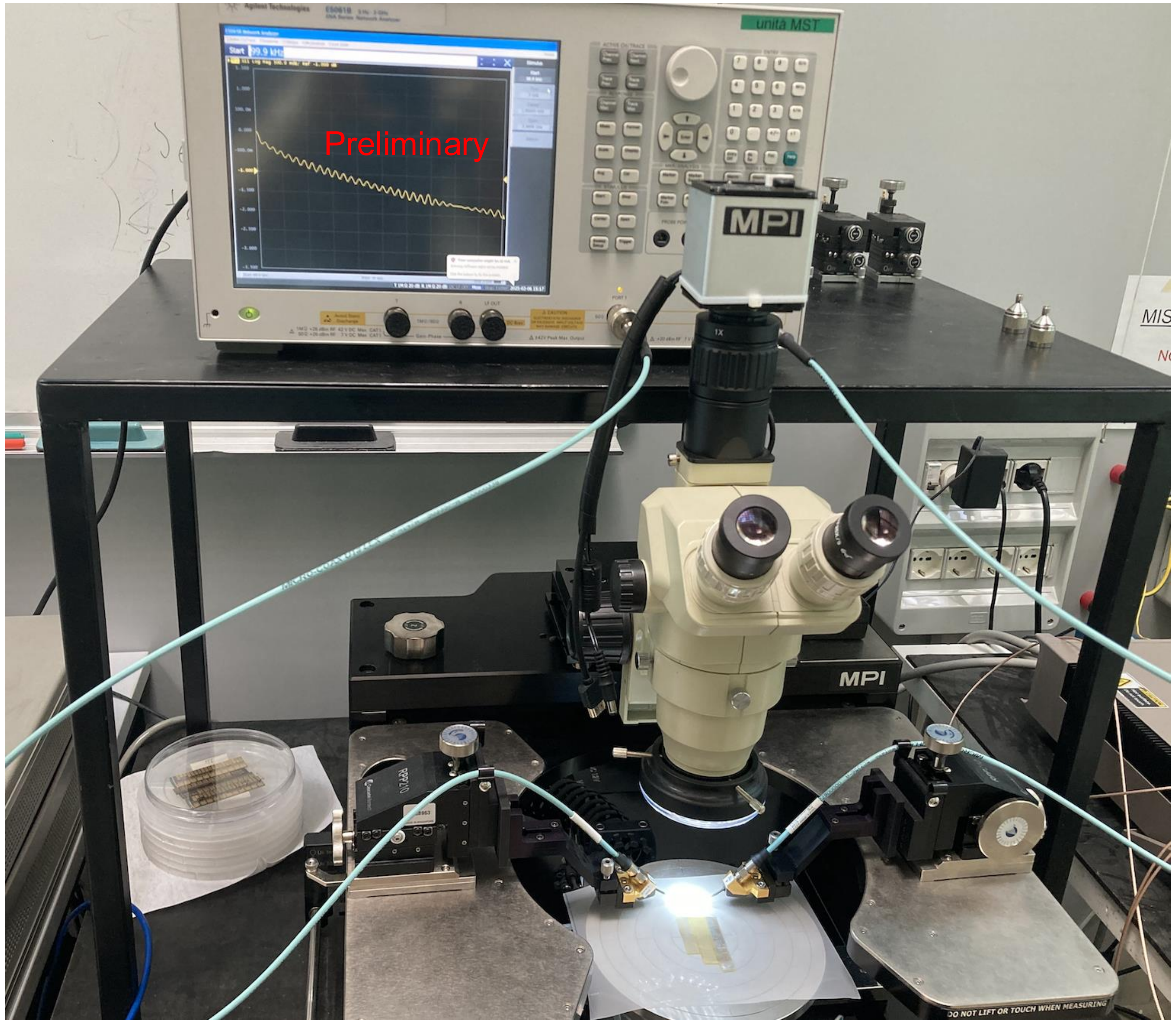
$$S_{21} = \frac{b_2}{a_1} = \frac{V_2^-}{V_1^+}$$

atlc2: Arbitrary Transmission Line Calculator
Palace: 3D Finite Element Solver for Computational Electromagnetics

Ongoing R&D
VNA measurements







VNA: Keysight E5061B 3 Ghz