MAX PLANCK SEMICONDUCTOR LABORATORY

Main Objectives of the project

- facilitate a distributed lab for **heterogeneous integration (HI)** of radiation detectors
  - interconnections/assembly of chips of various technologies/types:
    - **analogue + digital + memory + sensor + photonics + RF + MEMS …**
- integration technology survey and development
  - align currently available technologies within DRD7.6b labs
  - identify required new process steps, install and qualify these steps (or find and qualify external suppliers)
- define, practice, and qualify distributed process flow
- provide HI ”service” to detector community

heterogenous integration

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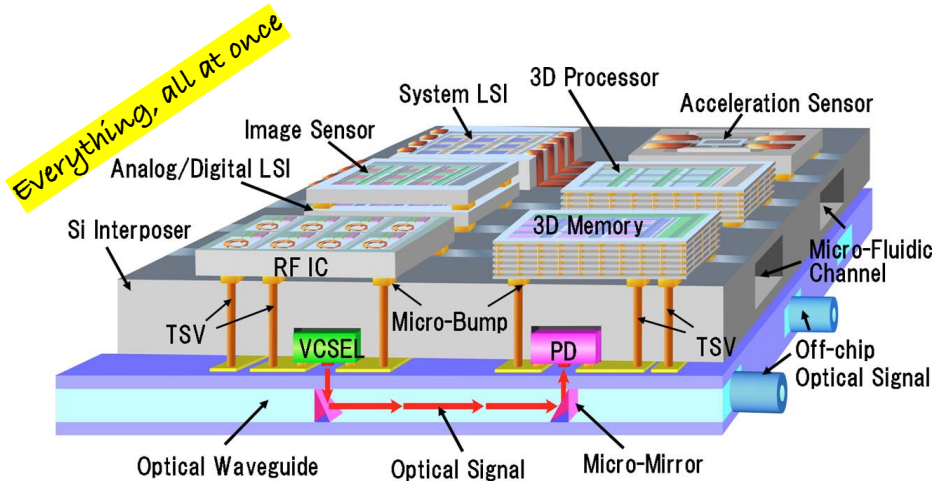
- **Very active field of R&D in industry**
  - Players are foundries and OSATs (**O**utsourced **S**emiconductor **A**ssembly and **T**est)
    - Intel/AMD/TSMC/Samsung.. and ASE/SPIL/Amcor...
    - See IEEE EPS Heterogenous Integration Roadmap
  - Large variety of technologies, solutions, techniques (and acronyms..)
    - Mostly proprietary, limited accessibility or expensive (for low volume production)

- There are extreme examples, mostly experimental:



Lee et al.: IEEE Transactions on Electron Devices (March 2011), **DOI:** 10.1109/TED.2010.209

- **Attempt to break it down in smaller pieces - easier to digest**

Technology building blocks overview

- **Interposer**
  - single sided
  - double sided → TSV
  - interposer with micro-channels
  - optical interposer

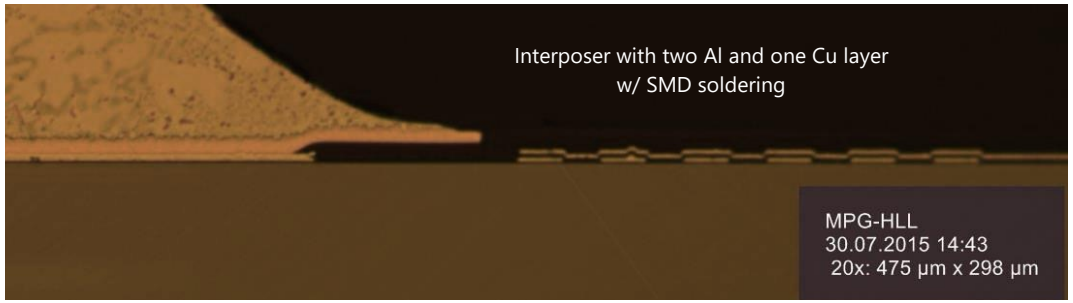
- **Assembly preparations**
  - Thinning of CMOS, Sensor, and/or interposer
  - Post-processing on Wafer level and chip level
    - std. solder bumps (“C4”)
    - µ-bumps w/ different metallurgy
    - Cu or Sn ep for SLID or hybrid bonding

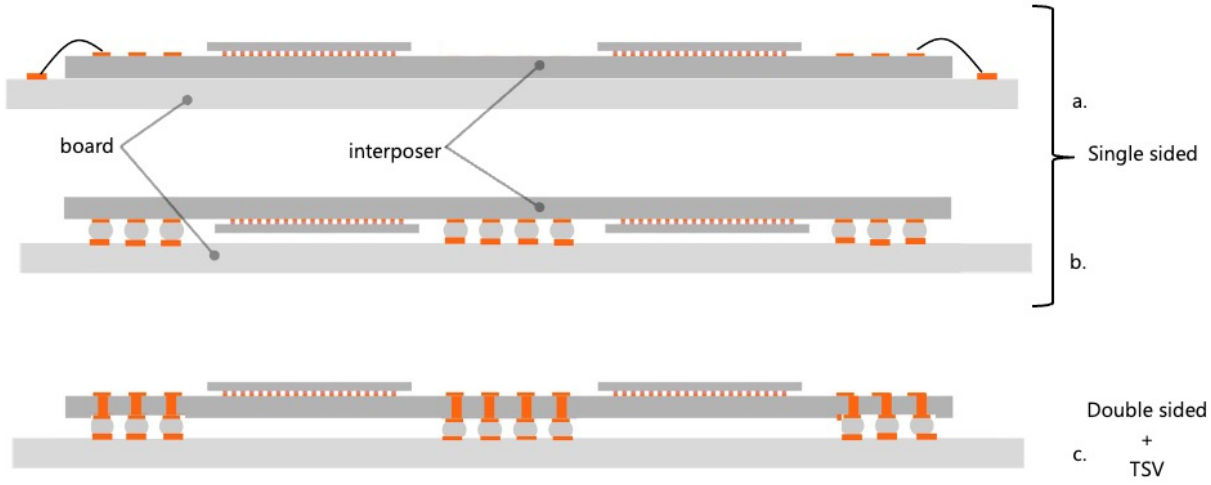
- **Assembly**
  - SMT passives
  - conventional bump bonding (flip-chip) – C2C
  - Bump-less interconnect
    - SLID - C2W, W2W
    - Hybrid bonding – C2W, W2W

Interposer

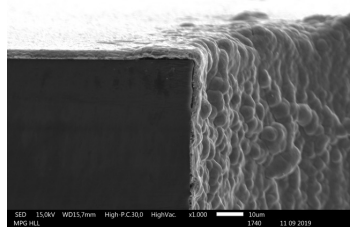
- Geometry and material
  - Few cm^2 to 6" and 8" wafer scale substrates
  - Preferably silicon wafers

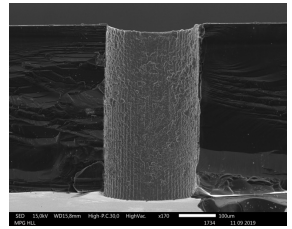
- Metal system (single sided)
  - State of the art at HLL
    - M1 and M2 is Al, 1µm, low temp. SiO_2 as ILD
    - LM Cu, 5 µm, BCB as ILD and for planarization
  - Impedance control
    - ground planes (implant or add. metal layer)
    - lowK dielectrics?
  - Design rules to be defined ← **application input**
    - line/space for leads, via sizes for ILD layers
- TSVs
  - Via formation
    - through via or blind via → req. thinning and CMP
    - Bosch Process or Laser
      - depth and diameter defined by max aspect ratio
    - Via first or via last
      - Defines required isolation (oxidation/HTO/LTO)
  - Via filling
    - Ep-Cu, liner or complete? ← aspect ratio
  - Back side metal
    - Cu RDL



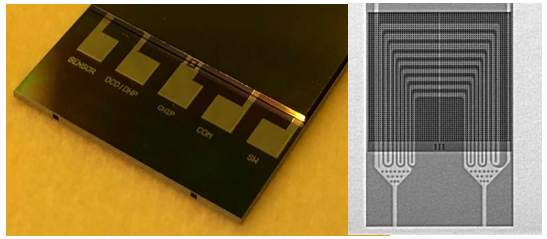


TSV feasibility test at HLL



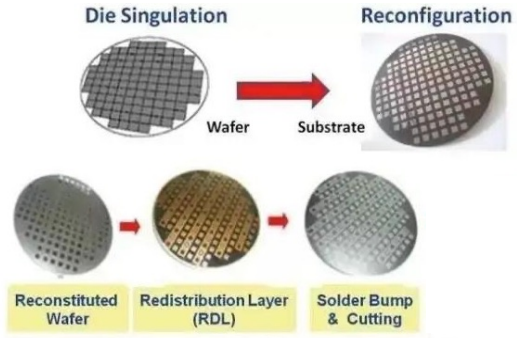


Interposer w/ micro channels at HLL

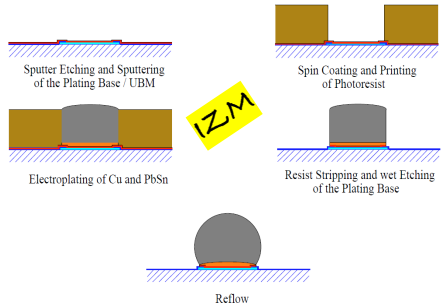


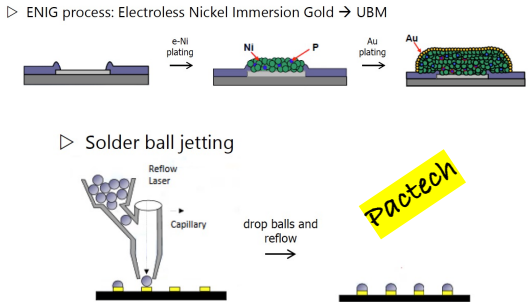
Post-processing

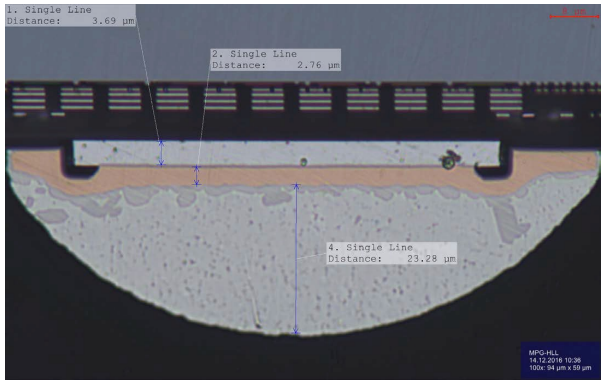
- Thinning of chips and wafers (CMOS and interposers)
  - External process services, network established, various suppliers: Disco, Optim, IZM...

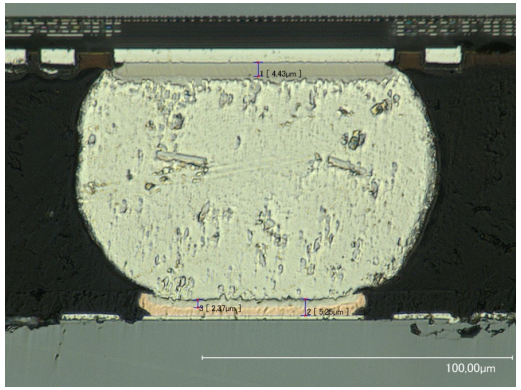


- Post-processing of CMOS – RDL/UBM
  - Wafer level re-passivation, Cu RDL, UBM
    - "In-house" on up to 8" wafers: HLL, ??, ??
  - Chip level
    - Possible, but needs R&D: **reconstitution of wafer**, then wafer level process
      - **Key technology** also for bumping, C2W bonding, **HLL interested**
- Bumping
  - Wafer level bumping possible via external services (Pactech, IZM ..)
    - need various solder alloys with different reflow temperatures
      - Towards smaller pitches, Cu pillars ← **application input**
      - availability of "in-house" bumping technology?? Where??
  - Chip level bumping
    - After wafer reconstitution (see above)
    - Single solder ball jetting (Pactech) on chip level → KIT??, elsewhere?
      - Requires still UBM (through mask, mask-less, or Au stud..)









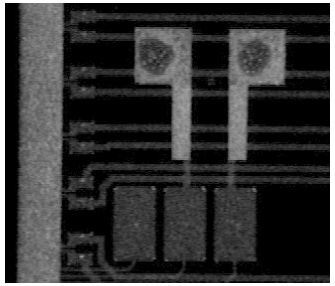
- Preps for bump-less interconnect
  - Wafer and chip level, similar to RDL topic
  - for SLID
    - Re-passivation and Cu/Sn plating
  - For hybrid bonding
    - Re-passivation, Cu plating, Cu-CMP

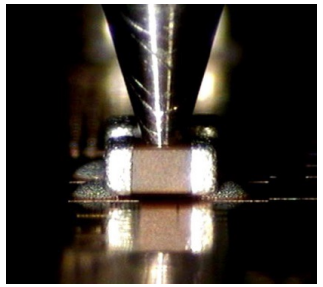
Assembly

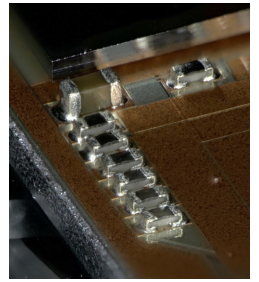
- Passives on interposer
  - Mount SMD components (R,C,L) and Si chip capacitors
    - Solder paste dispense – place SMD – common reflow
  - Available “in-house”: HLL, ??, ??, ??

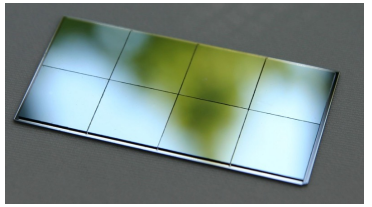
- Conventional bump bonding
  - Flip-chip with solder bump connection (flux-less / flux / underfill)
    - Pitch >50 µm, chips with bumps from different sources on interposer
  - Available “in-house”: HLL, ??, ??, ??

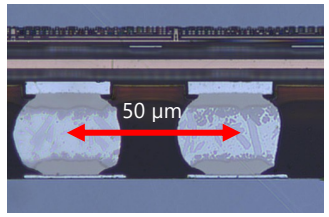
- Bump-less interconnections (→ higher interconnect density)
  - Cu pillars with Sn cap
    - To be discussed
  - Solid Liquid Interdiffusion, SLID
    - Eutectic bonding of C2W or reconstituted W2W
    - Fraunhofer, “in-house”??, some experience at HLL
  - Hybrid Bonding
    - Direct Cu-Cu interconnect based on CTE difference between Cu and SiO2
    - W2W, reconstituted W2W, experimentally even C2W or C2C
    - Process line to be installed end 2025 at HLL
    - Challenging preparations before bonding
      - High planarity, and smooth and clean surfaces required
      - External CMP tests and first qualification runs planned early 2025
      - Open for collaboration (Cu and Oxide deposition, CMP)

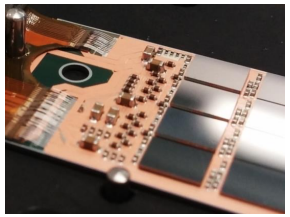


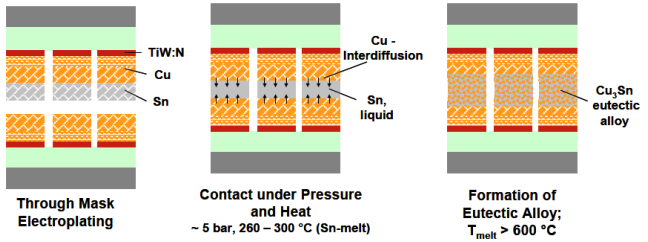


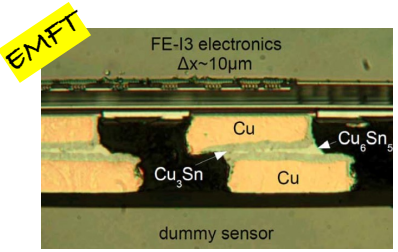


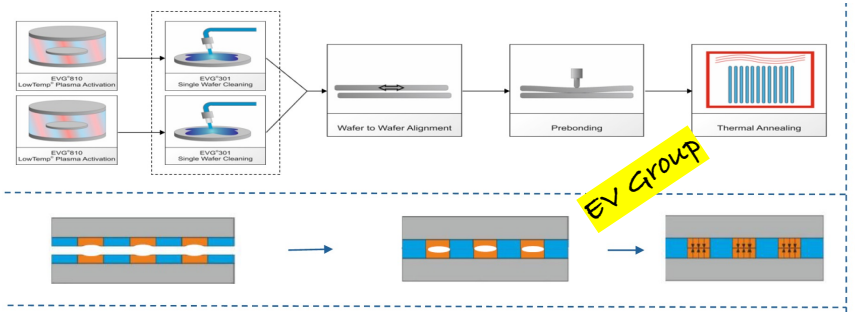












the next steps – the original proposal

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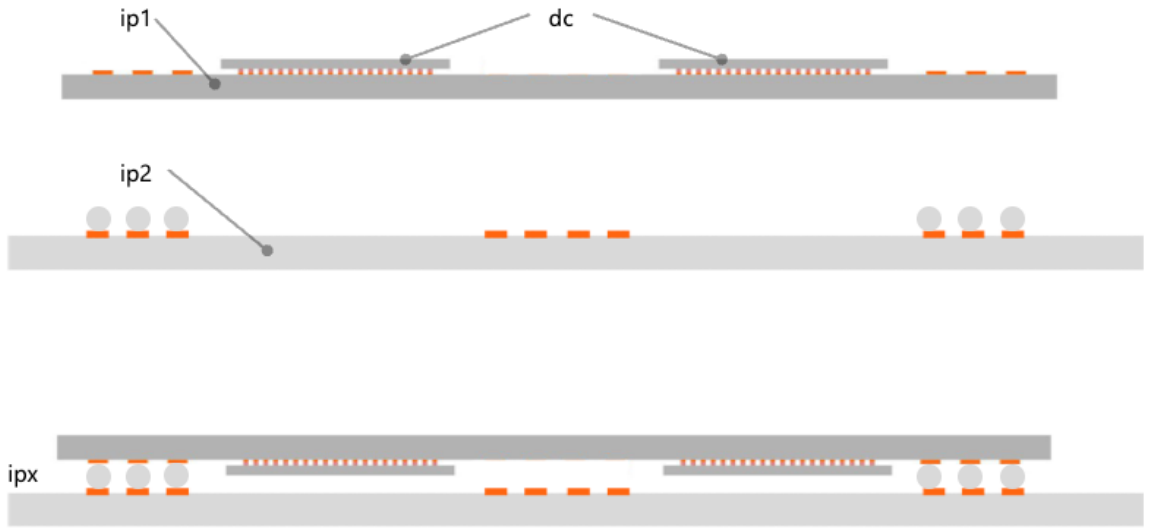
- **Joint project: complex silicon interposer**
  - Interposer 1 – "ip1"
    - Single sided metal Al/Cu
    - Bumped dummy chips with Al/Cu - "dc"
      - small, high melting solder bumps, or Sn cap for SLID
      - thinned to ~100 µm
    - Bump bond or SLID dummy chips to ip1
  - Interposer 2 – "ip2"
    - Single sided metal Al/Cu
      - big, low melting solder bumps
  - Flip and assemble ip1 and ip2 - "ipx"
    - Evaluate daisy chains, process characterization ....



- TSV pre-development at various sites
  - HLL, KIT ...
    - Need project plan with milestones: via formation – isolation – via filling ....
- Wafer reconstitution
  - HLL, ...
    - Need project plan with milestones: fabrication of test vehicles - adhesive candidates – placement – alignment - temperature stability – debonding ....
- Hybrid bonding pre-development
  - HLL in cooperation with equipment manufacturer EVGroup, ...
    - Need project plan with milestones: fabrication of test vehicles – CMP – alignment – bonding ....

the next steps – more realistic

- **Joint project: complex silicon interposer**
  - Interposer 1 – “ip1”
    - Single sided metal Al/Cu
    - Bumped dummy chips with Al/Cu - “dc”
      - small, high melting solder bumps, or Sn cap for SLID
      - thinned to ~100 µm
    - Bump bond or SLID dummy chips to ip1
  - Interposer 2 – “ip2”
    - Single sided metal Al/Cu
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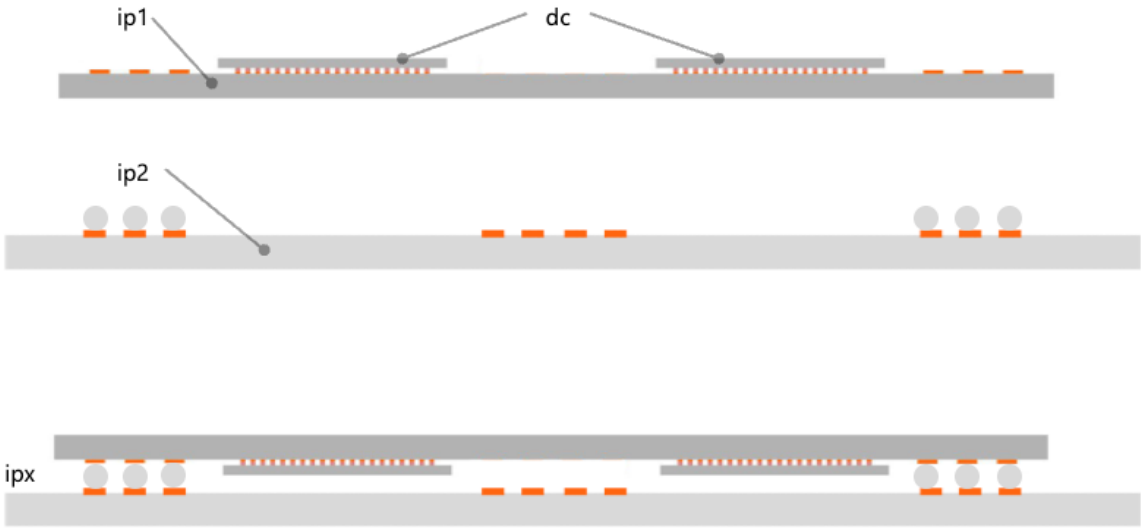
  - Flip and assemble ip1 and ip2 - “ipx”
    - Evaluate daisy chains, process characterization ....

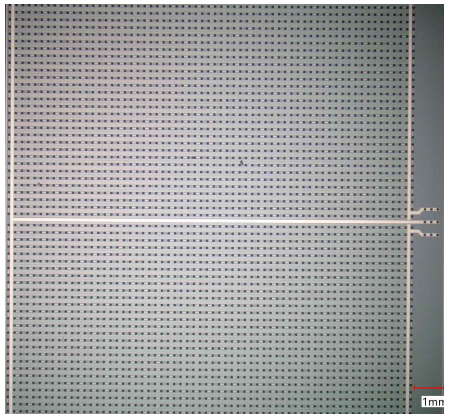


- pretty ambitious!
  - need thin dummy chips, two different solder alloys ....
  - takes quite some time to get results!

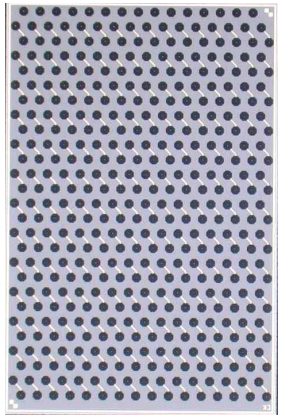
- **intermediate step**: heterogenous integration of **existing chips** on interposer
  - “only” tasks would be interposer production and bump bonding
  - add a few passives maybe

What's available

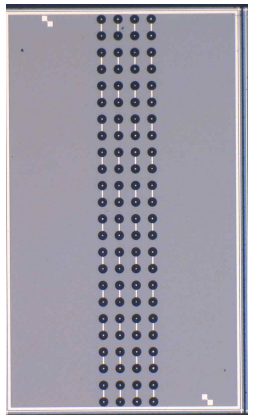
- various bumped dummy chips from past projects



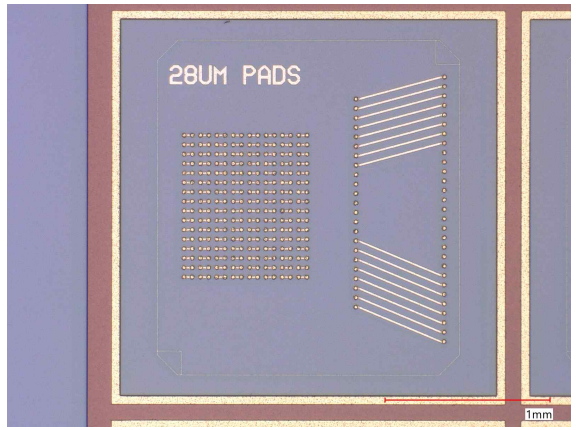
- 14x15 mm2 chip
- 64x64 SAC305 bumps
- bump pitch ~220 µm



- 3x5 mm2 chip
- 431 SAC305 bumps
- bump pitch ~200 µm



- 1.5x3.6 mm2 chip
- 96 SAC305 bumps
- bump pitch ~150 µm

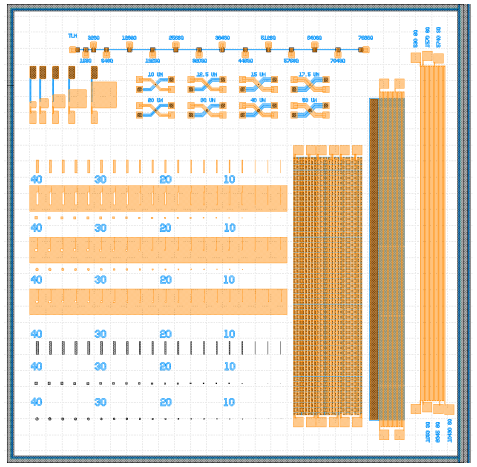


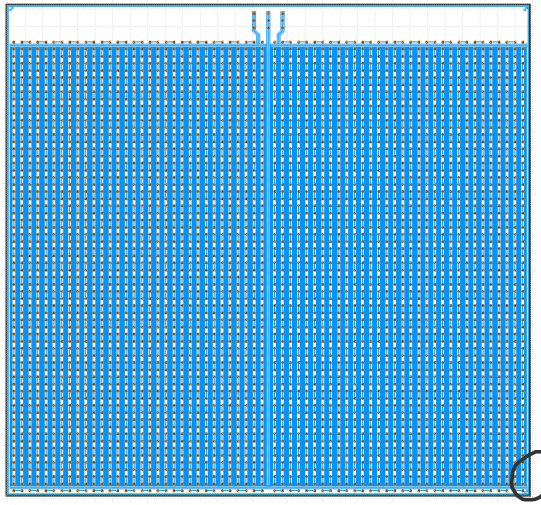
- 2.4x2.4 mm2 chip on wafer
- 16x16 SAC305 bumps
- bump pitch 50 µm

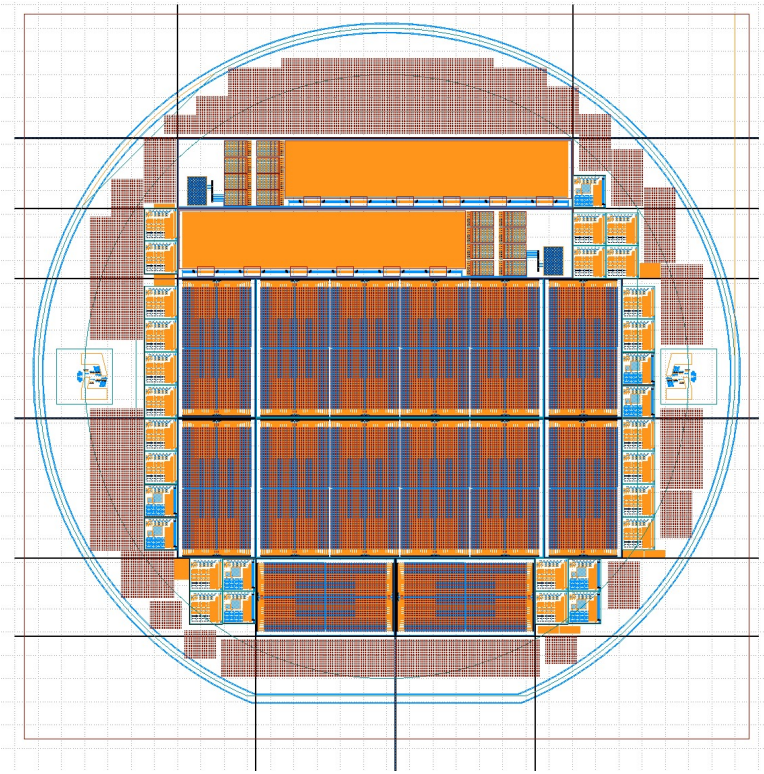
- O(50) chips of each type available → we should use them!

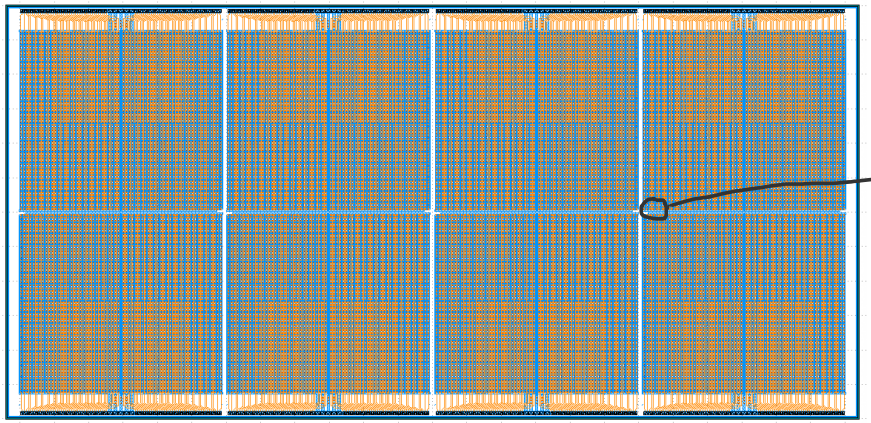
Interposer Wafer - example

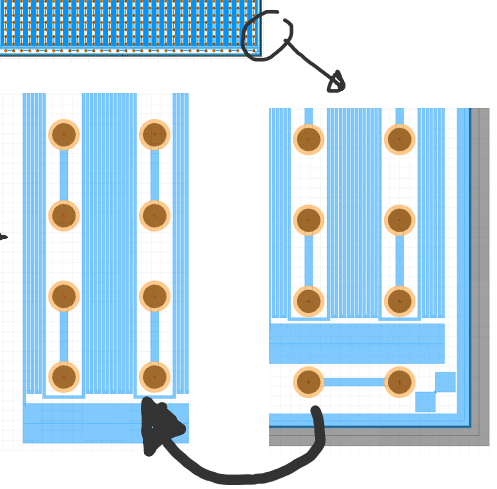
- Similar projects have been done in the past
- basic technology: Si wafer, ~ 500 nm Oxide, Alu, BCB, Cu
- various interposers on one wafer
- technology test structures

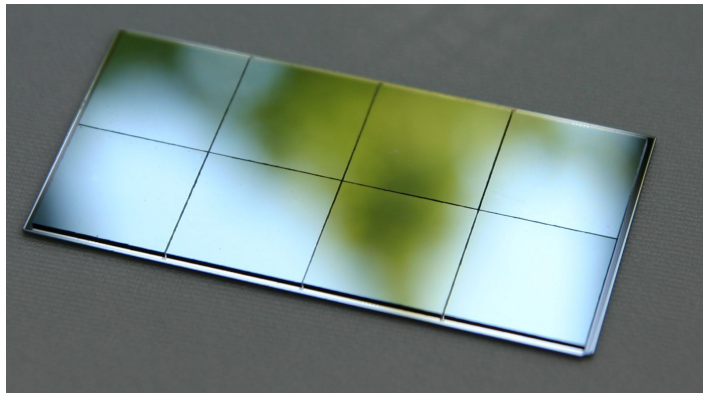








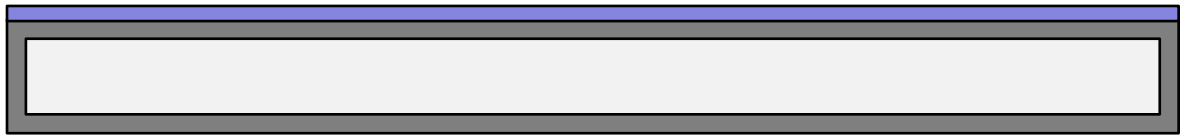




Interposer Process sequence I

- Thermal Oxidation
  - ~500nm wet or dry thermal oxide

- Al sputter
  - 1 µm Alu
  - sheet resistance ~30 mOhm/sq

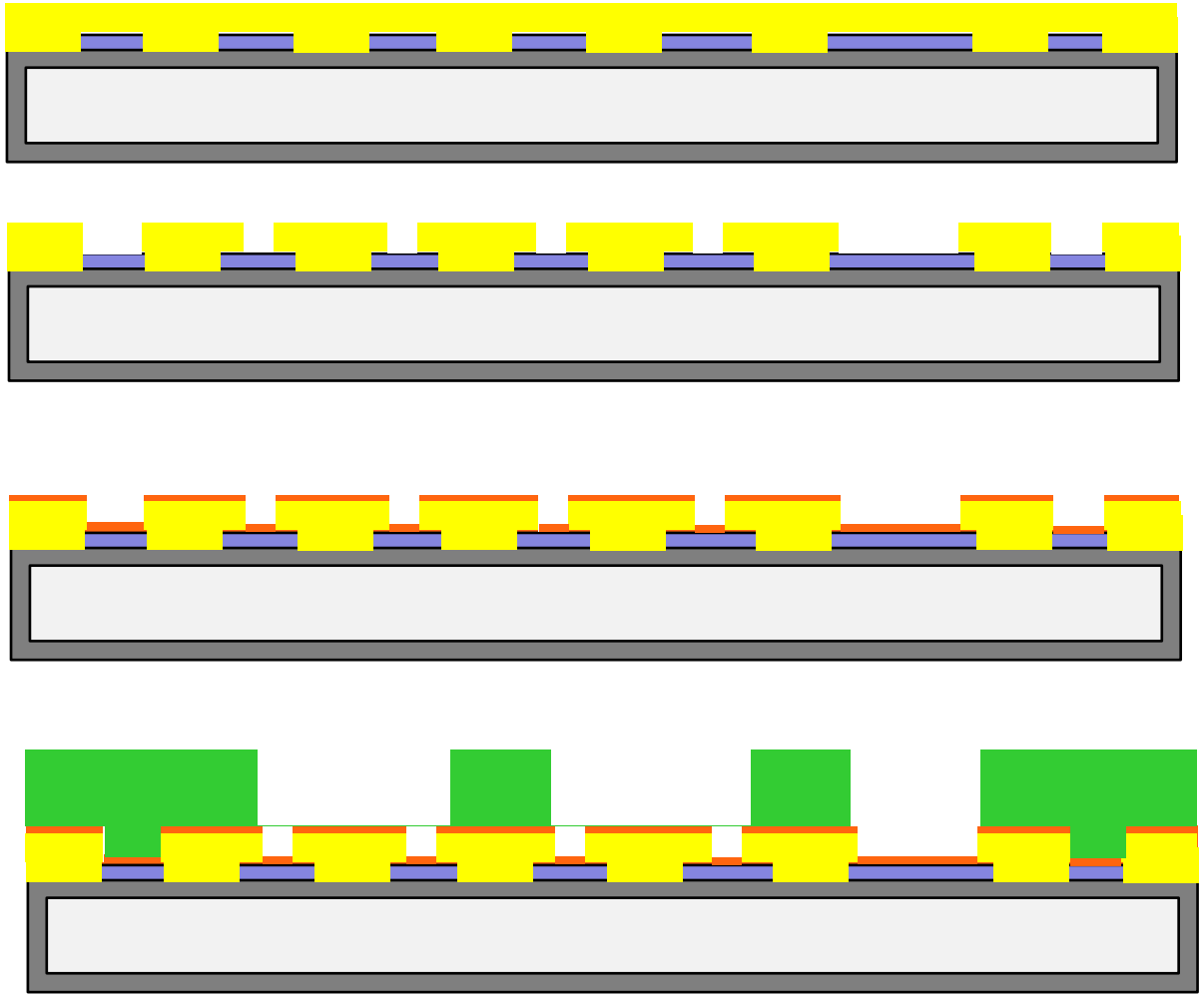


- Litho alu1
  - spin-on std. thin photo resist
  - **expose mask 1**, develop

- Etch Al
  - std. acid
- resist strip (solvent)

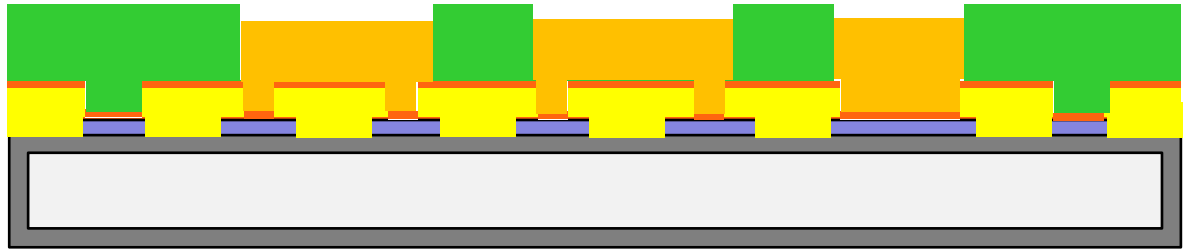
Interposer Process sequence II

- Interlevel Dielectric ILD1
  - deposition temp < 350 °C
  - LTO or similar
  - BCB - photo sensitive polymer (preferred)
    - coat 3 µm, **expose mask 2**, develop
    - hard bake at ~200 °C
    - descum contact holes in CF4 plasma
    - eps_r (BCB) = 2.65 @1 MHz
- Ti:W /Cu sputter seed layer
  - 100 nm/200 nm
- ep Litho
  - spin-on thick ep photo resist, ~7-9 µm
  - **expose mask 3**, develop



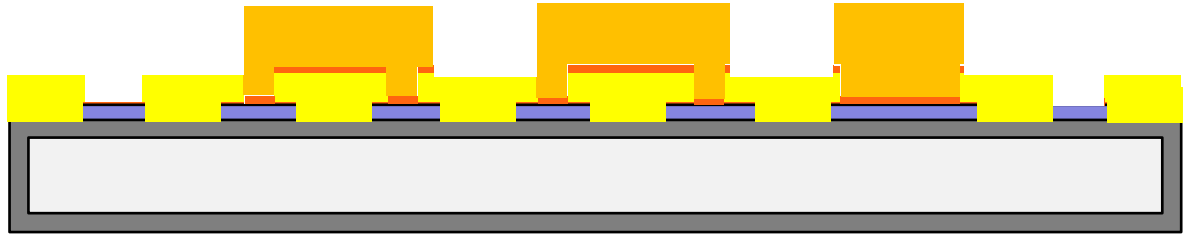
Interposer Process sequence III

- Through mask electro-plating
  - Cu, about 5 µm
  - sheet resistance for 1µm Cu ~17 mOhm/sq.



- resist strip
  - solvent

- seed layer etching
  - Cu and Ti:W etch, selective to Al



Interposer design and layout started by Michele