Post-processing, Assembly, and interconnection at MPG HLL: Status and Plans

- Who we are
- What we did
  - ↳ Interconnect and assembly
- Where we go

Ladislav Andricek

for the team at the Semiconductor Laboratory of the Max Planck Society

The Semiconductor Lab of the Max Planck Society – MPG HLL

2000 – 2023 @ Siemens Campus Neuperlach Munich

- 1000 m² of clean room area
- 330 m² of ISO 3 area
- Full 6 inch silicon process line

Central facility of the Max Planck Society

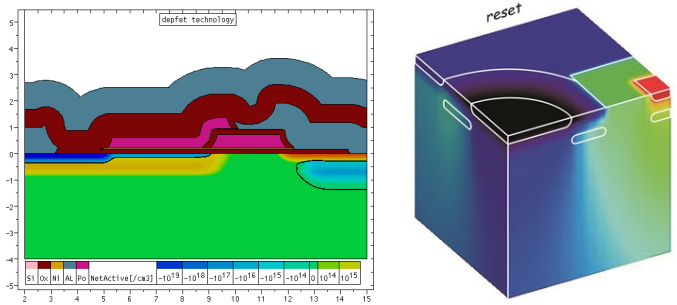
with ~40 employees

scientists, engineers, technicians, and students

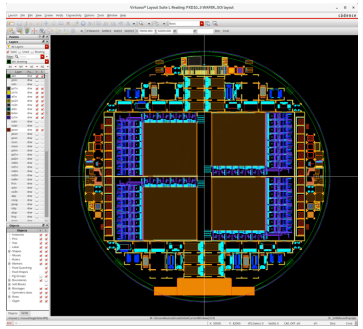
From 2024 @ Research Campus Garching

- 1500 m² of cleanroom area
- 600 m² of ISO 3 & ISO 4 area
- 8 inch silicon process line

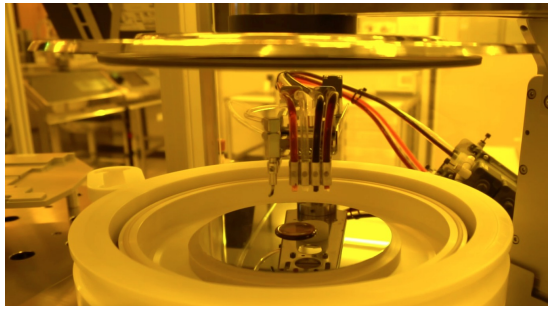
Process and Device simulation, 2D and 3D



State-of-the-art layout tools



In-house fabrication



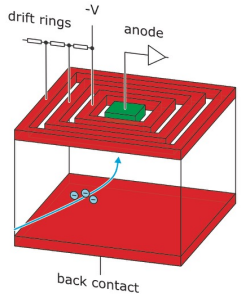
System assembly

- sensor design and fabrication
- interconnection, assembly
- system/camera design and test

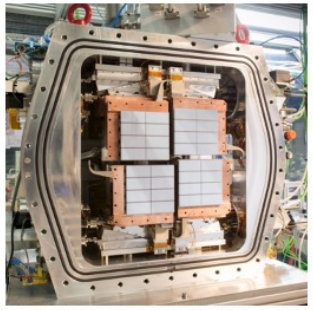
System test and evaluation

A selection of large detector projects - past and present

▷ Silicon Drift Detector

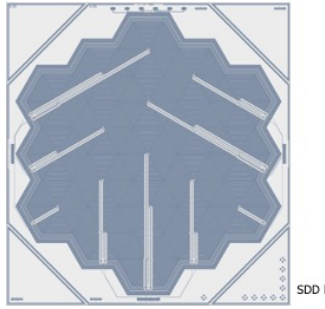


Mini SDD - DSSC @ EuXFEL
(imaging of X-ray diffraction patterns)



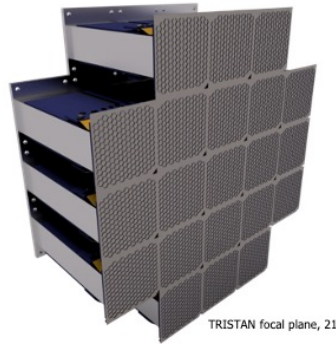
M. Porro et al., *The MiniSDD-based 1-Megapixel Camera of the DSSC Project for the European XFEL*, IEEE TNS 68(6), pp. 1334 - 1350, June 2021

eXTP (enhanced X-ray Timing and Polarimetry)
SFA (spectroscopic focusing array)
(fast time-resolved X-ray spectroscopy)



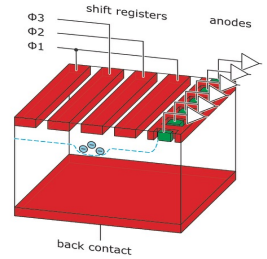
SDD layout plot

TRISTAN (tritium sterile anti-neutrino) @ KIT
sterile neutrino search by electron spectroscopy

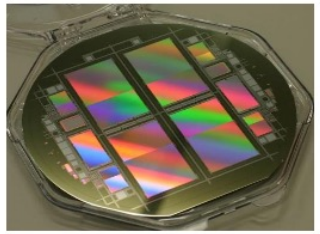


TRISTAN focal plane, 21 modules.

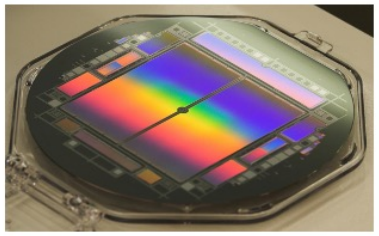
▷ pnCCD



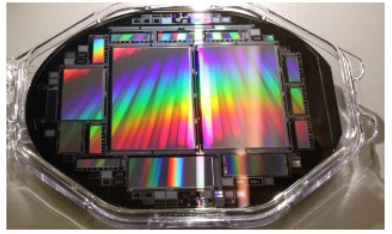
eROSITA
X-ray imaging & spectroscopy



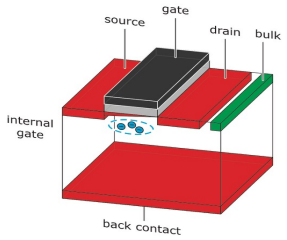
CAMP / LAMP
Soft x-ray camera for Photon science



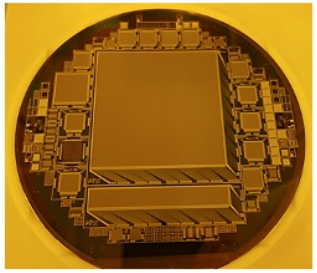
FSP – TNG for MAXIMUS
Fast Small Pixel – The Next Generation



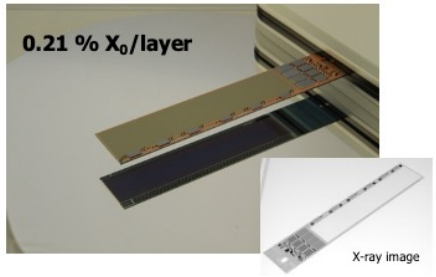
▷ DEPFET



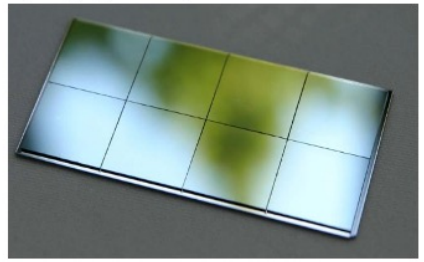
ATHENA Wide Field Imager
the **A**dvanced **T**elescope for **H**igh-**En**ergy **A**strophysics
as ESA's next-generation X-ray astronomy observatory



BELLE II pixel detector
High energy particle vertexing

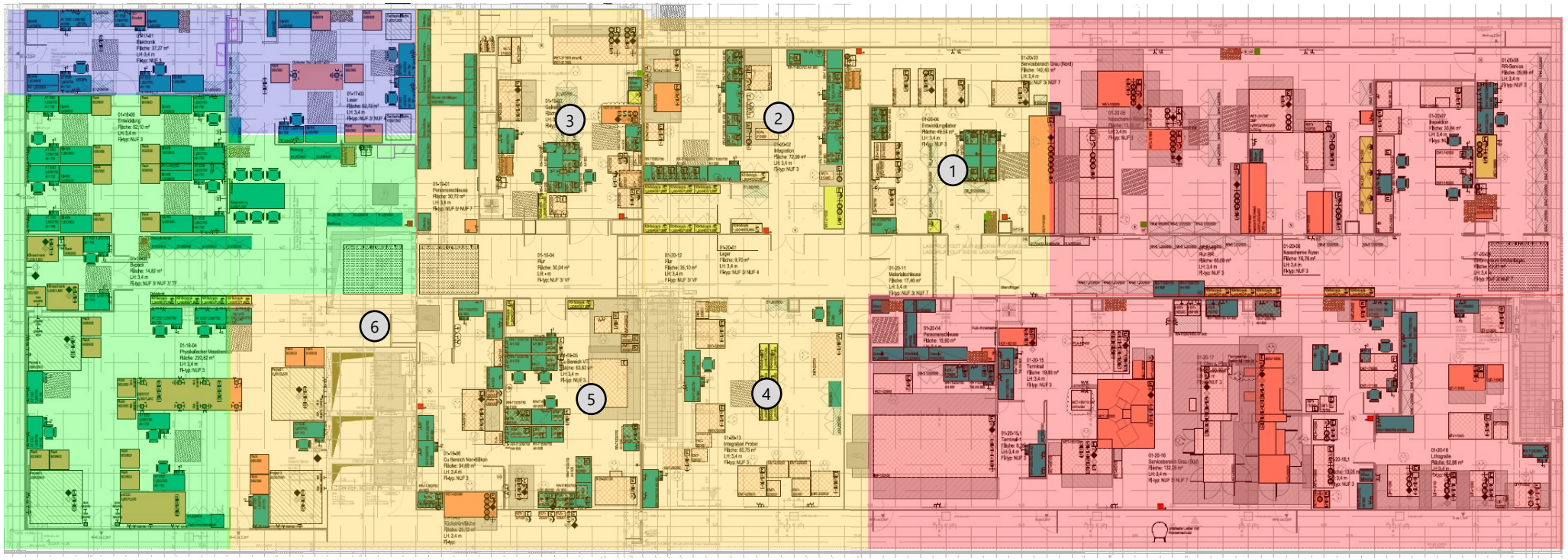


DSSC @ EuXFEL
DEPFET **S**ensor with **S**ignal **C**ompression
(imaging of x-ray diffraction patterns)



Inside HLL – 1500 m² lab space

▷ Electronics and Laser Lab



▷ ISO 8
- ↳ System development and test

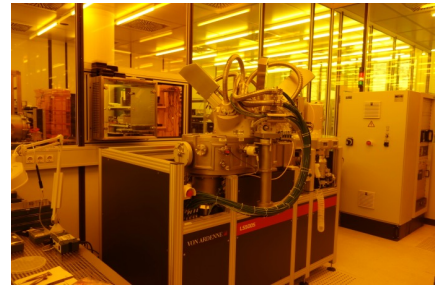
▷ ISO 4 - 6
- ↳ **1**: R&D Lab and post-processing of external wafers
- ↳ **2**: Singulation, wire bonding and assembly
- ↳ **3**: Cu Lab (UBM and RDL)
- ↳ **4**: Wafer-level test and characterization
- ↳ **5**: Vertical integration (flip-chip and wafer bonding)
- ↳ **6**: Quantum Lab – MQV (shared with WMI/TUM)

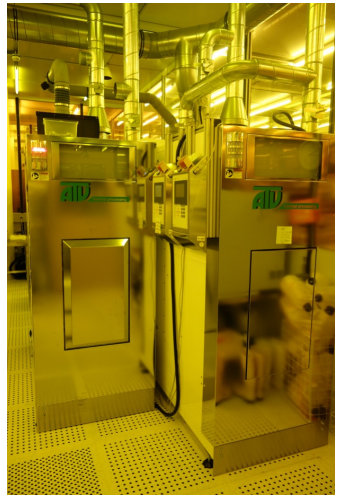
▷ ISO 3
- ↳ "CMOS line" adapted to fully depleted double-side processed silicon radiation sensors
  - ↳ implantation, thermal, metallization, lithography, wet/dry etching, cleaning, inspection ....
- ↳ Access only by qualified personnel
- ↳ Strict control of material inside

Post-processing and interconncet capabilities

- R&D Lab
  - Complete process line for small and experimental (test) projects
    - Pilot development of “non-standard” technologies with and on “non-standard” materials
    - Thermal processes, lithography, cleaning and wet etching, metrology
    - ICP-DRIE for TSVs and micro-channels being installed
    - Experimental sensors, test structures, micro-mechanics ...

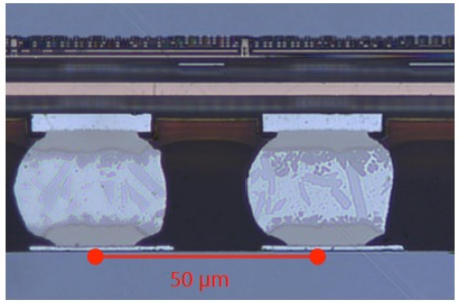
- Backend-of-line and interconnect Lab
  - Cu (and Al) redistribution layer (RDL), under bump metallization (UBM)
  - Wafer dicing, chip handling
  - Interconnect to read-out ASICs
    - Electrical: flip-chip, wire bonding, conductive adhesives
    - Mechancial: precision assembly of modules
    - Thermal: utilization of suitable materials (metals, ceramics, composite materials..)
    - Low temparature W2W, C2W, C2C bonding in preparation

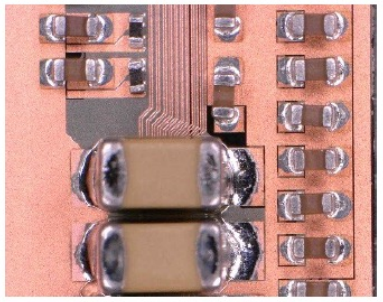




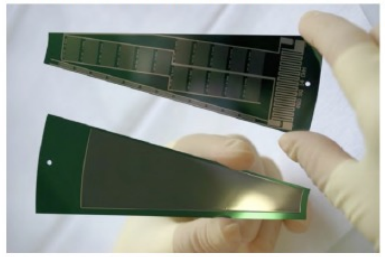
- Wafer format
  - All process tools set up for 6” wafers as baseline
  - 4” wafer processing possible, smaller wafers and even single chip processing with customized adapter wafers
  - 8” wafer processing after tool re-configuration, possible on most of the tools

A few pictures from past projects



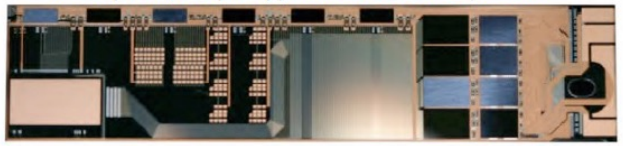


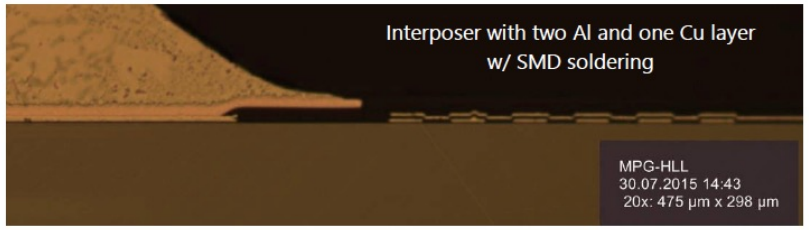
Thermo-mechanical modules

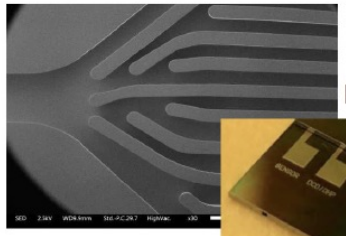


Thin Si with integrated heaters

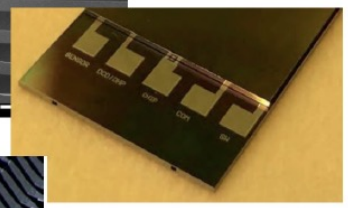
Si interposer /w flip-chipped ASICs and SMD passives



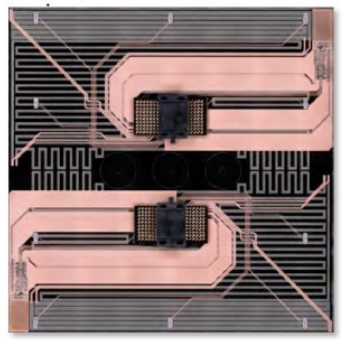


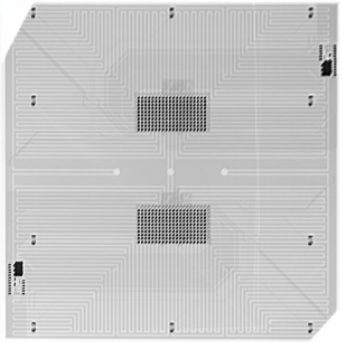


Micro-channel-cooling

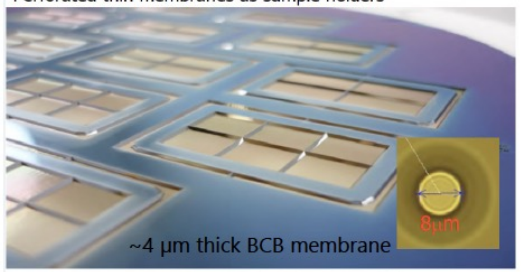


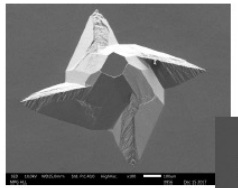
Interposer with integrated cooling channels

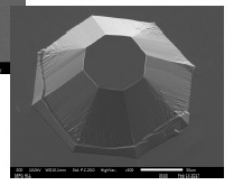




Perforated thin membranes as sample holders

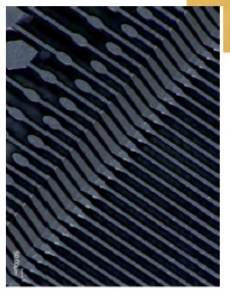


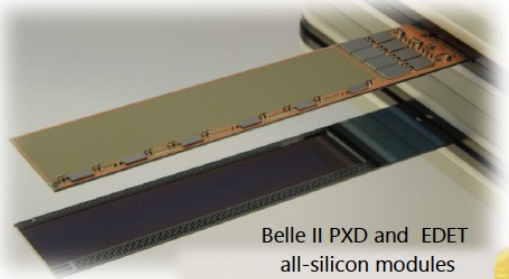




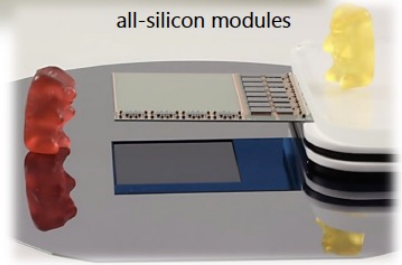
High purity Si pins
as crystal holders

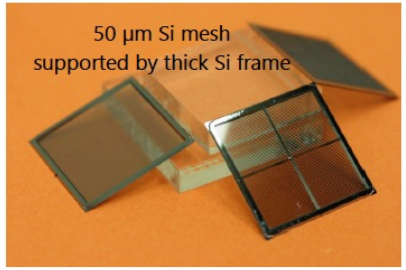
Metallization over
extreme
topography
"Molecular traps"

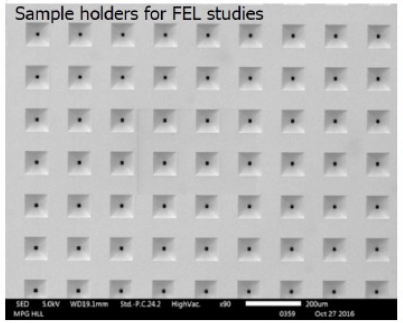


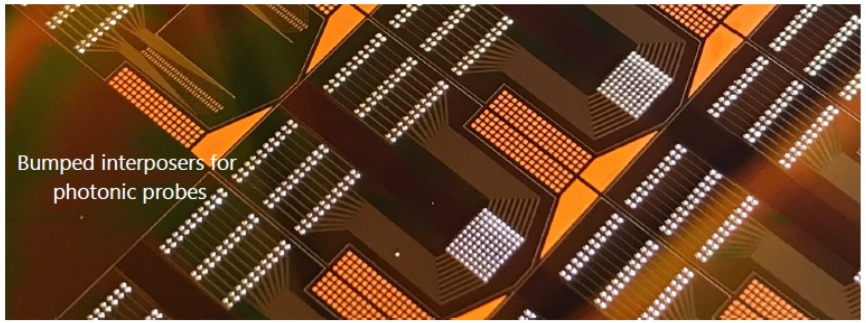


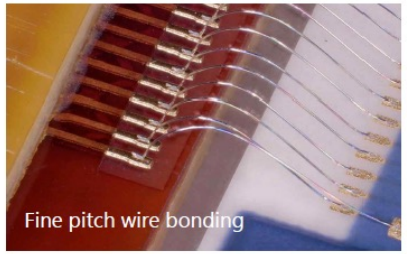
Belle II PXD and EDET
all-silicon modules





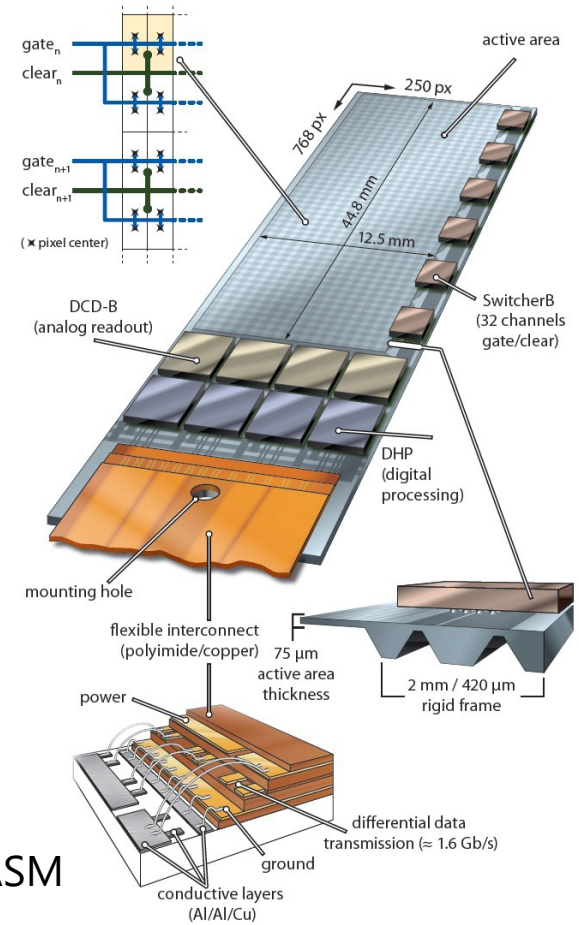


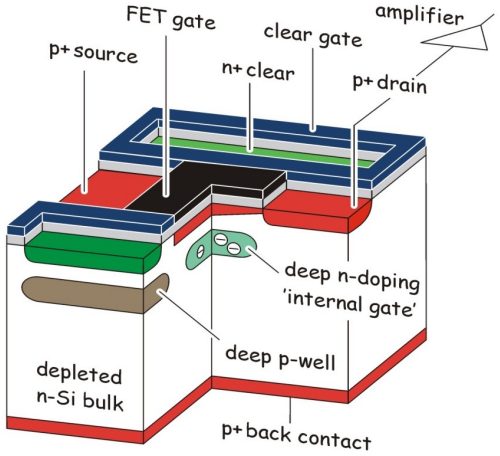


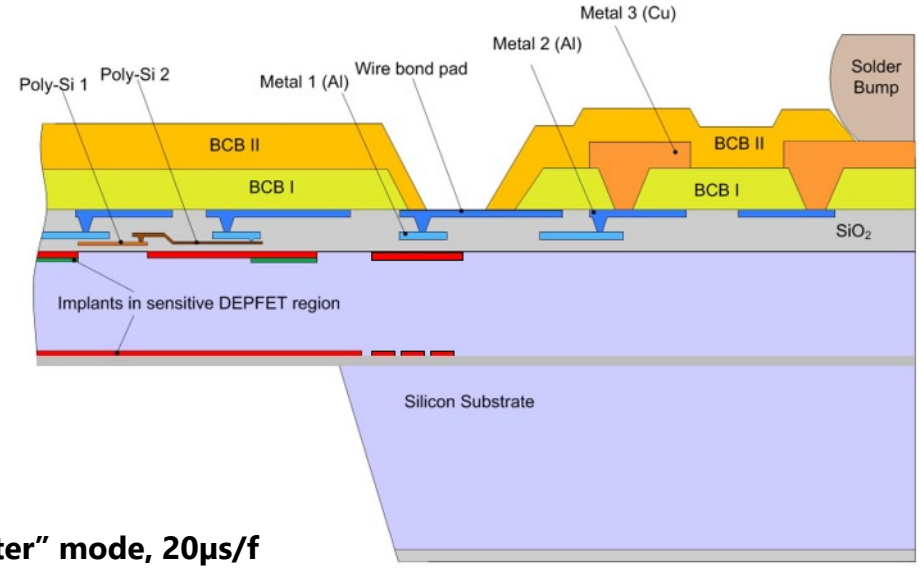


the DEPFET all-silicon module for Belle II PXD

- module design starts on wafer level
- module is one piece of silicon
  - Sensitive area (APS)
  - High density interconnect (HDI)
- HDI as board for non-sensor parts
  - UMC 180, TSMC 65, IBM/AMS/TSI 180
  - Passive components
  - On-module solder interconnect
- Off-module interconnect with flex
  - Solder and wire bonds
- "MCM-D", "2.5 D", "SoC" ... We call it ASM







All-Silicon Module

- **Thin pixel array operated in „rolling shutter" mode, 20µs/f**
  - **Only 4/768 rows active a time → low power in active area**

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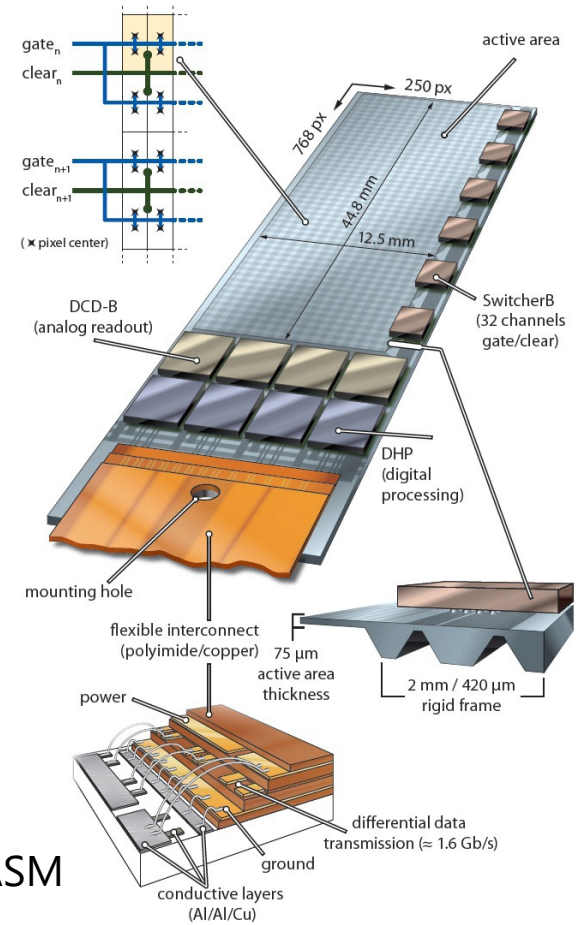
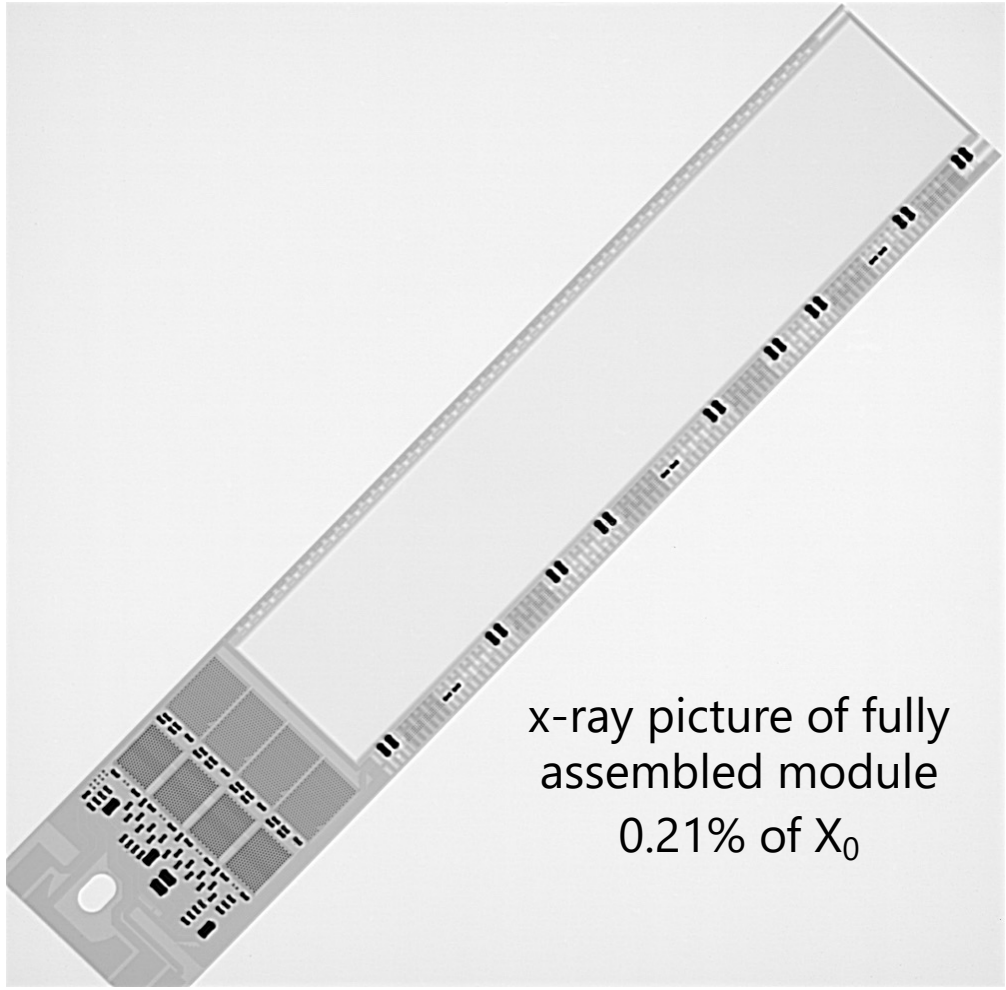
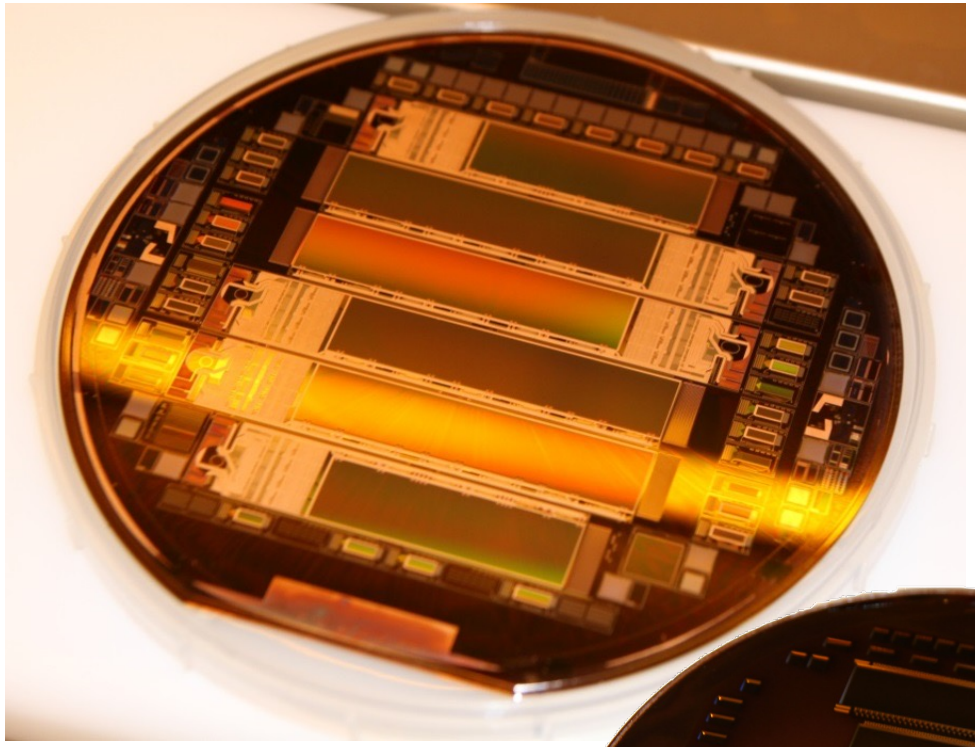
All-Silicon Module

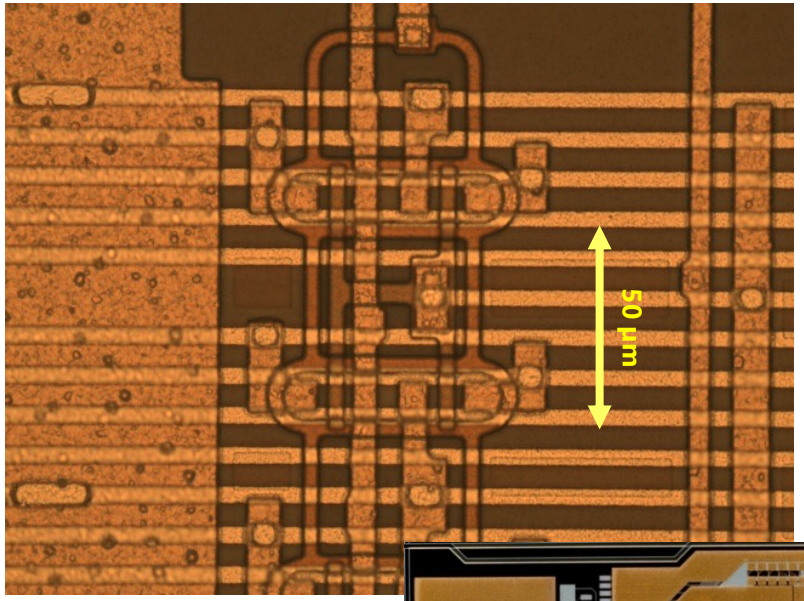


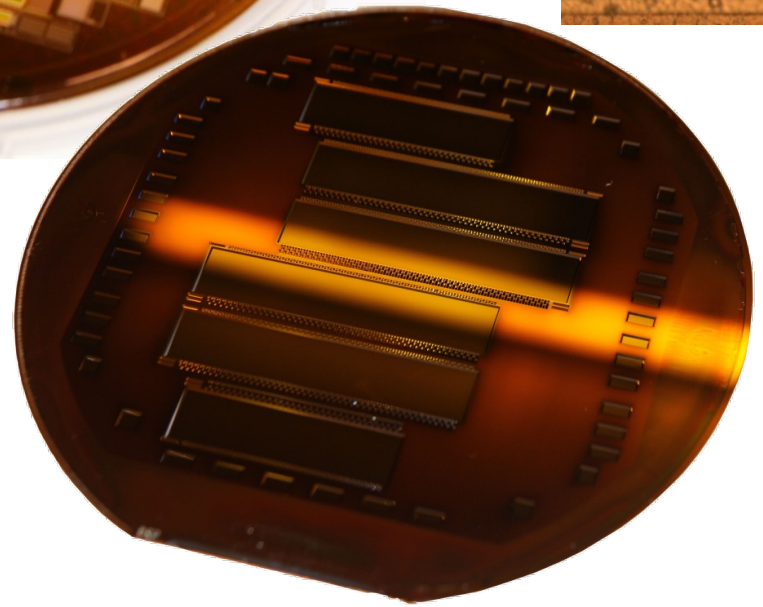


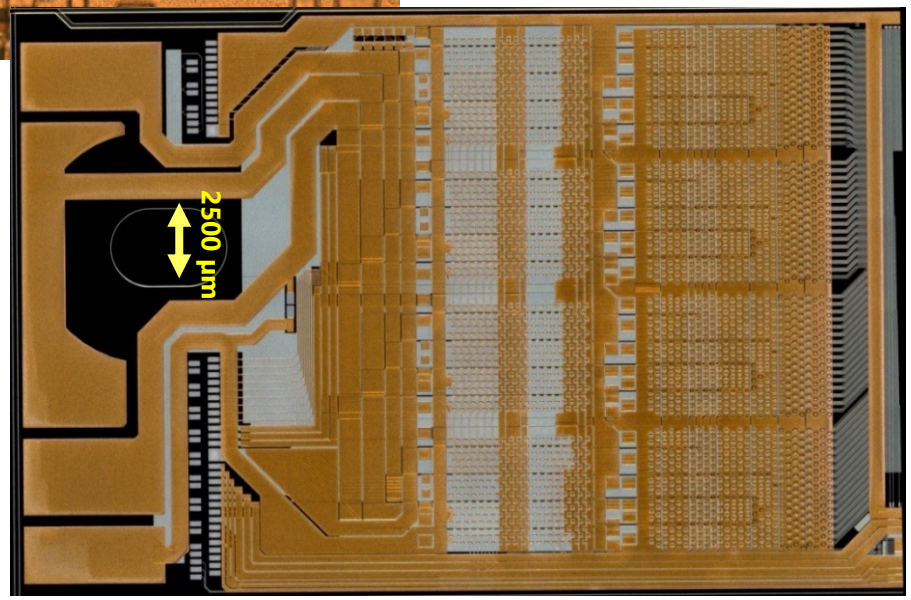
x-ray picture of fully assembled module
0.21% of X_0

Module design on wafer level

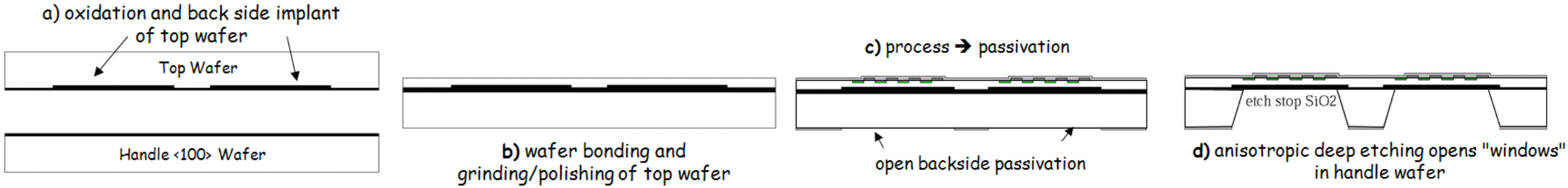


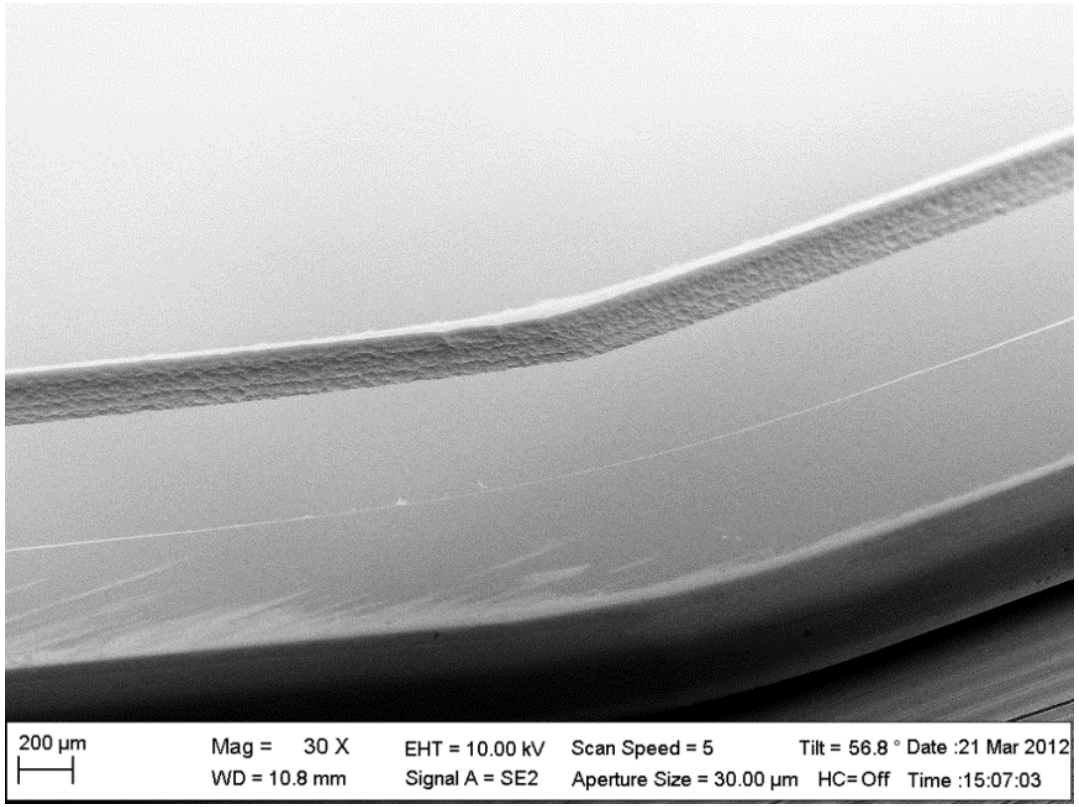


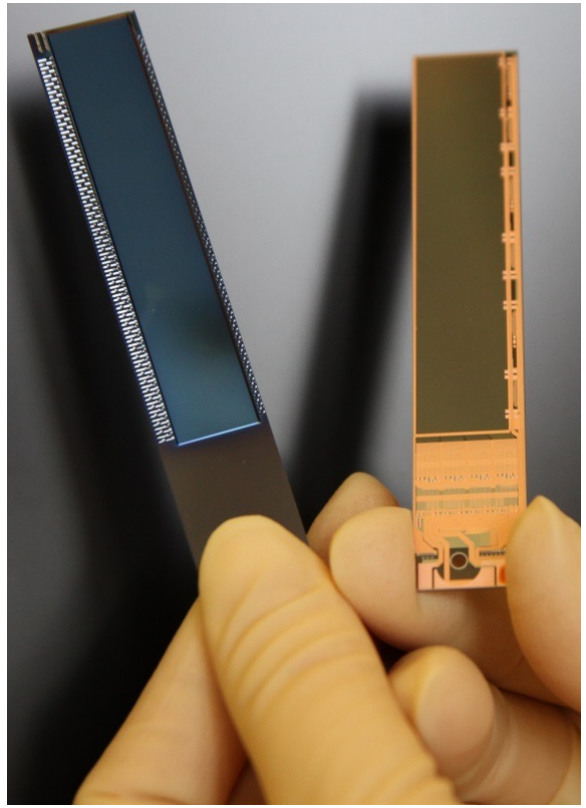




how to make thin DEPFETS







- thickness of the sensitive area is an (almost) free parameter
- thin area supported by a monolithically integrated silicon frame

module assembly overview

Flip Chip of ASICs (~240°C):

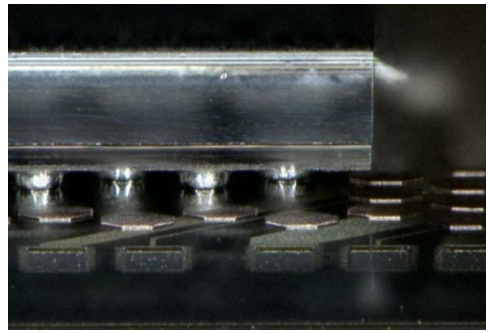
- Bumped ASICs have (almost) the same solder balls (SnAg)
  - ↳ DHP bumping at TSMC, DCD bumping via Europractice
  - ↳ SWB bumping on chip and wafer level as post-process
- Bump bonding on customized support plates
- Initially at IZM, then at HLL

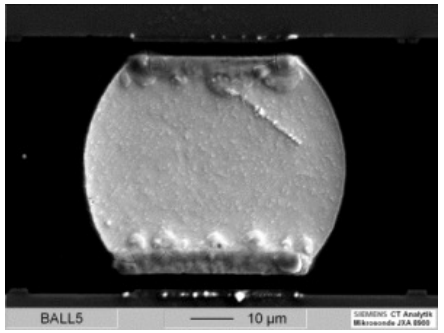
SMD placement (~200°C):

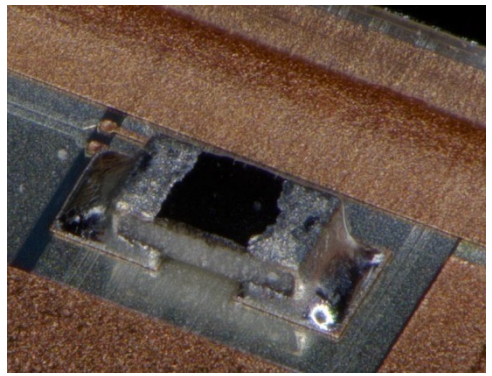
- Passive components (termination resistors, decoupling caps)
- Dispense solder paste, pick, place and reflow

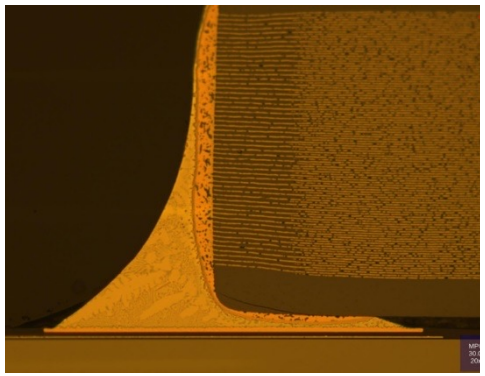
Kapton attachment (~170°C), wire bonding:

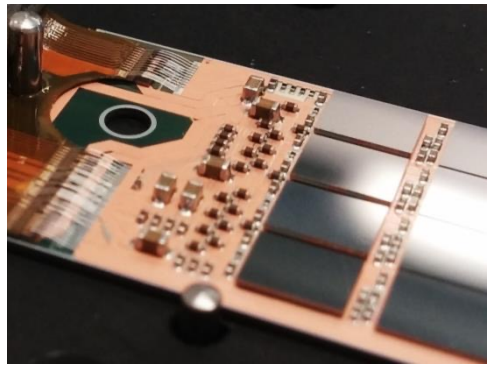
- Solder paste printing on kapton, vapor phase soldering
- Wire-bond, wedge-wedge, 32 µm Al bond wires

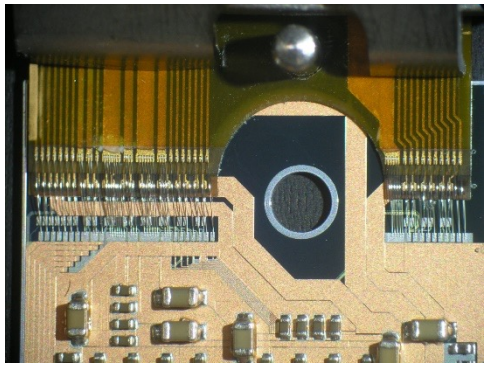






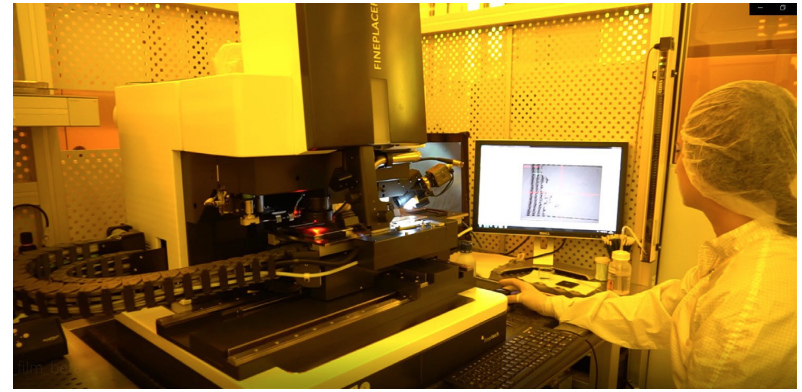




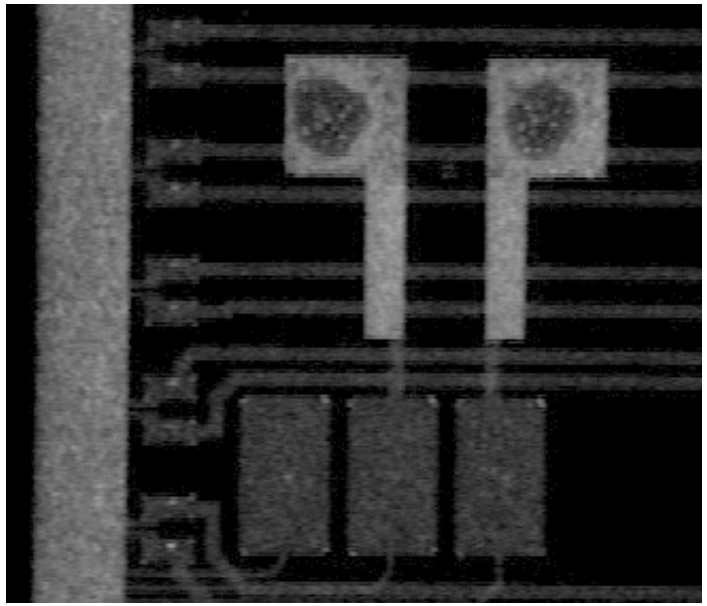


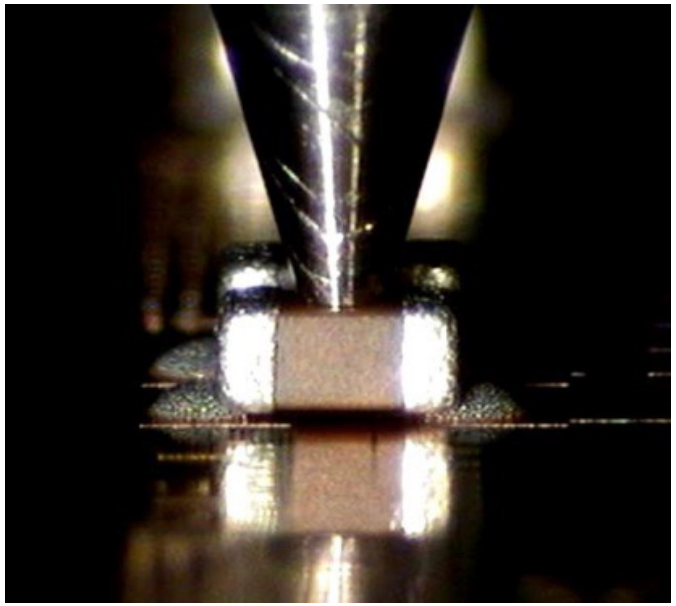
SMD assembly

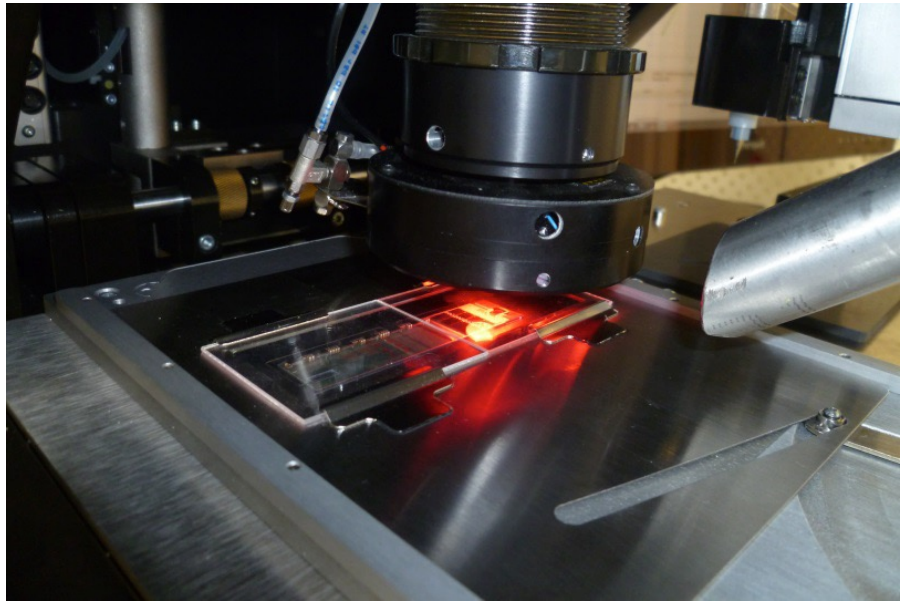
- Each module has about 100 capacitors and resistors of various formats (0402, 0201, 01005)
  - Very small footprint, no screen printing of solder possible, delicate handling of module ...
  - Adapted SMD technology installed at HLL



- Automated micro assembly tool, the same as for flip-chip
  - Additional dispense system
- Process flow
  - Condition module, dispense solder, place SMD parts, reflow in process chamber

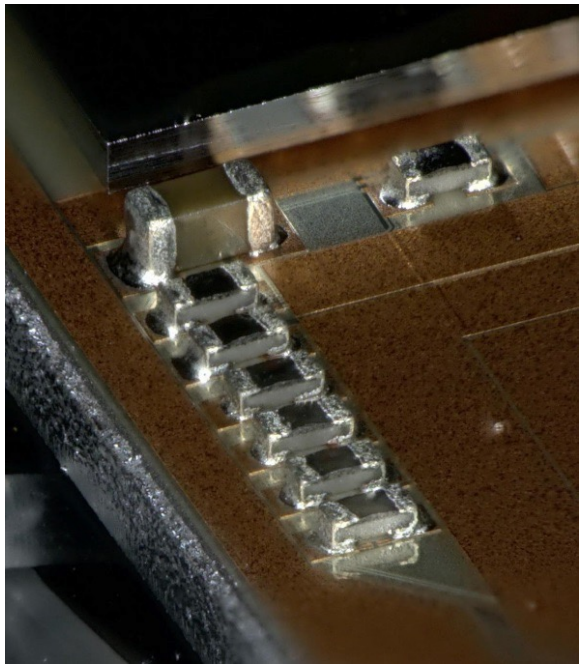


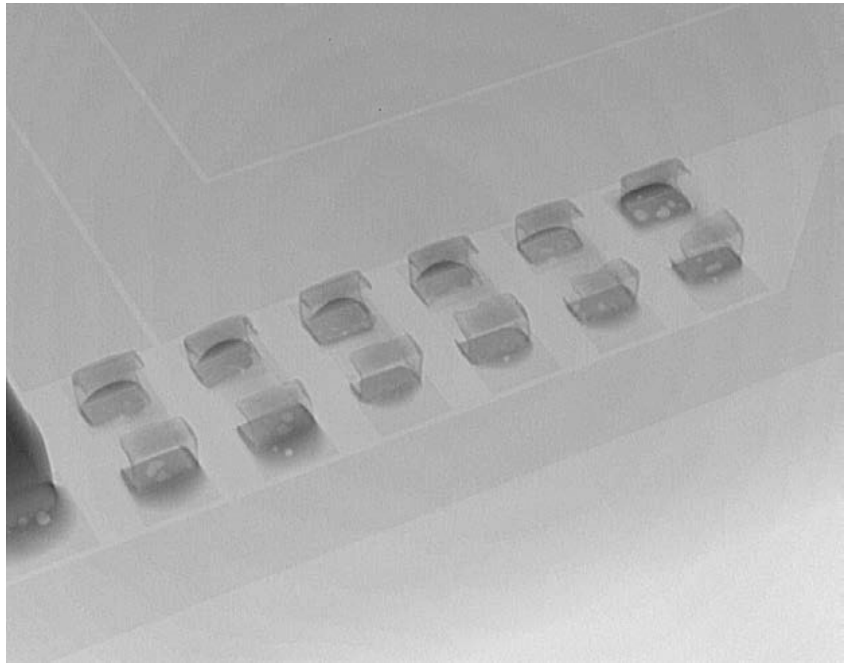




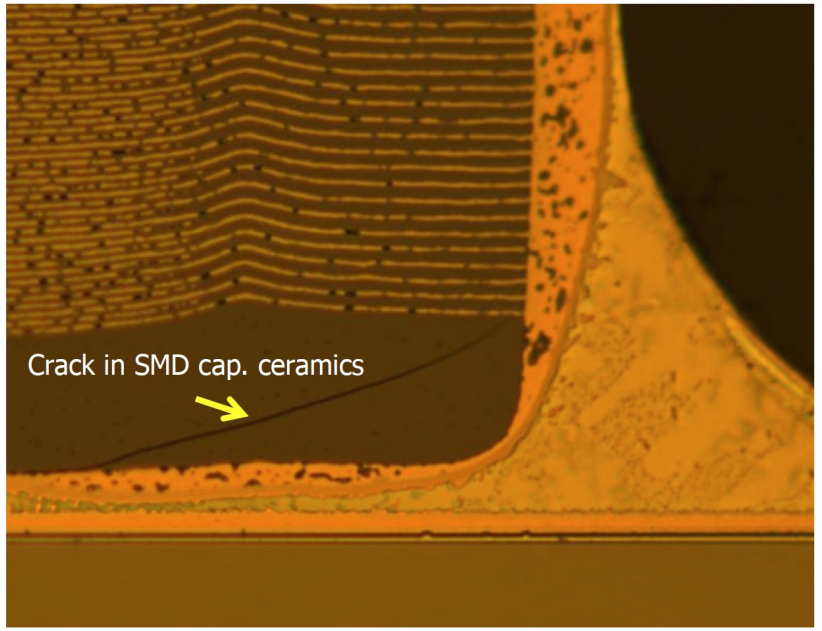
Process qualification

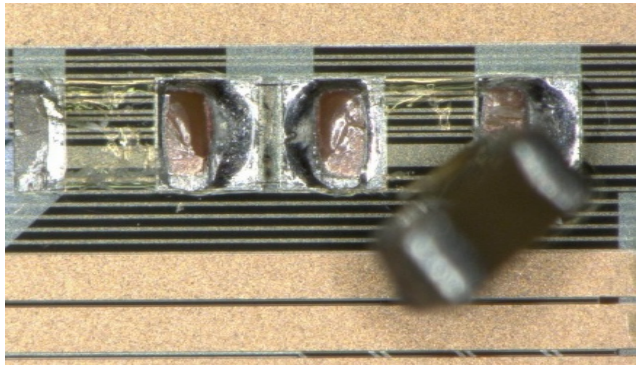
▷ Extensive tests and QC/QA: shear tests, cross section, metallurgy, thermal stress tests …

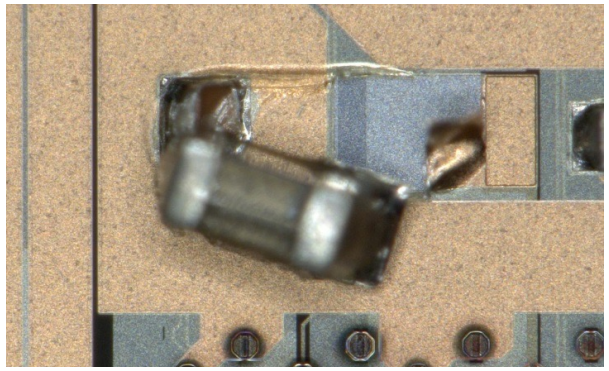


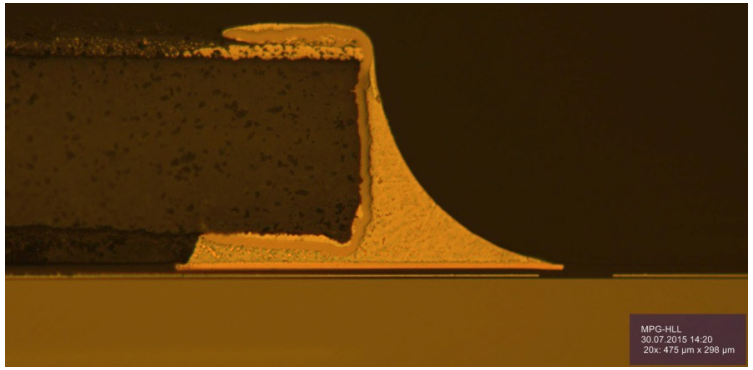


Optimization, fine tuning, reliability … → **need higher quality SMDs**

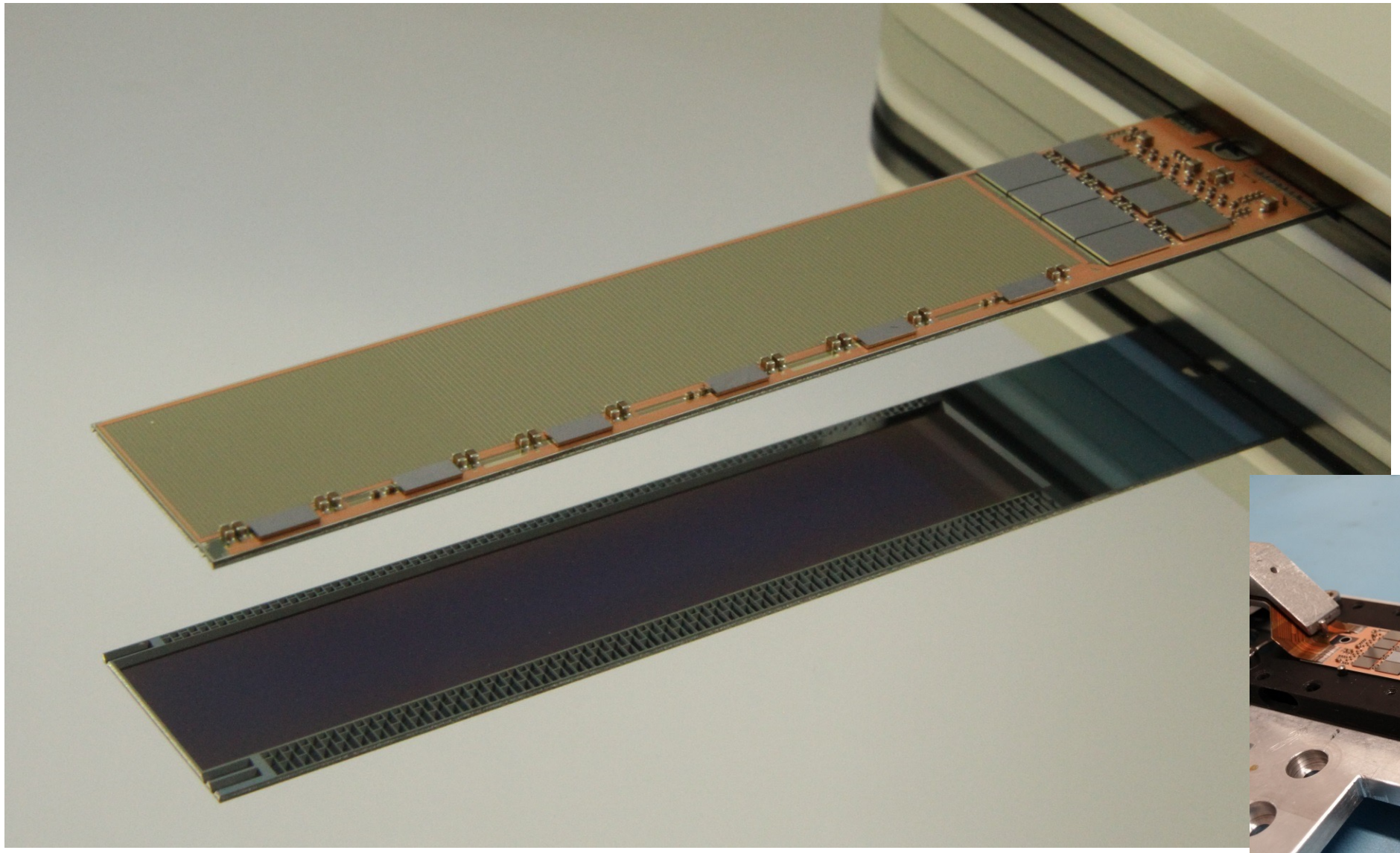


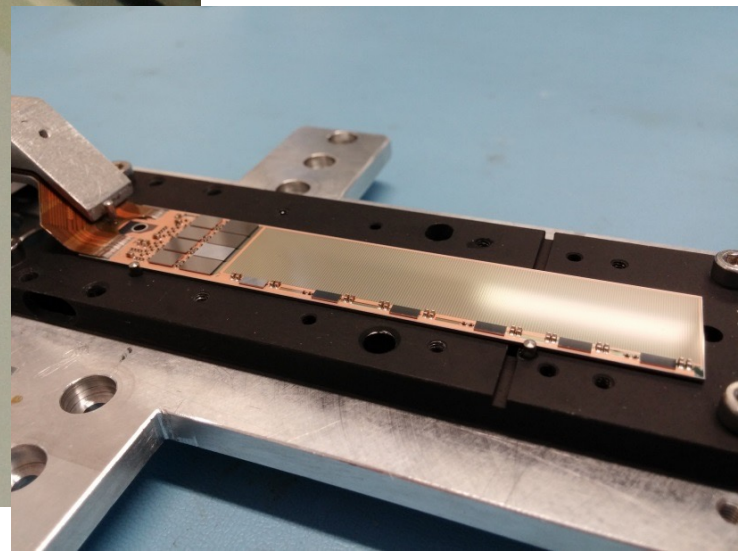






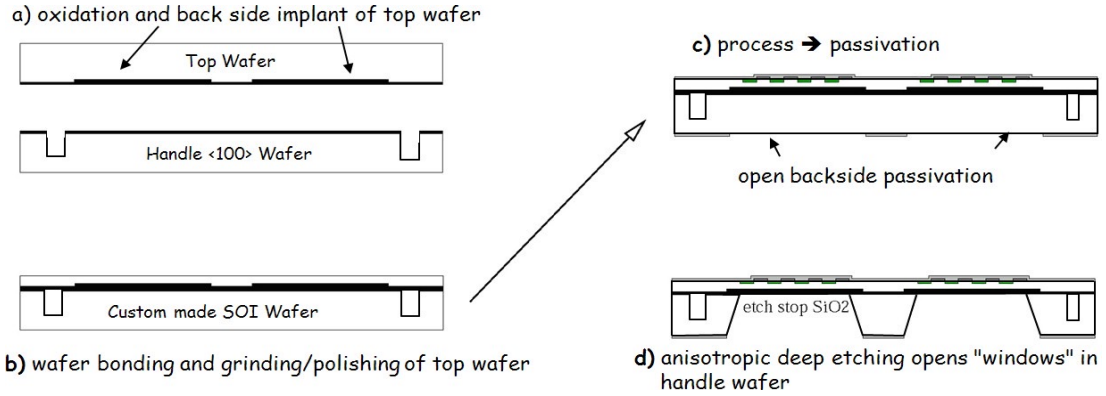
module 0

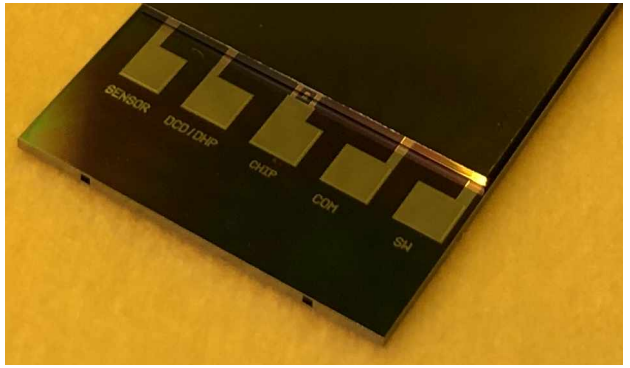


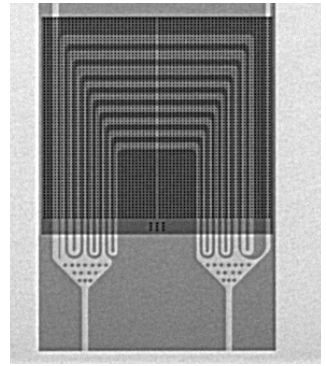


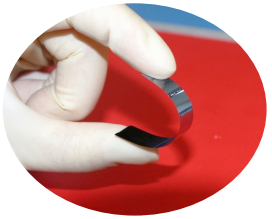
Evolution of this concept

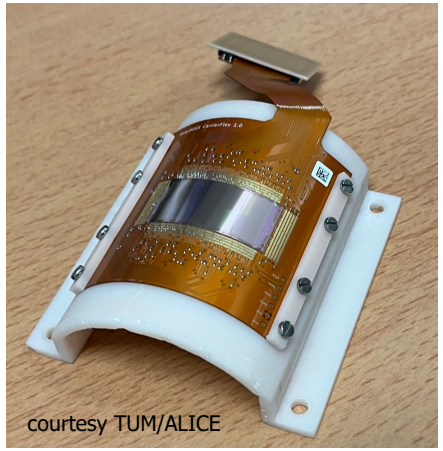
1. Adding **micro-channel cooling** to the ASM → **technology already proven and qualified**











2. **Going flexible**: remove the rigid thick silicon part completely → **next step**
   - ↳ Remove handle wafer chemically and/or mechanically
   - ↳ Embed in PI and/or BCB, add another Cu RDL for chip-to-chip interconnect and support for passives
   - ↳ Applicable also for std. wafer/chip thinning as post-process step

The way forward: **overview**

- Extend sputtering capability on existing sputter system
  - targets are easy to exchange
    - → new metals possible
  - replace 2/4 DC sputter guns with RF biased ones
    - → sputtering of isolators (SiO2, Al2O3 ..)
  - software upgrade for co-sputtering and reactive sputtering

- Improve lithography capability
  - Use of e-beam lithography system installed by MQV partner
  - HLL contribution: installation and qualification of required photo resist systems suitable for e-beam

- Extend structuring capability
  - Installation of ICP-DRIE for silicon
    - TSV, Si wave guides

- Extend interconnect capabilities and post-processing of ASICs and/or PICs
  - Install CMP of Cu and SiO2 as preparation for wafer bonding
  - Install and W2W and C2W direct and hybrid bonding
    - Low temperature bonding <350 °C mandatory

The way forward: **ICP-DRIE "dry etching"**

- Oxford Instruments Estrelas System, single wafer etcher for up to 8" wafers
  - Delivered to and installed at Garching
  - Hook-up, commissioning, process installation ongoing→ end of 2025

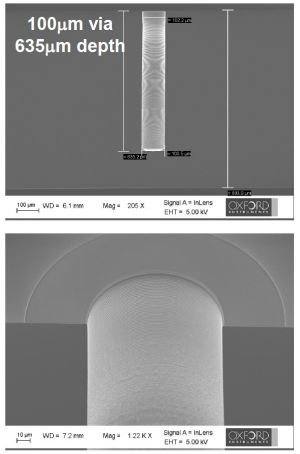
- Main process modules
  - Deep Si etch ("Bosch Process")
    - TSV, fluidic channels, large area partial thinning of wafers, also as post-process option
  - "mixed gas" process
    - Shallow Si etching with very smooth side walls for Si wave guides

3. Bosch: TSV etching

OXFORD INSTRUMENTS

- Advanced packaging applications
  - ~5% Si exposed on a 500 µm thickness wafer
  - Use SiO_2 as a stop layer

Parameter	a	b
Process Chemistry	SF_6-C_4F_8	SF_6-C_4F_8
Wafer size (mm)	**150**	**200**
Exposed area (%)	5	5
Clamping method	ESC	ESC
Via size (µm)	100	100
Depth (µm)	500	500
Etch rate (µm/min)	> 7	> 6
Selectivity to PR mask	> 70	> 70
Selectivity to SiO_2 mask	> 120	> 120
Profile control (°)	90±1	90±1
Bosch scallop (nm) (peak to peak)	< 200	< 200
Uniformity within wafer (±/%)	< 3	< 3

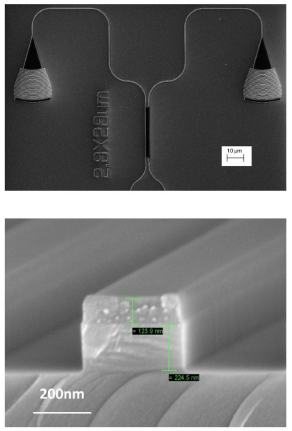


4. Mixed gas Si etching

OXFORD INSTRUMENTS

- Si waveguide applications
  - SOI wafers
  - Etch a top Si layer of 220nm thickness
  - Smooth sidewalls and accurate control

Parameter	a	b
Process Chemistry	SF_6-C_4F_8	SF_6-C_4F_8
Wafer size (mm)	**150**	**200**
Exposed area (%)	25	25
Clamping method	ESC	ESC
Trench size (µm)	5	5
Depth (nm)	220	220
Etch rate (nm/min)	> 50	> 40
Selectivity to PR mask	> 1.5	> 1.5
Selectivity to SiO_2 mask	> 2.5	> 2.5
Profile control (°)	90±2	90±2
Added sidewall roughness (nm)	< 2 (rms)	< 2 (rms)
Uniformity within wafer (±/%)	< 5	< 5



The way forward: **Wafer bonding**

- Very versatile basic process step for (heterogenous) integration
  - Wafer-to-wafer or collective chip-to-wafer bonding
    - Si to Si, Si to other materials like compound semiconductors, e.g.
    - “Hybrid bonding”: embedded Cu-Cu bonds for electrical interconnections

Plasma activation: EVG810

Cleaning/prep: EVG301

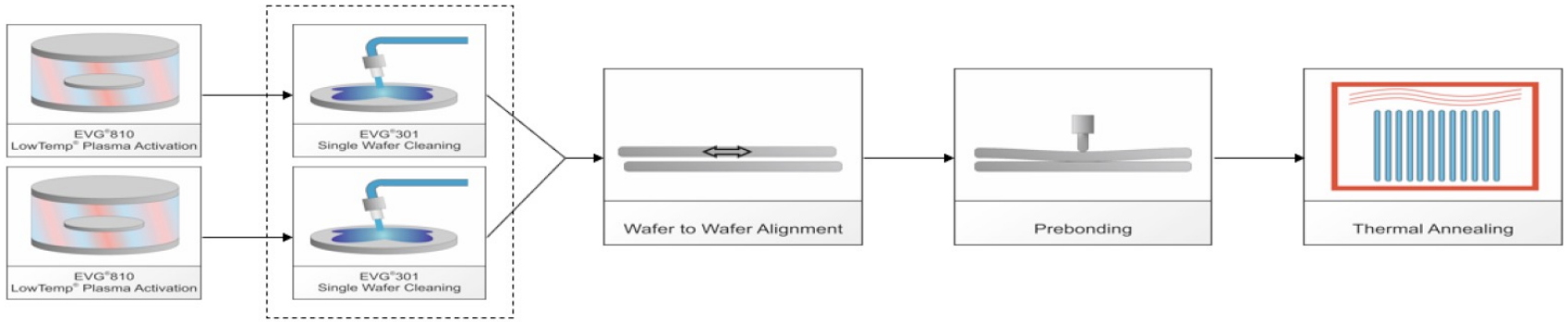
Direct and adhesive (temporary) bonding: EVG501
- SOI, C-SOI

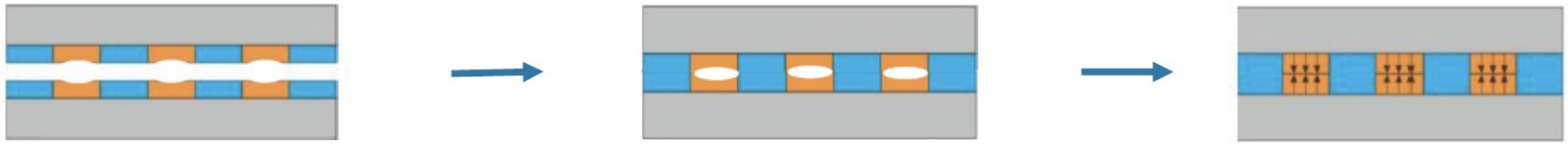
Hybrid Bonding: EVG Smart-View
- Aligned W2W bond

- Wafer preparation
  - “Bosch” Process for C-SOI
  - Post-processing: RDL on ASIC and sensor wafer
  - CMP
  - Re-constitution of Wafer from KGDs

- **all tools ordered, infrastructure in prep, installation expected Feb. 2026**

The way forward: **Hybrid bonding**

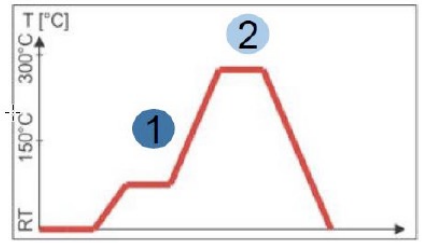




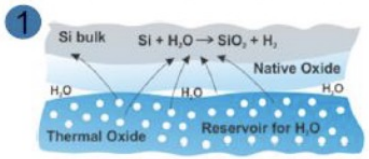
Wet cleaning and plasma activation are applicable for surface preparation.

Wet cleaning can include the use of chemicals for metal oxide removal

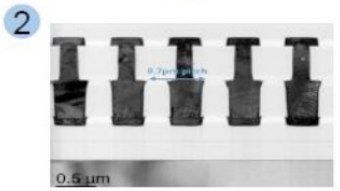
Wafers will be aligned using F2F optical alignment. Once aligned, wafers will be contacted at room Temperature.



Annealing Process



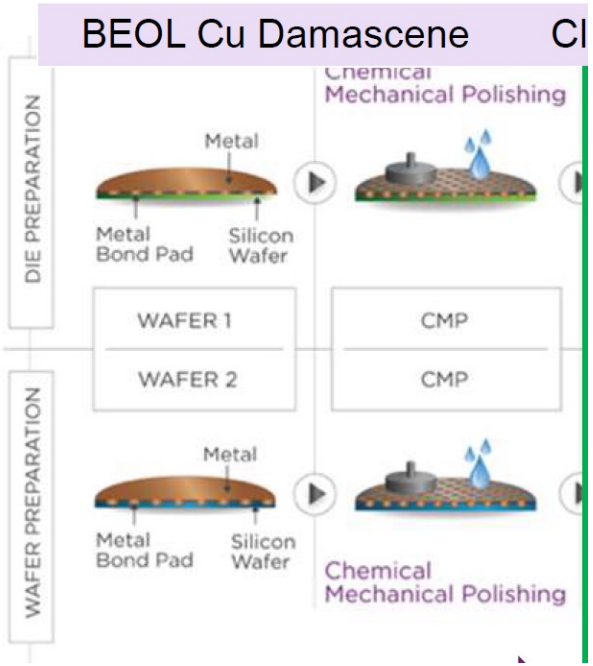
Dielectric layer Annealing



Interconnect gap closure due to different CTE of Dielectric bonding material and interconnect material

Hybrid bonding ←→ Cu CMP

- smooth mirror-like surfaces mandatory – CMP is key
- general idea is to add post-process steps and prepare CMOS wafers for hybrid bonding
  - ↳ adding a Cu Damascene process on passivated wafers
- basically, this is a simple single or dual damascene step with the requirement of a **defined Cu dishing at CMP**

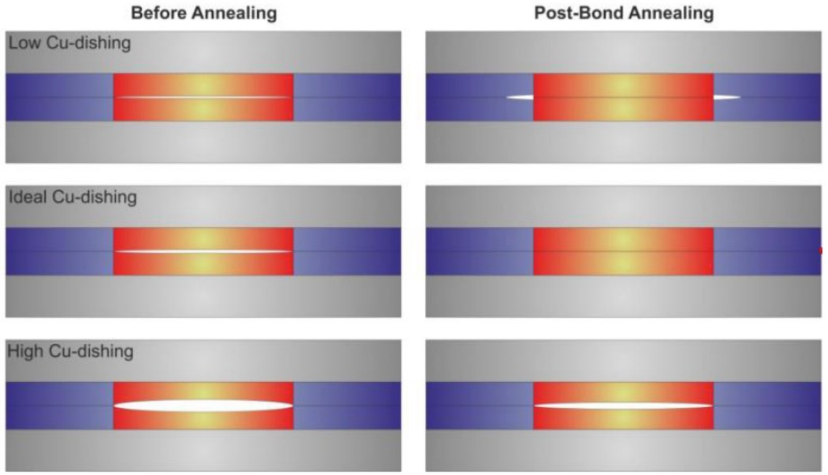


Cu Dishing Control

Void in the Dielectric Interface
Too little dishing, too high anneal temperature

Ideal Contact
Dishing is filled by thermal expansion through anneal (~ 300/400 °C anneal).

Void in the Cu Interface
Too much dishing, too low anneal temperature



- CMP dishing control is needed within a few nm (1-5 nm) range with adequate (~400 °C) anneal temperature [1].
- A close loop metrology can be set up to tune the annealing temperature by the dishing gap.
- Lower Cu surface roughness leads to more efficient contact area formation [2].

J. P. Mudrick at al., "Sub-11:11tm Pitch Hybrid Direct Bond Interconnect Development for Die-to-Die Hybridization" SAND2019-2384C (2019).

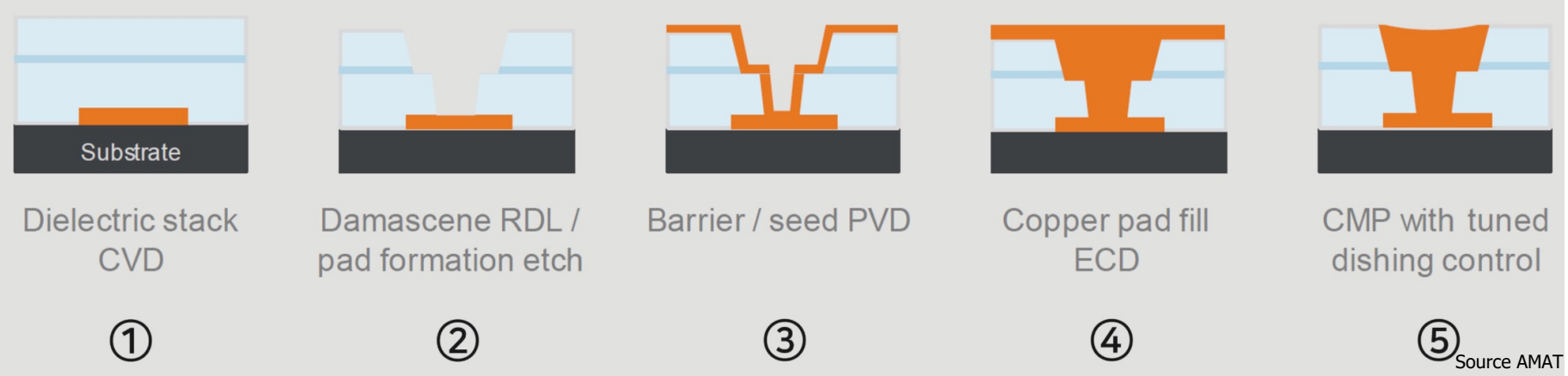
Hybrid Bonding process installation

- MPG HLL would provide test wafers:
  - single Al layer representing last metal on CMOS wafers
  - low-temp SiO2 deposition, via opening, ep Cu with overburden
  - step 1-4 in figure

Looking for partners, interested?

- partner to help with CMP removal of overburden – step 5
  - optimized for smooth oxide surface and defined Cu dishing

- Bonding tests (W2W) to follow at MPG HLL with exchange of results, joint publication possible



a few take-home messages

- MPG HLL moved to new lab
- there is quite some experience in post-processing, assembly, and interconnect for radiation sensors
- technology extension
  - ICP-DRIE of silicon being installed
  - wafer bonding including hybrid bonding towards more advanced heterogenous integration (“chiplets”)
- open for cooperation also for technology qualification
  - Copper CMP
  - ....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Embedding thin chips

- Not a new idea, there are various proposals and techniques
  - A possible sequence is UTCP (ultra thin chip packaging) by IMEC and Ghent University, 2009

    J. Govaerts,W. Christiaens, E. Bosman, and J. Vanfleteren, "Fabrication processes for embedding thin chips in flat flexible substrates," IEEE Transactions on Advanced Packaging, vol. 32, no. 1, pp. 77–83, Feb 2009.

- in general, there is always
  - Utilization of temporary bonding to support wafers
  - Application of various spin-on/spray-on polymers
  - Photolithography steps and structuring of the layers
  - Via formation (wet/dry etching or laser drilling)
  - sputtering of metals (Al, Ti:W, Cu)
  - Electroplating

- (Almost) all necessary steps are available in the R&D/Interconnect line of the HLL
  - Temporary bonding is planned for end 2025

- Technology test project to be defined
  - Best combination of polymers, metals and adhesives?
    - Minimize material budget, optimized for sensor perf. and HEP compatibility
  - multi-metal RDL?
    - Full FCB replacement!!
  - Test structures for technological and electrical characterization of the process
  - ....

- **Exciting extension of our technology!! Stay tuned!!!**

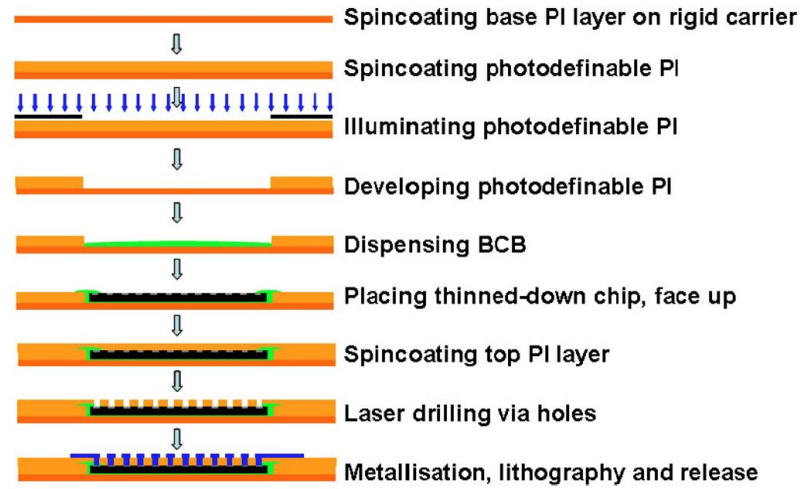

Fig. 2. Process flow design for the UTCP technology.