

# Beam position monitoring with a 5x5 HitPix3 matrix for ion beam therapy

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## Master thesis by Baudry Bartels 28.07.2025

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#### Ion beam therapy as cancer treatment



- Goal: kill tumor cells with precise particle energy deposition
- Why Ion beams?
  - Precise energy deposition in depth due to Bragg peak
    - less damage to healthy tissue
- Scanning of position and energy of beam to cover full tumor volume (Raster scan)
- Beam monitoring essential to ensure precise execution



Energy deposition as a function of penetration depth for photons and protons

Reference: https://doi.org/10.1016/j.urolonc.2018.11.012

# System at Heidelberg ion beam therapy center (HIT)



- Treatment plans with proton and carbon-ion beams
- Adjustable beam parameters:

parameter	steps	Proton	Carbon
Energy [MeV/u]	255	48 - 221	88 - 430
Width (FWHM) [mm]	4	8 - 20	4 - 12
Intensity [1/s]	10	8·10 <sup>7</sup> - 2·10 <sup>9</sup>	2·10 <sup>6</sup> - 8·10 <sup>7</sup>

- Current beam monitoring:
  - 2 multi-wire chambers and 3 ionization chambers at beam exit
- Current tumor position monitoring:
  - CT scan prior to beam treatment



**Beam acceleration and guidance system at HIT** Reference: https://www.klinikum.uni-heidelberg.de/interdisziplinaerezentren/heidelberger-ionenstrahl-therapiezentrum-hit/leistungsspektrum

#### **Future treatment ideas**

![](_page_3_Picture_1.jpeg)

- Current setup works well for fixed tumor positions
- Ambition: treat tumors in moving body parts (e.g. bowels)
- Idea: beam treatment during active magnetic resonance imaging (MRI)
- Problem: noisy environment, changing magnetic field
  - Current beam monitoring system not reliable inside the MRI

![](_page_3_Picture_7.jpeg)

The ARTEMIS Project: MRI guided Ion-beam therapy Credits: Heidelberg University Hospital

### **Beam monitoring requirements**

![](_page_4_Picture_1.jpeg)

**Requirements:** 

- High position (200 µm) and beam width (FWHM) (<5%) resolution</p>
- Good intensity measurement (0.5% accuracy)
- Low latency for position and width measurement (100 µs)
- New: work in MRI environment

Implementation:

- Radiation hard for 5 years ( $\Phi_{eq} \approx 10^{15} \text{ cm}^{-2}$ )
  - And/or simple to replace (cost/time efficient)
- Less than 0.35 mm water-equivalent thickness
- Cover target area of 25x25 cm<sup>2</sup>

### The HitPix sensor

- Idea: thin, pixelated sensor
  - Use monolithic active pixel sensor (MAPS) design
  - > In pixel counter to handle high intensity
- Silicon based HV-CMOS detector
- Radiation hard (operable after Φ<sub>eq</sub> ≈ 10<sup>15</sup> cm<sup>-2</sup>)
- good spatial resolution (~60 μm)
- Can be operated inside magnetic field/noisy environments
- Single sensor size: 2x2 cm<sup>2</sup>
  - Create interconnected matrix to cover target area (25x25 cm<sup>2</sup>)

![](_page_5_Figure_10.jpeg)

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Simplified cross section of an HV-CMOS sensor Reference: http://dx.doi.org/10.1088/1748-0221/10/04/C04007

![](_page_5_Figure_12.jpeg)

#### Sensor readout modes

![](_page_6_Picture_1.jpeg)

Counter readout: Sensor readout pixel by pixel

![](_page_6_Figure_3.jpeg)

- $\rightarrow$  Detailed information for each Pixel,
- → slow readout

Adder readout: Rows and columns summed up to form x and y projections

![](_page_6_Figure_7.jpeg)

- → Lose Details, keep 2D projection of hit profile
- → Faster readout (less data to pass)

**Pixel readout in the sensors in counter and adder mode** Reference: https://doi.org/10.3390/instruments7010009

#### The 5x5 HitPix3 demonstrator

![](_page_7_Picture_1.jpeg)

HitPix3: 48x48 pixels, 200x200 µm pixel size

![](_page_7_Figure_3.jpeg)

Picture of the 5x5 HitPix3 matrix mounted on the motherboard connected to the FPGA Credits: Bogdan Topko

## Karlsruhe Institute of Technology

### **Readout system**

- Pixel readout in sensor
- Data flow controlled by FPGA
- Measurement data is sent to PC via USB
- No online reconstruction at this point  $\rightarrow$  Main task of my thesis

![](_page_8_Figure_6.jpeg)

### **Beam parameter reconstruction: PC level**

![](_page_9_Picture_1.jpeg)

Unlock settings

Main interface

Tools -

#### HitPix user interface

![](_page_9_Figure_3.jpeg)

![](_page_10_Picture_0.jpeg)

#### Beam parameter reconstruction: PC level online

- For adder readout fitting time ~2-4 ms
- Fast enough for large frame sizes (5000 µs)
- Not fast enough to reconstruct every frame for sufficiently small frame sizes (ideally 50 µs to achieve 100 µs latency)
- Large frame sizes adequate for debugging and detailed beam diagnostics but not for the desired beam monitoring
- Procedure and system not optimized yet
  - Computing time could be reduced

![](_page_10_Figure_8.jpeg)

#### Time needed for GUI fitting procedure for beam reconstruction

#### Intermediate summary PC level reconstruction

![](_page_11_Picture_1.jpeg)

- Pre-existing GUI to initialize python scripts used for readout and configuration expanded with data analysis function
- Delivers user friendly depiction of detector data and simplifies handling the python readout scripts
- Data analysis latency too high for beam monitoring operation

Can be used for beam diagnostics

Idea to reduce latency: Reduce data load between FPGA and control system

#### **FPGA** basics

![](_page_12_Picture_1.jpeg)

- Reconfigurable integrated circuits
  - Can receive updates in contrast to dedicated microprocessors
- Consists of a finite number of logic slices, memory units, clock tiles and port connections
- Logic slices consist of look-up tables (LUTs) and flip-flops to assign and hold values
- Operates on bit-level, synchronized to a clock signal
- Parallel operations possible
- Ressources assigned to functions and connections via Hardware Description Language (HDL)

Input 1	Input 2	Output
0	0	0
0	1	0
1	0	0
1	1	1

LUT of a boolean "and" operation

#### **Beam parameter reconstruction: FPGA level**

![](_page_13_Picture_1.jpeg)

- Write design block that does weighted mean calculation on FPGA
- Reduce data sent from FPGA to PC
- Loses details but keeps relevant parameters
- Instantly have relevant parameters

- Working steps:
  - Break down formulas into single calculation steps:

![](_page_13_Figure_8.jpeg)

Generate control signals for single calculation blocks

### Beam parameter reconstruction: FPGA level

![](_page_14_Picture_1.jpeg)

#### Inputs:

Number of hits n per pixel as 14 bit integer

Positional values x stored in writeable register (measured and uploaded to FPGA before data taking)

x<sup>2</sup> stored and not calculated to save time

#### 2 Control signals

![](_page_14_Figure_7.jpeg)

Results: Intensity I , mean position  $\hat{x}$ , standard deviation  $\sigma$ as floating point values for each readout frame

Diagram of the whole calculation broken down into its steps for FPGA implementation Single calculations work at 32 bit floating point precision (later to be 16 bit floating point to further reduce data load)

#### **Beam parameter reconstruction: FPGA level:** simulation

![](_page_15_Picture_1.jpeg)

![](_page_15_Figure_2.jpeg)

- Calculated values on FPGA match expectations
  - Latency for first results after end of measurement frame (including read-in to calculation block):
    - simulation setup (24 pixel positions \* 1 sensor, 1D): I: 0.84  $\mu$ s;  $\hat{x}$ : 1.19  $\mu$ s;  $\sigma$ : 2.08  $\mu$ s
    - Scaled up to one row with 13 large sensors (96 pixels \* 13 sensors, 1D): I: 25.32  $\mu$ s;  $\hat{x}$ : 25.67  $\mu$ s;  $\sigma$ : 26.56  $\mu$ s
    - 100 MHz clock
- No data loss on consecutive frame input

![](_page_15_Figure_9.jpeg)

## Beam parameter reconstruction: FPGA level: implementation

![](_page_16_Picture_1.jpeg)

- Reconstruction designed to be insertable module
- No connection to FPGA board ports
- Need register to hold positional x values

![](_page_16_Figure_5.jpeg)

## Beam parameter reconstruction: FPGA level: implementation

![](_page_17_Picture_1.jpeg)

- Reconstruction designed to be insertable module
- Create module to connect ports
- Create module to hold USB positional values
- Generate control signals for reconstruction block
- Can be combined with existing readout firmware

![](_page_17_Figure_7.jpeg)

#### Beam parameter reconstruction: FPGA level: Resource utilization

![](_page_18_Picture_1.jpeg)

- Reconstruction block design needs to fit on the FPGA besides the existing readout design
- Additionally require space for the map registers
- Beam estimator block design only: 7.03 % LUT utilization on a Nexys Video FPGA
- With 48 position register (1 HitPix3 chip): 8.51 %
- With 240 position register (1x5 HitPix3 row): 23.46 %
- Scaling up to 13x13 matrix not possible within simulation
- Note: includes both x and x<sup>2</sup> registers
  - can omit x<sup>2</sup> register and calculate for each position (trade utilization for computing time)

## Beam parameter reconstruction: FPGA level: Scaling ideas

![](_page_19_Picture_1.jpeg)

Need to scale to 2D:

- Use calculation module twice in parallel (faster, more resources)
- Use calculation module two times in a row (slower, less resources)
- Need to scale to full matrix:
  - Remove x<sup>2</sup> map, calculate instead (slightly slower, much less resources)
  - In case x map needs to many resources:
    - Use counter for pixel positions and convert to mm seperately (less precision, much less resources)

#### To be evaluated and tested

#### **Outlook and next steps**

![](_page_20_Picture_1.jpeg)

- Go to 96x96 pixels for a single sensor
- Scale up the matrix to cover target area (25x25 cm<sup>2</sup>)
- Improve on GUI to present fit results every n<sup>th</sup> frame
- Implement beam reconstruction on FPGA to existing readout and check scaleability
- Plan to move to more powerful FPGA

### **Conclusion on beam monitoring**

![](_page_21_Picture_1.jpeg)

- Currently built a 5x5 HV-CMOS detector demonstrator matrix for beam monitoring
- Online beam reconstruction work in progress
- PC level reconstruction using a fitting procedure:
  - Good tool for offline beam diagnostics
  - For online analysis only large frame sizes or not every frame

#### FPGA level reconstruction:

- Reduces the data load sent to beam control system
- Works in 1D, in principle in 2D as well
- Needs more work:
  - Check scaleability
  - Implement in readout process