

Readout Systems for Cryogenic Circuits (Sensors & Qubits)

Luis Ardila-Perez, Daniel Crovo, Marvin Fuchs, Robert
Gartmann, Georgia Manifava, Timo Muscheid,
& Lukas Scheller

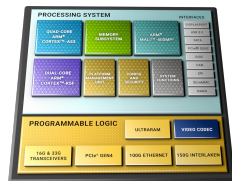
Quantum Interface Controller (QIC)

Objectives:

- Full-stack DAQ development for Superconducting Quantum Detectors (MMCs, MMBs, MKIDs) and Qubits using custom designed boards and COTs boards ([Presentation](#))
- Tools and methods for building firmware/software for heterogeneous devices (MPSoCs, RFSocS)

Interests:

- Develop DAQ systems targeting future large-scale arrays of superconducting quantum detectors (to be coordinated with DRD5)
- Evaluation of new IP cores available for FDM signal processing in VERSAL



ZynqUS+ MPSoC



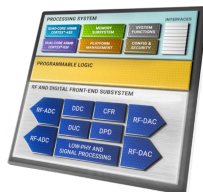
DTS100G



AD/DA



Mixer



ZynqUS+ RFSoc



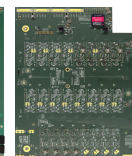
ZCU216



Front-End



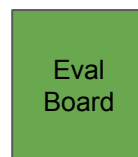
ZCU216



DirectRF FE



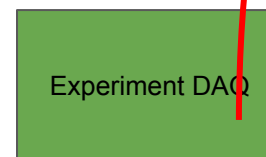
VERSAL RF



Eval Board



Custom FE



Experiment DAQ



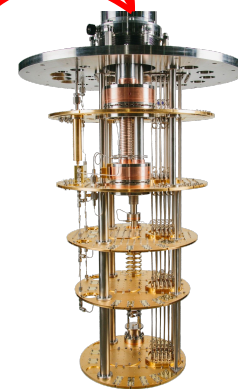
QIC – ECHO



QIC – BULLKID-DM



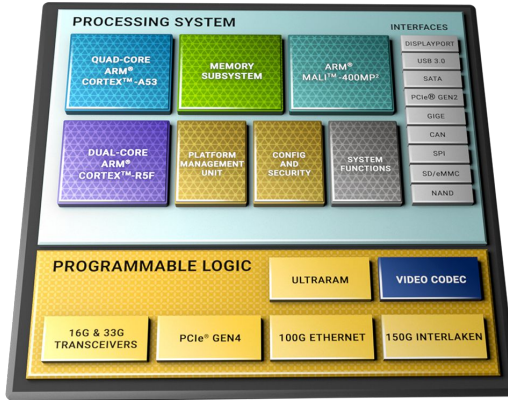
QIC – SC Qubits



MMCs/ MKIDs / Qubits
currently installed at
KIT-IPE
KryoDAQ Lab

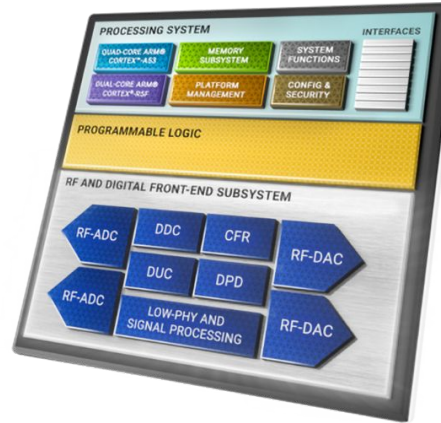
Heterogeneous devices

ZynqUS+ MPSoC



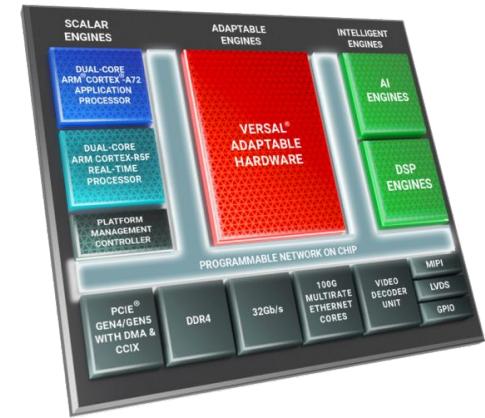
- Quad Arm Cortex-A53
- Dual Arm Cortex-R5F
- Arm Mali™-400MP2
- 16nm FinFET+ Programmable Logic

ZynqUS+ RFSoc



- RF-DACs (9.85 GSPS)
- RF-ADCs (2.5 or 5 GSPS)

Versal ACAP

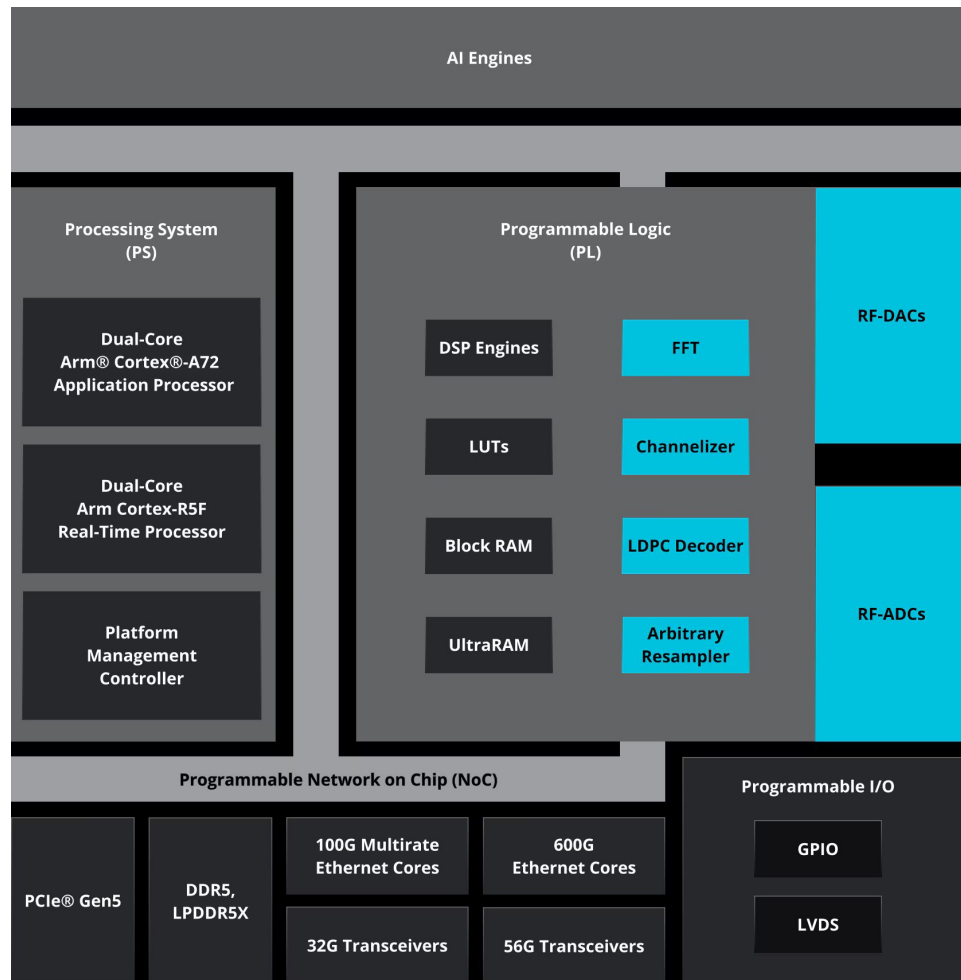


- 7nm FPGA + Processors + AI Engines
- Network-on-chip backbone
- High bandwidth & low latency
- Built in arbitration

VERSAL RF

Several Hard IP cores are of interest for evaluation within the new VERSAL RF device architecture

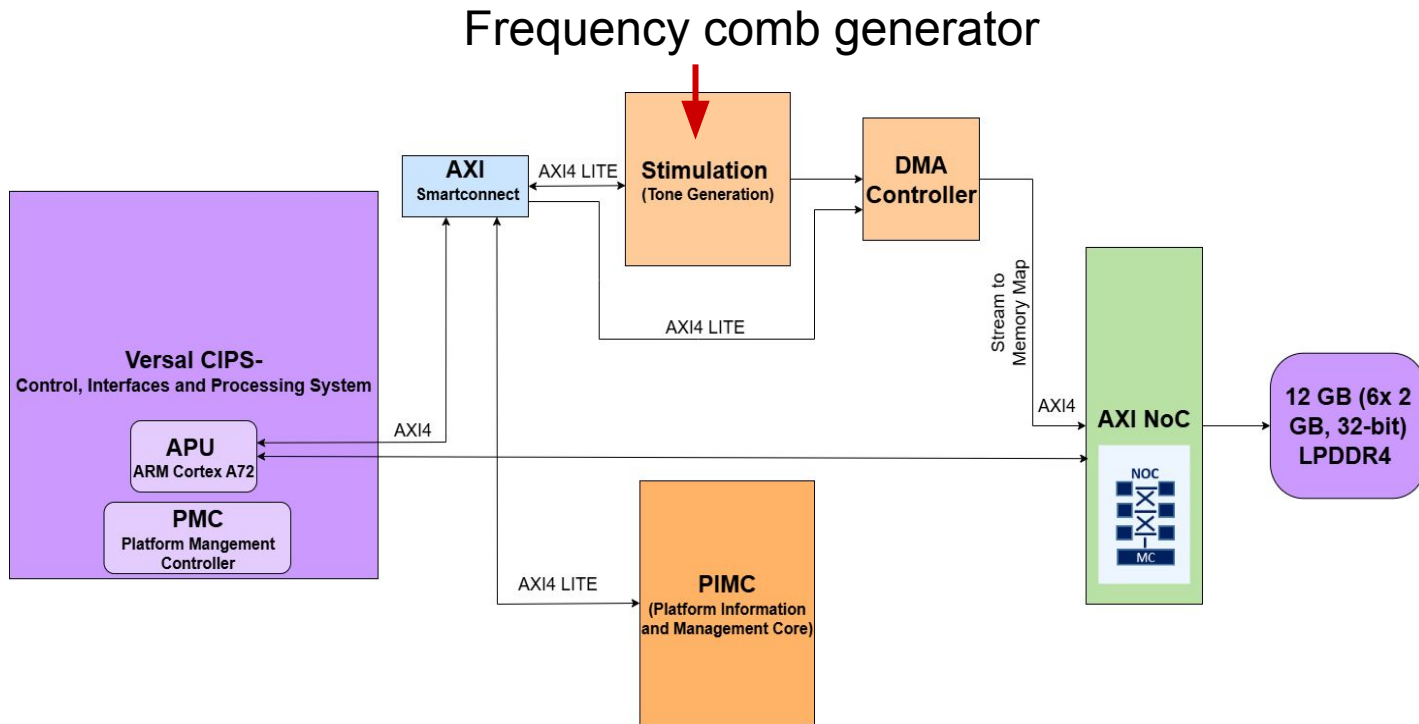
- FFT
- Channelizer
- RF-DACs (16 GSPS)
- RF-ADCs (8 or 32 GSPS)
- PCIe Gen5
- DDR5
- 56G Transceivers
- Faster Programmable Fabric
- AI Engines



Migration of our Firmware/Software Infrastructure

Necessary steps:

- Upgrade to Vivado 2024.2 for VEK280 board support
- Replace ZynqMP core with CIPS core
- Add the NoC core
- Remove the DDR core and connect things to the NoC instead
- Adjust device tree to configure memory addresses for DDR



Demonstrator firmware successfully runs on the VEK280 board!

SoCks (SoC Blocks)

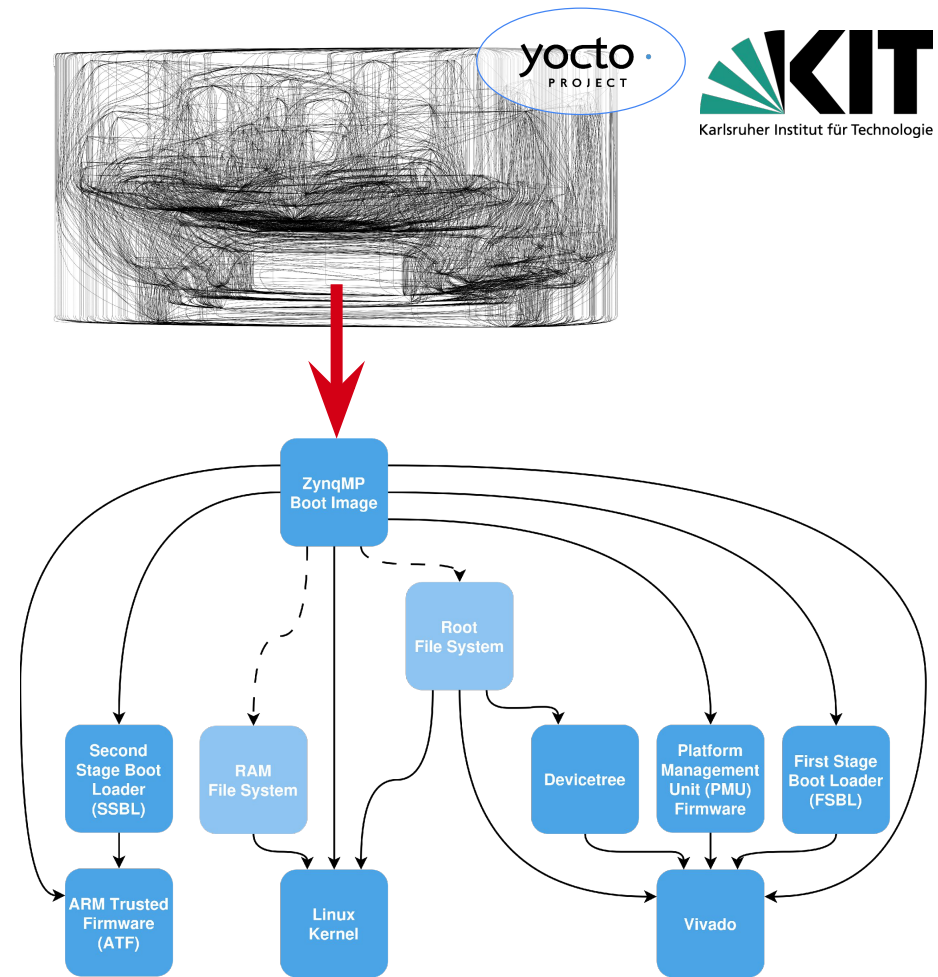
Presented in April 2025

Objectives:

- Reduced complexity of the build process
- Easy to learn and use
- Fast and reliable
- Simple debugging of projects
- Full compatibility with GitLab CI/CD
- Encourage reuse of software and firmware

Ideas:

- Divide and conquer
- Introduce a new abstraction layer (blocks)

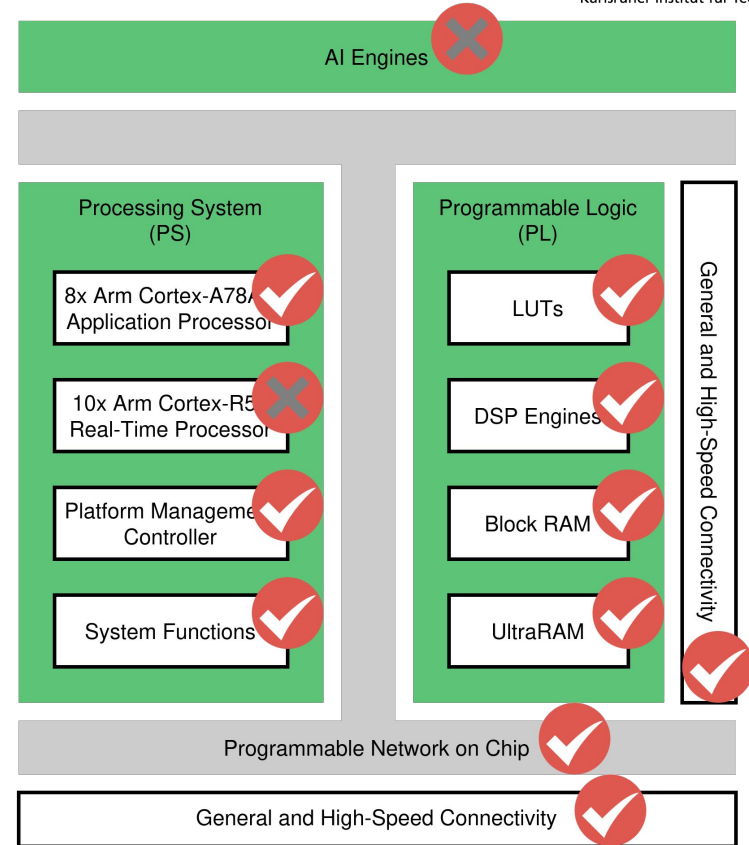


SoCks (SoC Blocks)

SoCks can already build AMD Versal images and supports most features.

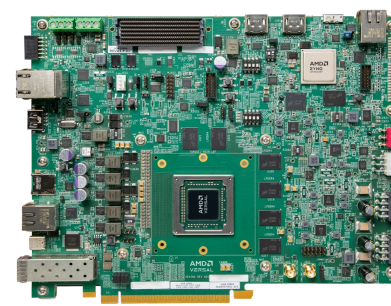
- Currently a reduced number of blocks
- Components that we do not use in our current projects are not currently supported
 - Real-time processor
 - AI engines

→ Can be solved by adding additional blocks and builders

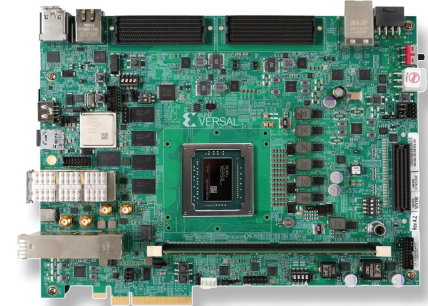


Plans

- SoCks:
 - Benchmark performance
 - Release as open source software
 - Detailed publication with tutorials ([SoC workshop in October 2025](#))
 - Add support for AI engines (2026)
- Channelization Firmware ([presentation](#)):
 - Benchmark performance and resources in US+ fabric vs Versal fabric vs AI Engines
 - Compare against hard IP core in Versal RF once available
 - Release module code and documentation
- Advanced Trigger Algorithms (Optimal Filter):
 - Implementation and comparison on US+, Versal Fabric, and AI engines



VEK280



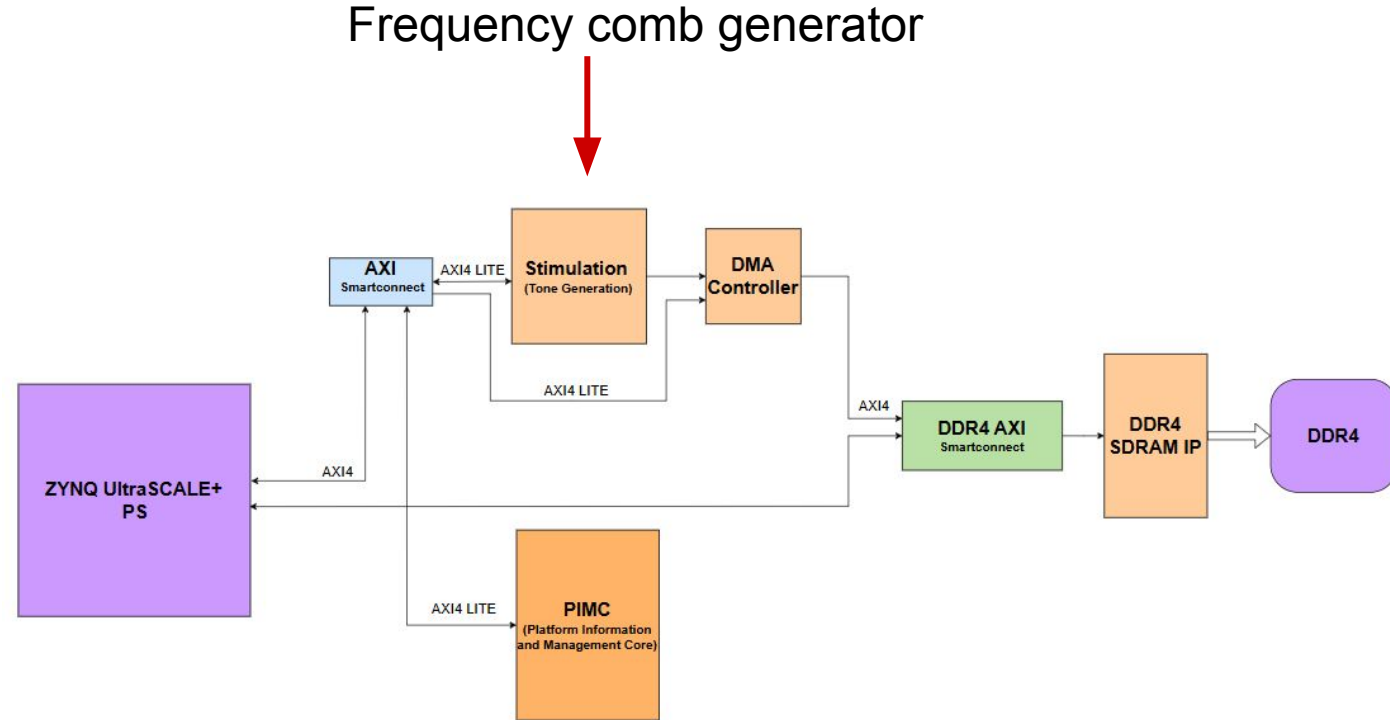
VCK190

VERSAL RF
Evaluation Board
(Once Available)

Migration of our Firmware/Software Infrastructure

Zynq US+ Demonstrator:

- Signal generation module directly connected to DMA Controller
- Modules configurable at runtime via servicehub and AXI
- Custom PIMC module for health checks
- This demonstrator showcases our full infrastructure



Goal: Migrate demonstrator to Versal architecture to prove feasibility