ECHo electronics for µMUX readout

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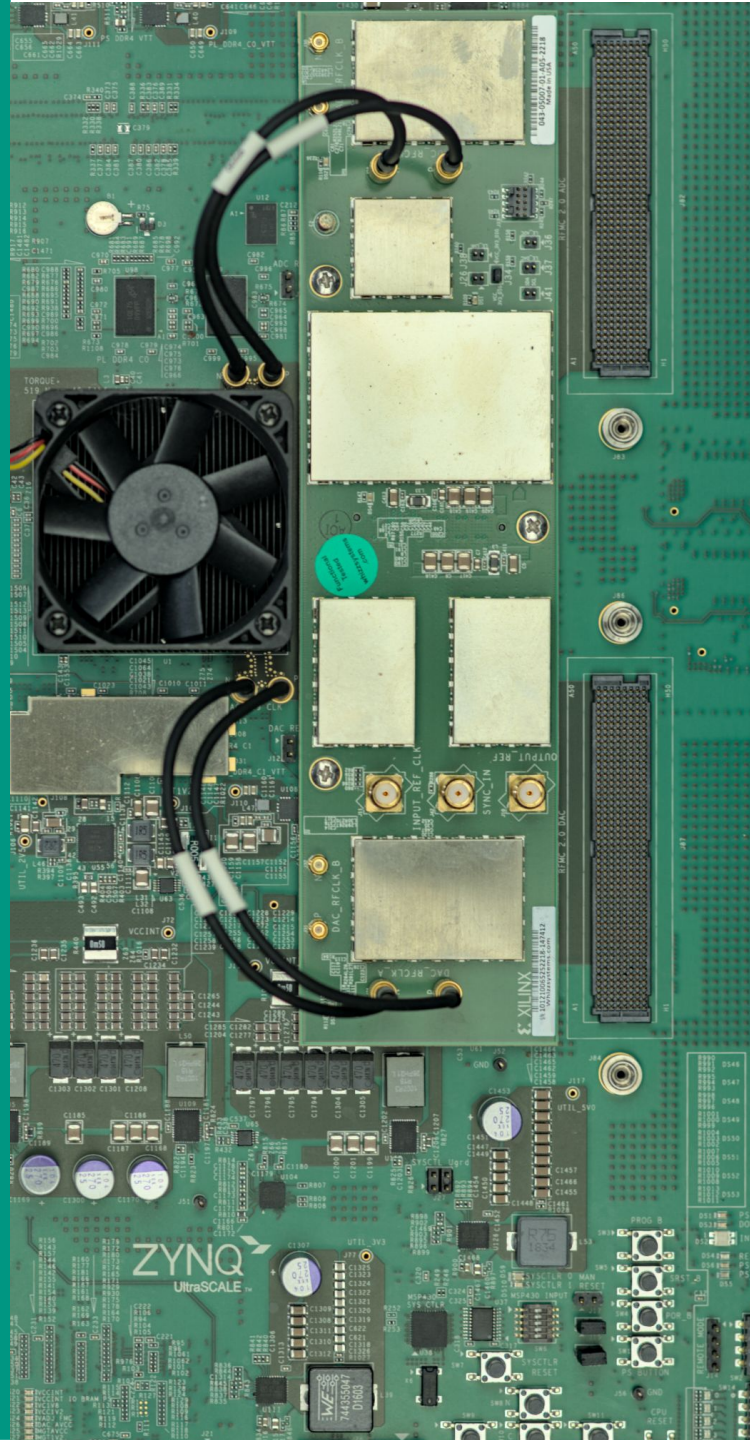
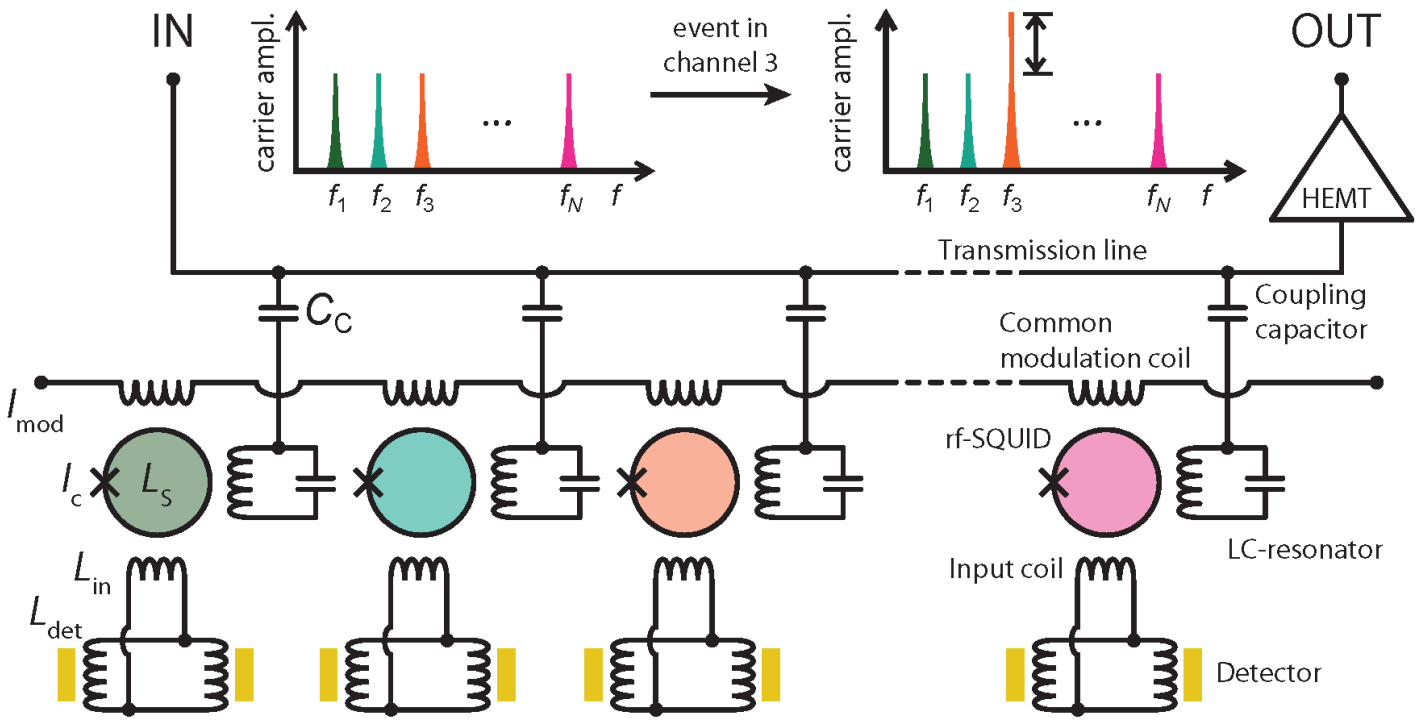
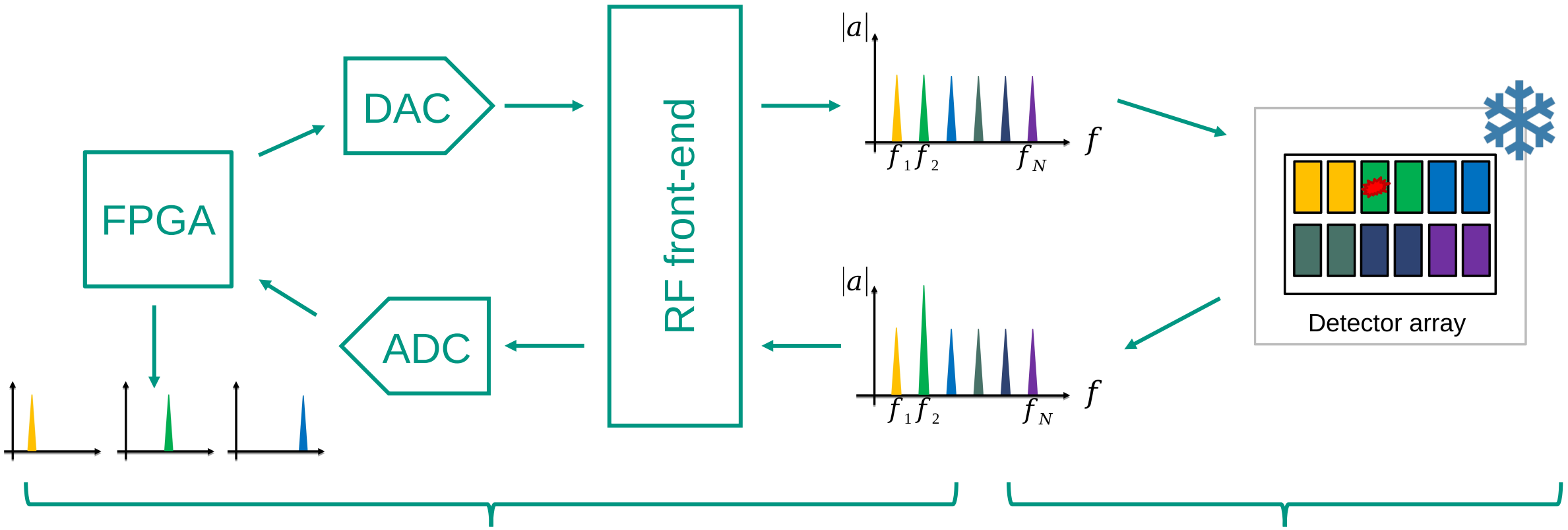


ECHo-100k Detector Design

- Frequency band: 4-8 GHz
- 400 Channels, 800 MMCs
- Spacing 10 MHz
- Detector bandwidth: 1.6 MHz
- 15 systems for 12k detectors



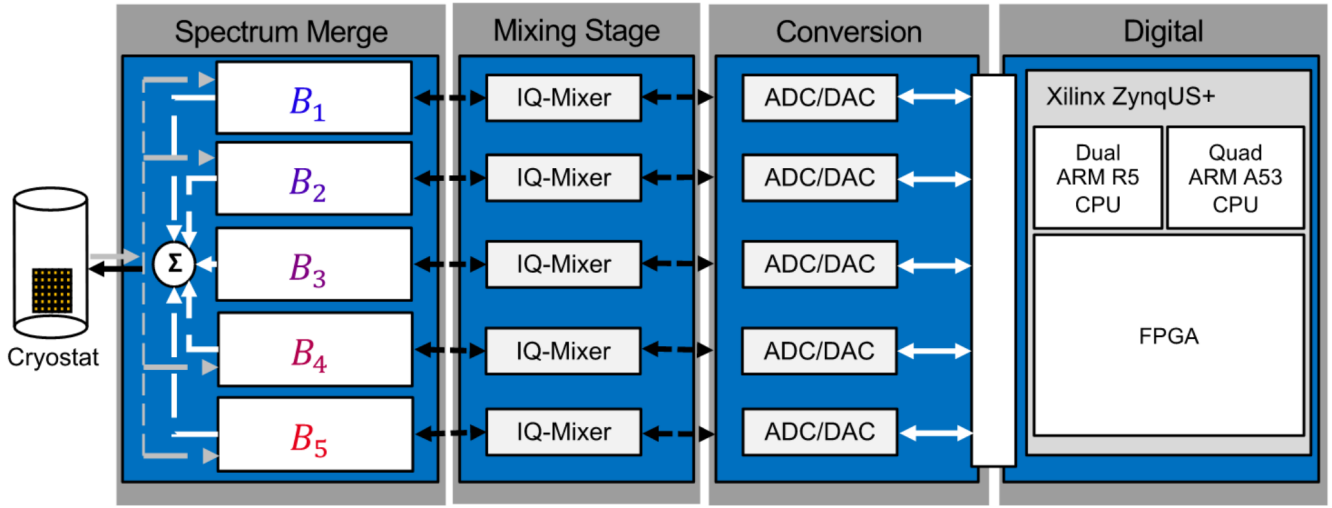
Software-Defined Radio approach

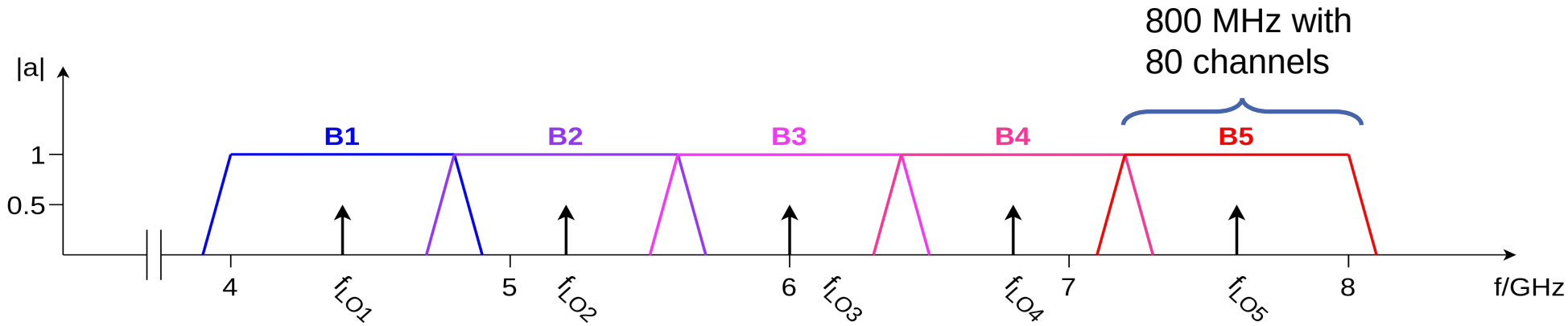


Usable for readout of microwave SQUID multiplexed MMC and TES, as well as KID and KICS

ECHo-100k DAQ Architecture

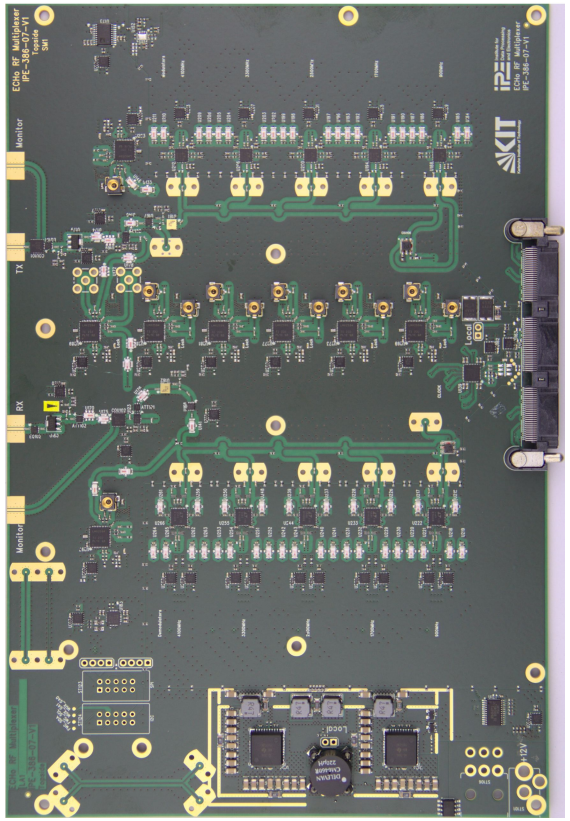
- Digital signal processing on FPGA
- DAC + ADC operate at 1 GS/s
- Merge 5 bands of 800 MHz
- Mix from baseband to RF



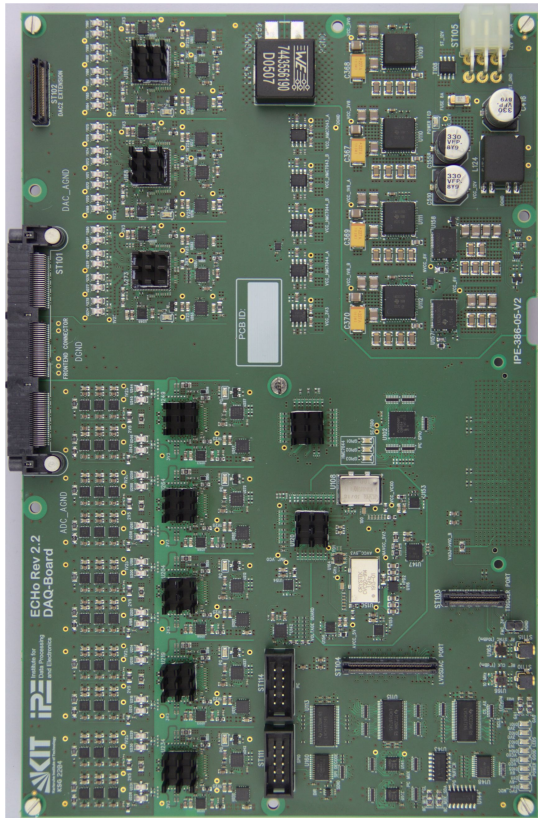


ECHo-100k Hardware

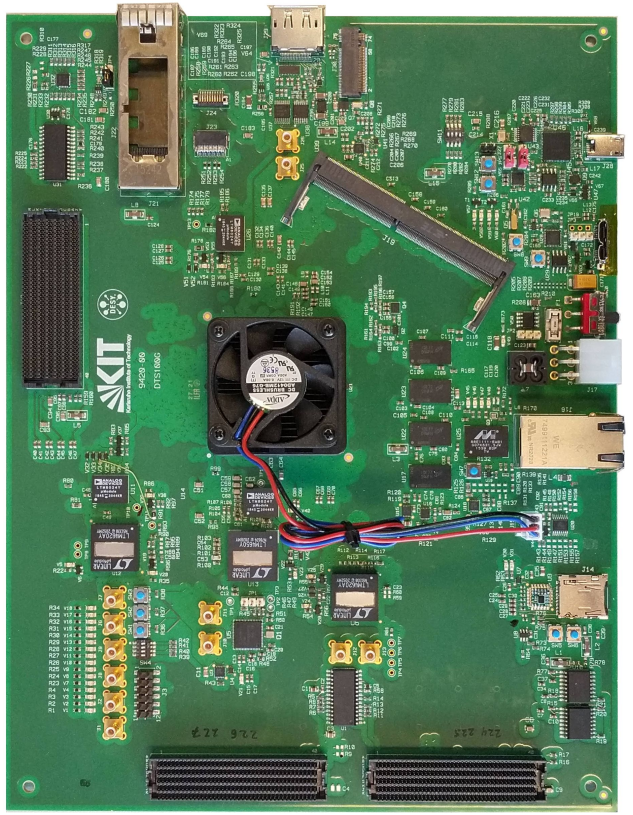
RF-Frontend



Conversion Stage

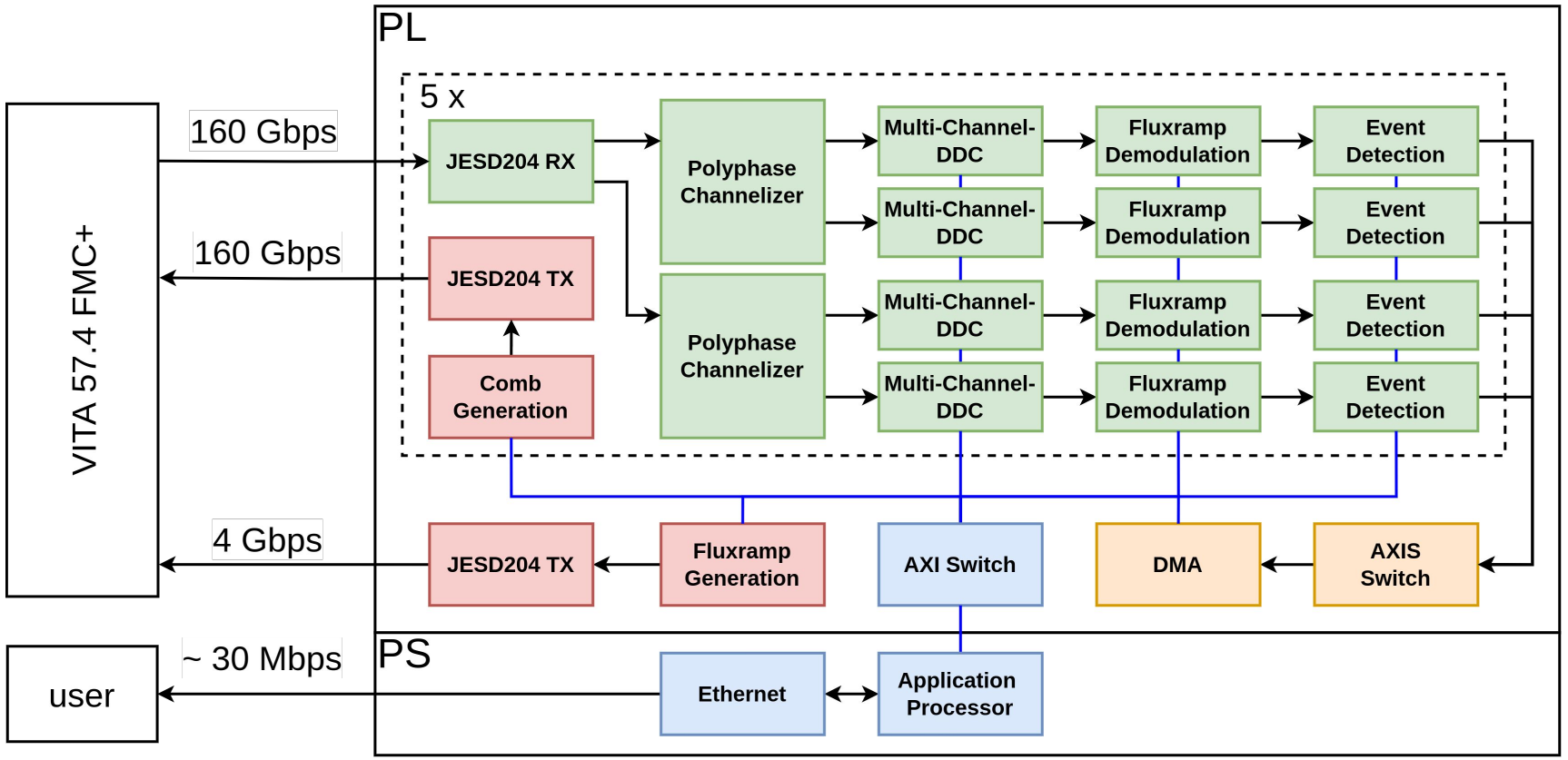


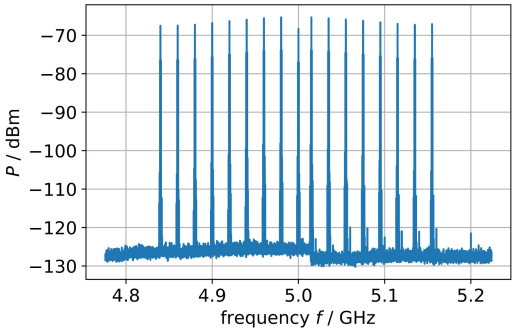
FPGA-Board

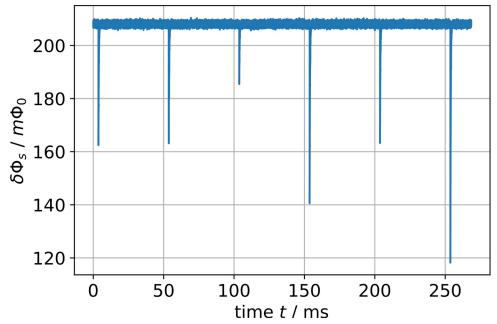


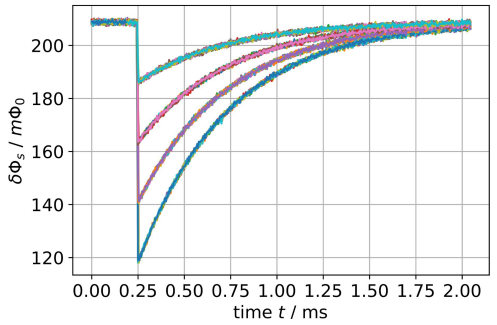
Three custom boards for modular architecture

ECHo-100k Firmware





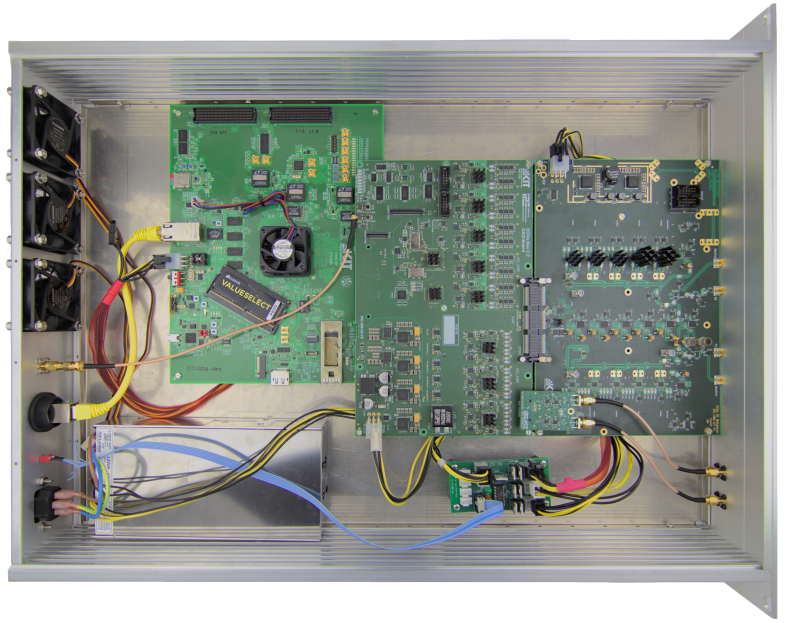




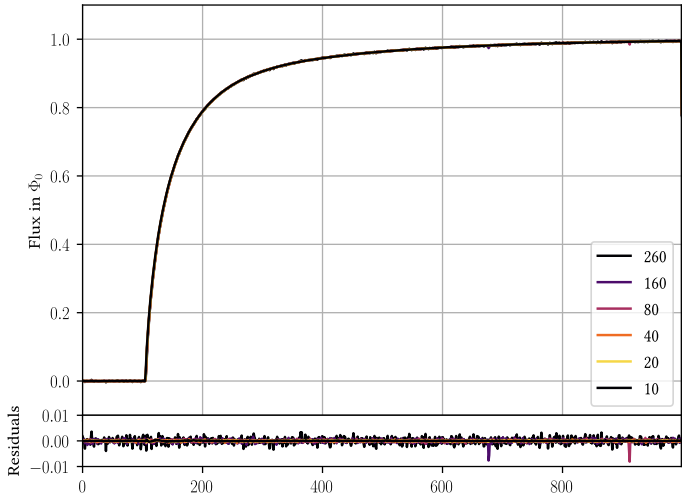
Real-time data processing on FPGA to reconstruct detector signals and reduce data rate

Current status

- 15 Units assembled & commissioned
- Fully functional firmware
  - Carrier tone generation
  - Fluxramp generation
  - Frequency demultiplexing
  - Trigger System
- Successfully used in small-scale measurements
- Verification with digital detector emulator



Analysis of reconstructed pulse:



ECHo-LE Requirements

- Goal: Readout of 20.000 MMCs
- 800 detectors per MUX: 25 systems
- DAQ work packages from ERC Grant:
  - Assembly of 10 additional systems
  - Integration of Tone Tracking feature

<u>Lessons learned from ECHo-100k DAQ:</u>

- Development of custom hardware is laborious
- FPGA – Converter interface is difficult to setup
- Complex hardware architecture, not adaptive

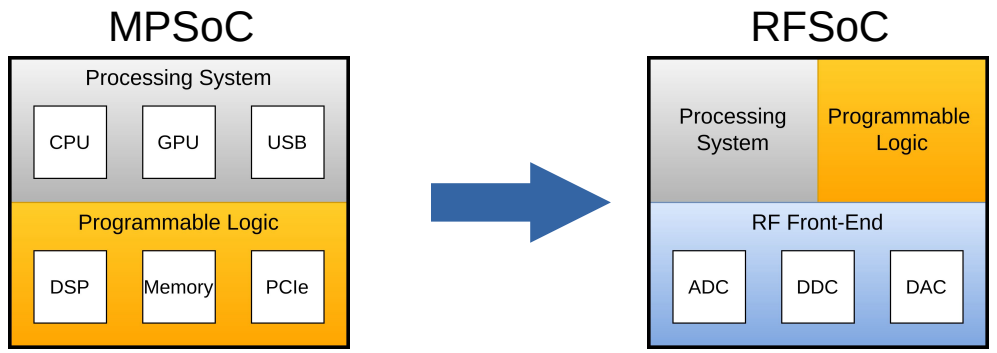
<u>Enhanced readout capability:</u>

- Extension of FPGA firmware
- Static readout tones limit multiplexing factor

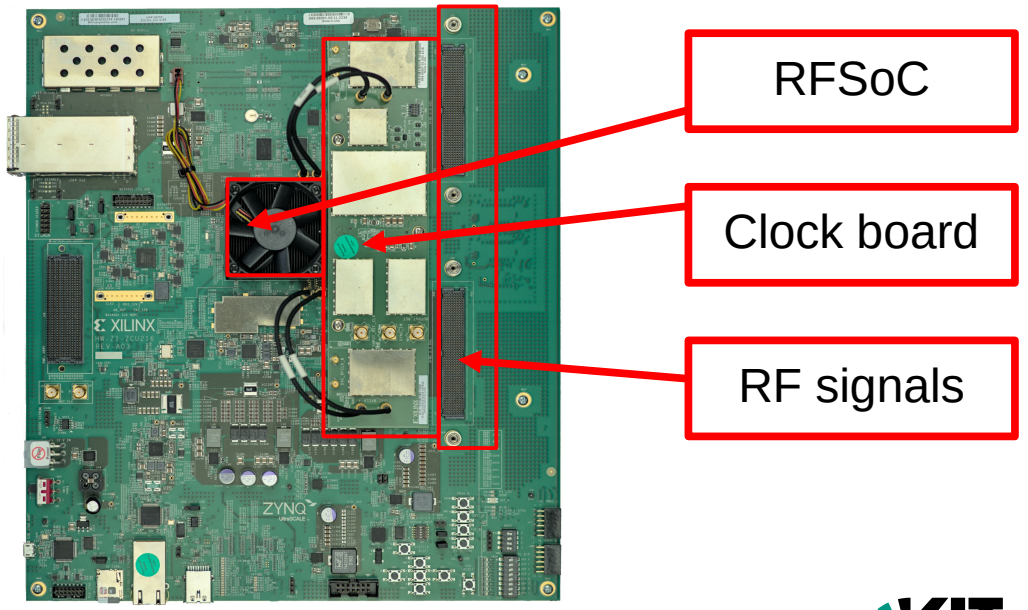
New DAQ systems will be improved using previous knowledge

ECHo-LE Hardware Proposal

- AMD offers single-chip solution: RFSoC
- Advantages:
  - Higher integration
  - Easier interface to converters
  - Higher sampling rates
- Same architecture (Zynq UltraScale+)
- XCZU49DR device:
  - 16 DAC with 10 GS/s
  - 16 ADC with 2.5 GS/s



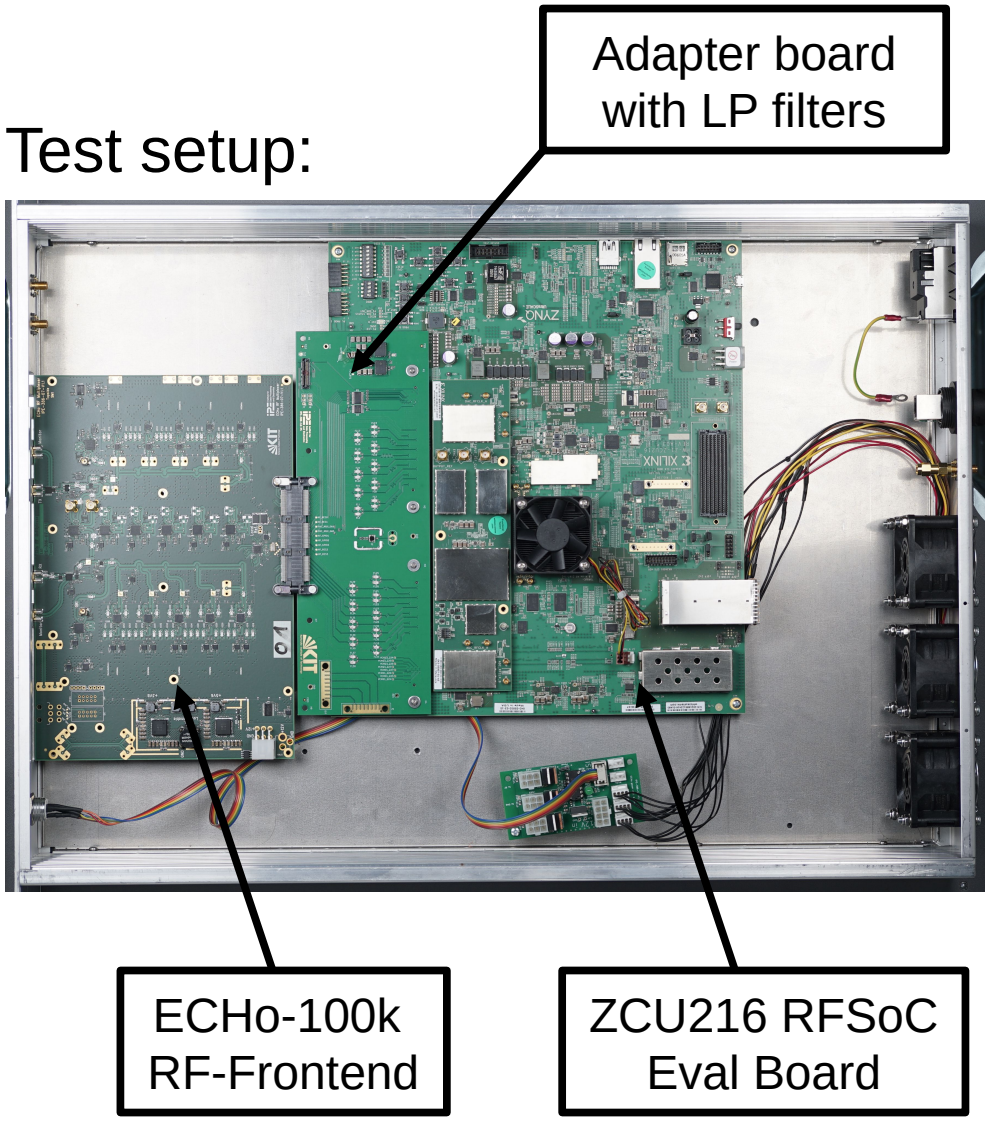
AMD ZCU216 Eval board:



ECHo-LE Hardware Architecture

- RFSoC system
  - ZCU216 Evaluation board
  - SoM with custom base board
- Custom adapter card
  - Map DAC / ADC to RF channels
  - Low pass filter for signal conditioning
  - Connector for fluxramp board
- Analog front-end from ECHo-100k

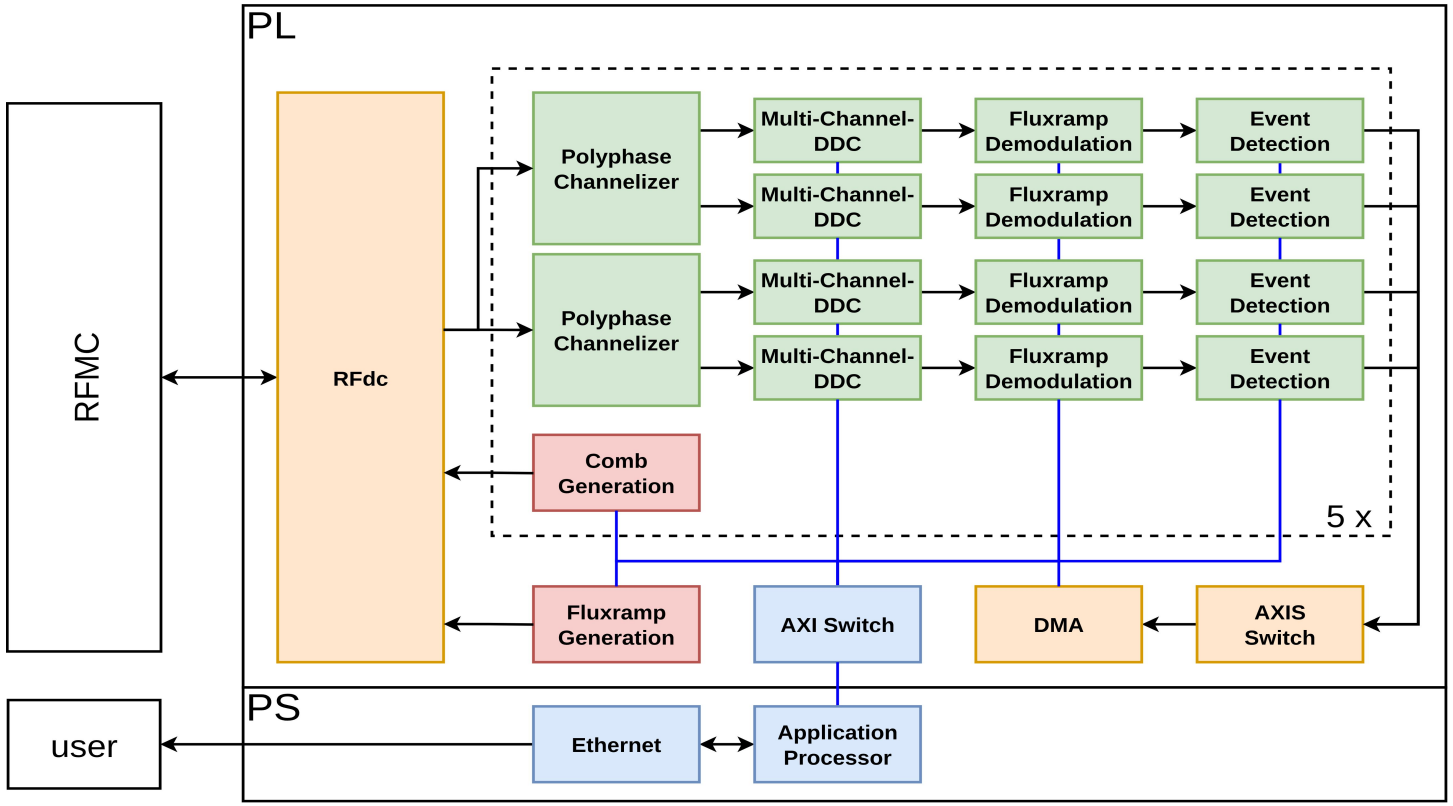
Test setup:



RFSoC-based setup to evaluate performance

ECHo-LE Firmware

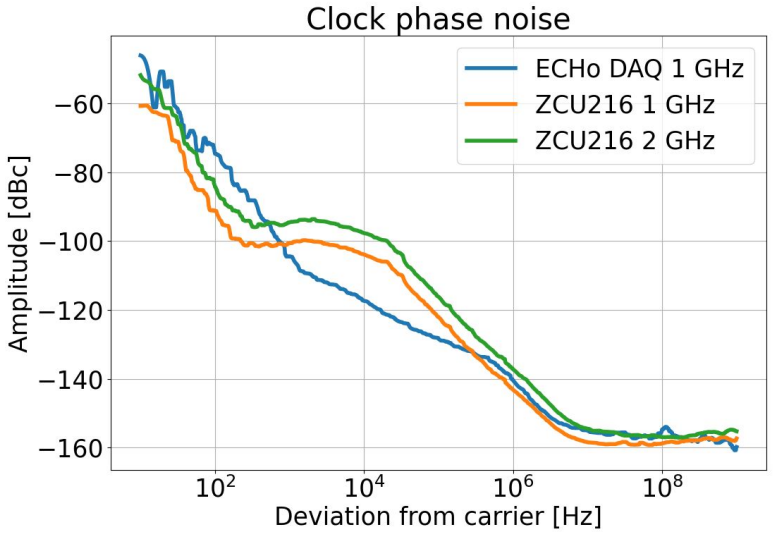
- Replace JESD204 Protocol
- Use RFdc (AMD IP-Core)
  - Up-/ Downmixing
  - Interpolation/ Decimation
- Firmware migration complete
- More DSPs enable additional algorithms

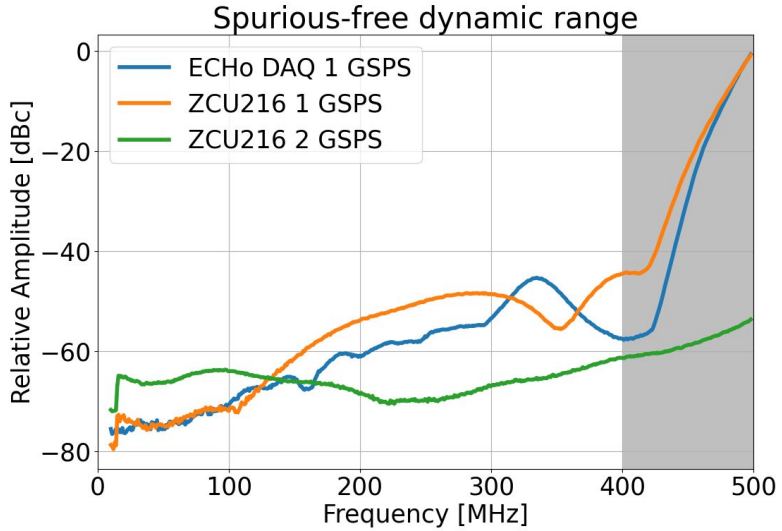


Type	MPSoC (ZU19EG)	RFSoC (ZU49DR)	ECHo-LE FW
LUT	523k	425k	323k
Logic cells	1143k	930k	544k
Memory	80.4 Mb	73.5 Mb	34.8 Mb
DSP	1968	4272	1334

RFSoC Characterization

- ZCU216 comparable to ECHo hardware
- Clock quality limited by eval card, could be improved with custom clock board
- Higher sampling rates of DAC and ADC improve SFDR





Previous work:

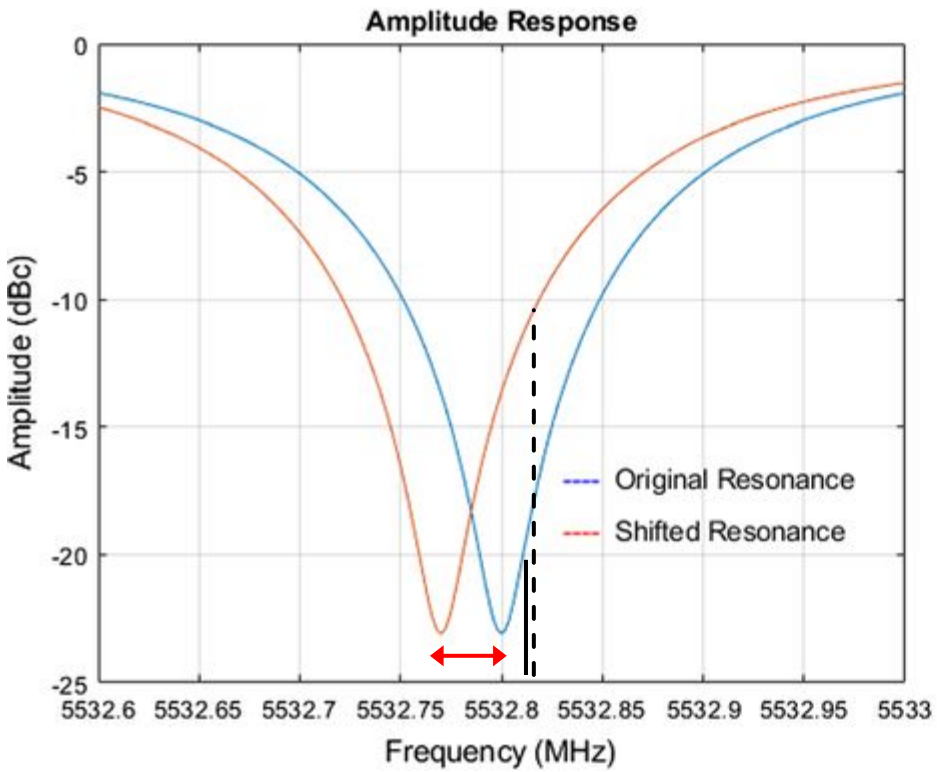
M. Garcia *et al*., "RFSoC Gen3-based SDR Characterization for the Readout System of Low-Temperature Bolometers"

R. Gartmann *et al*., "Evaluating the RFSoC as a SDR readout system for Magnetic Microcalorimeters"

RFSoC-based DAQ shows comparable performance as custom hardware

Tone Tracking

- Resonance frequency moves periodically
- Variable input power at HEMT amplifier, may lead to clipping
- Track resonance frequency with readout tone
- Requirements:
  - adaptive tone generation
  - control loop to correct frequency error



Firmware feature currently under active development

Conclusions

- 15 ECHo-100k DAQ systems ready for use
- 10 additional systems for ECHo-LE
- New systems will be based on RFSoC
- Similar performance, higher clock rates
- Tone Tracking under active development