Development of Readout Electronics of the IceCube-Gen2 Surface Array

The ARGO Readout Board
ARENA 2026 - Karlsruhe

Frederik Schmitt and Matthias Kleifges **for the IceCube-Gen2 Collaboration**
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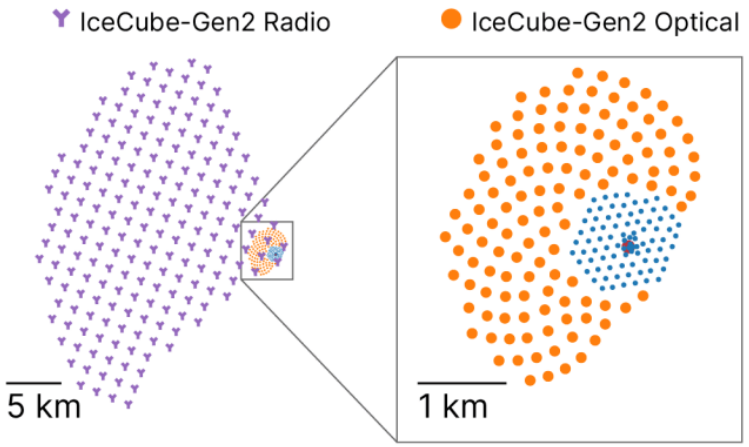
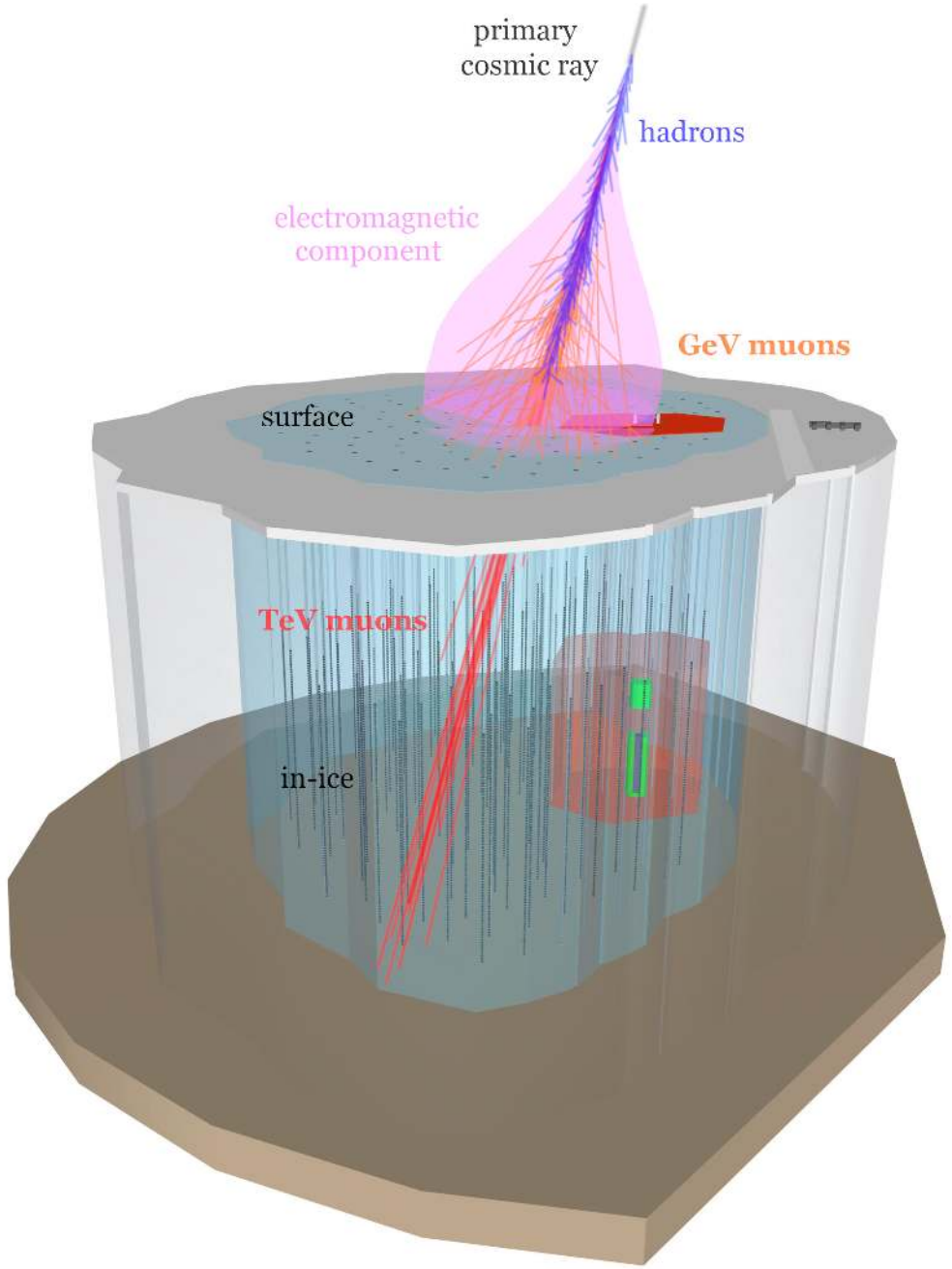
IceCube Gen2

Proposed next generation neutrino observatory

Detector components:

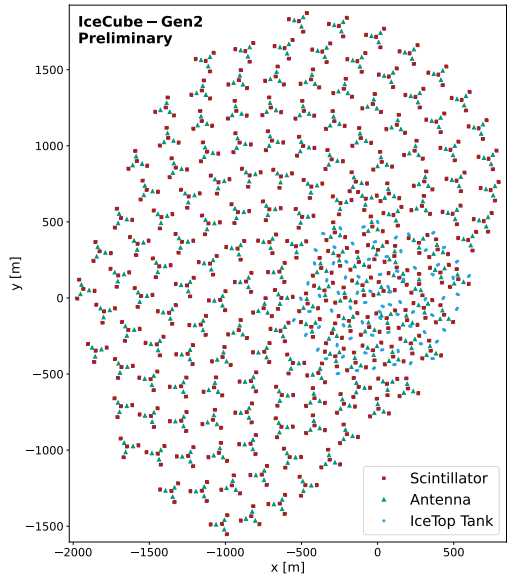
- 8 km^3 In-ice Neutrino detector
- 500 km^2 In-ice radio array
  - For extremely high energy neutrinos
- 6.6 km^2 Surface air-shower detector
  - **This Talk**

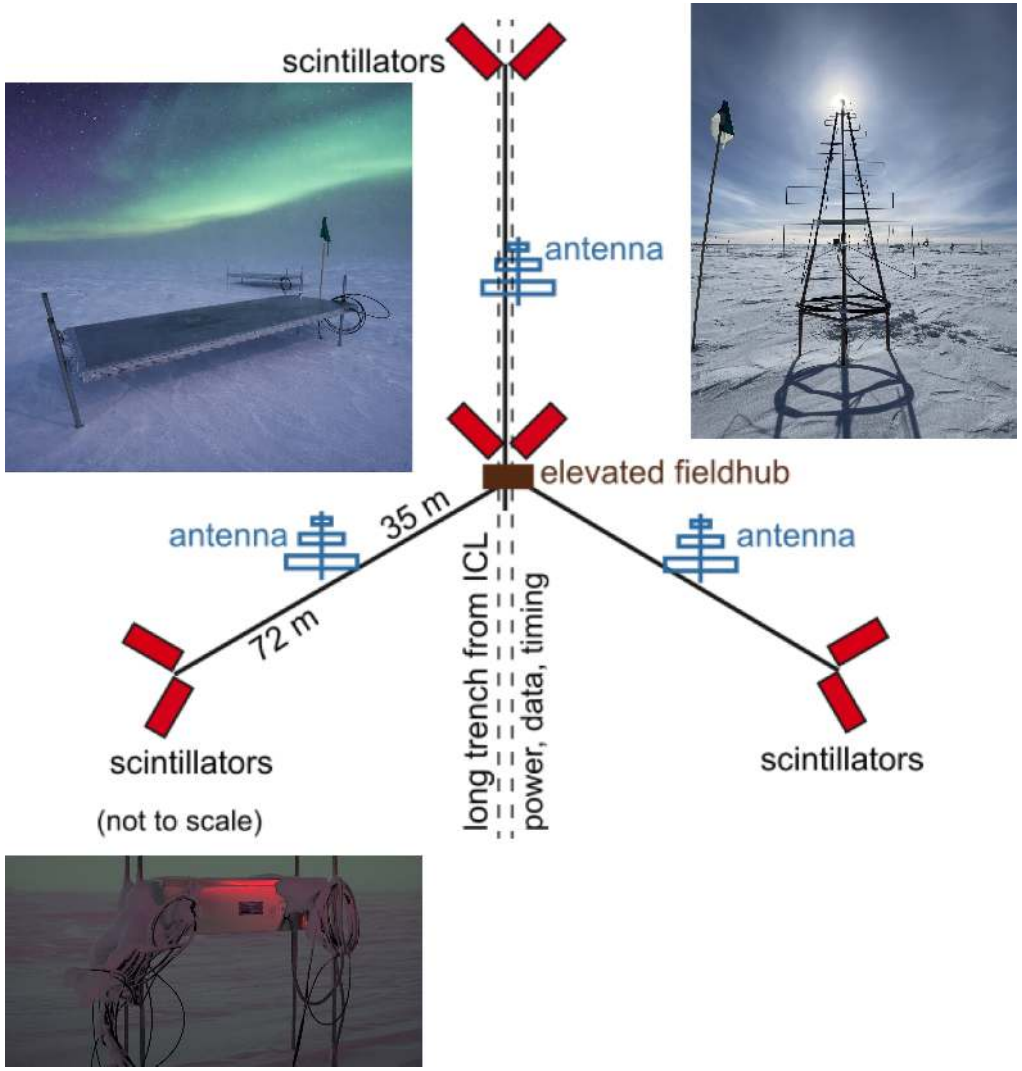




The IceCube Surface Stations

- 8 Scintillators:
  - 1.5 m^2 plastic scintillator
  - Readout via SiPM
  - Frontend “uDAQ” digitization PCB in module
  - RS485 communication with station
- 3 SKALA-v2 radio antennas
  - LPDA antenna
  - Prototypes of the SKA Low antenna
  - 70 – 340 MHz bandwidth
  - Triggered by scint coincidence
- **1 DAQ board (This Talk)**





IceCube Surface Array Enhancement

The Project:

- Extension of IceTop with 32 surface stations

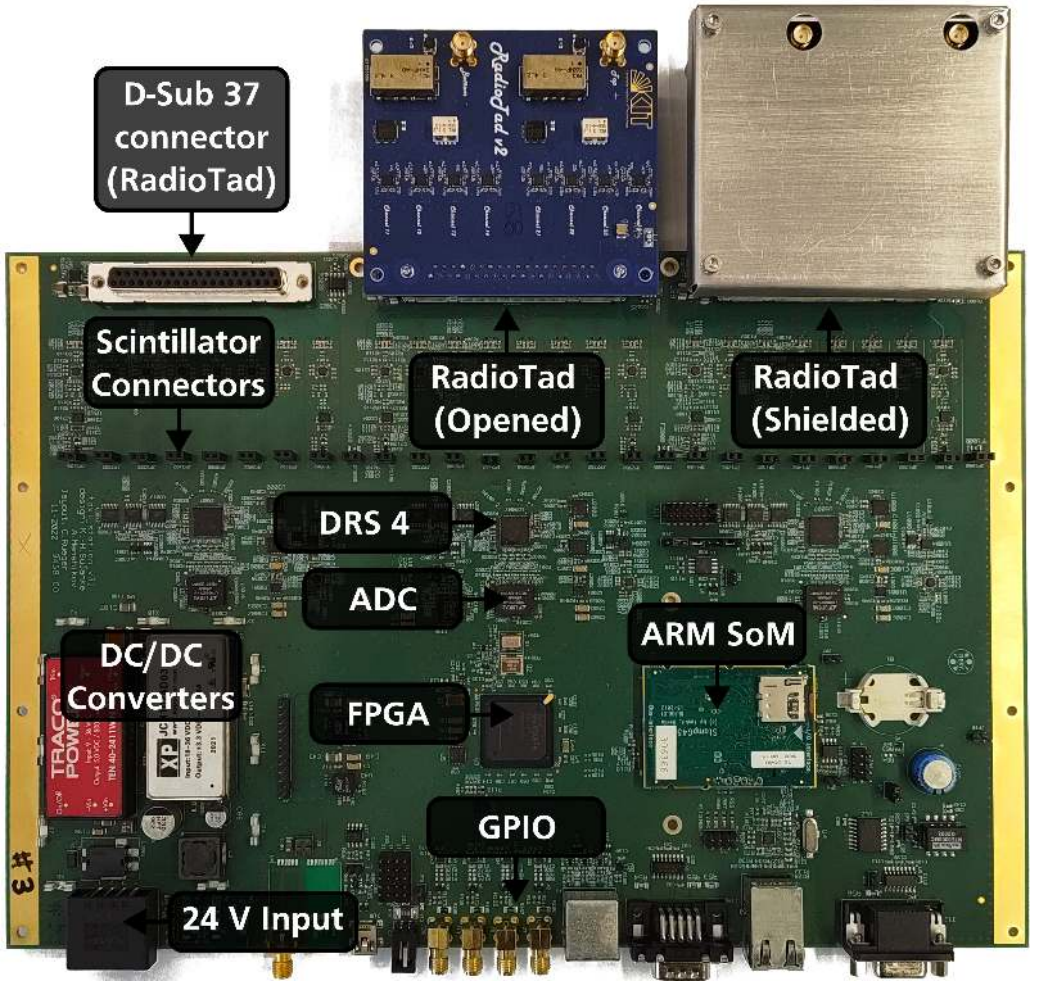
TAXI DAQ Board:

- Readout Board for the SAE
- Radio Buffers based on DRS4 analog Ringbuffer
  Fixed size of max. 4096 values per channel (≈ 4 µs)
- Several parts no longer available

Status:

- 3 stations deployed
- 4 ready to deploy
- Stations at Auger and TA

Talks by C. Merx, F. Schöder, M. Venugopal and S. Verpoest



Readout Requirements for the Surface Array of IceCube-Gen2

- **Idea:** Keep mainboard experiment agnostic
  $\Rightarrow$ Realize experiment specific parts with **daughter-boards**
  - 8 scintillator channels
  - 8 radio frontends (Filters, Amplifiers, Test Pulsers)
- $<$ 1 ns timing accuracy (GPS or WhiteRabbit)
- Power budget **40** – **60 W** per station
- Keep board cost optimized

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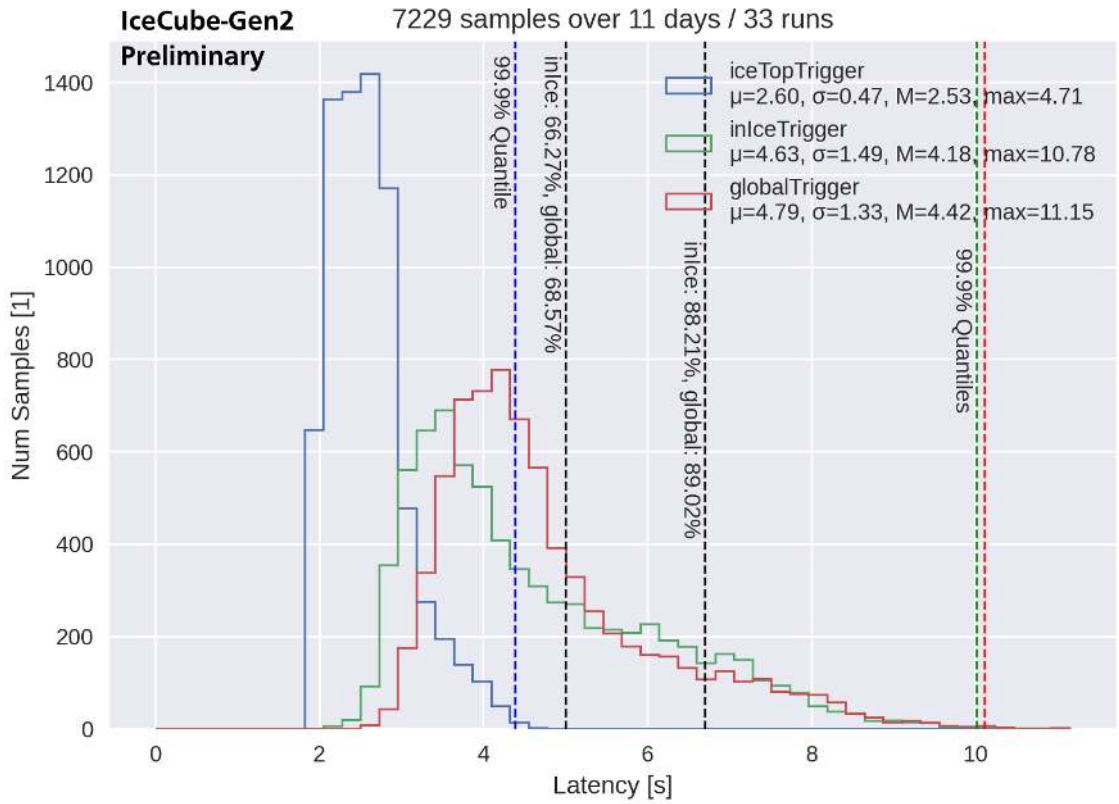
  - Station internal: Scint coincidence
  - Global software trigger:
    e.g. InIce detection (**up to 5-10 s delay**)
  - $\Rightarrow$ Deep buffers needed (5 s $\approx$ **16 GB per antenna**)



IceTop and IceCube trigger delay time.
By Mirko Kugelmeier

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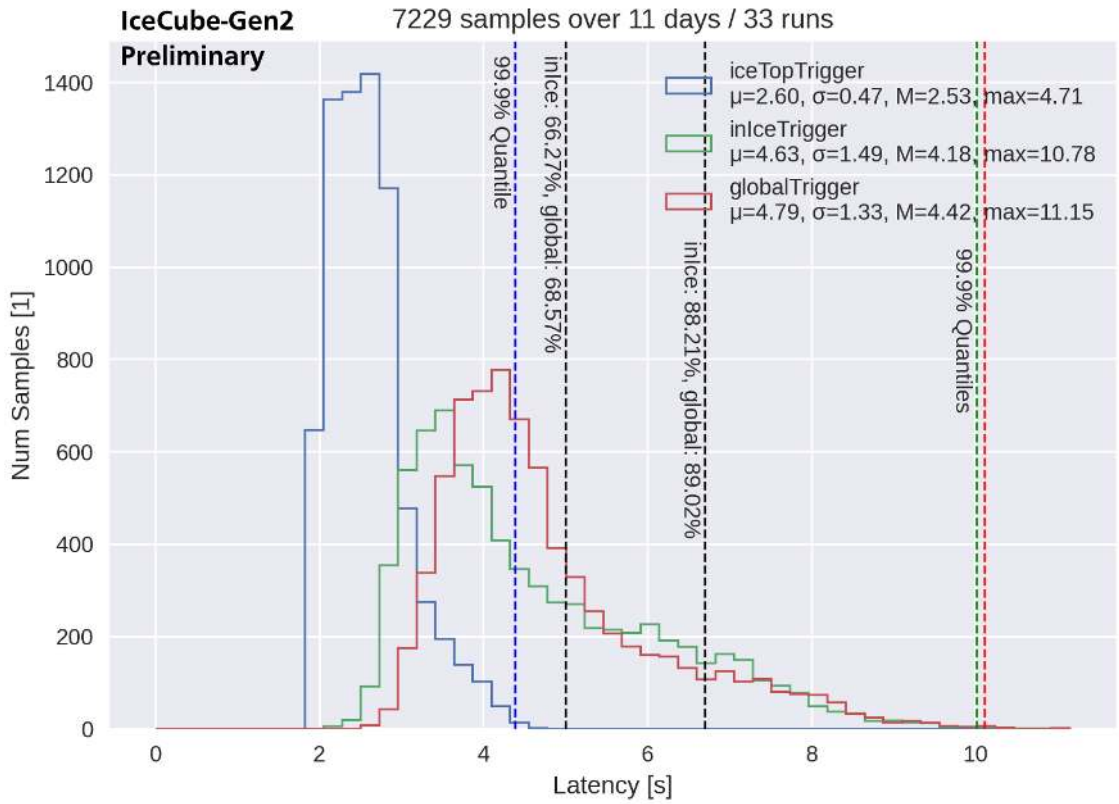

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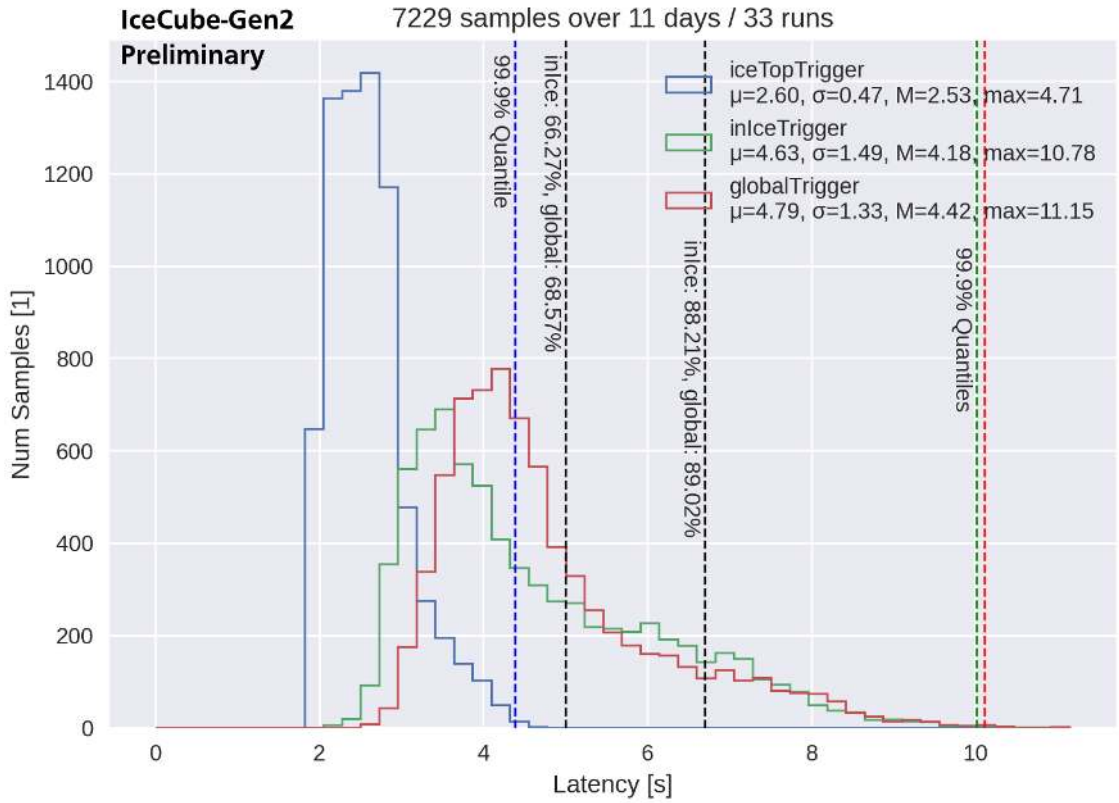
But: We can combine them



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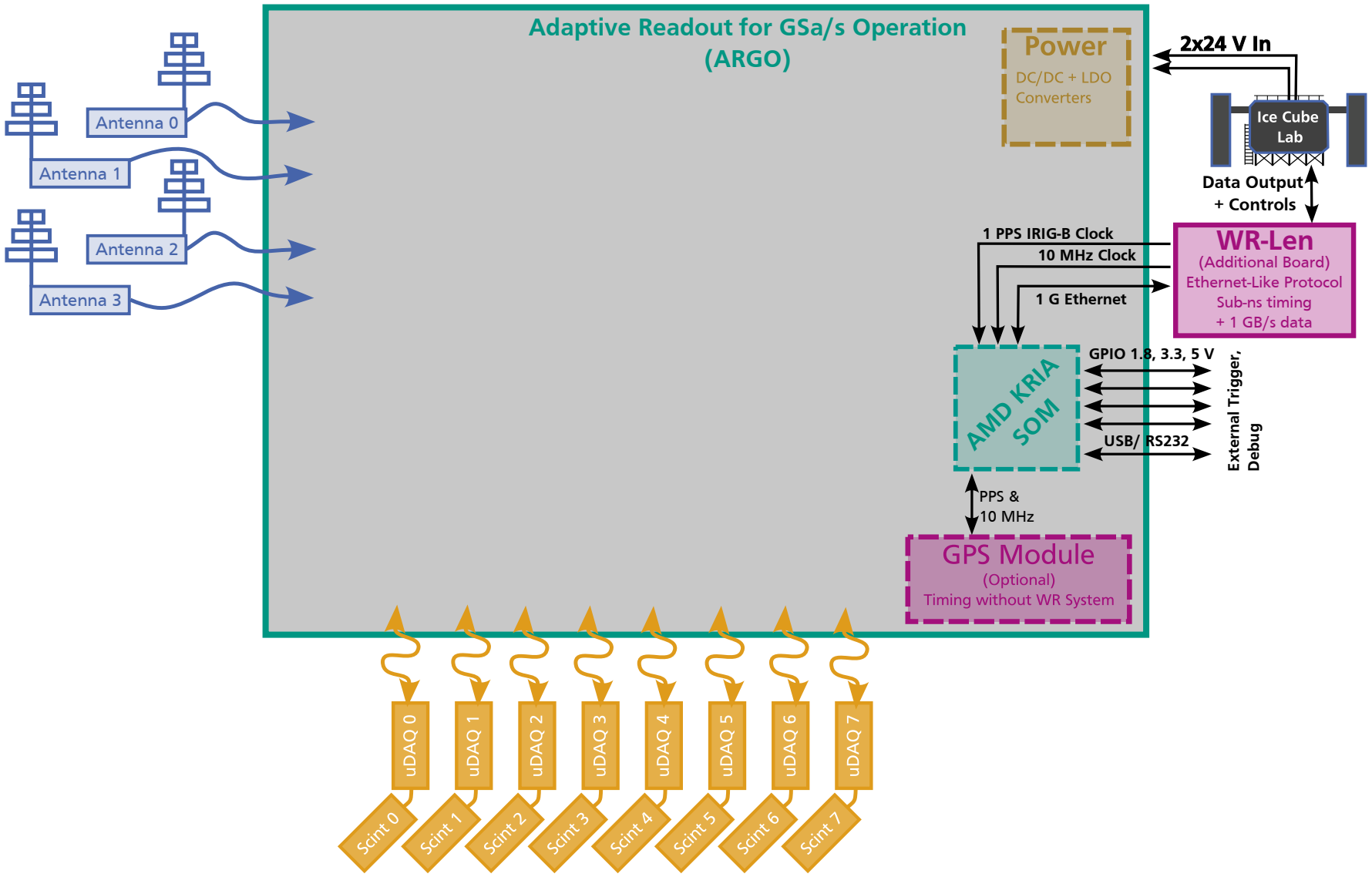
ARGO: Adaptive Readout for GSa/s Operation



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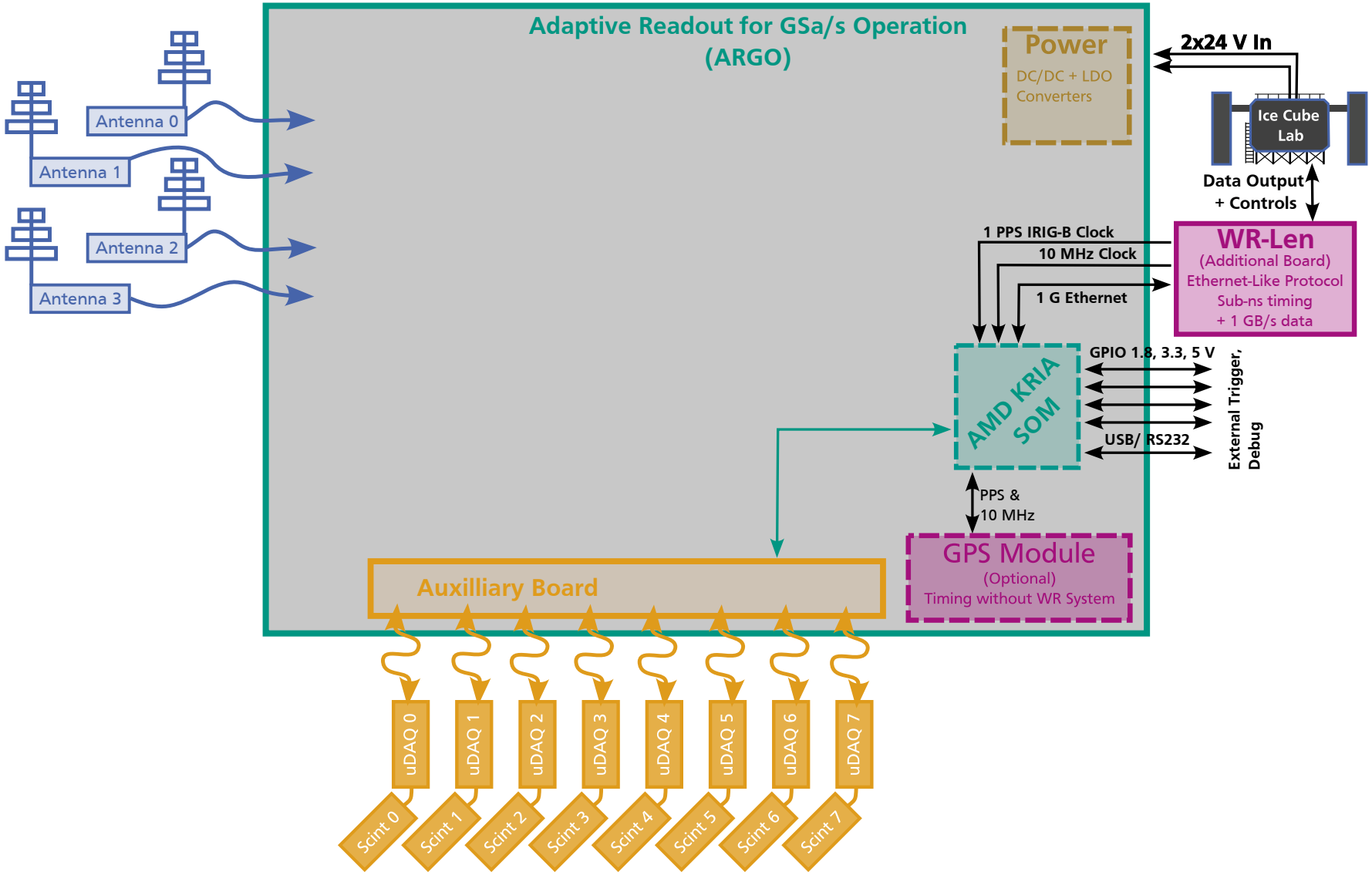

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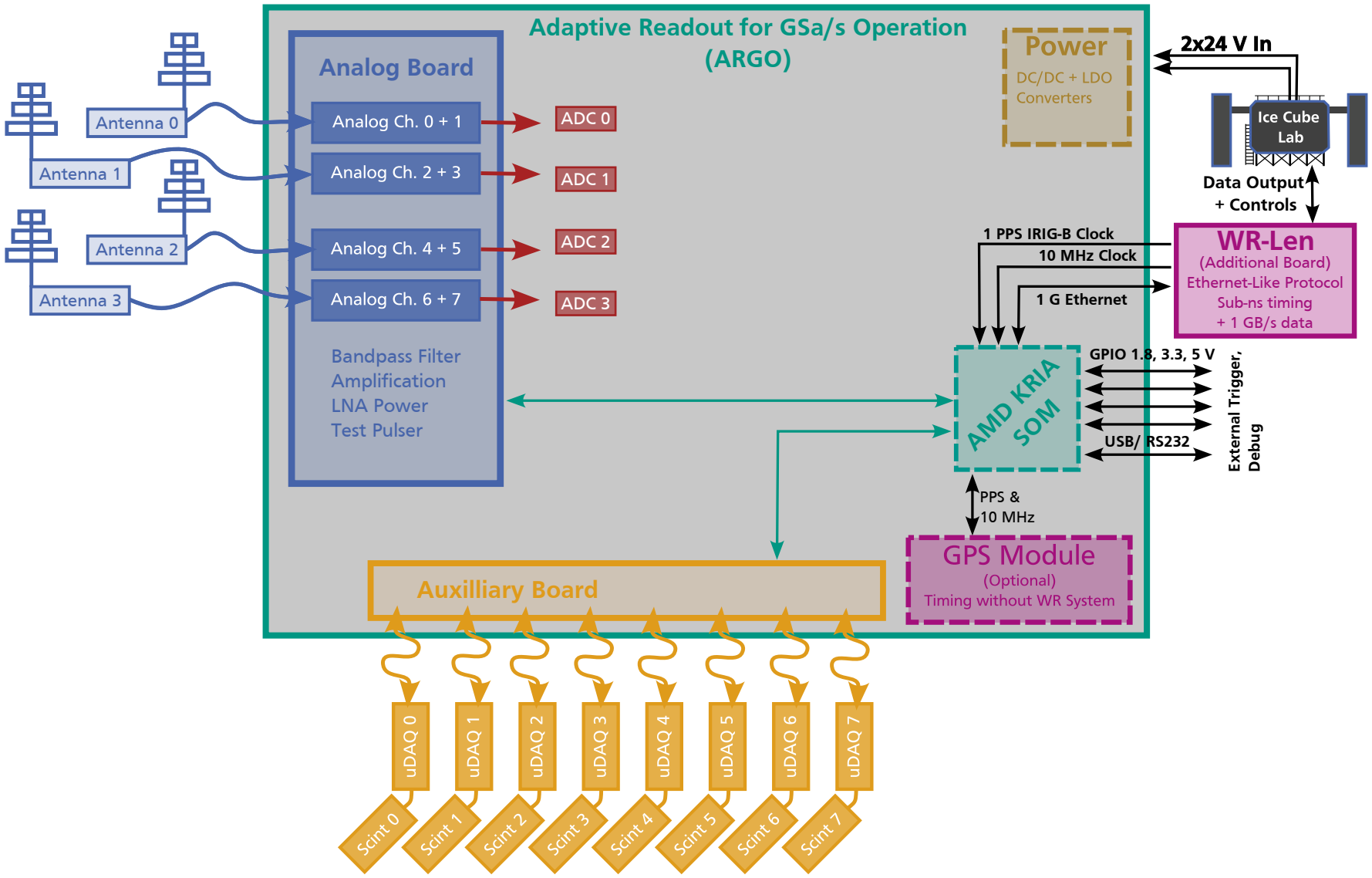

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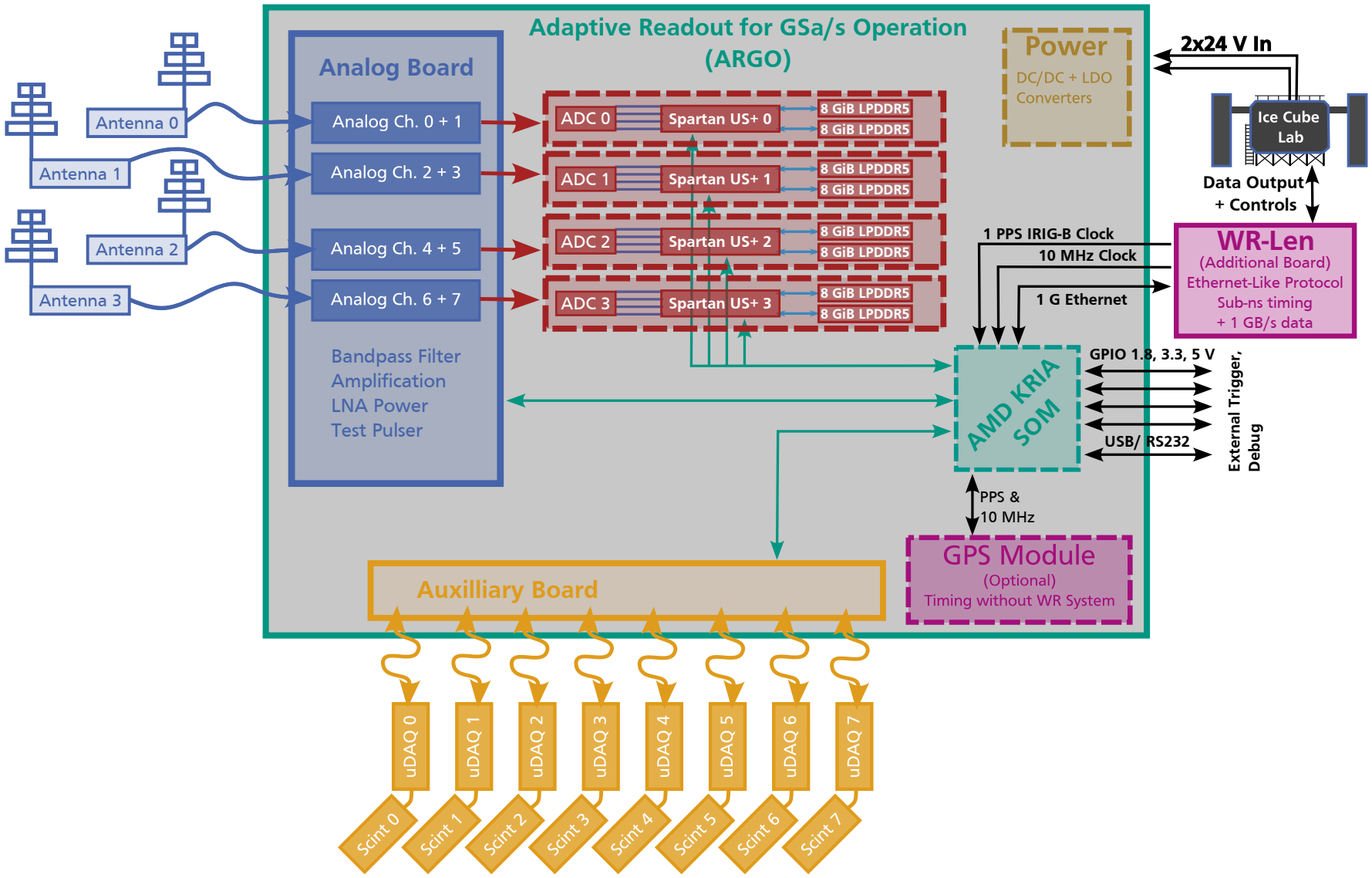


Status of Development

Analog Board

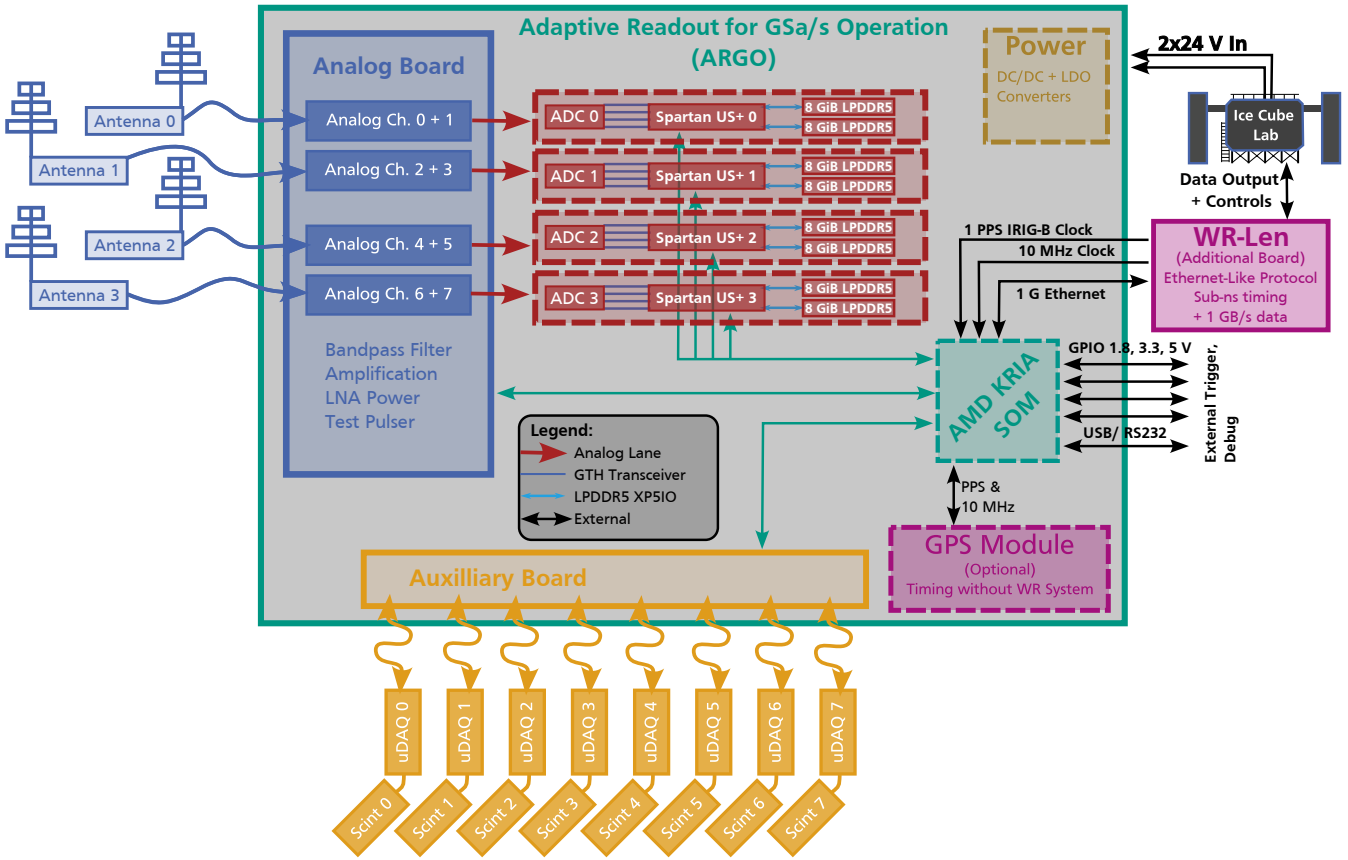
- Layout design finished
- IPE currently designing a test board

Auxiliary Board

- Schematics almost ready, approaching layout stage

ARGO

- Entering schematic design soon
- By then: Working on ADC & FPGA test hardware



Institute of Experimental Particle Physics

Institute for Astroparticle Physics (IAP)

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