A Flash Introduction to a Physicist

IPE Seminar: Getting to Know

Ahmed Qamesh | April 16, 2026

Institute for
Data Processing
and Electronics

Outline

Section 1

Motivation

Motivation

Karlsruhe Institute of Technology

- The **”Getting to Know”** seminar series aims to welcome new colleagues at Institute for data Proceeding and Electronics (IPE).
- I am here for more than a year but it is always an exciting step – and a great opportunity to **meet people**!
- I would like to take this chance to tell you a bit about:
  - Where I come from and how I got here
  - The experiences that shaped my research
  - What I am looking forward to working on at IPE
- I hope this talk is the beginning of many great **collaborations and conversations**!

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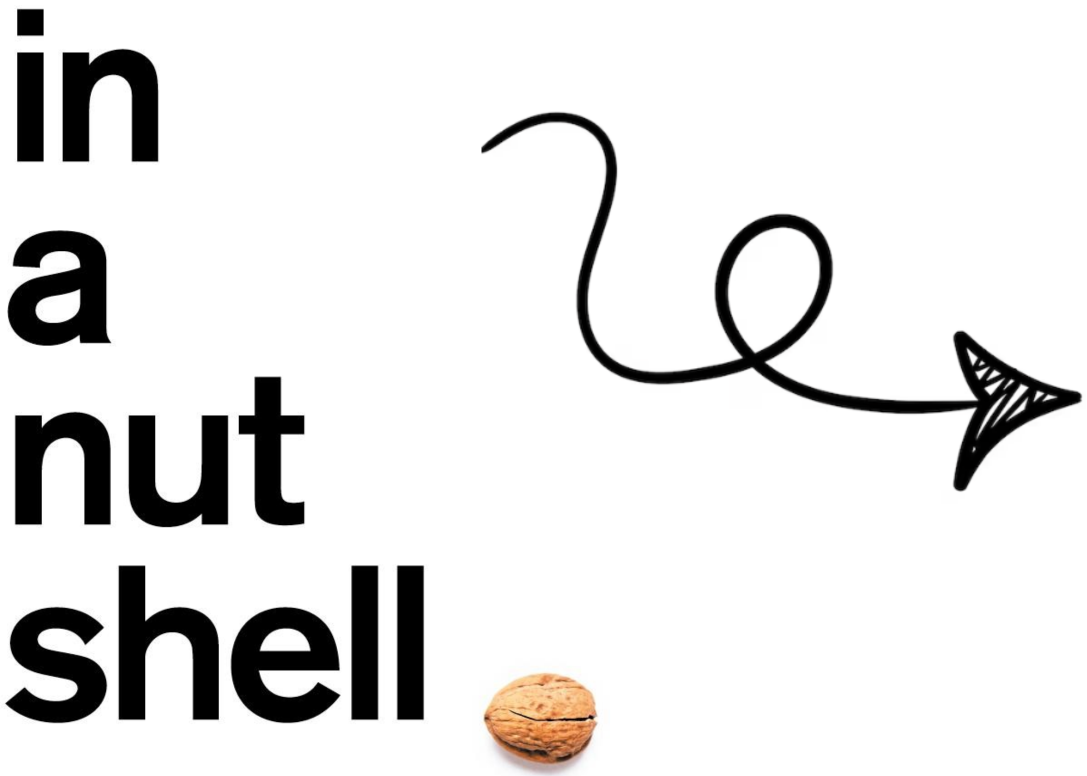
in
a
nut
shell

Institute for Data Processing and Electronics

Motivation



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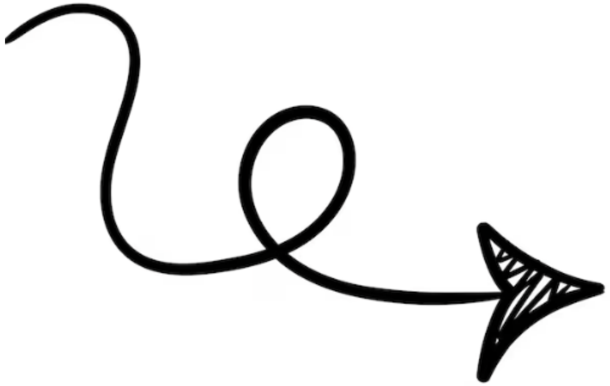

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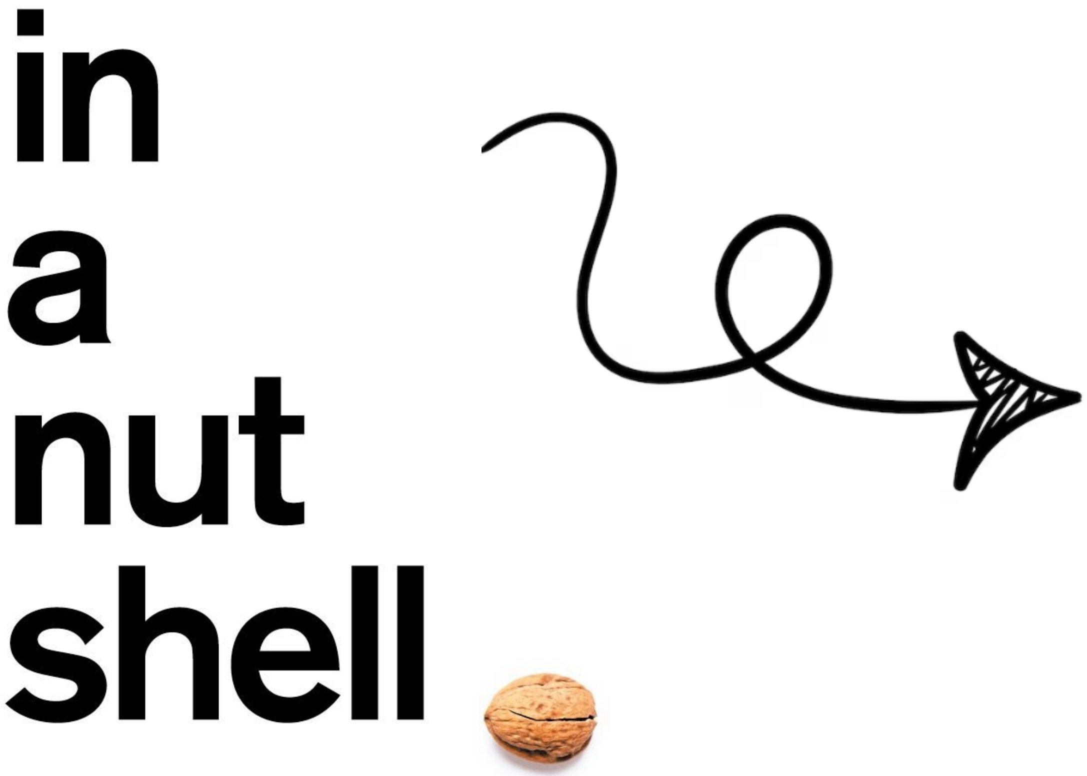

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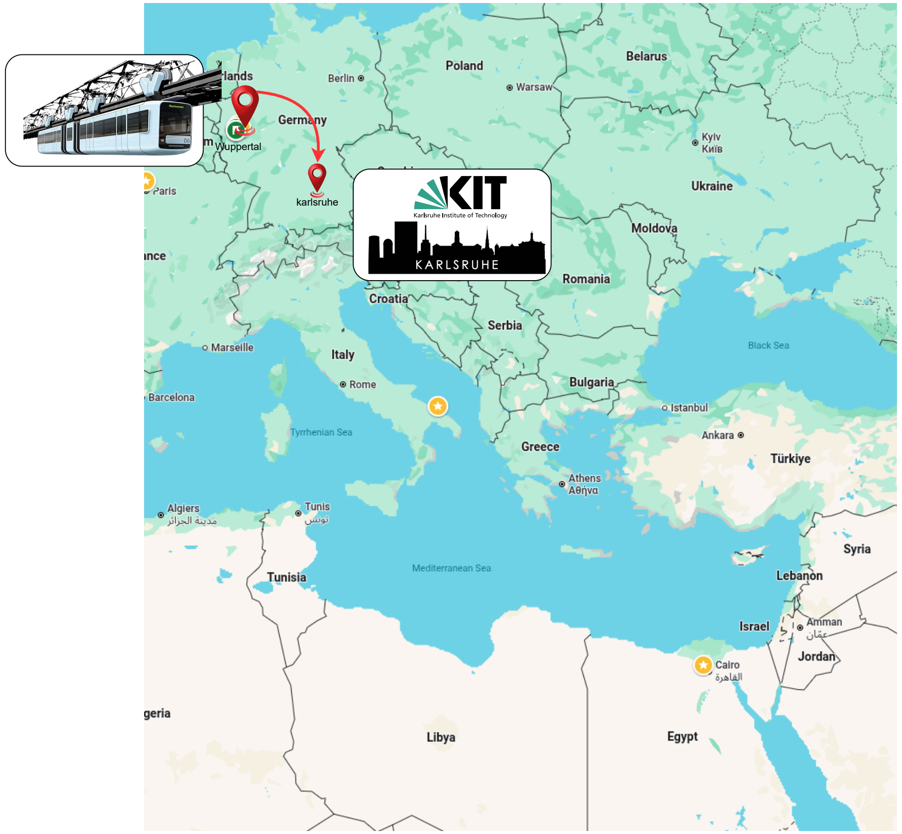

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Employment History:

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Employment History:

Research Interest:

- Detector development, including beam tests, system debugging, and hardware testing.
- Development of firmware and software for FPGAs and embedded systems.
- Further development, construction, and testing, integration of existing systems.

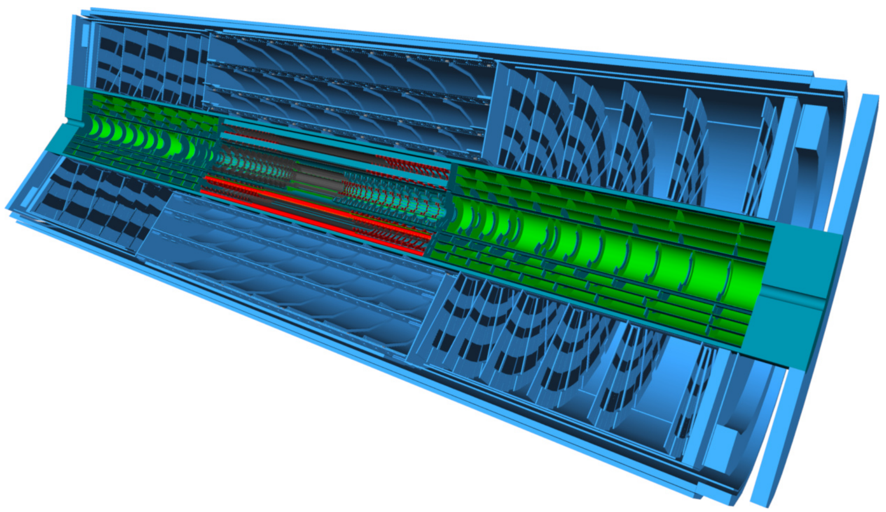
Section 2

My PhD Journey So Far...

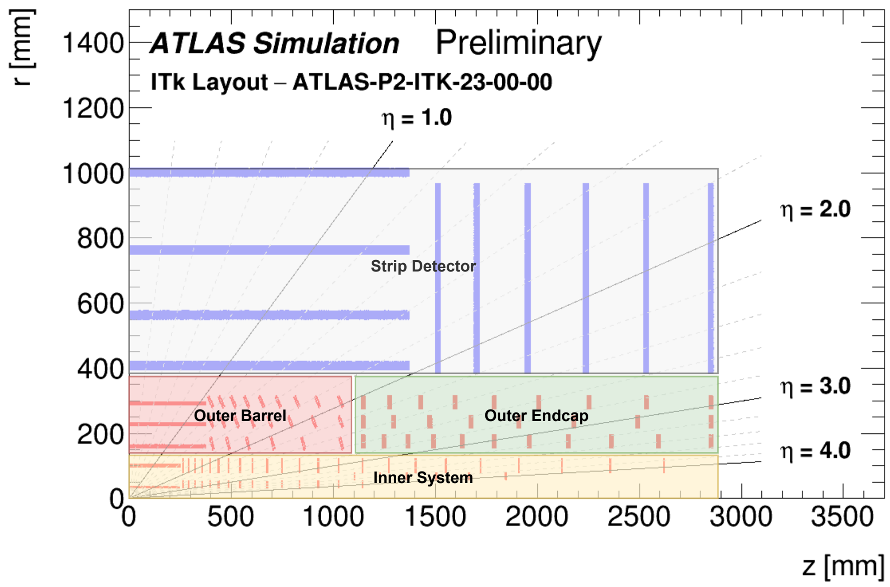
The LHC and its Upgrade

The ATLAS Inner Detector in the New Upgrade

- The High Luminosity LHC (HL-LHC) demands major upgrades to the Inner Detector (ID) of the ATLAS Detector (Slide 38):
- The ID will be replaced by the all-silicon-based **Inner Tracker (ITk)**.
- The Pixel detector area of the ID will increase from $2\,\mathrm{m}^2$ to $13\,\mathrm{m}^2$.



(a) The ATLAS Phase-II ITk layout [1].



(b) A quadrant from the point of interaction [2].

- A **Serial Powering (SP)** approach is used for the Pixel detector powering.
  - Reduce the material budget.
  - Decrease cable power losses.
- A new **Detector Control System (DCS)** is required for Monitoring and control of hardware.

Detector Control System (DCS) for the ITk Pixel Detector

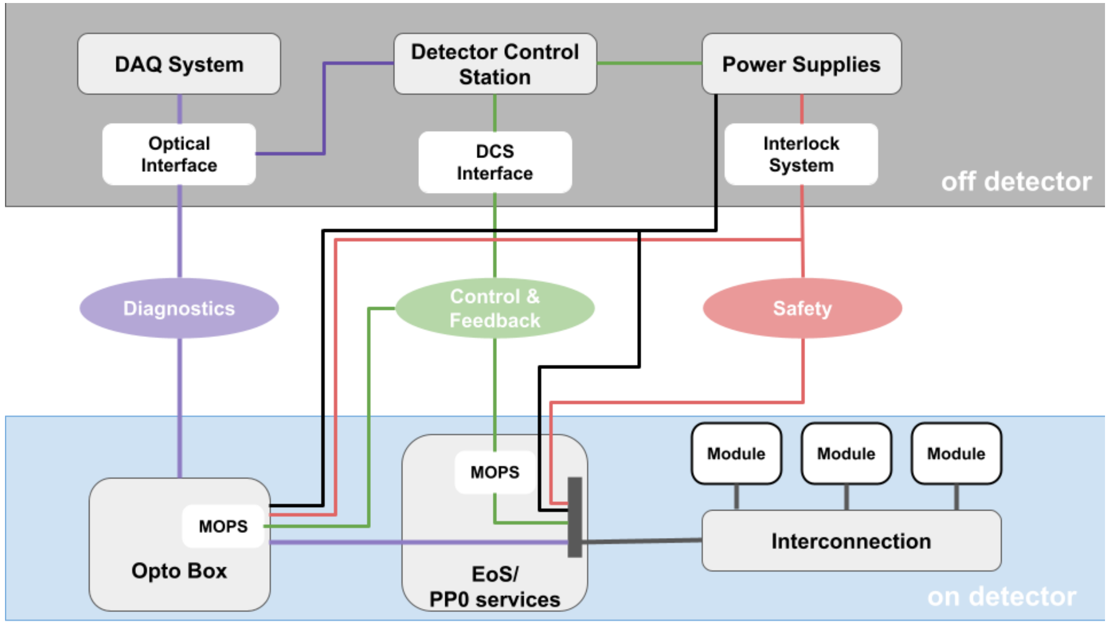
- The Detector Control System (DCS) ensures the safe operation of the ATLAS detector.
- Meets high demands on control, measurement, and safety imposed by the ITk detector.

What it does:

1. Monitoring and control of hardware.
2. Ensures reliable data acquisition.
3. Guarantees the detector safety.

The Pixel DCS Pathways:

1. Safety path (Slide 39).
2. **Control & feedback path**).
3. Diagnostics path (Slide 40).



The new Pixel DCS system, based on [1].

MOPS and the Serial Powering Chain

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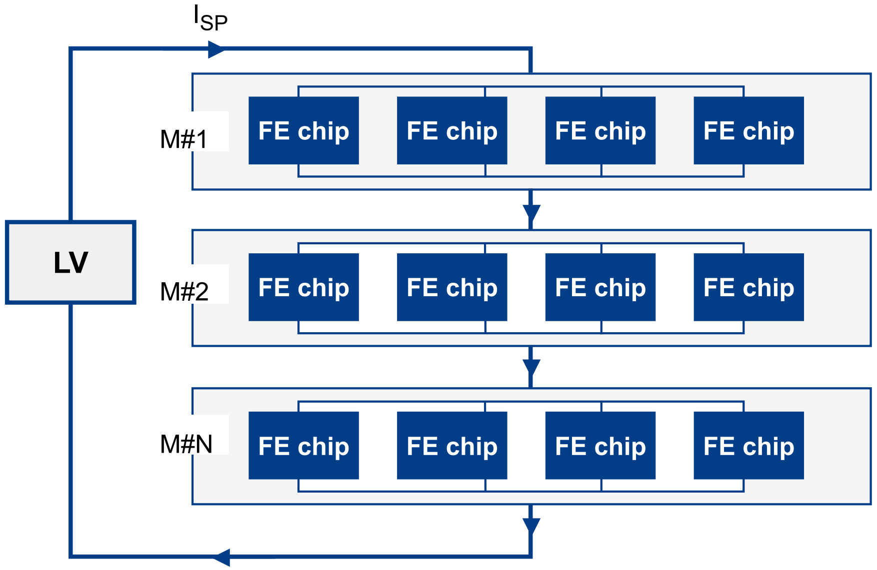
The Serial Powering Scheme:

- All the modules are powered in series.
- The FEs on a single module are powered in parallel.
- Up to 13 modules per SP chain.
- One Monitoring Of Pixel System (MOPS)/ SP chain.



The New Monitoring Of Pixel System (MOPS):

- Feedback per detector module is managed by an on-detector chip, known as the **MOPS** [3, 4].
- Monitors the temperatures and voltages of individual modules in the SP chain.
- High reliability across all operational phases (commissioning, calibration, and data-taking).
- Active even when the detector is idle.

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The Need for a Scalable Solution for MOPS

1. **Powering Scheme:**
   - Voltage supply (1.4 V to 2 V).
   - Independent of the Serial Powering chains and the Opto-System.
2. **Monitoring Scheme:**
   - Real-time data aggregation for $\approx$ 1200 MOPS.
   - Refresh rate ≈ 5 s.
   - Control is provided via the DCS computer ($\approx$140 m of cabling).
3. **Communication Scheme:**
   - **840 CAN buses** for all on-detector components ($\leq$2 MOPS per CAN bus).
   - **64 CAN buses** for the Opto-System ($\leq$4 MOPS per CAN bus).

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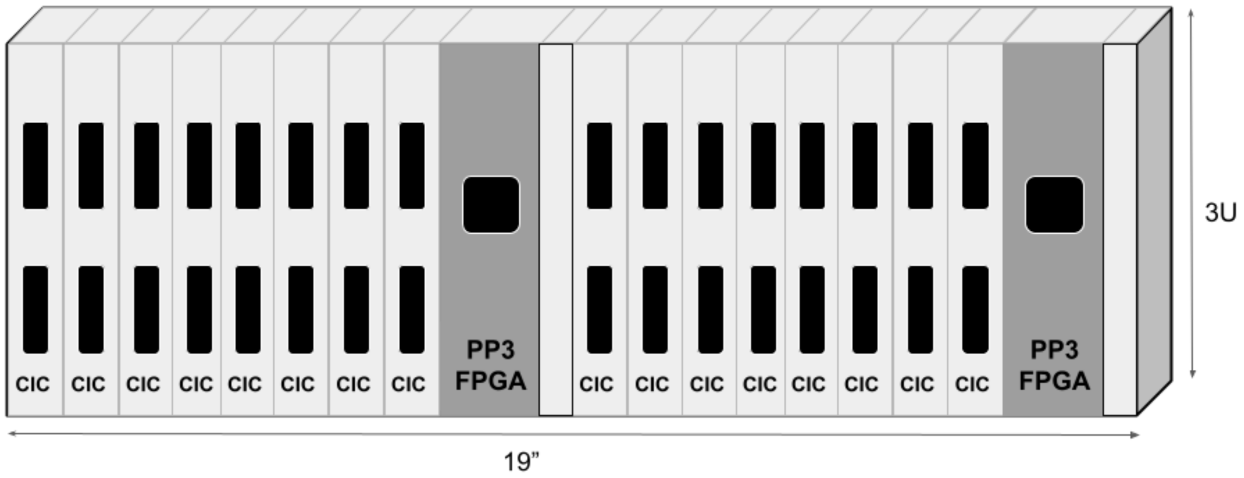
The Integration Solution of the MOPS Chip

MOPS-Hub

An FPGA-based interface designed to aggregate monitoring data between the MOPS chips and the DCS computers.

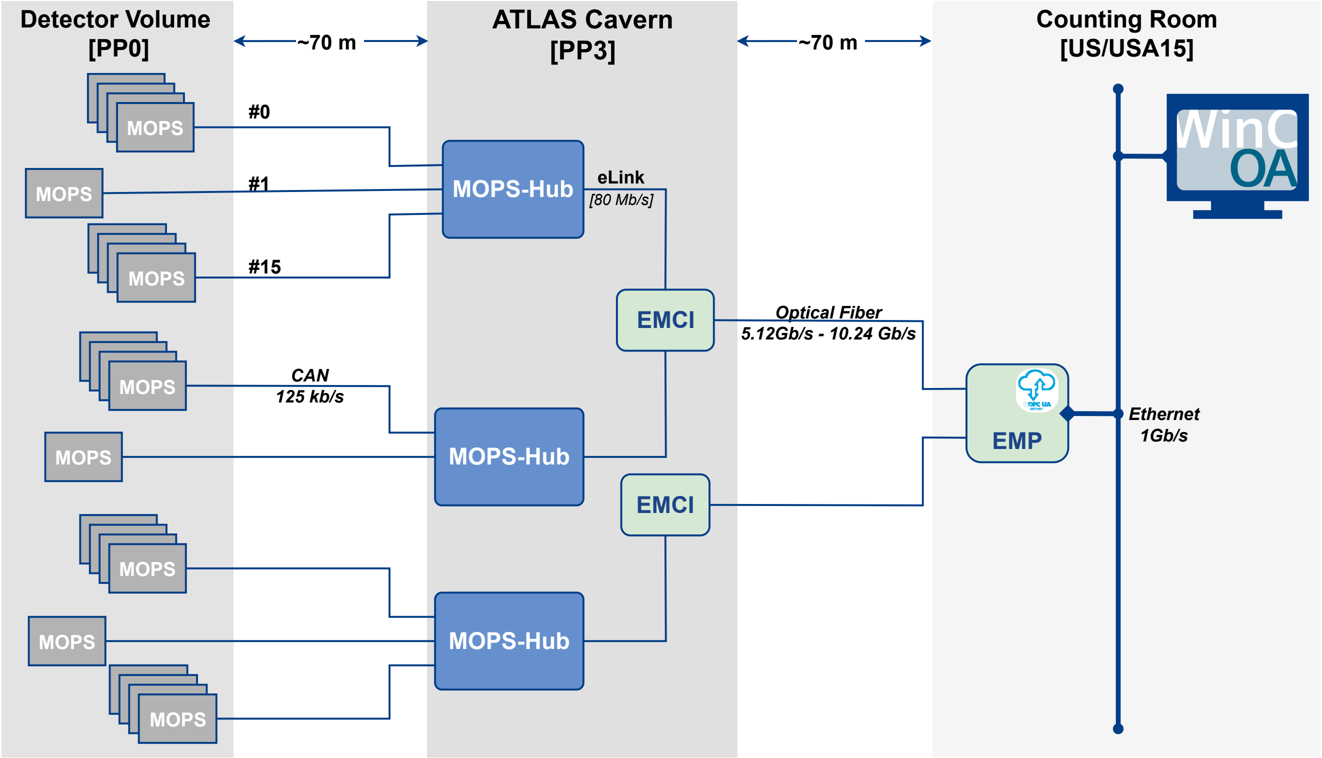


The MOPS-Hub Crate [front view].

Location : On the walls of the ATLAS Cavern, a connection area called **Patch Panel 3 (PP3)**.

- **Power distribution**: on PP3-Power module.
- **The CAN interface**: in a hardware called CAN Interface Card (CIC).
- **The CAN protocol**: in the FPGA firmware, called PP3-FPGA.
- All hardware components are housed in what is called the MOPS-Hub crate.

Design and Architecture of the MOPS-Hub

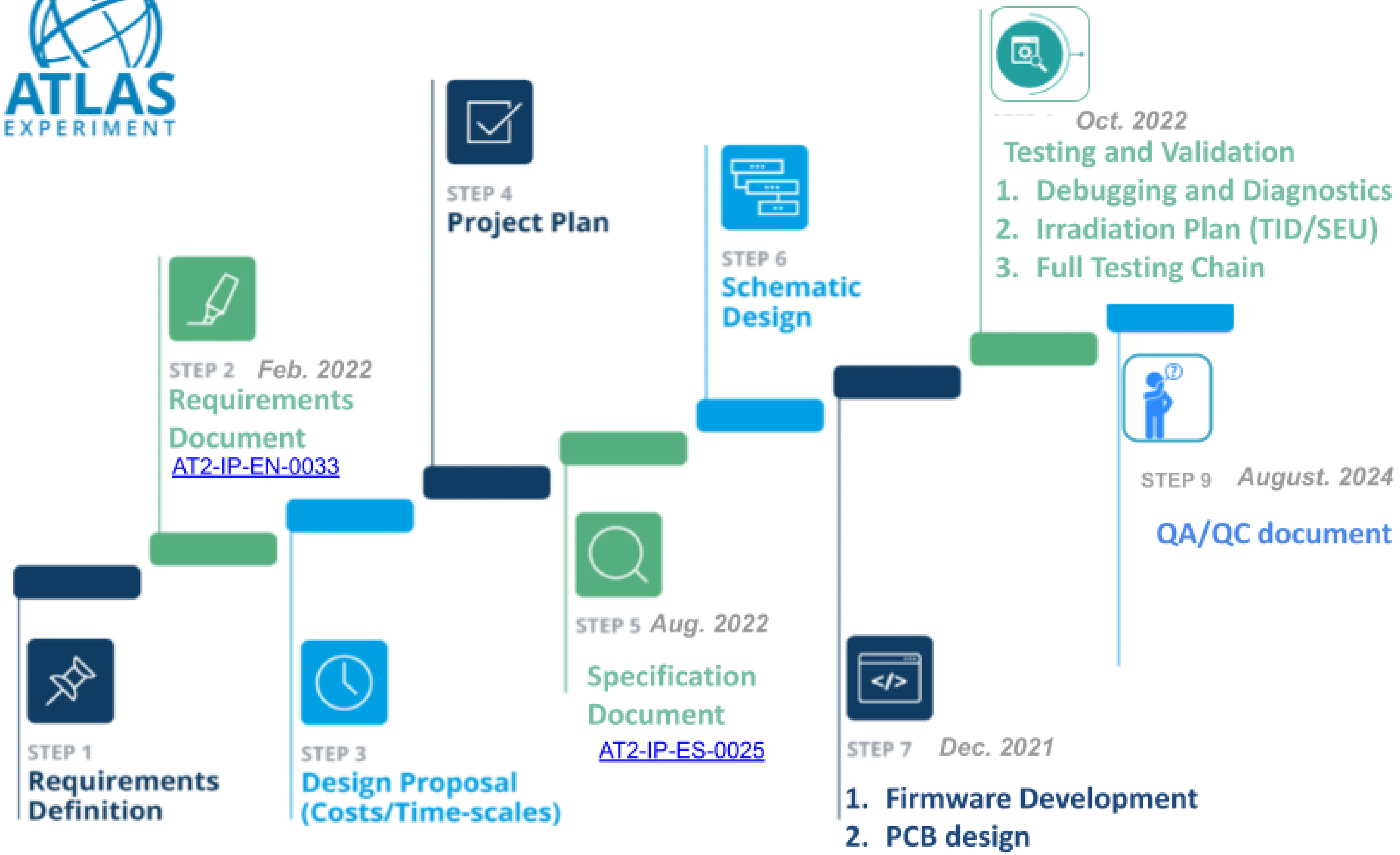


The complete MOPS-Hub network.

- ATLAS standard components:
  - Embedded Monitoring and Control Interface (EMCI) (with lpGBT as a core omponent).
  - Embedded Monitoring Processor (EMP).

My PhD Life Cycle

ATLAS EXPERIMENT

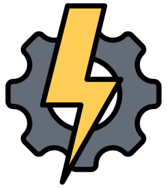


MOPS-Hub From Concept to Reality

MOPS-Hub Requirements

- The MOPS-Hub lives at **PP3** – on the walls of the ATLAS cavern (not a friendly environment!).

1. **Electrical:**
   - Must be **isolated** from the detector ground
   - Must tolerate voltage drops over 70 m of cabling
   - Operates at only 1.4 V to 2 V
2. **Magnetic Field:**
   - Exposed to ≈100 mT from the ATLAS solenoid
   - Standard components may simply **fail**
3. **Communication:**
   - **CAN buses:** non-standard 1.2 V physical layer
   - **eLinks:** low-voltage differential lines to EMCI
   - **SPI:** board monitoring and power control
4. **Radiation:**
   - Total Ionizing Dose (TID) up to ≈90 Gy (with safety factor)
   - Neutron fluence up to $9 \times 10^{11}\ \mathrm{N_{eq}/cm^2}$
   - Hadron fluence up to $6 \times 10^{-7}\ \mathrm{cm^{-2}/pp}$
   - Every component must be **radiation tolerant**



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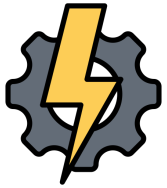

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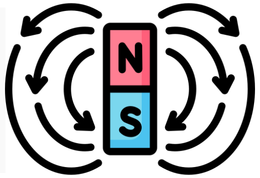

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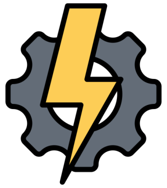

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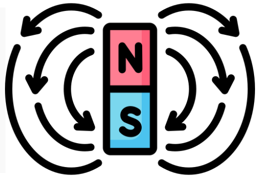

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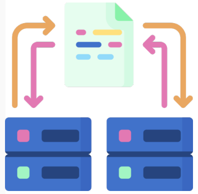

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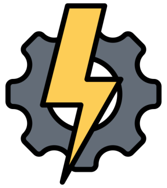

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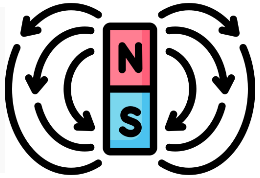

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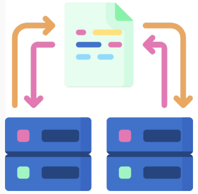

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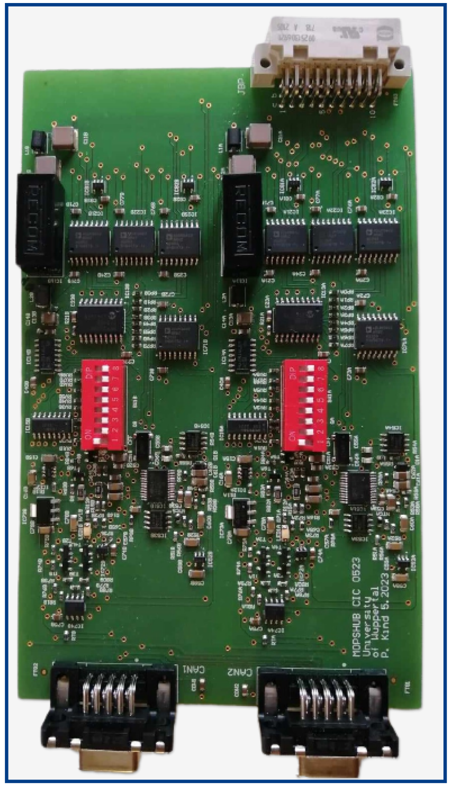
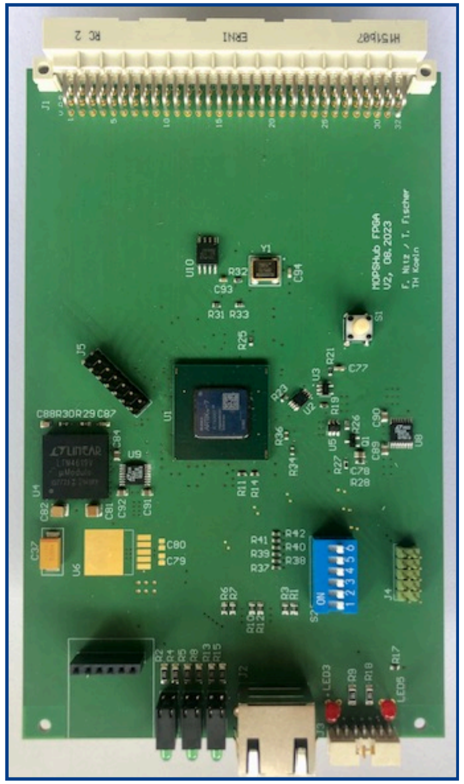
MOPS-Hub Hardware Components

PP3 Power Module
v1



CAN Interface Card
v4



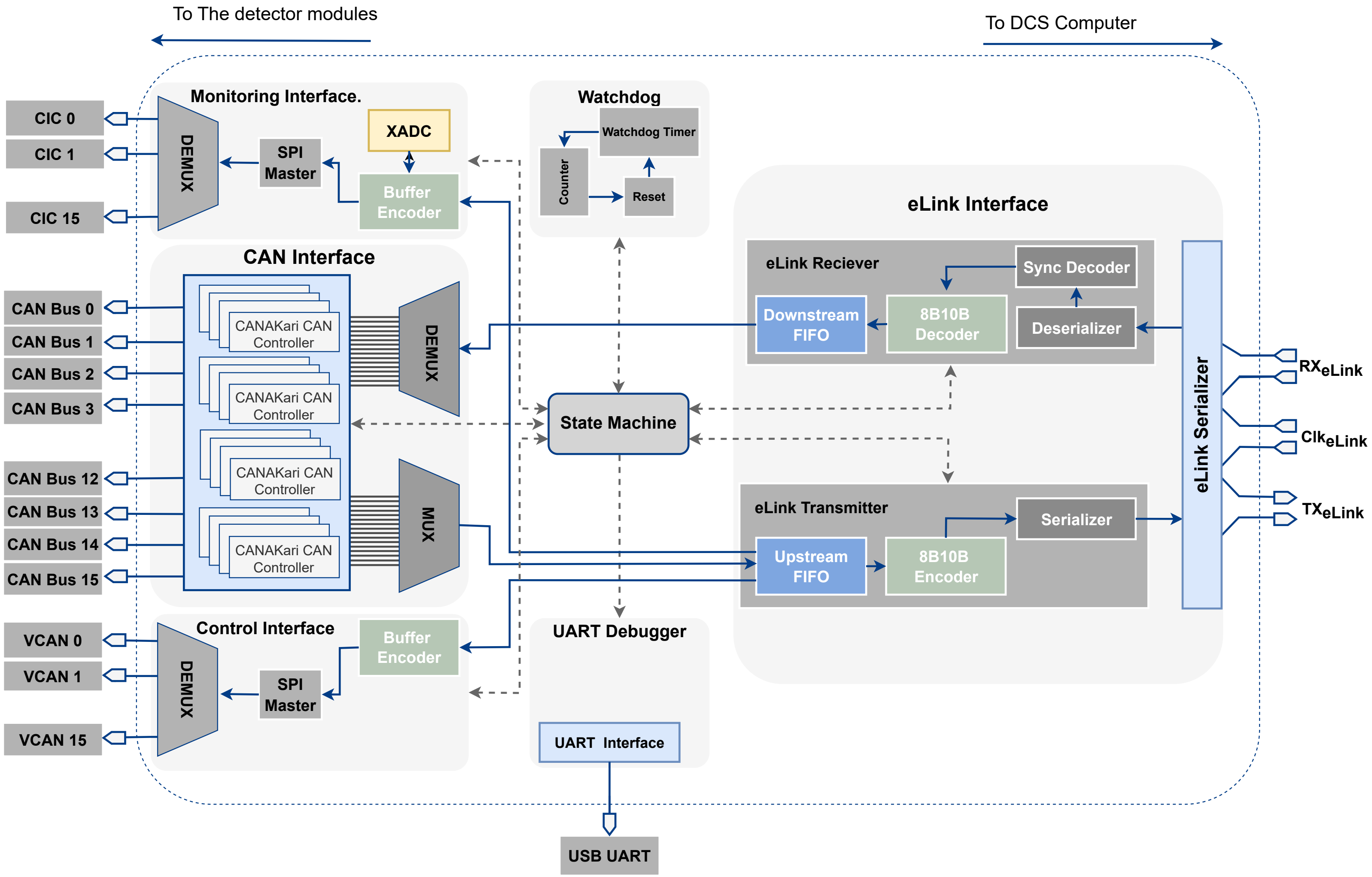
PP3-FPGA Board
v3

The MOPS-Hub hardware components.

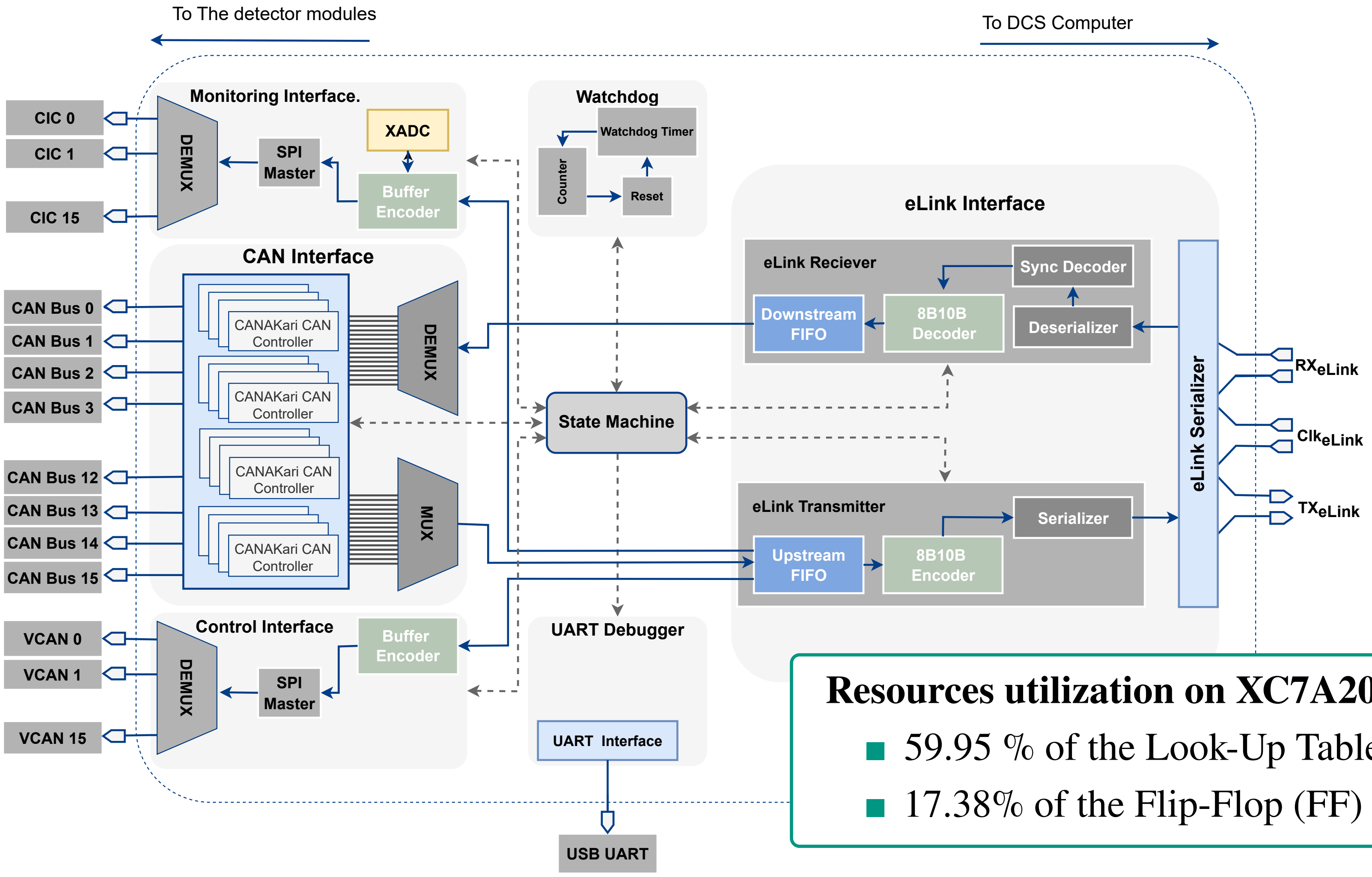
- **Credit for the hardware development goes to**: Group members from the University of Wuppertal and Cologne University of Applied Sciences.

Firmware Description and Verification

MOPS-Hub Firmware Architecture



MOPS-Hub Firmware Architecture



Resources utilization on XC7A200T FPGA:

- 59.95 % of the Look-Up Tables (LUTs).
- 17.38% of the Flip-Flop (FF)

SEU Mitigation Strategies in the Design

Strategy 1: State Machine and Logic
- **Mitigation Technique:** Watchdog

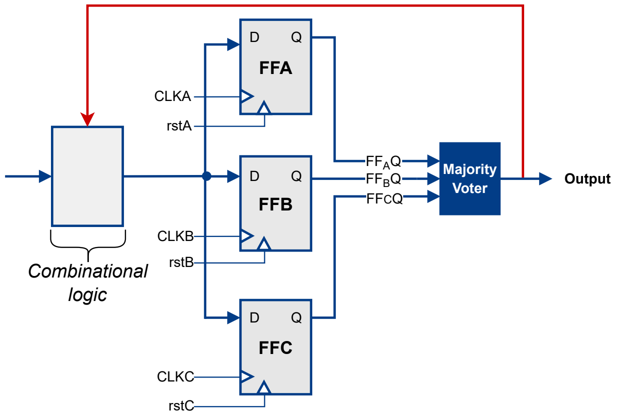
Strategy 2: Fabric logic elements
- **Mitigation Technique**: TMR

Strategy 3: Configuration Memory **[**Up to 2-bits upset**]**
- **Mitigation Technique**: Soft Error Mitigation (SEM) tool from Xilinx [ECC/CRC detection]

Strategy 4: Configuration Memory **[**Multi-bit upset**]**
- **Mitigation Technique**: Multi-boot Auto Reconfiguration.

Radiation hardening strategies for the PP3-FPGA.

- Partial Triple Modular Redundancy (TMR):
  - Only FFs.
  - By group members from FH Dortmund.
- The board utilizes an external Watchdog, controlled from the firmware.



Partial TMR.

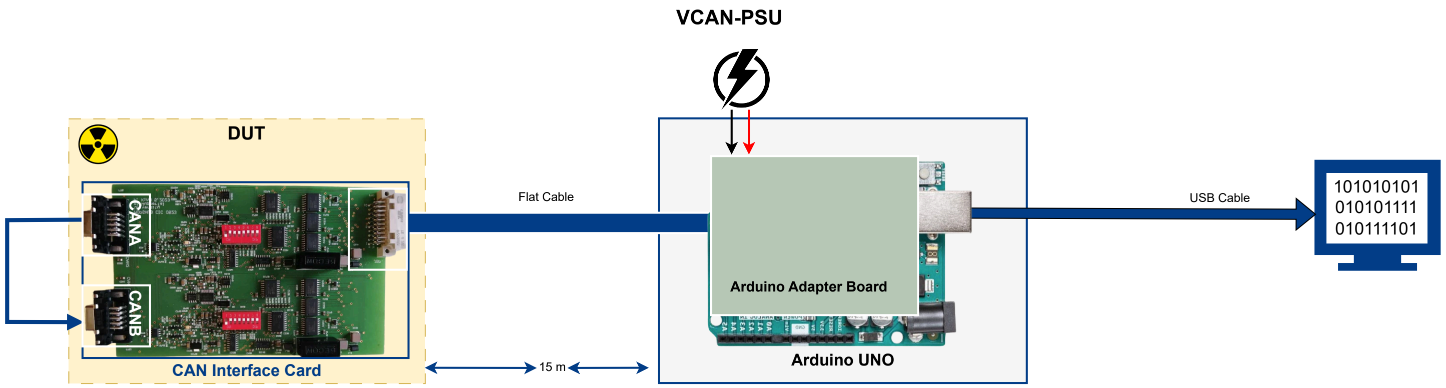
Hardware Testing and Validation

Testing Framework for Hardware Modules

Test Procedure:

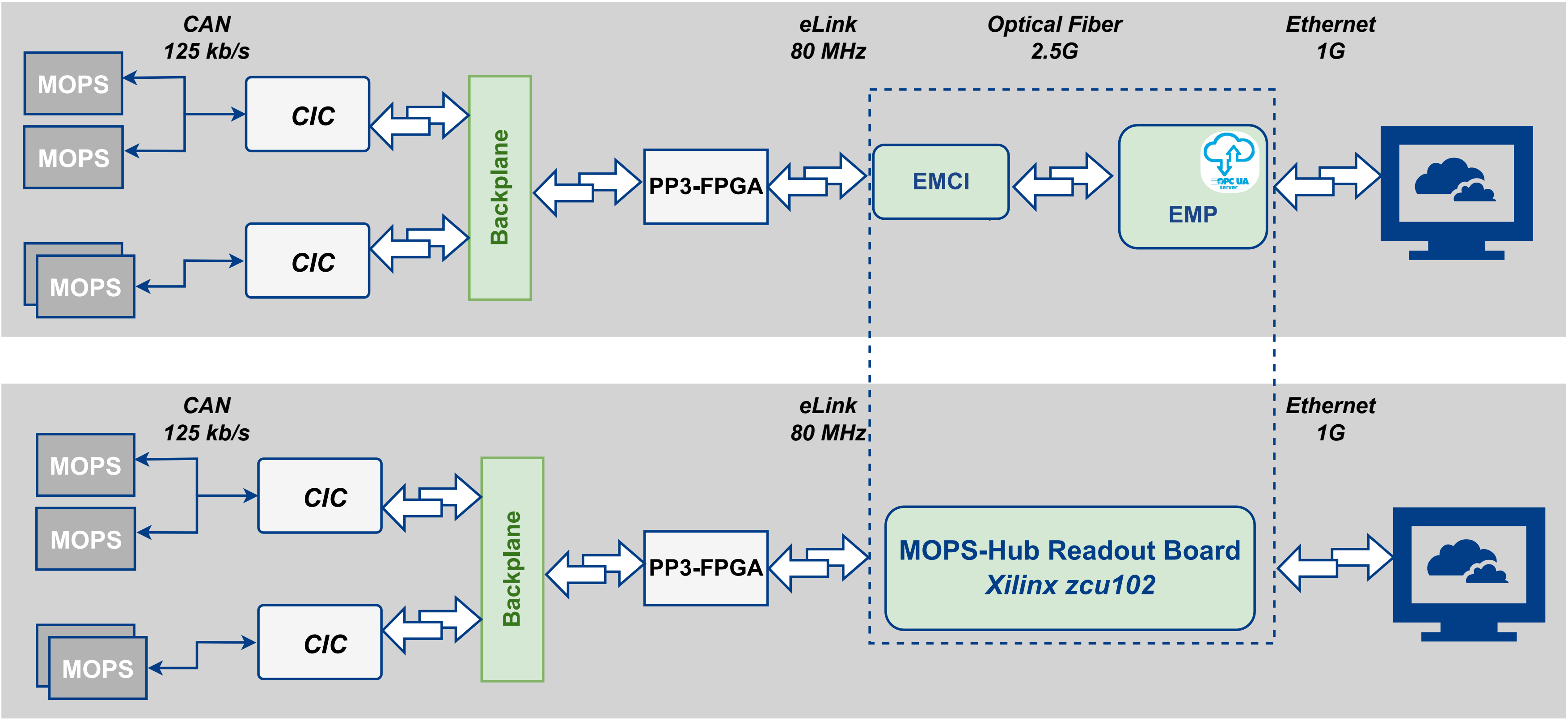
- Arduino-based setup to test each module.
- Targeted key parameters:
  - **PP3-Power module**: Input vs. output voltages and total current consumption.
  - **CAN Interface Card (CIC)**: CAN bus voltages, power consumption and internal parameters.
- System Automation: using a Python script running on a PC.
- Data was collected continuously over an extended period and saved for post-test analysis.

An Example of a Test Setup:



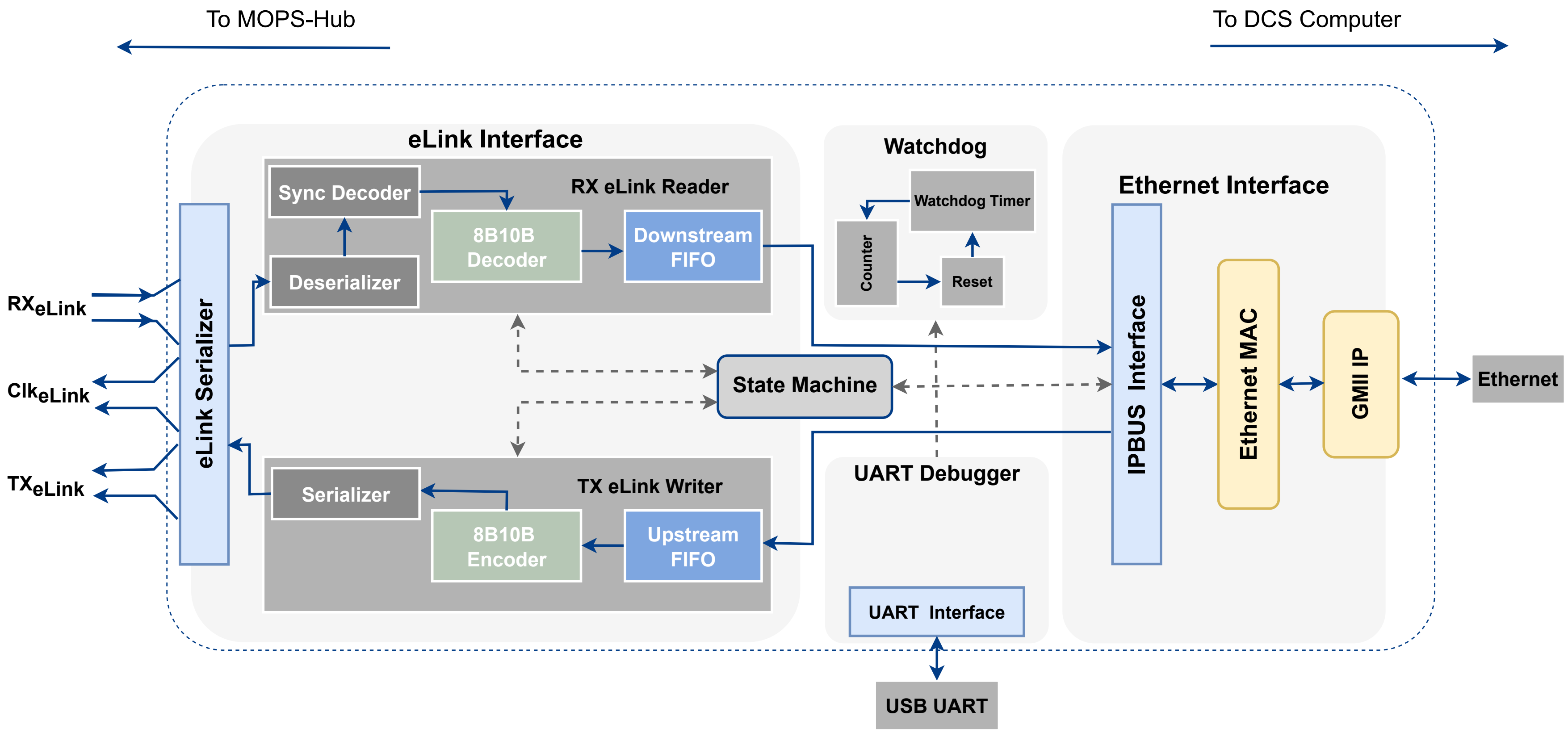
Example of the test setup designed to evaluate the CIC under controlled conditions.

Testing Framework for the Full System



Core component: MOPS-Hub Readout Board (Zynq UltraScale+ Evaluation Kit).

MOPS-Hub Readout board Firmware Architecture



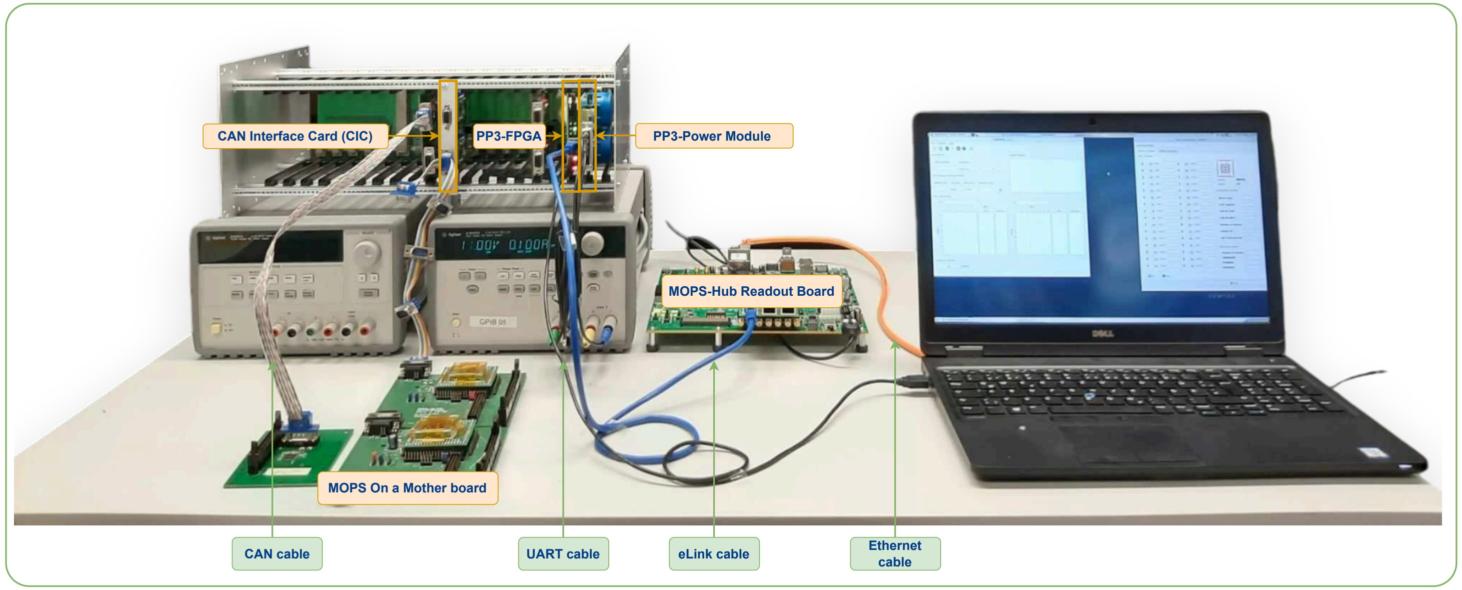
Firmware design of the MOPS-Hub Readout board.

- Employs the IPBus interface for address-based read and write communication via Ethernet.
- Python-based software for managing operations between the board and the local computer.

Lab Testing System [Set-Up]

Table: Summary of the MOPS-Hub performance test.

Parameter	Results
Requested CAN Messages	550,407 messages
Responded CAN Messages	550,407 messages
Failed Messages	0 messages
Test Duration	72 hours
Number of CICs	3
Activated Buses	3
Connected MOPS per Bus	2



Lab test setup for MOPS-Hub.

Irradiation Tests

Total Ionizing Dose (TID) Campaigns

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Facility: GIF++ at CERN [^{137}Cs gamma source, dose rate of $\approx 2\,\mathrm{Gy/h}$].

Table: Detailed information about the TID campaigns for the MOPS-Hub hardware components at GIF++.

Item	CIC	PP3-Power module	PP3-FPGA module
Test Date	May 2024	March 2023	May 2024
Focus of Interest	Electrical parameters	Physical layer Electrical parameters	Electrical parameters Temperature
Total Exposure Time	84 hours	72 hours	84 hours
Radiation Level	$168\,\mathrm{Gy}$	$91\,\mathrm{Gy}$	$168\,\mathrm{Gy}$
Test Set Up	Arduino Based	Arduino Based	Tester-based

- The PP3-FPGA and the CIC: tested by group members from Cologne University of Applied Sciences.

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Neutron Campaign

Facility: TRIGA neutron reactor at JSI, Ljubljana (Supported by the EURO-LABs program.).

Table: Information about the neutron irradiation campaign for the MOPS-Hub components.

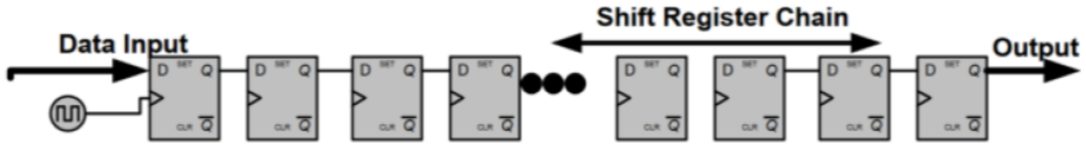
Item	**Details**
Test Date	June 2024
Facility	TRIGA neutron reactor at JSI
Total Exposure Duration	0.6 hours
Neutron Fluence	$10^{12}\,\text{n}/\text{cm}^2 \pm 10\%$

- A long-term test was conducted to all the boards before and after the Neutron irradiation (No misbehavior was observed).

Proton Campaign

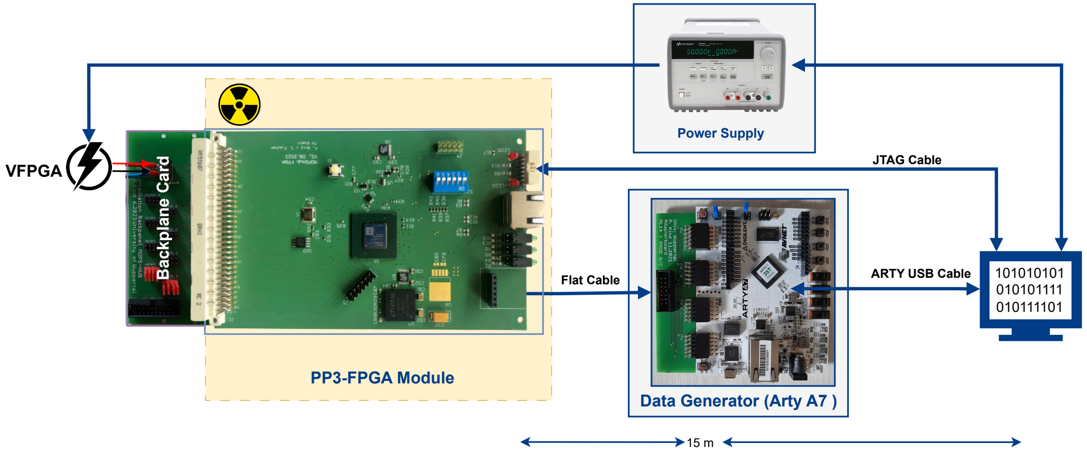
SEU Estimation Plan

- A 3000-bit shift register in the firmware for Single Event Upset (SEU)s estimation.



- An ARTY board is used as control unit (data aggregation, and comparisons) @ 1 MHz.
- Data was shifted with a hold time of 1 s.
- Data mismatches were reported as SEUs.

Test Setup:



Schematics for the test setup during proton beam testing at HIT.

Proton Campaign

SEU Estimation Plan

Facility: Heidelberg Ion Beam Therapy Center (HIT)
[Energy range = 48 MeV to 221 MeV, Beam intensity = up to 3.2×10^9 protons/s].

Table: Detailed information about the proton irradiation campaign for the PP3-FPGA module at HIT.

Item	Details
Test date	August 2024
Facility	Proton beam facility at HIT
Focus of interest	CRAM behavior and SEU estimation
Total test duration	4 hours
Accumulated proton fluence	7.5×10^{12} protons/cm^2

Test Procedure:

- Two scenarios were considered:
  1. External Watchdog enabled for Multi-boot Auto Reconfiguration (mBAR) functionality checks.
  2. External Watchdog disabled to estimate SEUs in CRAM.
- Supply current was monitored to avoid Single Event LatchUp (SEL).

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Proton Campaign

Campaign Results

CRAM Behavior (Watchdog: Enabled):

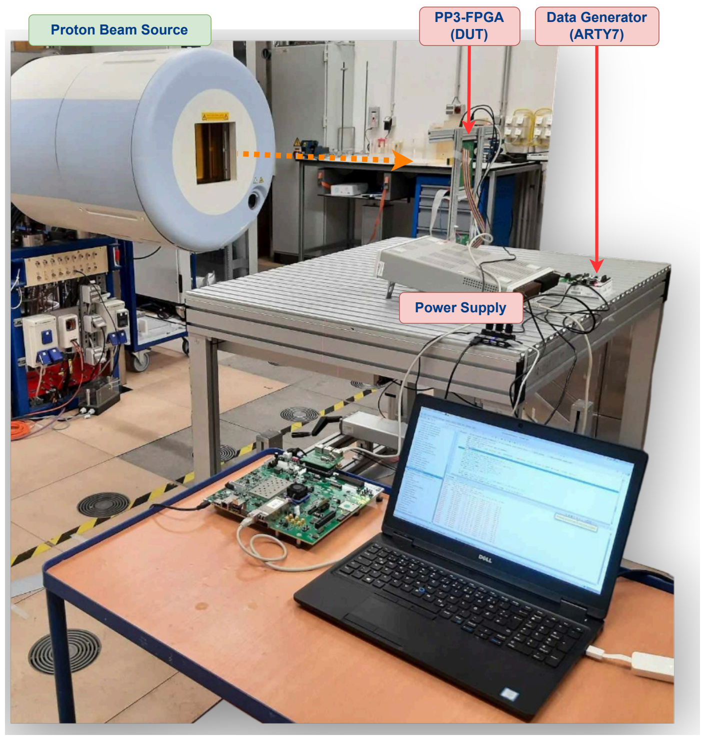
- SEM IP from Xilinx is able to correct up to two upsets/frame (Multi-bit upsets/frame $\rightarrow$ uncorrectable).
- Accumulation of multi-bit upsets $\rightarrow$ Global clock corruption $\rightarrow$ System failure.

Solution: Multi-boot Auto Reconfiguration (mBAR)

SEU Estimation (Watchdog: Disabled):

- σ_{SEU} is of order 10^{-15} cm^2/bit (Compatible with Xilinx results for XC7A200T-FPGA)
- The SEUs rate in 10 years of the LHC at PP3 (ϕ *is the fluence* $=2 \times 10^{-7}$ cm^2/pp):

$$\text{N}_{\text{SEU}} \approx 25{,}349 \text{ SEUs}$$



Test setup during proton beam testing at HIT.

$$\sigma_{\text{SEU}}(\text{bit}) = \frac{\sigma_{\text{SEU}}(\text{device})}{\text{N}_{\text{bits}}} = \frac{\text{N}_{\text{SEU}}}{\phi \times \text{N}_{\text{bits}}} \quad [\text{cm}^2/\text{bit}]$$

MOPS-Hub in Production (2024)

- Four MOPS-Hub crates were in the pre-production stage.
  - **Objective**: readout operations for multiple MOPS chips integrated into large detector structures.
- A few MOPS-Hub crates were in production.

(a) Front View

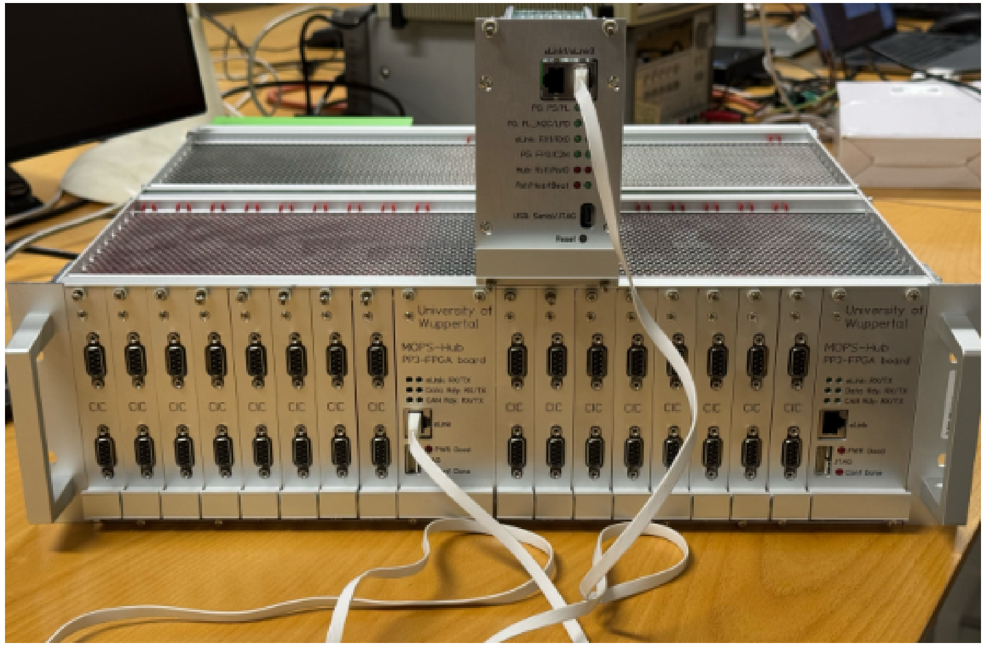
(b) Back view.

First assembled MOPS-Hub crate for Pre-production (October 2024). Taken by: Matías Henríquez

Credit goes to: Group members from Instituto Milenio SAPHIR in Chile.

MOPS-Hub after 2 years (2026)

- MOPS-Hub Readout board is developed to the Intermediate Readout board (IRb) [Kria K26 SOM]
- Intermediate Readout board (IRb) has the capability to host an OPC UA server
- WinCC OA client construction ongoing



Recent assembled MOPS-Hub crate with IRb (2026).


Pre-production MOPS-Hub crates ready for shipment (Mar. 2026). Taken by: Felix Nitz

Section 3

My Postdoc Journey (2025 till Now)

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My Postdoc Journey...

What I Bring to IPE

- Make use of my solid foundation in **detector instrumentation, FPGA firmware, and hardware validation** in a real experiment.
- At IPE, I want to build on this – and go further.

My Postdoc Journey...

What I Bring to IPE

Karlsruhe Institute of Technology

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1. Calorimeter Commissioning and Operation

- Take an active role in the commissioning and operation of calorimeter systems at IPE.
- Connect instrumentation work to **real physics results**.

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2. Real-Time Machine Learning on FPGAs

- Deploy **ML inference on FPGA** hardware for real-time trigger and data acquisition.
- Build on my firmware background to explore **AI-powered online monitoring**.

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- Make use of my solid foundation in **detector instrumentation, FPGA firmware, and hardware validation** in a real experiment.
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- Take an active role in the commissioning and operation of calorimeter systems at IPE.
- Connect instrumentation work to **real physics results**.

2. Real-Time Machine Learning on FPGAs

- Deploy **ML inference on FPGA** hardware for real-time trigger and data acquisition.
- Build on my firmware background to explore **AI-powered online monitoring**.

3. Detector R&D for Future Experiments

- Contribute to next-generation detector technologies beyond the HL-LHC era.
- Focus on **radiation-hard FPGA co-design** for future high-granularity calorimeters.

My Postdoc Journey...

What I Bring to IPE

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“Civilization is the accumulation and transmission of knowledge from generation to generation.”
— Will Durant, *The Story of Civilization/Vol. 1: Our Oriental Heritage*

4. Knowledge Transfer and Community Building

- **Passing the Torch:** I believe science only grows when knowledge is shared, not guarded.
- **Mentorship:** Active interest in student supervision and open collaboration.

My Postdoc Journey...

Postdoc Progression Framework

Postdoc Progression Framework

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Integration

Stakeholder Alignment
Supervisor, team leaders, colleagues

Intra-Group Collaboration
within the HGCAL group at IPE

Intra-Institute Networking
(collaboration across the institute)

My Postdoc Journey...

Postdoc Progression Framework

Integration

Stakeholder Alignment
Supervisor, team leaders, colleagues

Intra-Group Collaboration
within the HGCAL group at IPE

Intra-Institute Networking
(collaboration across the institute)

Expansion

Inter-Institute Collaboration
KIT Institutes with similar Interests

National Research Collaboration
Outside KIT

Interdisciplinary Collaboration
(non-physics institutes at KIT)

Section 4

Summary

Summary

A Project that Grew into a Community

By walking you through my PhD journey, you see how my PhD project evolved from a concept into a real-world solution.

Technical Success

- A new FPGA-based system was developed during my PhD to upgrade the DCS for the ATLAS ITk Pixel detector as part of the HL-LHC upgrade.
- MOPS-Hub has transitioned to **pre-production and QC**, with setups now repurposed for detector integration.

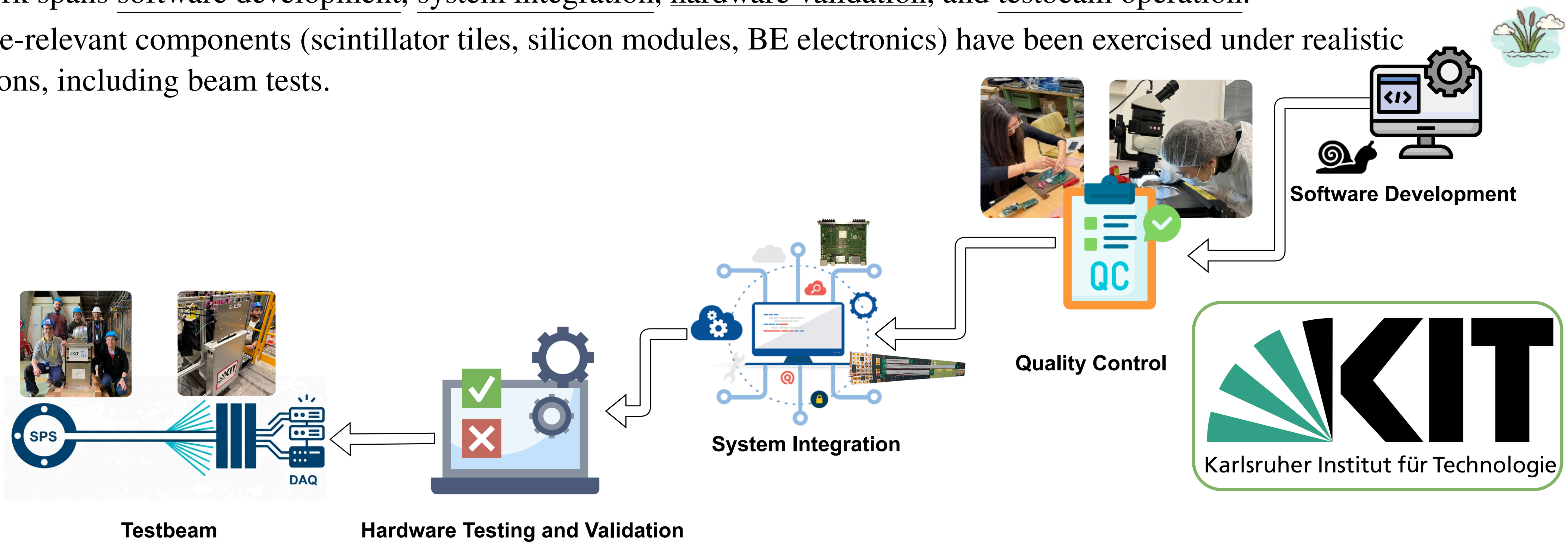
Academic Legacy

- **7+ Publications:** Detailed in JINST and presented at international conferences [5, 6, 7].
- **Student Growth:** Foundation for 4+ Theses (B.Sc./M.Sc.) at TH Köln and FH Dortmund [8, 9, 10, 11].
- It was rewarding to see the MOPS-Hub used as a teaching tool during 2026 edition Summer interships SAPHIR , Chile

Summary

A Community that will Grow a Project

- After a year of integration, I am fully ”up to speed” with the Calorimeter Group.
- We have built solid end-to-end experience with different Back-End (BE) systems (e.g. **Serenity** and **VCU118**).
- The work spans software development, system integration, hardware validation, and testbeam operation.
- Cassette-relevant components (scintillator tiles, silicon modules, BE electronics) have been exercised under realistic conditions, including beam tests.



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Discussion

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Section 5

Backup Slides

The ATLAS Inner Detector

The ID provides tracking information of charged particles in PP collisions.

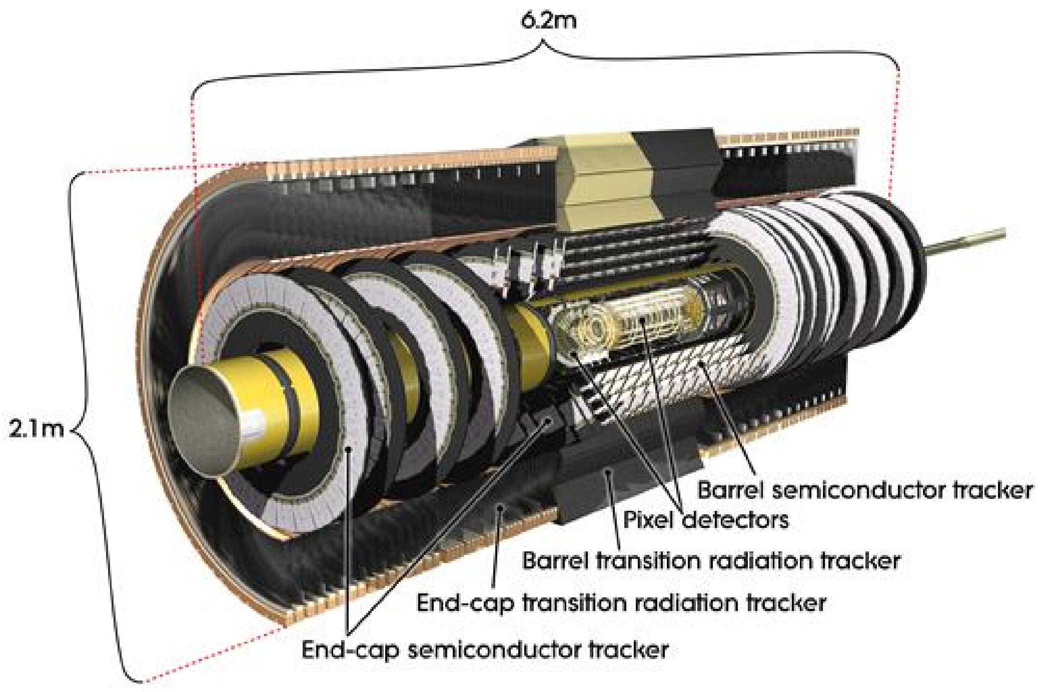
Purpose: Determining the trajectory, momentum and charge of the charged particles.

Components of the current ID:

1. The Pixel Detector
2. The Semiconductor Tracker (SCT)
3. The Transition Radiation Tracker (TRT)

Phase-II Shutdown Upgrades:

- The tracking system will be replaced by an all-silicon detector known as the **ITk** (Slide 7).
- The ITk consists of several layers of silicon Pixel detectors and Microstrips arranged around the beam pipe.



The current ATLAS Inner Detector [12].

Safety Path of the ITk DCS

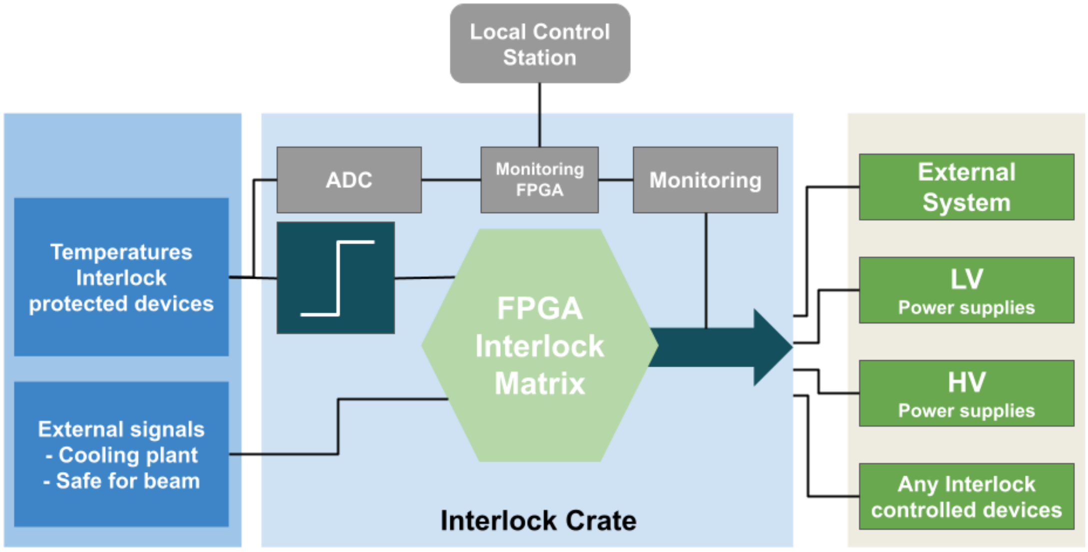
- Based on a robust interlock system.
- Protects interlock-controlled units (e.g., power supplies) from risks.
- Ensures the highest reliability and availability as the last line of defense for the ITk DCS.

Functionality:

- Collects signals from:
  - Temperature sensors of interlock-protected devices.
  - ATLAS-Detector Safety System (DSS) (e.g., cooling failures, humidity, smoke, global risks).
  - ATLAS-Beam Interface System (BIS) (e.g., dangerous beam conditions).
- Reacts to critical conditions with immediate actions to safeguard operations.

Key Components:

- Modular system housed in a Local Interlock & Safety System (LISSY) crate:
  - IO-modules for signal input/output.
  - Interlock FPGA (ILK-FPGA).
  - Monitoring FPGA.



Topology of the Interlock System [13].

Diagnostic Path of the ITk DCS

- Enhances detector performance through monitoring and debugging of Front-Ends (FEs).
- Operates at the level of individual FE chips.
- Allows for detailed calibration scans and tuning.

Key Components:

- **Opto-system:**
  - Converts FE electrical signals to optical signals via Opto-boards.
  - Transmits data to the off-detector Data Acquisition (DAQ) system.
- **Opto-box:**
  - Houses opto-electrical transceivers and ASICs for data handling [14].
- **Front-End Link eXchange (FELIX) Card:**
  - Aggregates the received optical signals, where it is separated and forwarded to DCS.

ITK Pixel Services and Patch Panels

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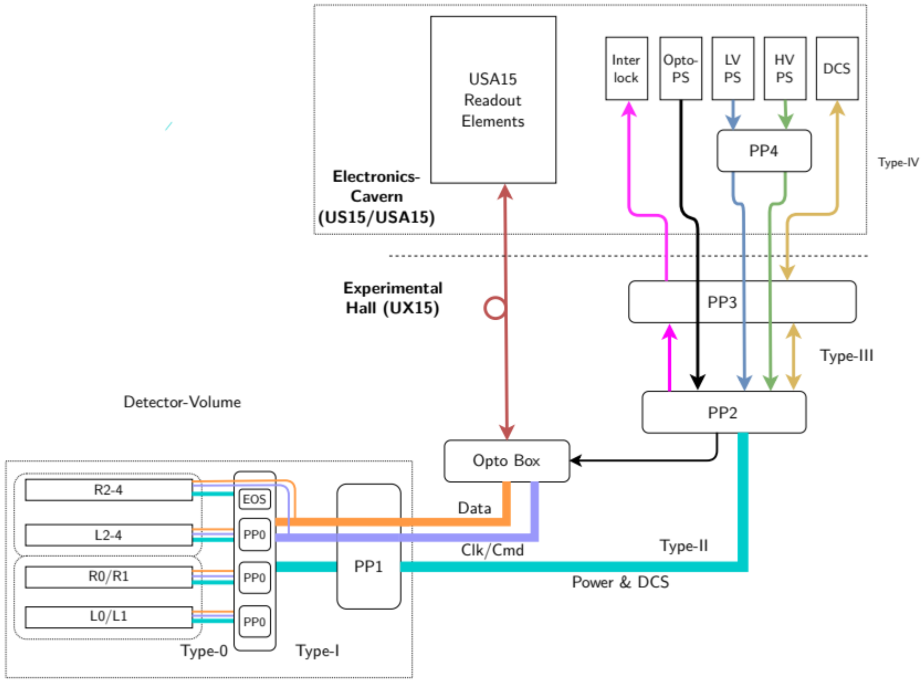
The ITk Patch Panels

- The ITk Pixel Services, including data, commands, monitoring, and power, are routed out of the detector volume via designated breakpoints called Patch Panels (PPs).
- The PPs serve as interfaces for different service connections.

Patch Panels in the ITk Power Chain:

- **PP0 (or EOS)**: Located at the detector volume.
- **PP1**: Located at the A and C sides of the primary Faraday Cage wall.
- **PP2**: Located inside the Muon spectrometer.
- **PP3**: Located inside the collider hall, on the walls of the ATLAS cavern.
- **PP4**: Located at the power supply racks in US15/USA15.



Overview of the ITk Pixel services [15].

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The New Monitoring Of Pixel System (MOPS)

Table: *Specifications of the MOPS chip.*

Parameter	Specification
Technology	65 nm technology
chip size	2×2 mm^2
Package size	9×9 mm^2 QFN package
Communication protocol	CAN and CANopen protocol
Chip powering	1.4 V to 2 V
Voltage monitoring precision	15 mV
Temperature monitoring precision	1 K
Radiation hardness	500 Mrad
Operational temperature	−40 °C to 60 °C

- The powering and communication for the MOPS are completely independent of the SP-chains or the Opto-System.
- Communication via 1.2V CAN-bus.
  - Standard CAN protocol with partial CANopen implementation.
  - Lower voltage due to constraints of the 65nm technology.
- Powering of the chips is provided from the outside (less than 2 V).
- MOPS V3 can detect the difference of the frequency of its own oscillator to the nominal value (Trimming feature).

Hardware Testing Results

CIC Tests:

- CAN voltage level .
- VCAN configurations and Noise measurements.
- DC/DC converter functionality.
- ADC monitoring channels.
- Magnetic field test.
- Irradiation tests (Slide 26 and 27).

Table: Characteristics of the CIC.

Parameter	Characteristics
CAN voltage level	1.2 V
VCAN levels	2.0 V to 4.8 V
Noise level (VCAN)	60 mV to 70 mV_{pp}
Magnetic field tolerance	$\approx$ 380 mT
TID level	91Gy$\pm$15%
Neutron fluence level (Φ^{Si}_{eq})	10×10^{12} N_{eq}/cm^2

PP3-Power Module Tests:

- DC/DC converter functionality.
- Start Up behavior.
- Magnetic field test.
- Irradiation tests (Slide 26 and 27).

Table: Characteristics of the PP3-Power Module.

Parameter	Characteristics
Input voltage VPP3	6 V to 40 V
Output voltage V_{FPGA}	5 V
Noise level (V_{FPGA})	$\approx$ 155 mV to 170 mV_{pp}
Magnetic field tolerance	$\approx$ 380 mT
TID level	168Gy$\pm$15%
Neutron fluence level (Φ^{Si}_{eq})	10×10^{12} N_{eq}/cm^2

Proton Campaign Results

■ CRAM Behavior

Table: Run details summary for the proton irradiation at HIT (watchdog enabled).

Run	**Energy** [MeV]	**FWHM** [mm]	**Intensity** [protons/s]	**Duration** [min]	**Fluence** [protons/cm^2]	**Rest rate** [resets/s]
1	48.2	66	3.2×10^9	23	4.42×10^{12}	1
2	102.61	66	3.2×10^9	10	1.92×10^{12}	2
3	145.46	23	3.2×10^9	5	9.60×10^{11}	1
4	145.46	23	8.0×10^7	12	5.76×10^{10}	1

■ SEU Estimation

Table: Run details summary for the proton irradiation at HIT (watchdog disabled).

Run	Energy [MeV]	FWHM [mm]	Intensity [protons/s]	Duration [min]	Fluence [protons/cm^2]	SEUs [N]	σ [cm^2/bit]
7	145.46	11.5	8×10^8	37	8×10^{11}	7	2.92×10^{-15}
8	155.82	10.8	8×10^8	39	8×10^{11}	9	3.75×10^{-15}
9	165.89	10.2	8×10^8	17	4×10^{11}	4	3.33×10^{-15}

- The results align with other measurements reported by Xilinx for the Artix-7 family.
- The estimated rate of SEUs in the Configuration Memory (CRAM) of the **XC7A200T-FPGA**[1] at PP3 $\approx$ 25349 SEUs.

$$\mathrm{N_{SEU}} = 3.75\times10^{-15}\,[\mathrm{cm}^2/\mathrm{bit}]\times 2\times10^{-7}\,[/\mathrm{cm}^2/\mathrm{pp}] \times 40\times10^6\,[\mathrm{pp/s}]\times 200\,[\mathrm{Collisions}] \times 3.14\times10^7\,[\mathrm{s}]\times 10\,[\mathrm{years}]\times 13\,455\,360\,[\mathrm{bits}]$$

[1]Total RAM Bits in XC7A200T-FPGA = 13455360 bits

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Glossary

CAN Controller Area Network

CERN Conseil Européen pour la Recherche Nucléaire: European Organisation for Nuclear Research

CIC CAN Interface Card

DCS Detector Control System

EMCI Embedded Monitoring and Control Interface

EMP Embedded Monitoring Processor

FPGA Field Programmable Gate Array

HL-LHC High Luminosity LHC

LHC Large Hadron Collider

mBAR Multi-boot Auto Reconfiguration

MOPS Monitoring Of Pixel System

PP0 Patch Panel 0

PP1 Patch Panel 1

PP2 Patch Panel 2

PP3 Patch Panel 3

PP4 Patch Panel 4

SEL Single Event LatchUp

SEU Single Event Upset

TID Total Ionizing Dose