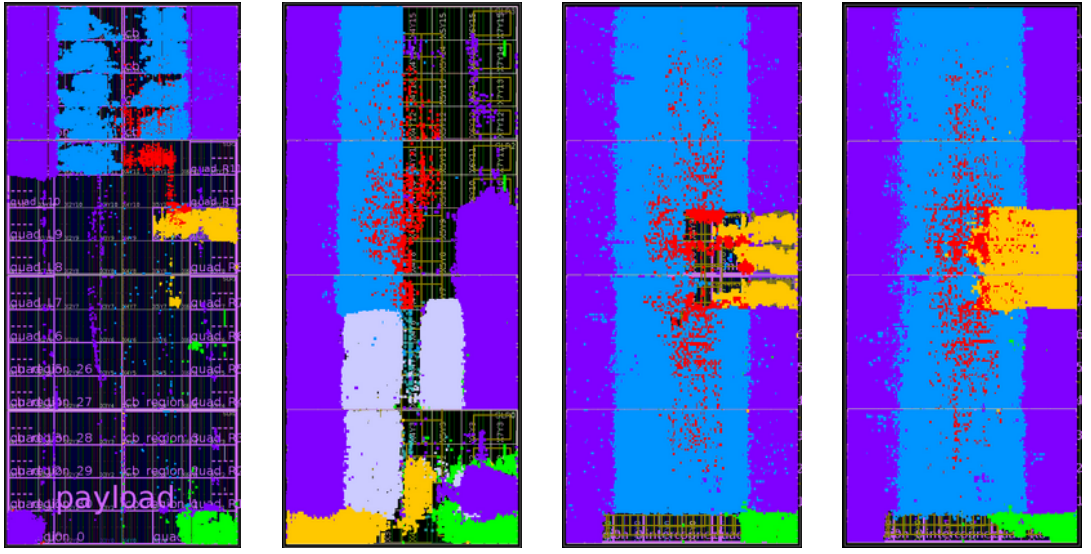
Modular multi-TB/s readout for the CMS HGCAL Data Acquisition System

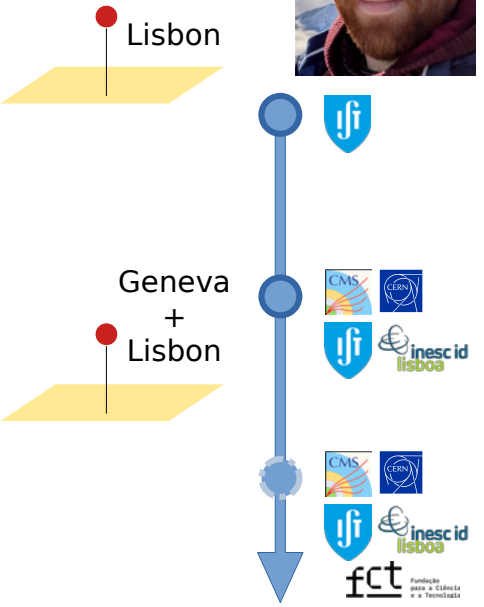


Seminar @ KIT/IPE
17th September 2026

Martim Rosado

About me

- BSc in Electrical and Computer Engineering (2020)
- Joined CMS in 2021 working on the HGCAL for MSc thesis
- MSc in Electrical and Computer Engineering (2022)
- Started PhD (ECE) in 2023 on the HGCAL DAQ system
- Graduation expected Q1 2027



Besides digital electronics design, I’m also interested in:

- Analogue and mixed signal electronics
- High-performance computing

Outline

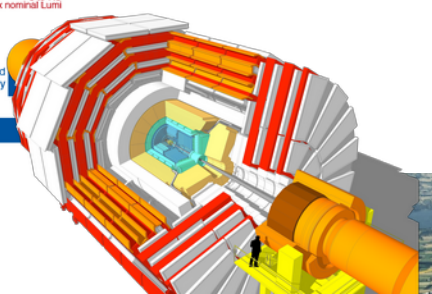
- **When, why, and where to HGCAL?**
- What readout for the HGCAL DAQ?
- Present-day Challenges
- Conclusions

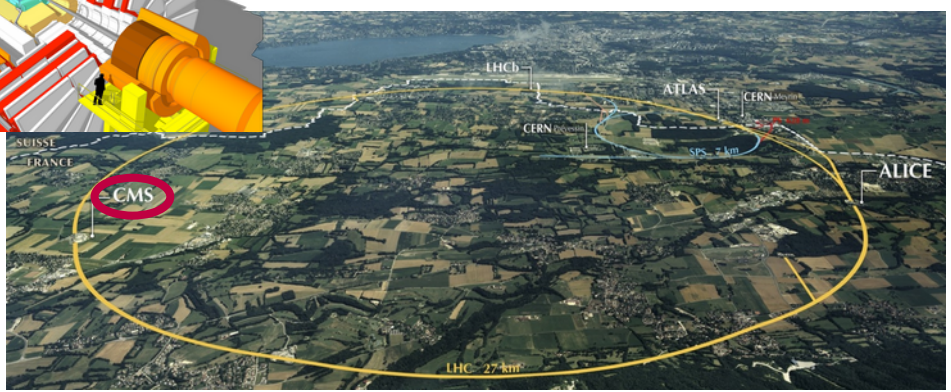
The LHC is over, the next run is High-Lumi!

The High Luminosity LHC upgrade will deliver more collisions to the detectors:

- Pileup will increase 40 → 140-200
- More pileup requires more granularity
- More granularity → more data

You are here!



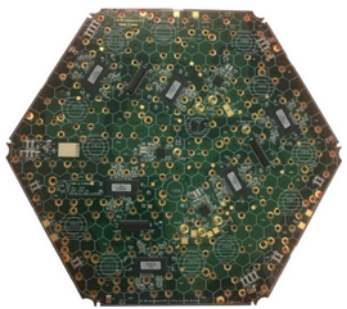


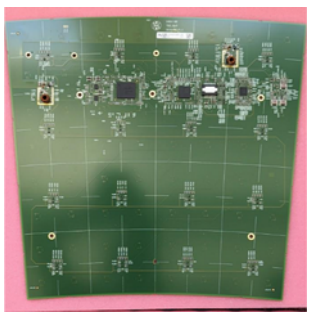
CMS will replace its endcap calorimeters as part of an extensive detector upgrade to cope with the HL-LHC operating conditions.

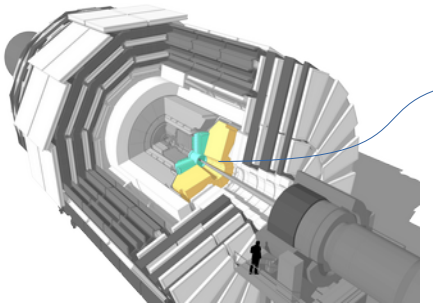
LHC schedule, LHC aerial view, and CMS figure

New endcap calorimeters for CMS

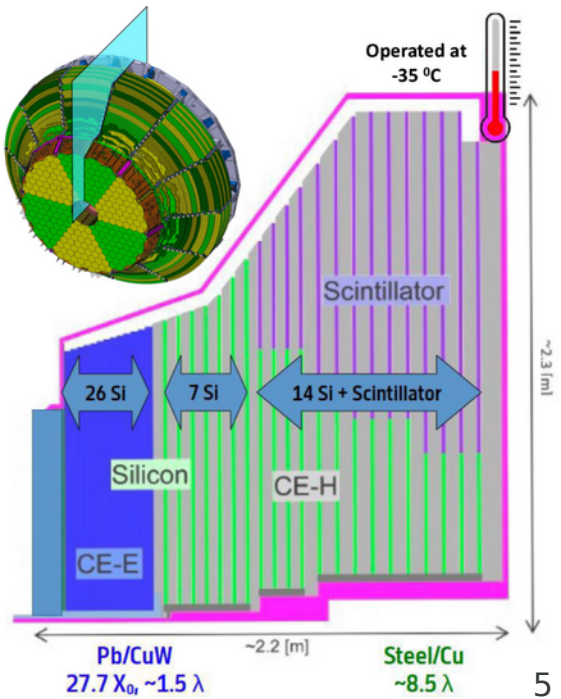
The new High-Granularity Calorimeter (HGCAL) will replace the current CMS endcap calorimeters, increasing the sensitive channels from ~170 k to 6 million, providing unprecedented high resolution measurements of position, energy, and timing.







The CMS endcap calorimeters



Two sensor technologies are used to deliver the required performance while being cost effective.

Hexaboard, Tileboard, CMS figure, and HGCAL figure

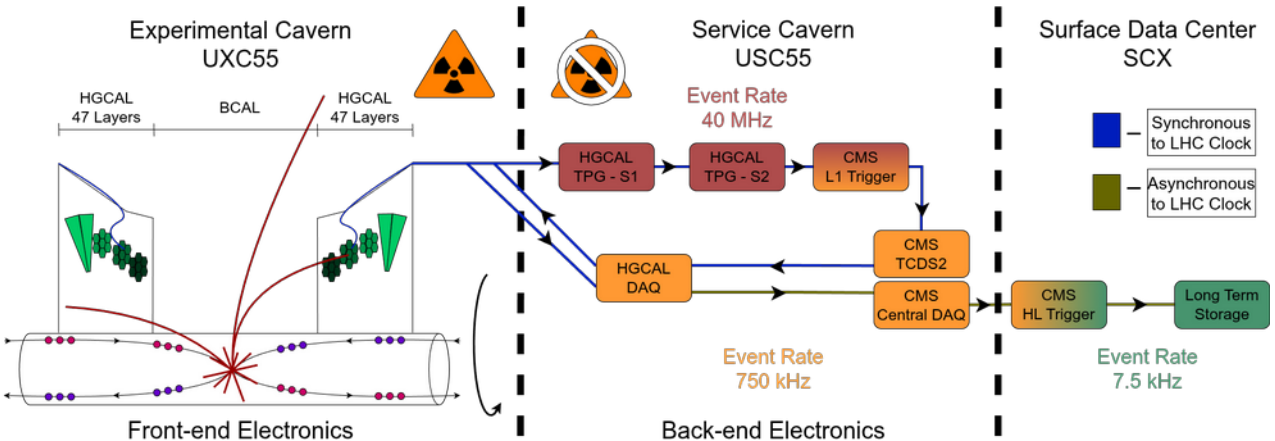
The HGCAL electronics have four paths

The HGCAL electronics sub-divide into:

- **Front-end electronics (FE)**
  Custom radiation-tolerant ASICs, residing in the experimental cavern.
- **Back-end electronics (BE)**
  302 **Serenity** boards, residing in the service cavern.

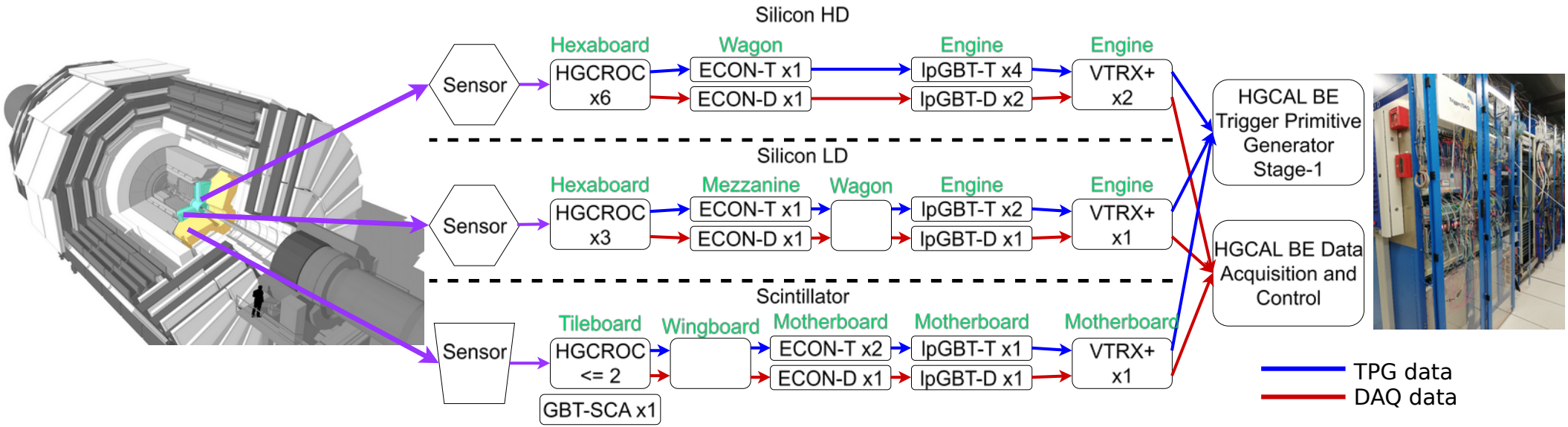
Four main functionalities
needed by FE and BE:

- Collisions are filtered (Trigger)
- Data are stored (DAQ)
- Configuration (Async)
- Clock and Control (Sync)

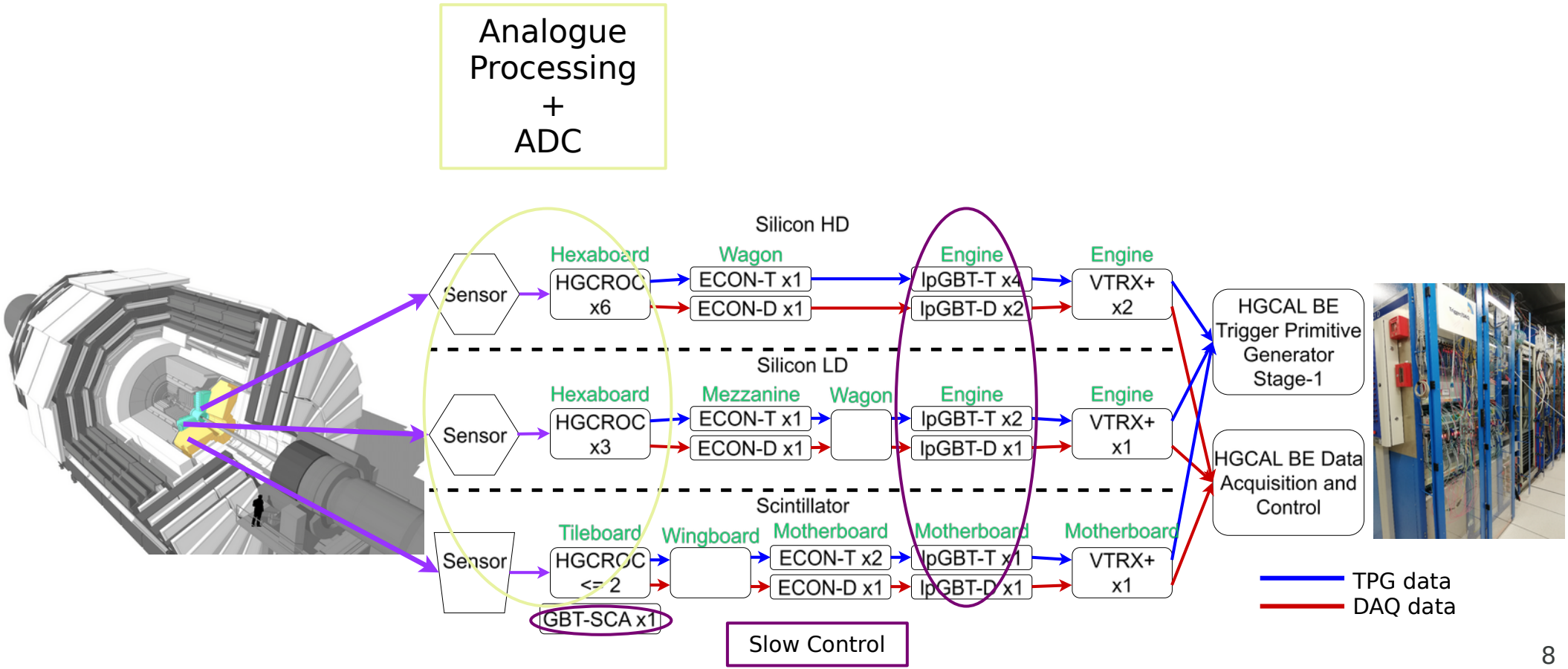


Three FE flavours, two uplink paths

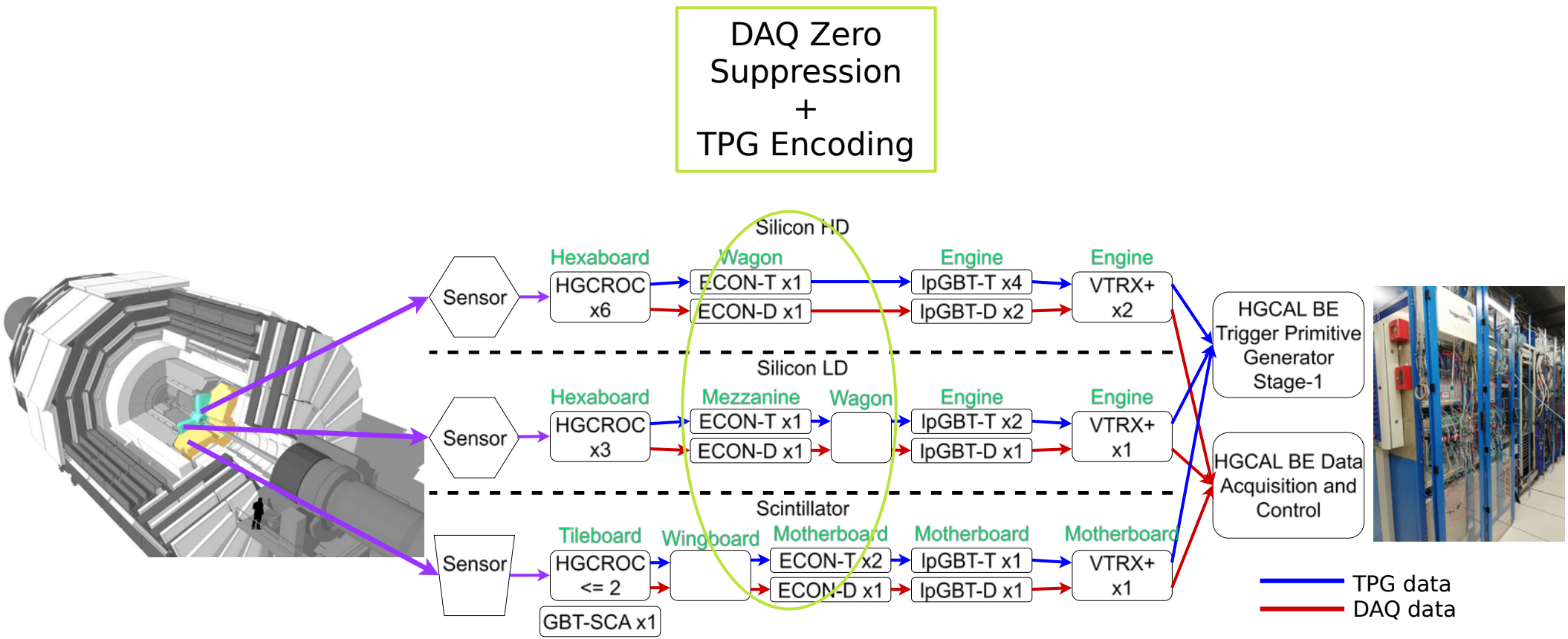
Highly heterogeneous FE:
→ 11 hexaboard varieties,
→ 49 wagon varieties,
→ 32 tileboard varieties,
→ 2 wingboard varieties, ...



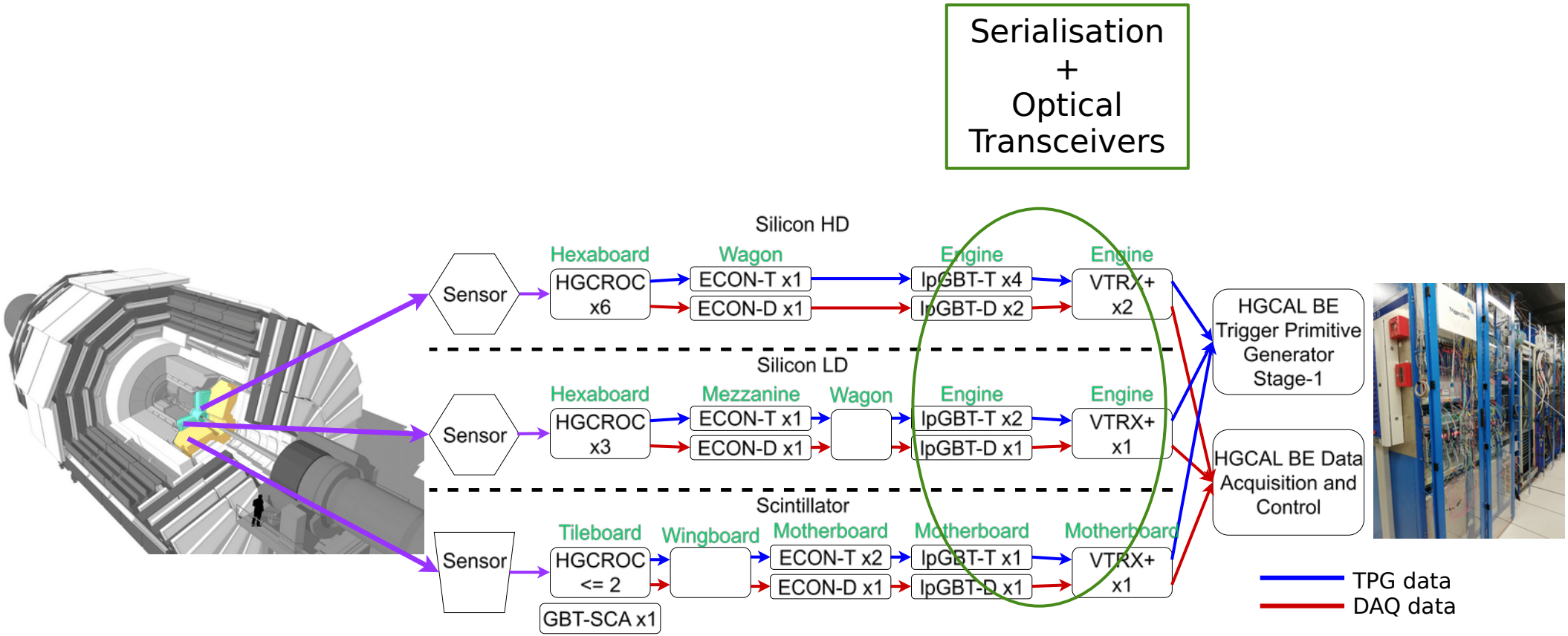
Three FE flavours, two uplink paths



Three FE flavours, two uplink paths



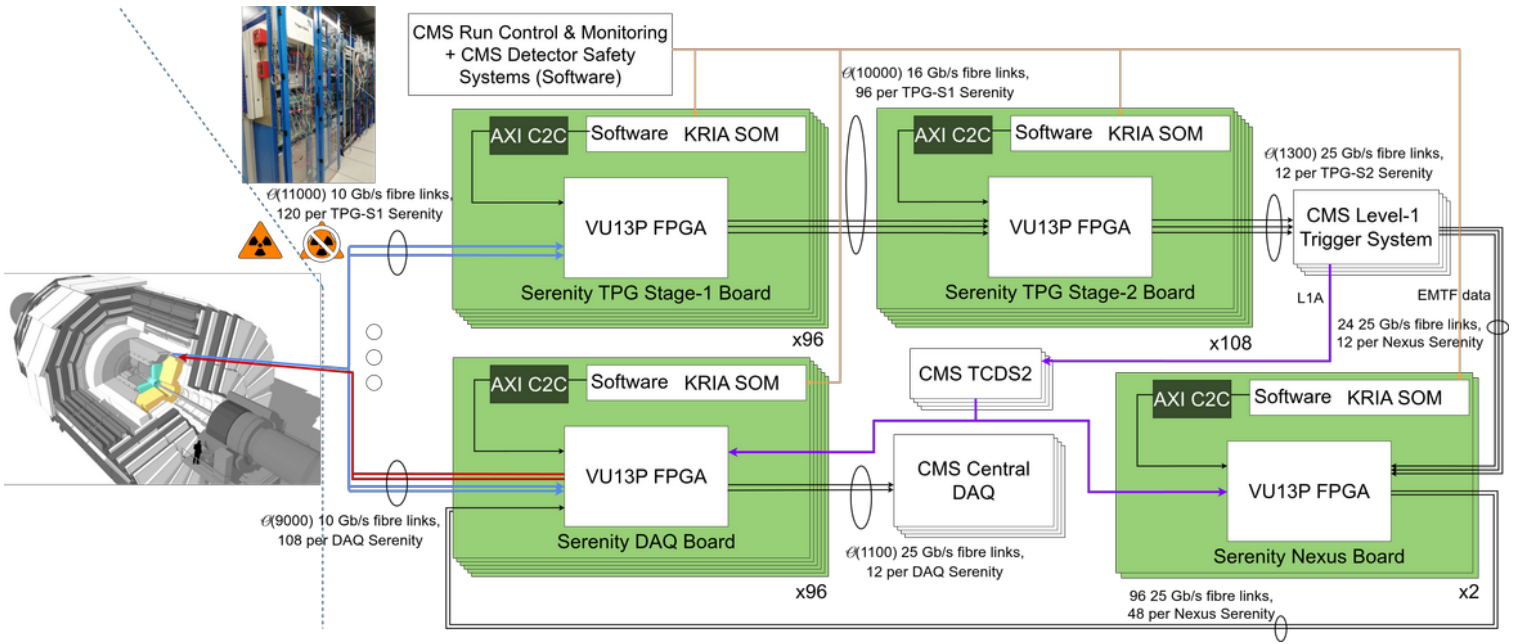
Three FE flavours, two uplink paths



Around 30k ASICs send 2 TB/s of DAQ data to the Serenity boards

The HGCAL BE comprises 302 Serenities grouped into 4 sub-systems that interface with:

- The central DAQ system
- The Level-1 Trigger (L1T) system
- The Timing Control Distribution (TCDS2) system
- The Run Control & Monitoring system (RCMS)



From 108x 10 Gb/s to 12x 25 Gb/s

Each DAQ BE board is required to interface:

- **108 optical fibre pairs from the FE**,
- **12 optical fibre pairs to the central DAQ**,
- 1 optical fibre pair from the Nexus sub-system.
- The TCDS2 clock and control system.
- The RCMS system via software.

Objective of my work:

- Implement and validate the DAQ gateware.

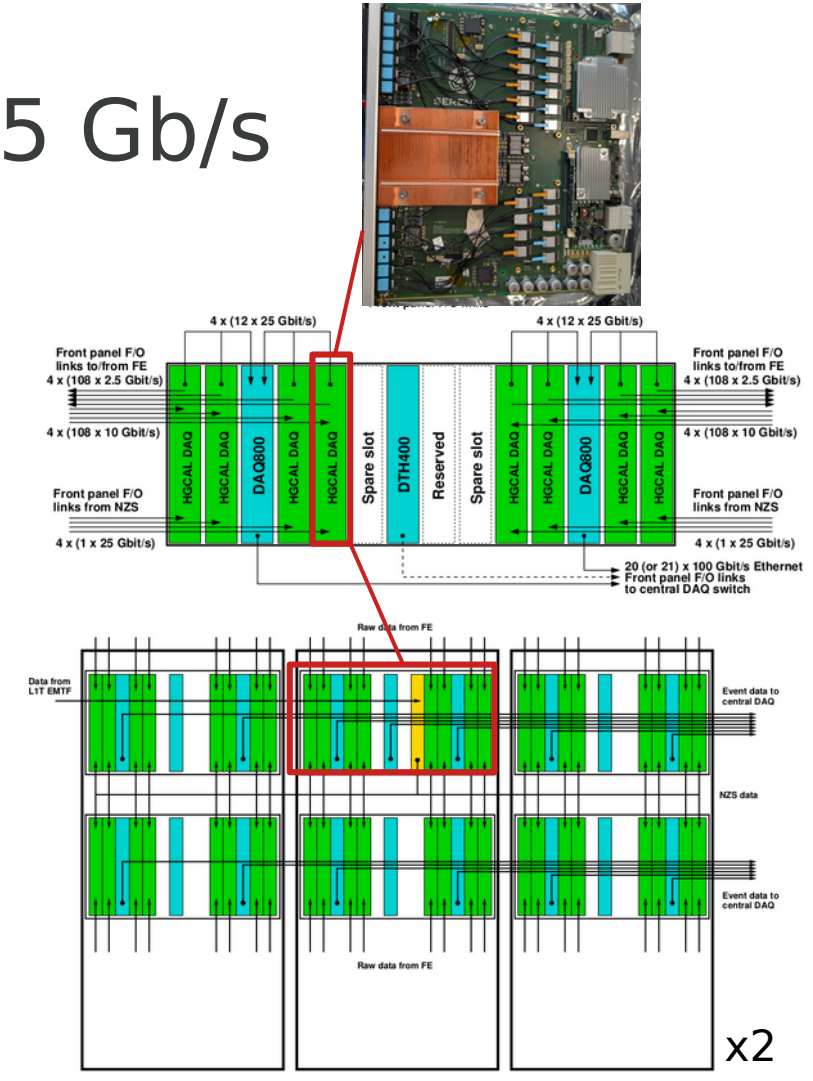
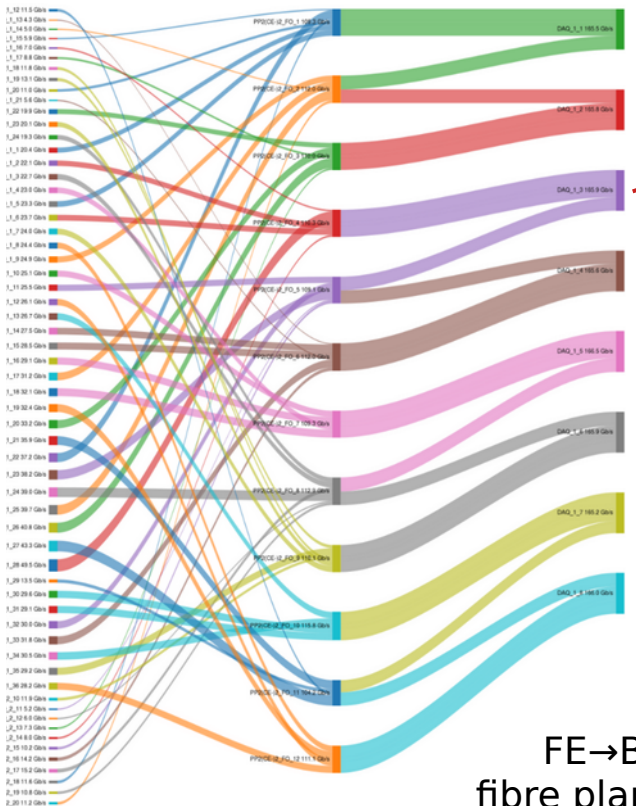


Figure adapted from the HGCAL Back-end PRR

Outline

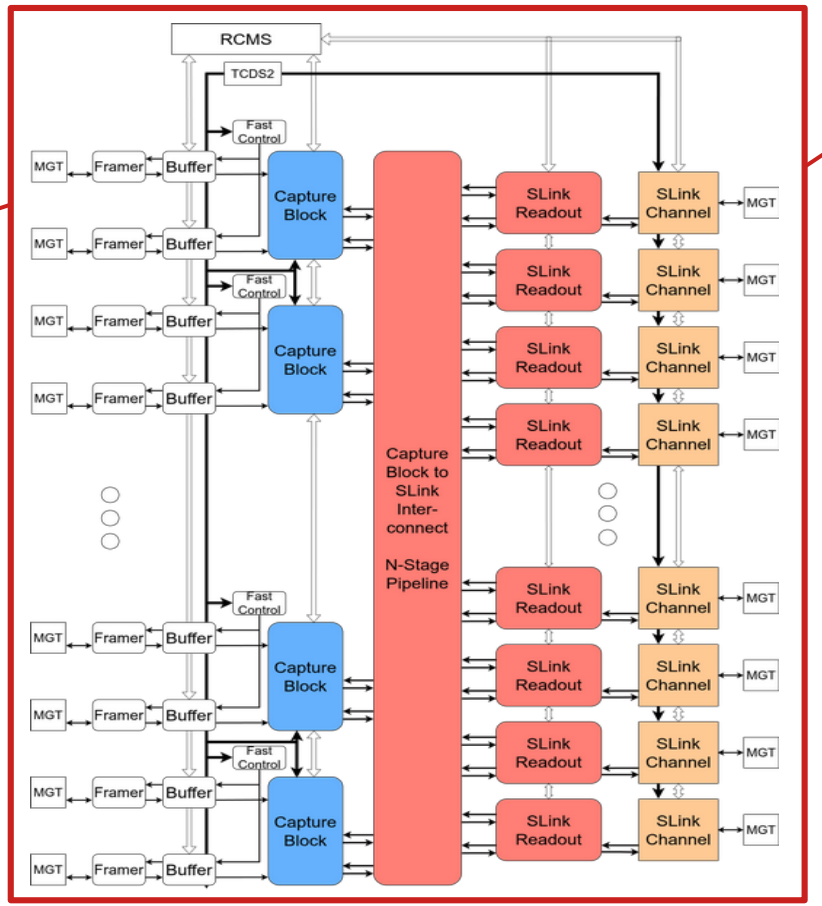
- When, why, and where to HGCAL?
- **What readout for the HGCAL DAQ?**
  - **One bitfile to balance a highly heterogeneous data load**
- Present-day Challenges
- Conclusions

One single highly configurable design for all Serenity boards



FE→BE
fibre plant
limited load balancing

Plot courtesy of C. Amendola



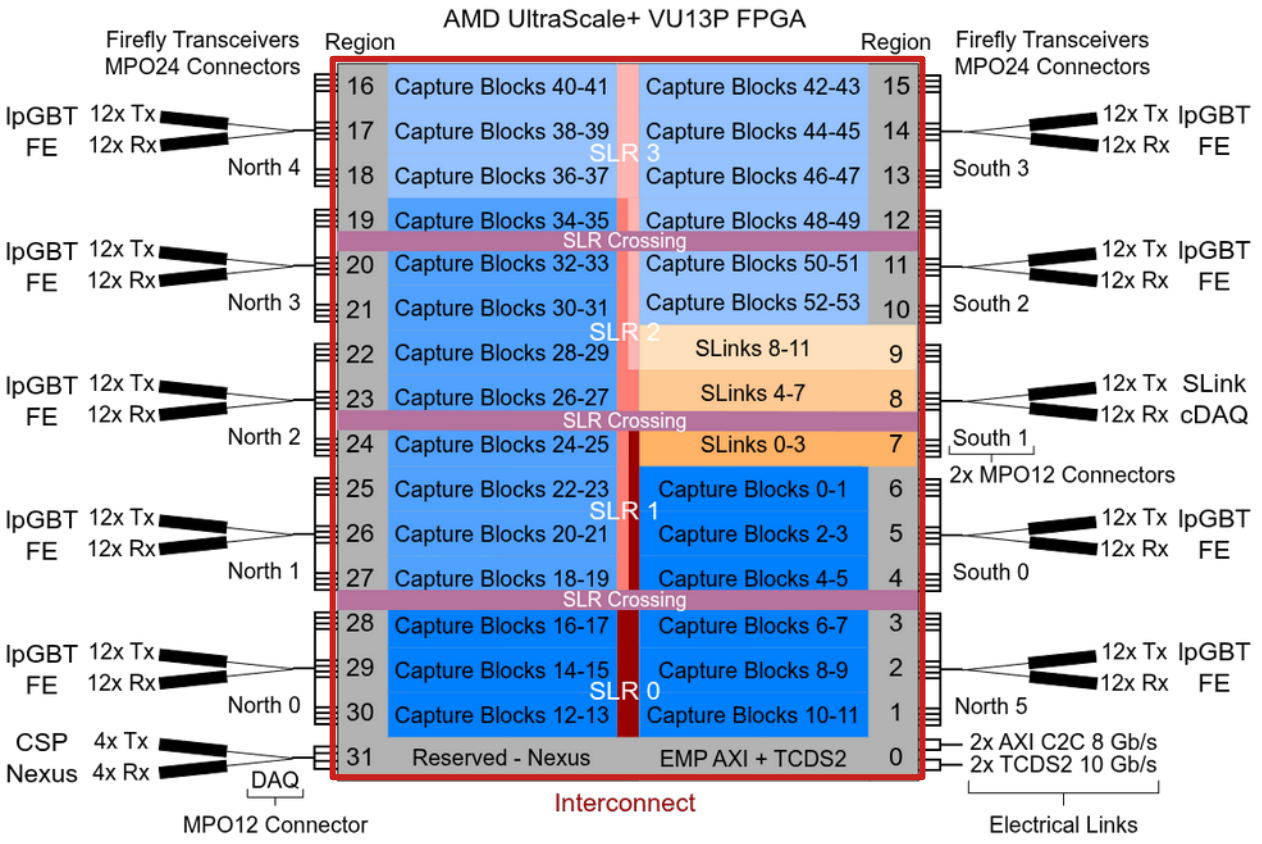
Challenges:
- 108 input packet building
- Aggregation into 12 outputs

16 different gatewares are not maintainable!

One single highly configurable design for all Serenity boards

Contributions in three functional blocks:

- The Capture Block.
- The SLink Interconnect.
- The SLink readout.



Minimisation of SLR crossings crucial for timing closure!

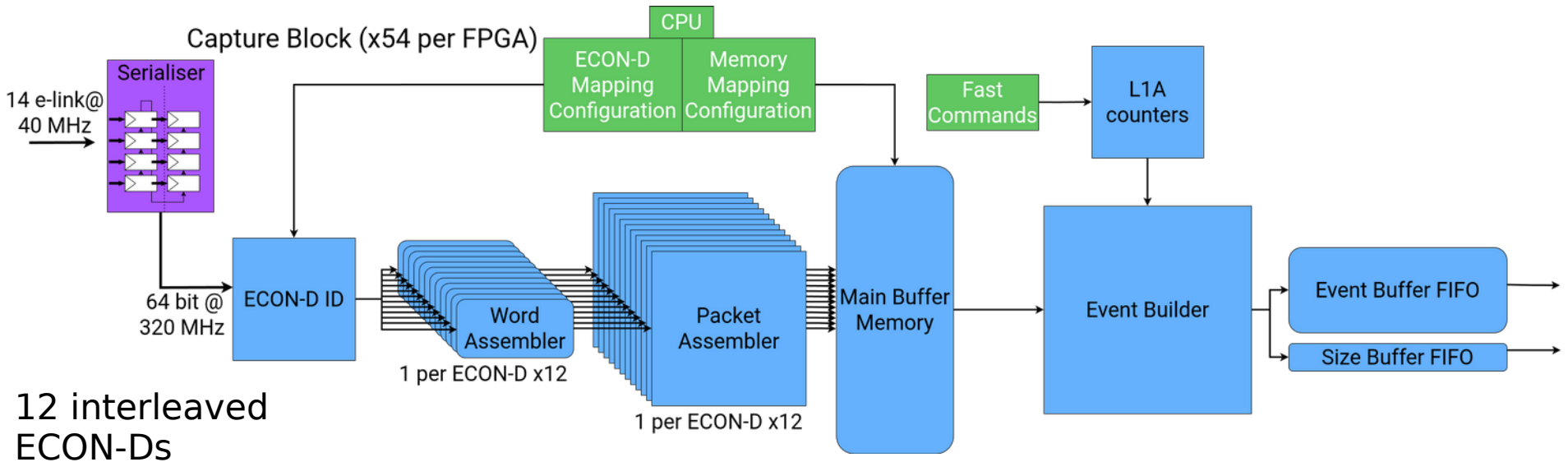
Outline

- When, why, and where to HGCAL?
- **What readout for the HGCAL DAQ?**
  - **One processing block to interface multiple FE mappings**
- Present-day Challenges
- Conclusions

Capture Block: one single and highly run-time configurable circuit for all fibre mappings

The processing to be done to the ECON-D data can be divided into two parts:

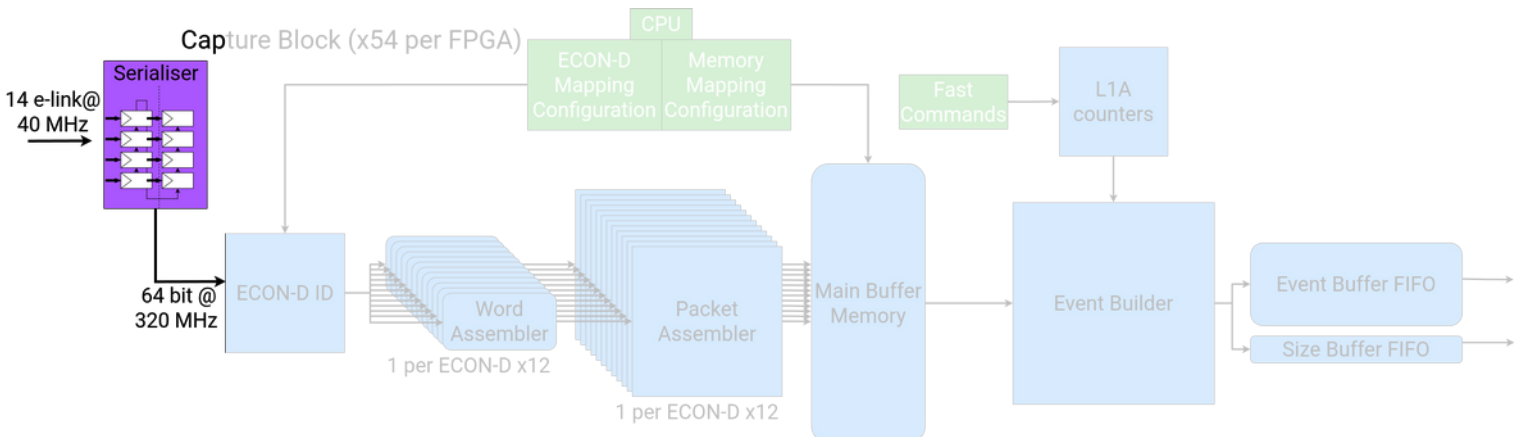
- Packet Detection
- Event Building



A FE ↔ BE conversation

A **delicate balance** was achieved between the **FE PCB routing** and the **BE e-link reordering**.

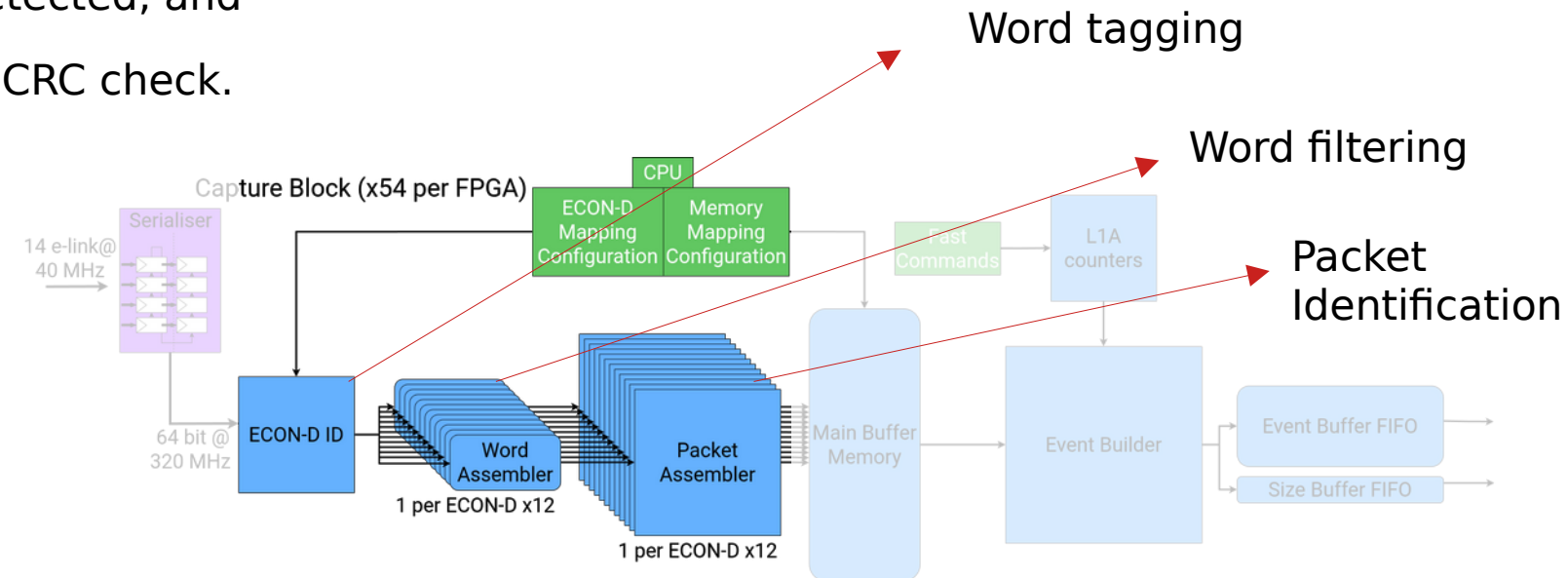
- **E-links from the same ECON-D** must be received by the Capture Block in a consistent **monotonic order**.



Packet detection in 12 data streams

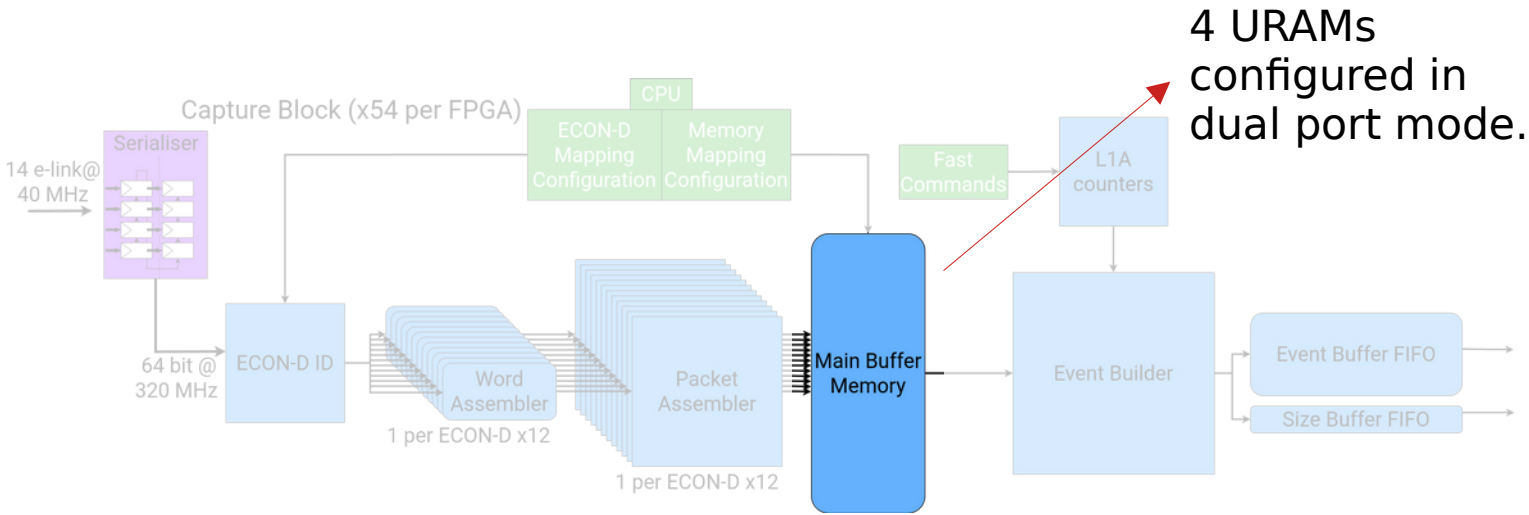
Packet detection extracts valid packets from up to 12 ECON-D (FE ASIC) from two lpGBT data streams when:

- ECON-D header detected
- Idle words detected, and
- Valid header CRC check.



Run-time buffer memory allocation

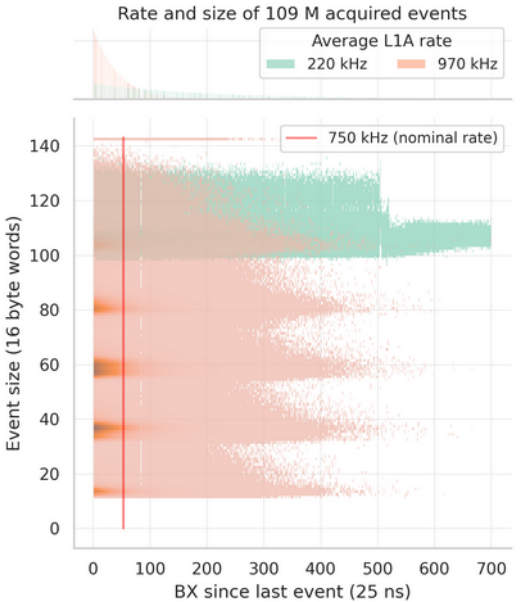
- Not possible to implement individual buffers for all 648 ECON-Ds per FPGA.
- The main buffer memory can be partitioned in up to 12 FIFOs with programmable depths.
- Software programmed registers control these depths at runtime.

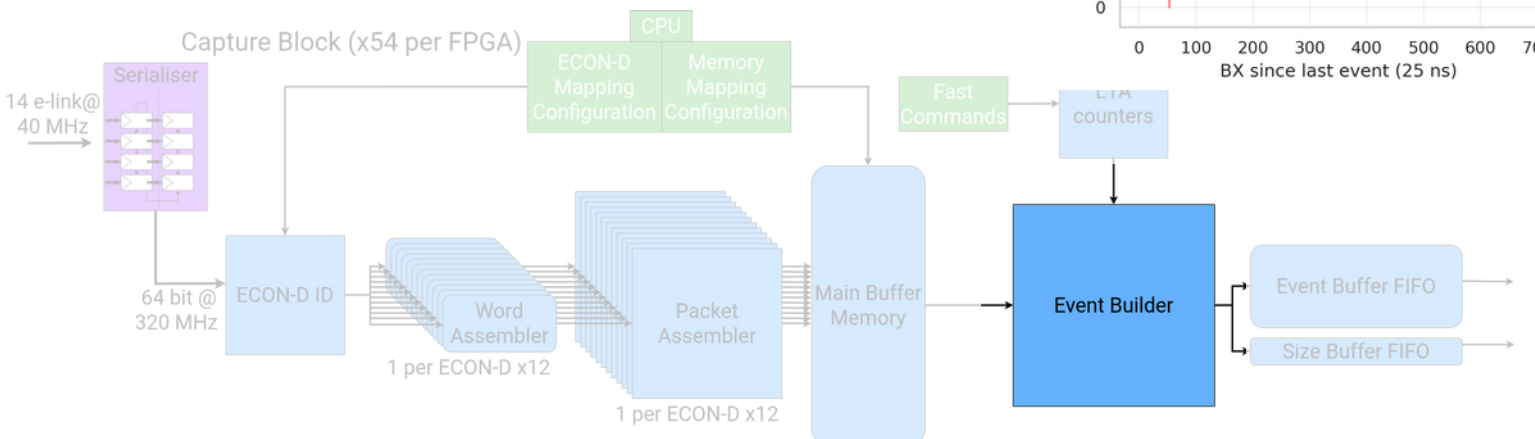


Event building at 750 kHz

The Capture Block has been validated in several beamtests since 2023 at CERN’s north area.

These tests allowed to operate the Capture Block at the nominal 750 kHz L1A trigger rate with final-like hardware components!





Plot: https://dx.doi.org/10.1088/1748-0221/20/03/C03028

Outline

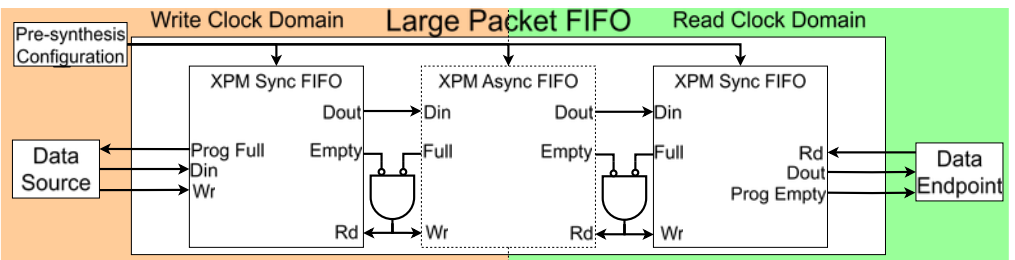
- When, why, and where to HGCAL?
- **What readout for the HGCAL DAQ?**
  - **Design and resource allocation for scalability**
- Present-day Challenges
- Conclusions

Implementation of asynchronous FIFOs with URAMs freed up 30% BRAM usage

Storage	BRAM (%)	URAM (%)
Utilisation	**76.8**	16.9

Storage	BRAM (%)	URAM (%)
Utilisation	**48.6**	25.3

- The **event buffer** was **redesigned with URAMs** to reduce BRAMs in the large scale design.
- Challenging to use the single clock URAMs in asynchronous FIFOs.



FIFO diagram: https://doi.org/10.1109/FPL68686.2025.00021

Gitlab-CI automated test flow

- Optimise development time
- Simulations triggered by git push action
- All fibre mappings tested in O(20) parallel simulations
- Failed simulations saved as gitlab artifacts

Modular git repo able to work with:
→ Other designs (e.g. lpGBT pair)
→ Other FPGAs (e.g. KU15P)
→ (Other mappings)

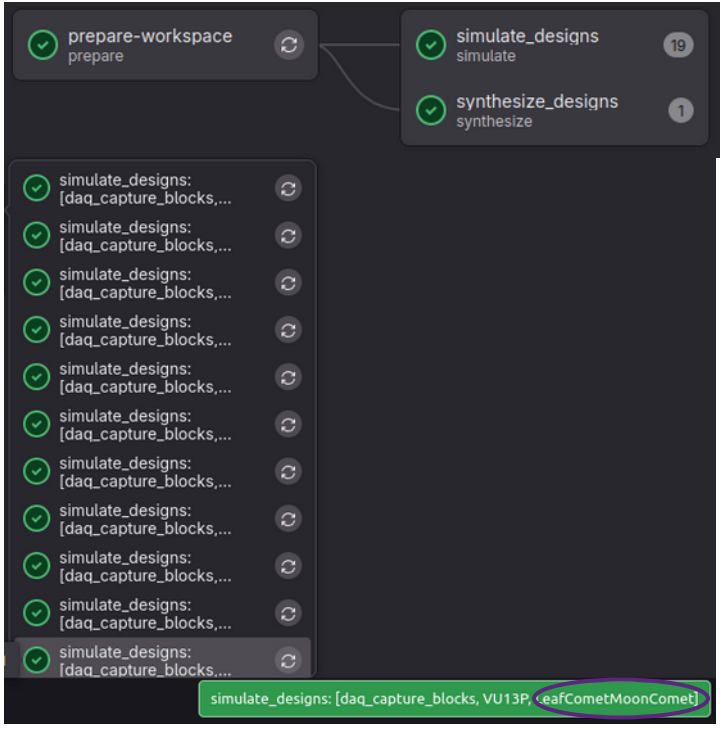
Waggon_mappings.yml 918 B

```
Pineapple:
  - 2F2F2F1212010F
  - "3"
Banana:
  - 0F0F1F1F2F2F2F
  - "3"
Pumpkin:
  - 0F0F1F1F1F2F2F
  - "3"
Apple:
  - 002F2232321311
  - "4"
Grapes:
  - 0F0F1F1F3F232F
  - "4"
Cherry:
  - 0F1F1FFFFFFFFF
  - "2"
Avocado:
  - 1F11212F220200
  - "3"
LeafMushroomMoonMushroom:
  - 0202FFFF1314F5
  - "6"
LeafPaperClipMoonPaperClip:
  - 0314FFFF2526F7
  - "8"
LeafCometMoonComet:
  - 041526FF3738F9
  - "A"
LeafBirdMoonBird:
  - 031414FF2526F7
  - "8"
```

“git push”

Python extracts from the mapping VHDL configurations and generates fake ECON-D packets for simulation.

Simulations stimulate the capture blocks with up to 6 L1As in 1024 64b frames.



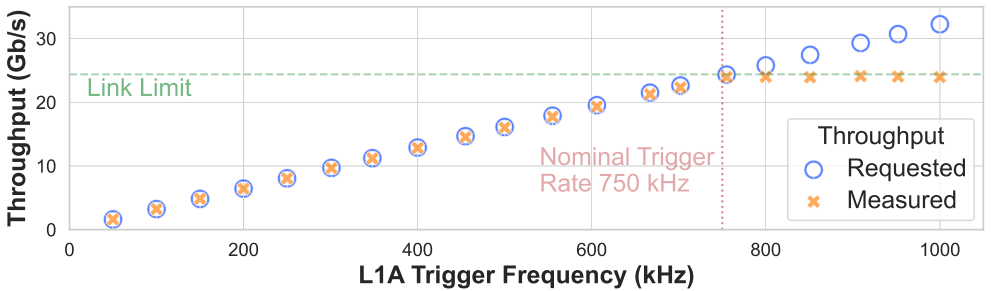
Outline

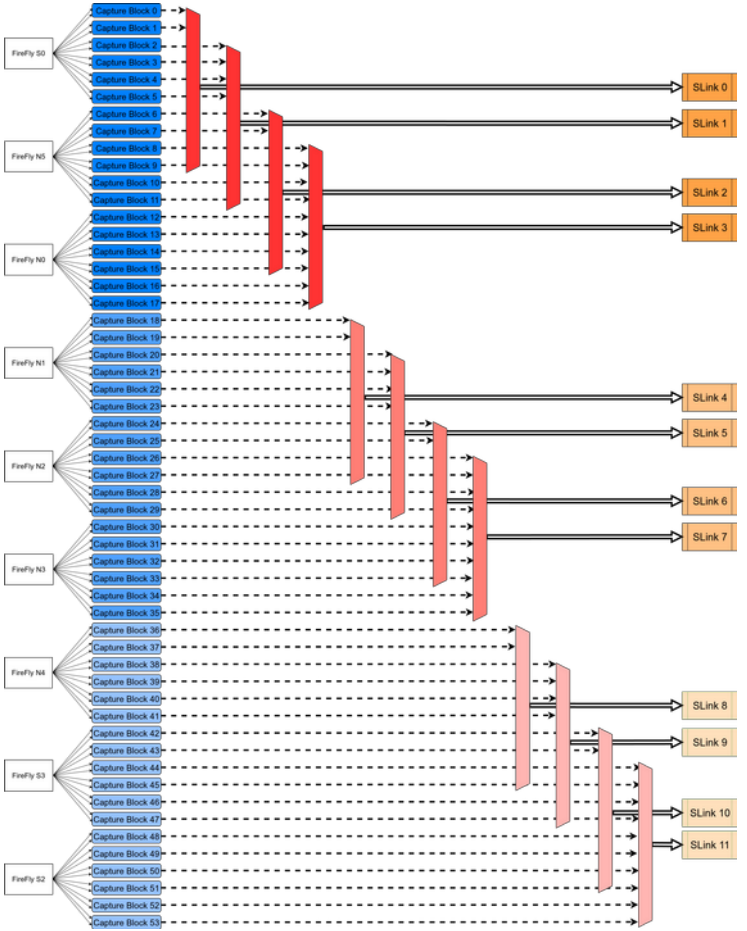
- When, why, and where to HGCAL?
- **What readout for the HGCAL DAQ?**
  - **One configurable aggregator to cross SLRs**
- Present-day Challenges
- Conclusions

A scalable pre-synthesis and run-time configurable CB packet aggregator

A **new readout circuit was developed**, allowing to extract data from CBs, convert them into an SLink stream:

- Compliant with backpressure.
- Parametric number of CB inputs.
- Latency agnostic.
- Fully parametric Interconnect.





Plot: https://doi.org/10.1109/ISCAS56072.2025.11044120

Outline

- When, why, and where to HGCAL?
- **What readout for the HGCAL DAQ?**
  - **One template for multiple systems**
- Present-day Challenges
- Conclusions

Progressive scale-up and system integration

The HGCAL BE DAQ has been under constant development and validation in reduced-scale detector prototypes used in beamtests since 2023!

2023
- 2 Silicon Modules
- 1 Capture Block
- Custom 10GbE readout

2026
- 12 Silicon layers
- 2 Scintillator layers
- 18 Capture Block
- SLink-based readout

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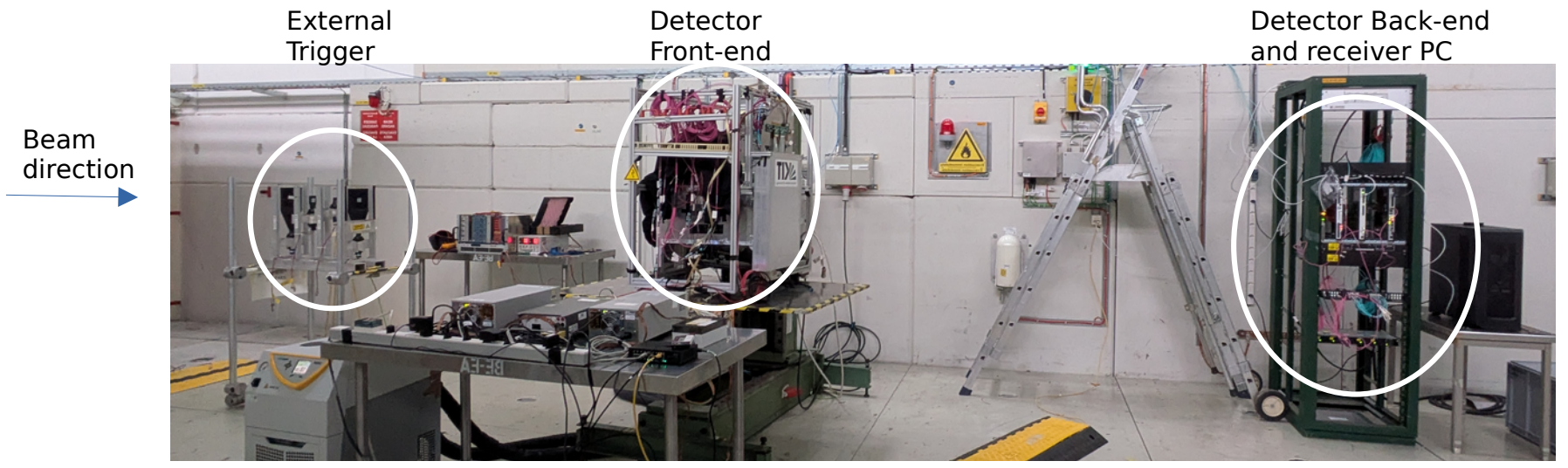

Beamtest setup from May 2026 at the CERN PS

Different systems with evolving requirements

But what about maintainability?

Identical blocks in all designs!

Parametric approach!

	dietDAQ	SCT	MCT-DAQ	fullDAQ
Capture Blocks	9	18	54	
SLink MGT Quads	1		3	
SLink Fibres	2	4	3	12
SLink Mux Factor	5	7	18	10

Scope				
Proof of Concept	✓			
Development	✓	✓		
Prototyping		✓		
Production Testing		✓	✓	
Final System				✓

New DAQ VHDL template: from monolithic to parametric!

	dietDAQ	SCT	MCT-DAQ	fullDAQ
Capture Blocks	9	18	54	
SLink MGT Quads	1		3	
SLink Fibres	2	4	3	12
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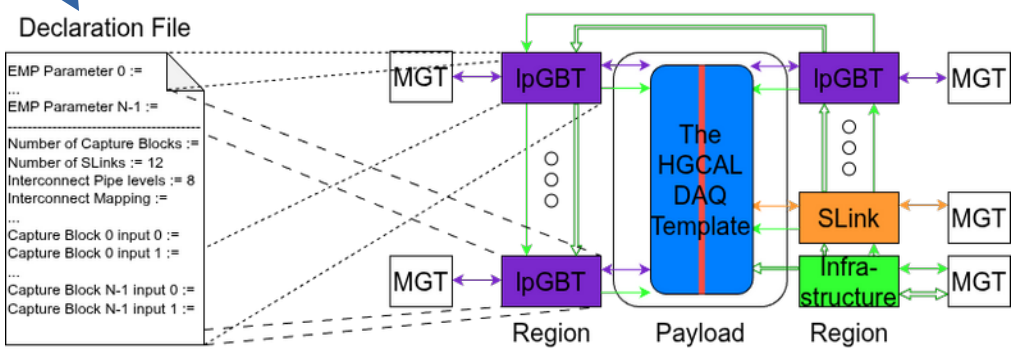
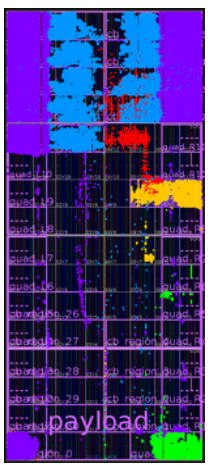
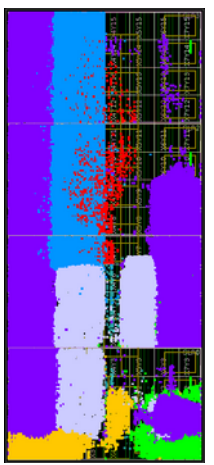
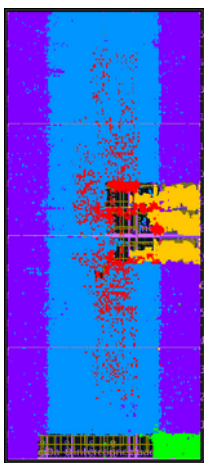
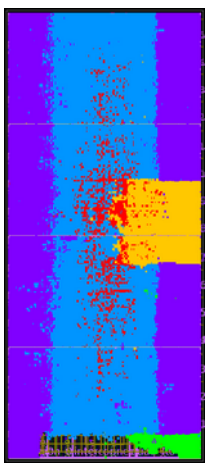


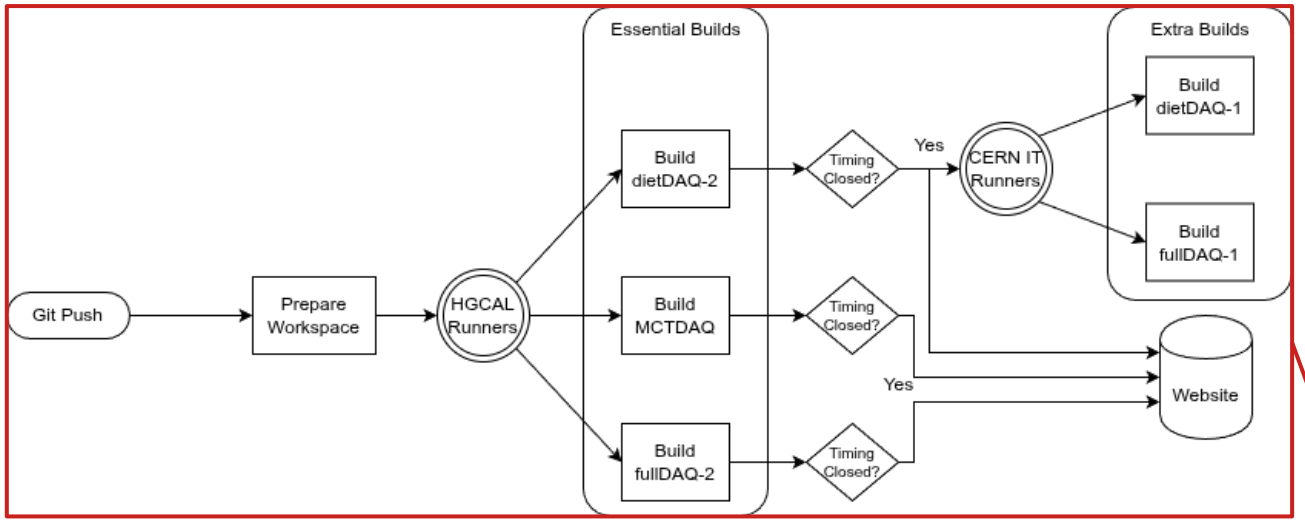








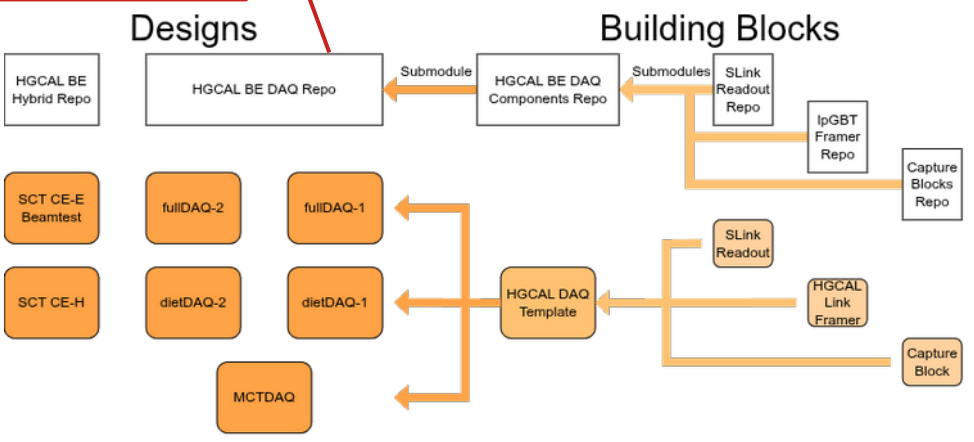
Complementary modular gitlab workflow



The **designs** are **built in parallel** and diagnostics are extracted automatically.

Essential Builds are run in **dedicated PCs** while Extra Builds use shared PCs.

All designs are built with the same modular VHDL code improving development and maintenance.



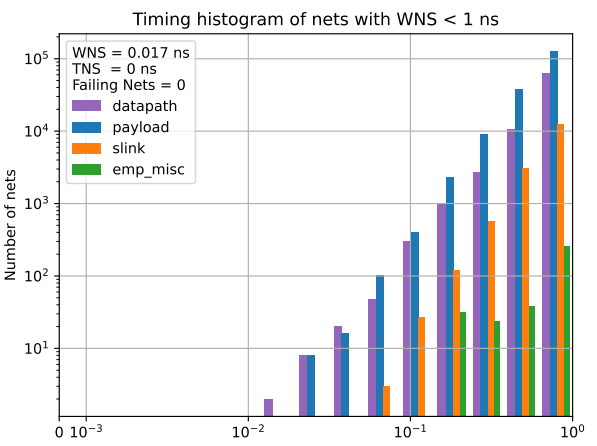
The final system design: fullDAQ!

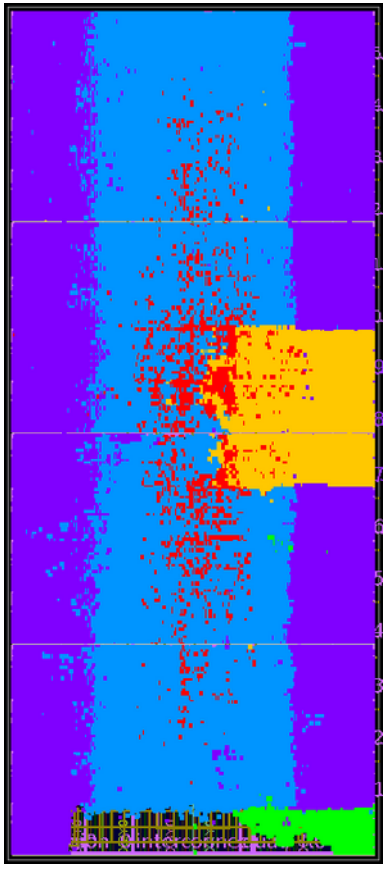
First full-scale prototype integrated with Serenity's EMP framework!

Brittle timing closure in Vivado 2022.2
- WNS ≃ 10 ps!
- Utilisation close to the recommended 70 %.

Presented at the HGCAL BE Procurement Readiness Review*.

Ongoing challenges:
- Limited SLink bandwidth
- More pervasive error detection
- Improvements for timing closure
- Automated tests without FE hardware availability





* - M. Rosado, A. Şarkışla, "DAQ firmware design"
Plot scripts available!

Outline

- When, why, and where to HGCAL?
- What readout for the HGCAL DAQ?
- **Present-day Challenges**
- Conclusions

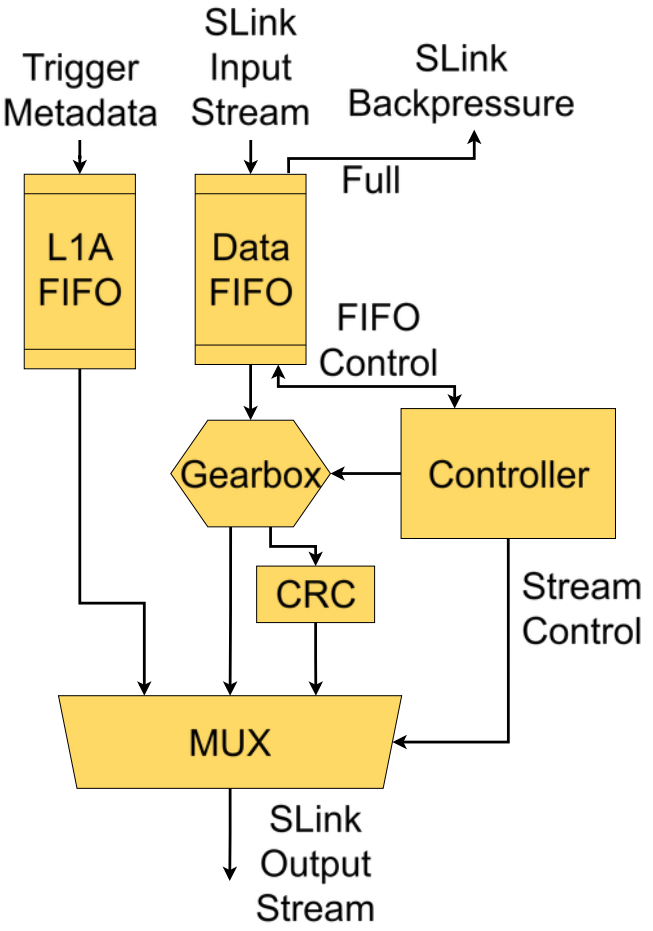
Modular streaming SLink

The SLink formatter in the EMP framework **currently limits**:

- Packet **size**
- **Bandwidth** to 20.5 Gb/s (nominal 25 Gb/s)
- **RAM usage** and consequent output buffer instantiation

A new SLink streaming formatter was implemented with **customizable**:

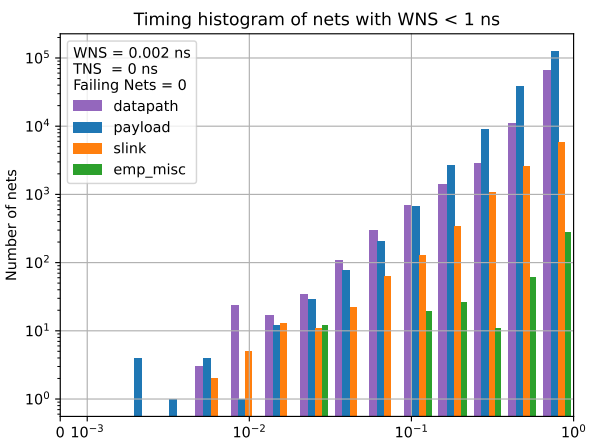
- SLink **clock** and respective CDC, propagated to the user
- Event **metadata** source (user-defined or provided by EMP)
- **Width** of data bus

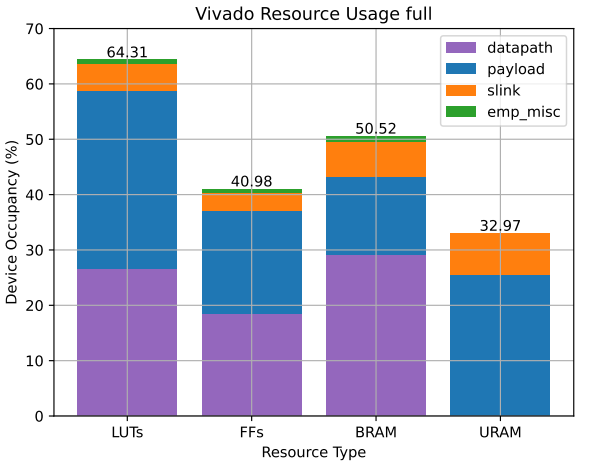


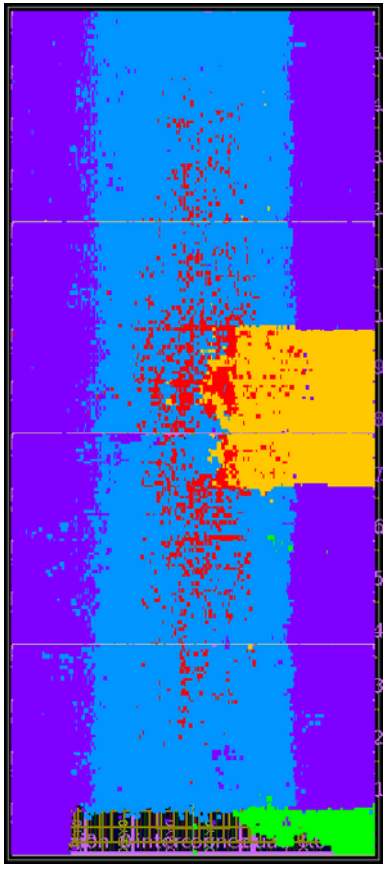
fullDAQ: SLink streaming impact

With the new SLink streaming:

- SLink **output buffers increased** from one per quad (**3**) to one per channel (**12**)
- **Increased bandwidth** to 23 Gb/s (maximum allowed by the SLink clock)
- **Timing** closure and **resource usage** remain **relatively unchanged** despite more challenging interconnect clock frequency!
- **Preliminary tests** with Capture Block emulator data **passed** without errors!





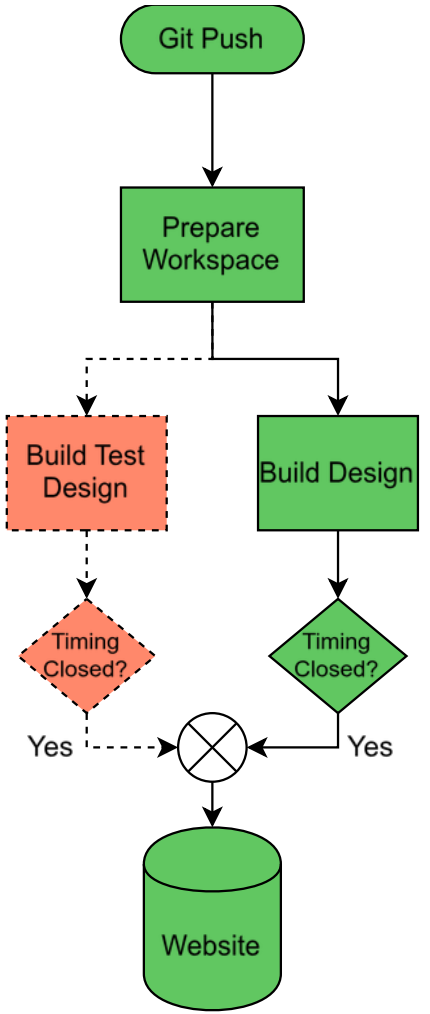


Git-based testing on hardware

- **As the HGCAL DAQ scales** in size and design variety, **automated tests become necessary.**

- Past efforts expanded the gitlab CI infrastructure to run small tests in a surrogate board, the mSerenity (HTG-940).

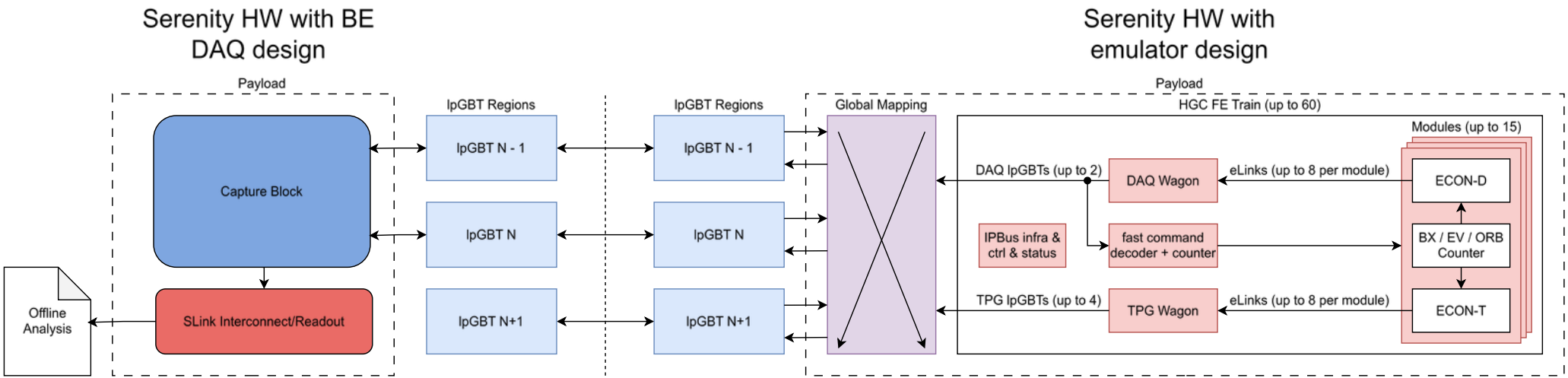
- The **reduced amount of available FE electronics** motivates **alternative stimuli** sources.



Towards configurable FE emulation

Current collaboration with KIT and H. Krause to **integrate** his FE **emulator** in the HGCAL DAQ **testing procedures**.

Readily available “FE” allows to stimulate the design with error injection, extending the emulator use to development and debugging.



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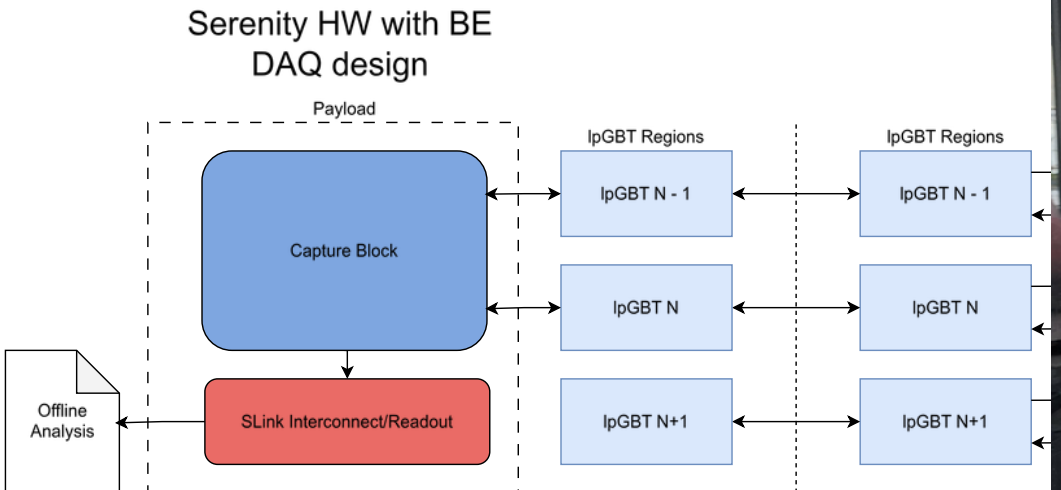
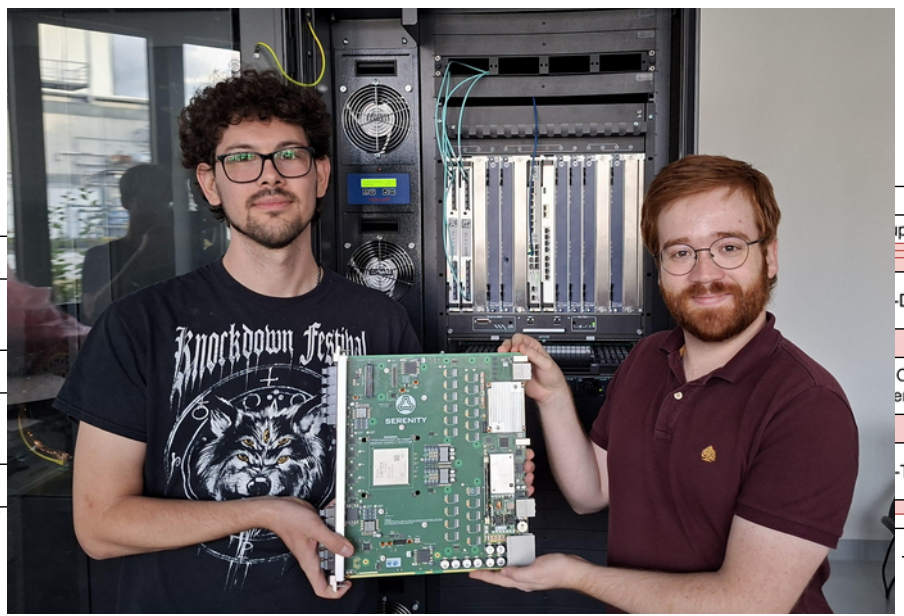




Outline

- When, why, and where to HGCAL?
- What readout for the HGCAL DAQ?
- Present-day Challenges
- **Conclusions**

A Marathon

The HGCAL Back-end DAQ represents a multi-year collaboration:

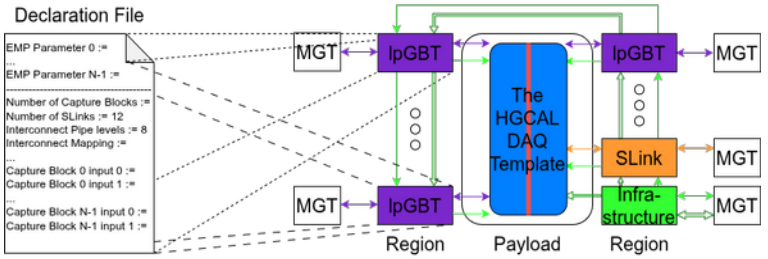
- 2020 - 2022: The design’s **development** began with the basic **architecture** and creation of **core blocks**, including the capture blocks, interconnect logic, and **feasibility studies**.
  - Contributors: Stavros Mallios & Paschalis Vichoudis

- 2022 – Present: **Integration with the EMP framework** followed, with **extensive testing across Serenity boards**, beam tests, lab setups, and simulations. The core design remained, while many bugs were fixed, blocks were rewritten, and **additional functionality** was added.
  - Contributors: **Martim Rosado** & Alp Şarkışla

Personal contributions to the system

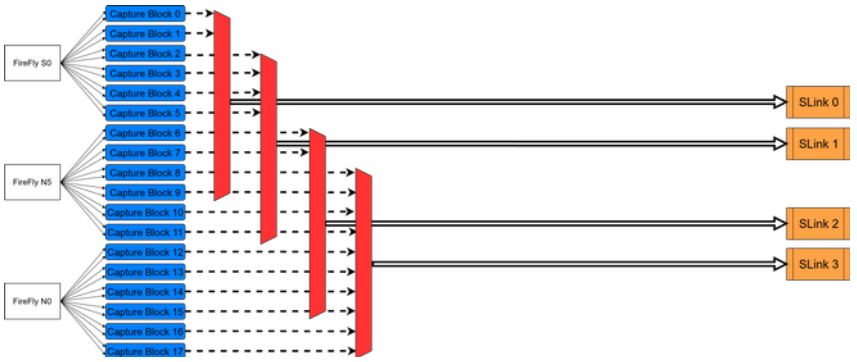
Shared contributions:

- Capture Block integration and commissioning.
- Development of the HGCAL BE DAQ template.
- Development of the Gitlab-CI build infrastructure.



Individual contributions:

- Design and commissioning of the Capture Block ↔ SLink readout:
  - Capture Block event buffer
  - Capture Block packet aggregator
  - SLink streaming formatter



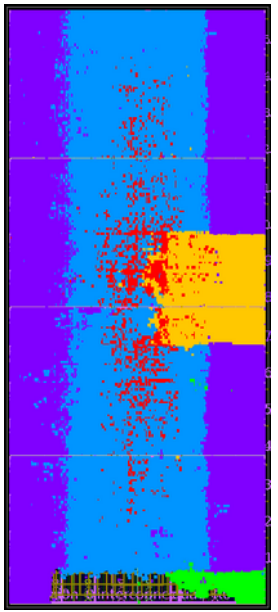
Summary and outlook

The **HGCAL DAQ** is **implemented** across **several systems** and Serenities that:

- Interface up to **108 lpGBT** fibres,
- Transmit data across up to **12 SLink** fibres,
- **Balance** heterogeneous **data load** with a **single design**.

Until 2030, the HGCAL **DAQ design** will **undergo improvements** to:

- **Augment** its **bandwidth**,
- Improve **resilience to errors**, and
- Achieve a more **stable timing closure.**



Thank you!

Q.A.

Backup

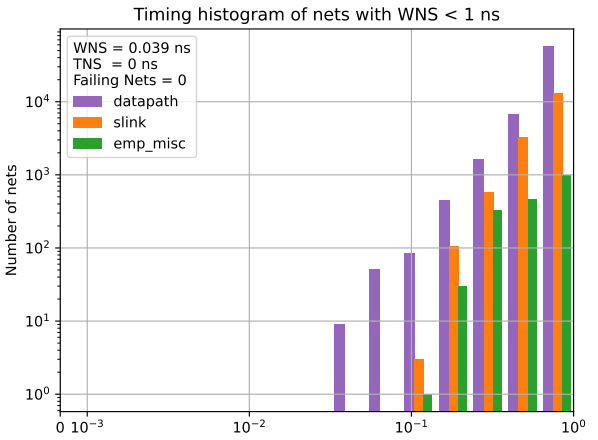
Publications

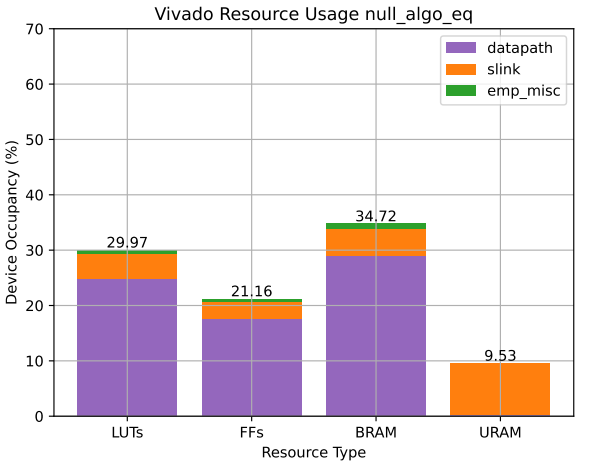
- M. Rosado, A. Şarkışla, S. Mallios, B. Akgün, A. David, N. Roma, P. Tomás, P. Vichoudis, and on behalf of the CMS Collaboration, “Back-end DAQ system prototype testing and integration on a full detector test system for the CMS HGCAL detector,” Journal of Instrumentation, vol. 20, no. 03, p. C03028, Mar 2025.
- M. Rosado, P. Tomás, N. Roma, and A. David, “High-throughput packet aggregator for the back-end DAQ of CERN CMS HGCAL detector,” in 2025 IEEE International Symposium on Circuits and Systems (ISCAS), 2025.
- M. Rosado, P. Tomás, N. Roma, and A. David, “URAM-based asynchronous FIFO design for improved throughput and FPGA RAM usage”, in 2025 International Conference on Field-Programmable Logic and Applications (FPL), Leiden, September 2025.
  - Ongoing follow up with a team from AMD working on development of FPGA fabric.

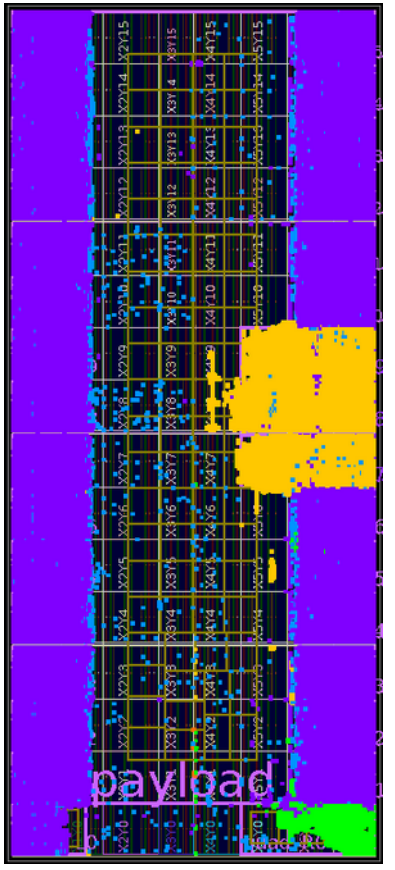
Timing closure successful – “null” algo

“Empty” design with the EMP framework components required for the HGCAL BE DAQ design.

Used in development to isolate potential issues when changing EMP versions.



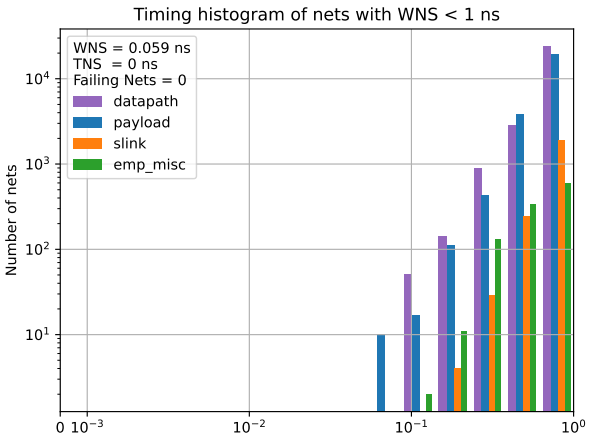


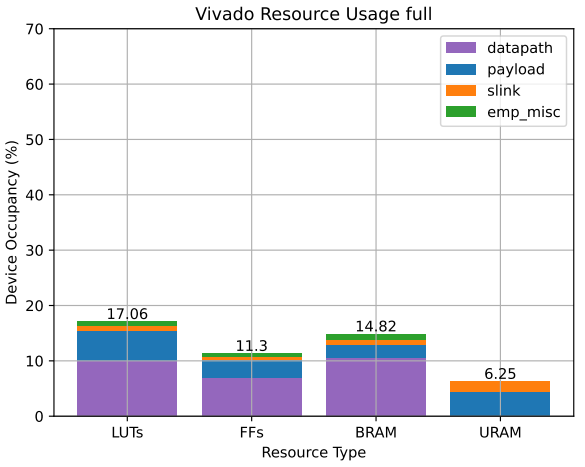


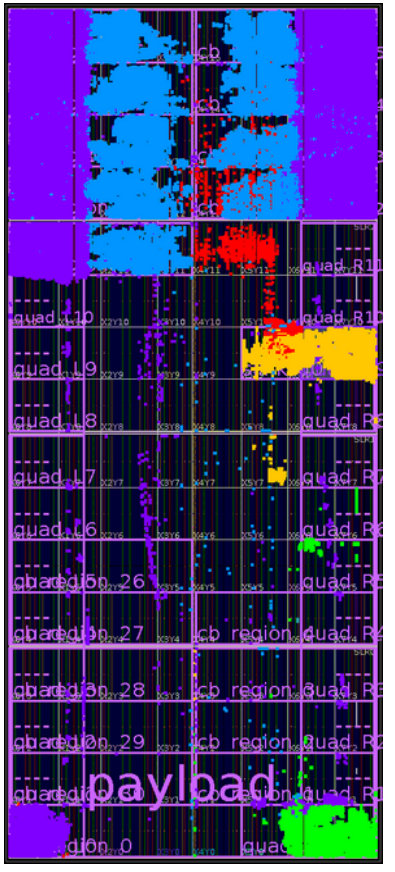
Timing closure successful – dietDAQ

Minimal size version of the HGCAL BE DAQ design allowing to test the majority of the functionality.

Used mainly in development due to its fast build time (< 60 mins) enabling faster identification of issues before the fullDAQ build is concluded (< 4 h 30 mins).



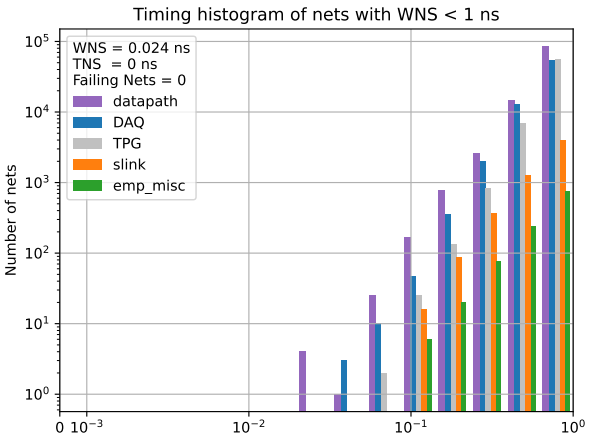


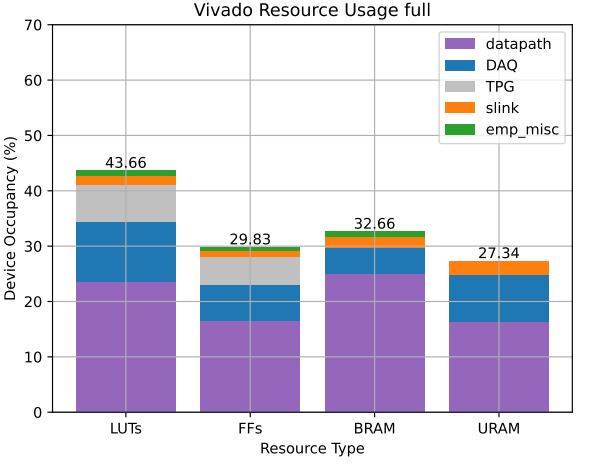


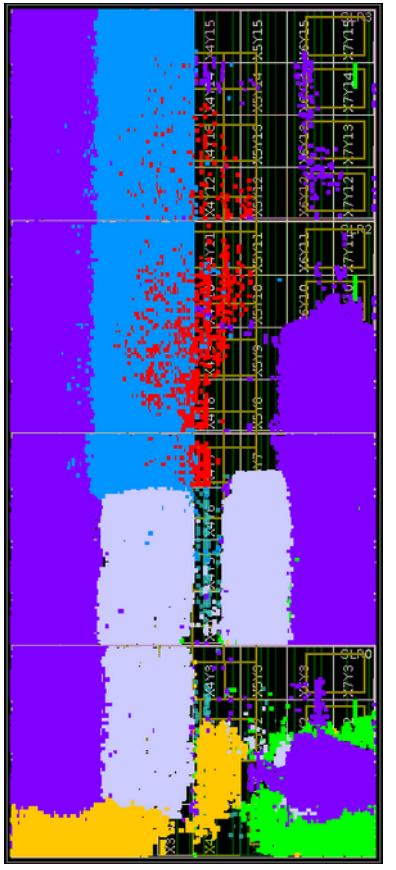
Timing closure successful – Single Cassette Tester

Hybrid design with both HGCAL BE DAQ and TPG-S1 components.

Used as the current system for the BE boards in beamtests and for testing single cassettes.





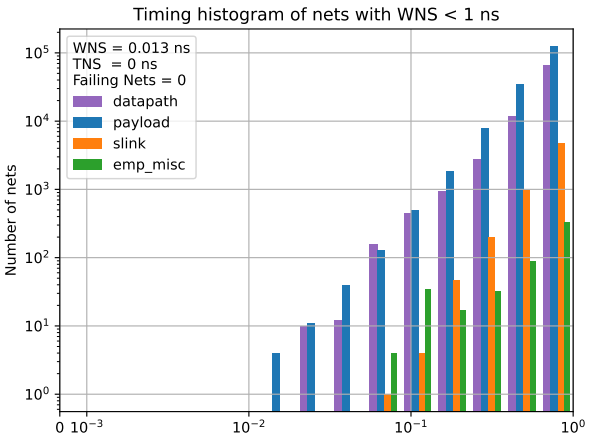


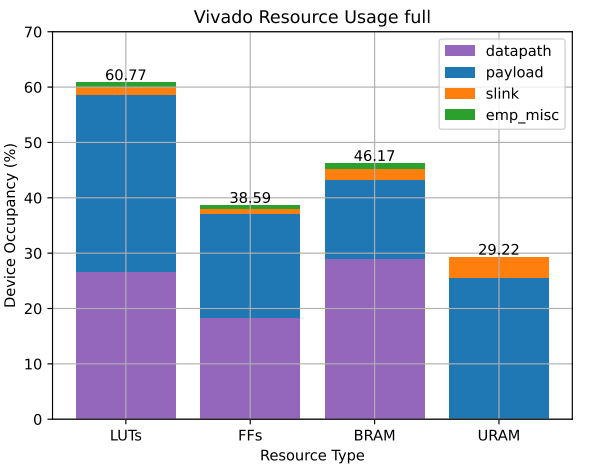
Timing closure successful – Multi Cassette Tester

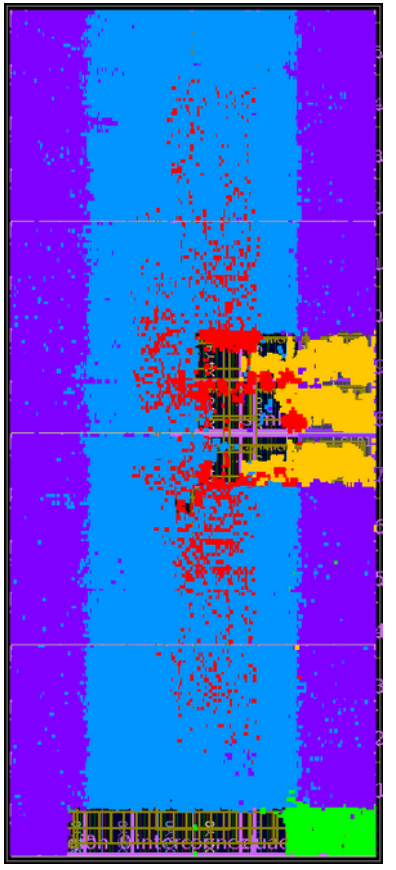
Design with slightly smaller dimensions when compared to the final system.

Designed and maintained to be deployed as the gateware for the BE DAQ boards of the multi cassette tester systems.

Fewer SLink channels are used due to the hardware availability constraints of the DTH400 and DAQ800 boards.







One single highly configurable design for all Serenity boards

Each fibre pair receives data from 2 lpGBTs over 14 e-links.

Each group of 14 e-links transmits data from up to 12 ECON-Ds.

Each ECON-D may use up to 6 e-links.