Intel Technologies for HPC

GridKa 2012
28 August 2012
Herbert Cornelius
Intel

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Notice revision #20101101

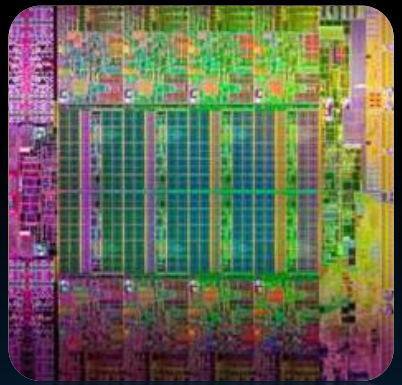
COMPUTING 2020

(Source: IDC Directions 2010, March 2010, ICT Outlook forecast)

Intel's Approach to Cloud Solutions

Define and Prioritize Cloud Requirements

Intel Building Blocks to Address Requirements



Complete Partner Solutions

Moore's Law is Transforming the Economics of HPC

1960s

1970s

1980s

1990s

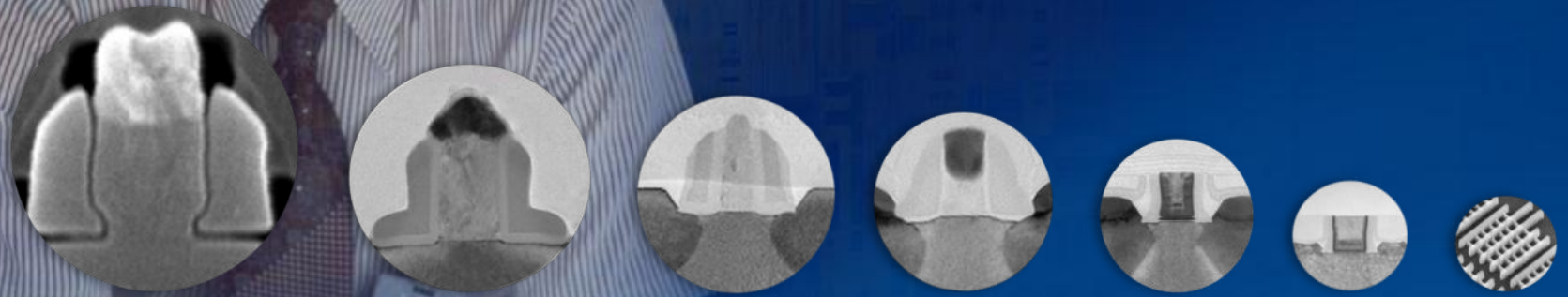
2000s

1997	**1 TFLOPS**	**$55,000 / GFLOPS**
2009	**>500 TFLOPS**	**<$100 / GFLOPS**
	>500x more performance	***>550x less costs***

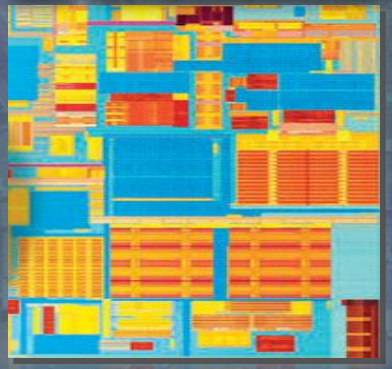
Predictable Silicon Track Record

Executing to Moore's Law

Enabling new devices with higher functionality & complexity while controlling power, cost, and size

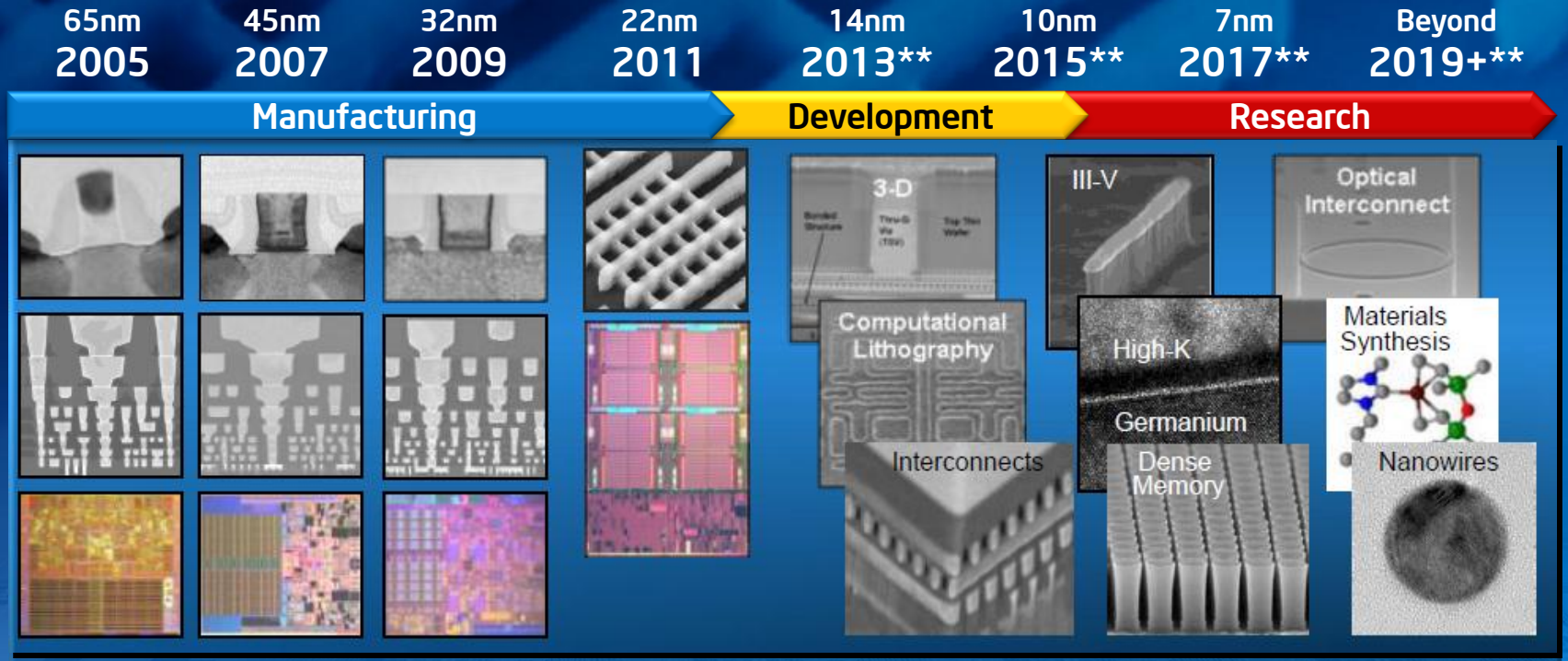


14nm



well on track

Process Technology Research @ Intel



**projected

Potential future options, no indication of
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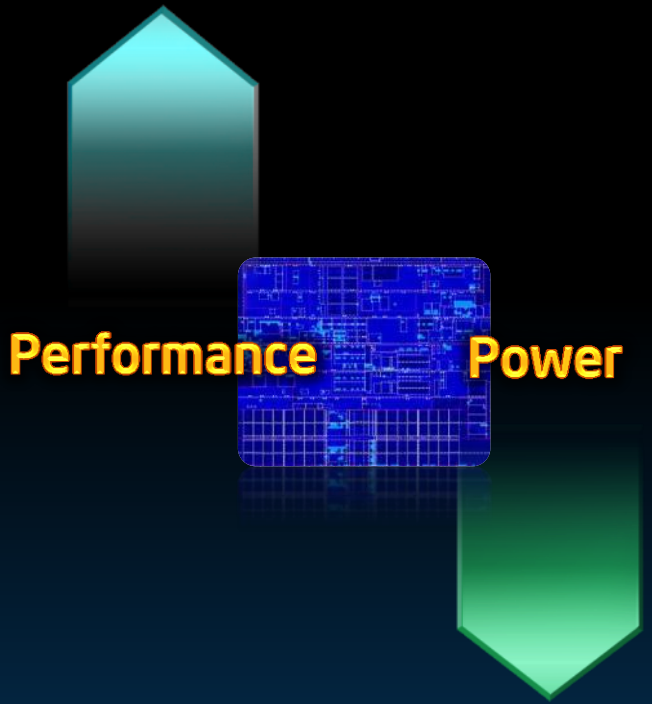
Computing Trends and Design Points



Just Arrived ...

THE UNBELIEVABLY FAST

XOLO

X900

with Intel Inside

XOLO | intel inside

MYTH:

Energy Efficient
Performance
can only be achieved with
(very) Special architected
Hardware, Software and Tools

1997: THE FIRST INTEL® TERAFLOP COMPUTER
consisted of:

9,298 INTEL PROCESSORS

and occupied:

72 SERVER CABINETS

THE INTEL® XEON® PHI™ COPROCESSOR
will provide:

1 TERAFLOP OF PERFORMANCE

and occupy:

1 PCIe SLOT

intel inside
Xeon Phi

Intel in High-Performance Computing

Dedicated, Renowned Applications Expertise

Large Scale Clusters for Test & Optimization

Tera-Scale Research

Exa-Scale Labs

intel Cluster Ready

Defined HPC Application Platform

intel Software

Broad Software Tools Portfolio

Industry Standards

Manufacturing Process Technologies

intel Xeon®

Leading Processor Performance, Energy Efficiency

intel Xeon Phi™ Coprocessor

Many Integrated Core Architecture

Platform Building Blocks, Fabric

A long term commitment to the HPC market segment

intel

Intel Technology is Changing HPC

Performance, Energy Efficiency, Reliability, TCO

PROCESSORS

Scalable Performance and

Energy Efficiency,

Multi- and Many-Core

SOLID STATE DISKS

Optimize Performance for

I/O Intensive Apps and

Boot Drive Replacement

NETWORKING

1GbE , 10GbE (with RDMA, LOM)

InfiniBand*, Fabrics

Unified Networking

A platform approach to high performance

[picture sizes not to scale and for illustration only]

What's Intel Doing in 2012 in HPC …

Intel® Xeon® Processor:
E5-2600/4600 Product Families

Intel® Many Integrated Core Architecture

Fabric Technologies:
Cray's Aries Interconnect, Qlogic's TrueScale Product Family

Intel® Software Development Tools

Intel Fabrics Environment

HPC Expertise
Intellectual Property
World-class Interconnect s

CRAY THE SUPERCOMPUTER COMPANY

HPC Expertise
Fabric Management & Software
Highest Performance, Scalable IB Products

QLOGIC

Low-latency Ethernet Switching
Data Center Ethernet Expertise
High Radix & Low Radix Switch Products

FULCRUM microsystems

Market Leading Compute & Ethernet Products
Platform Expertise

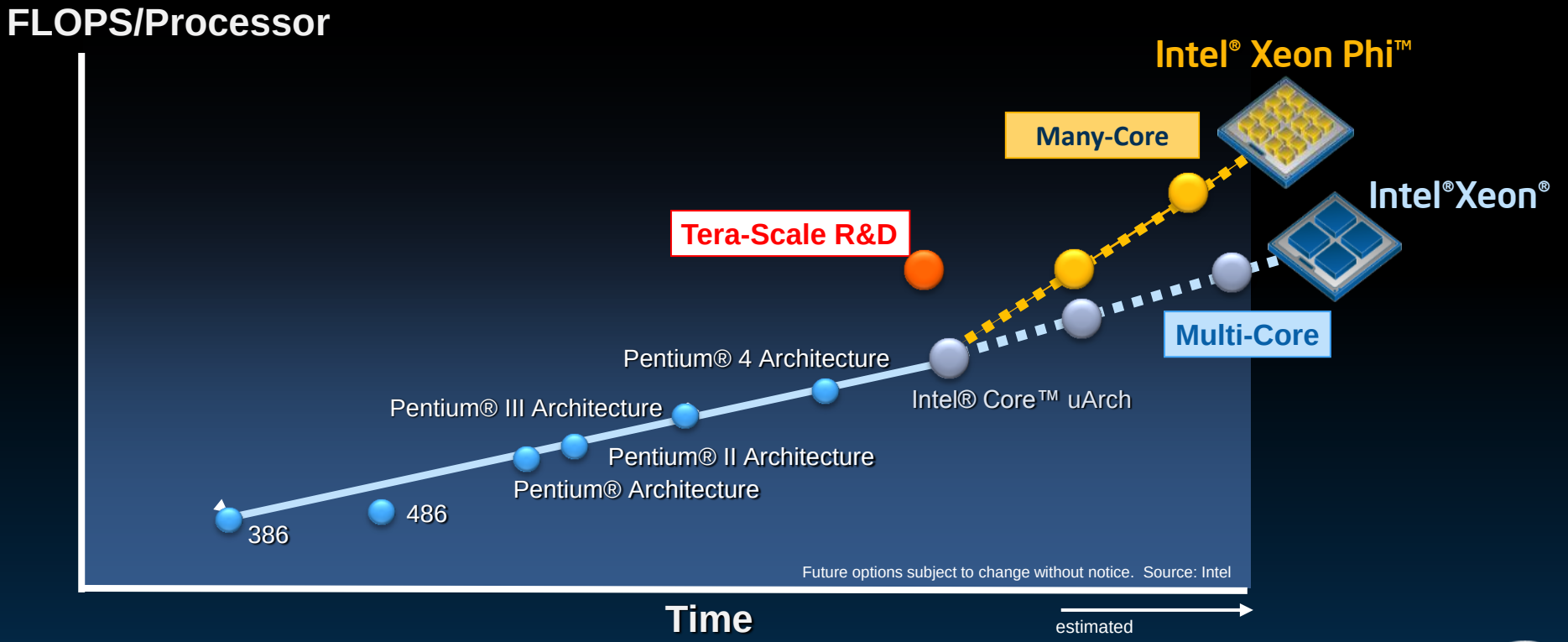
intel

Intel's Comprehensive Connectivity and Fabric Portfolio

intel

Increasing Processor Performance

Through Many-Core Technologies for Highly Parallel Workloads



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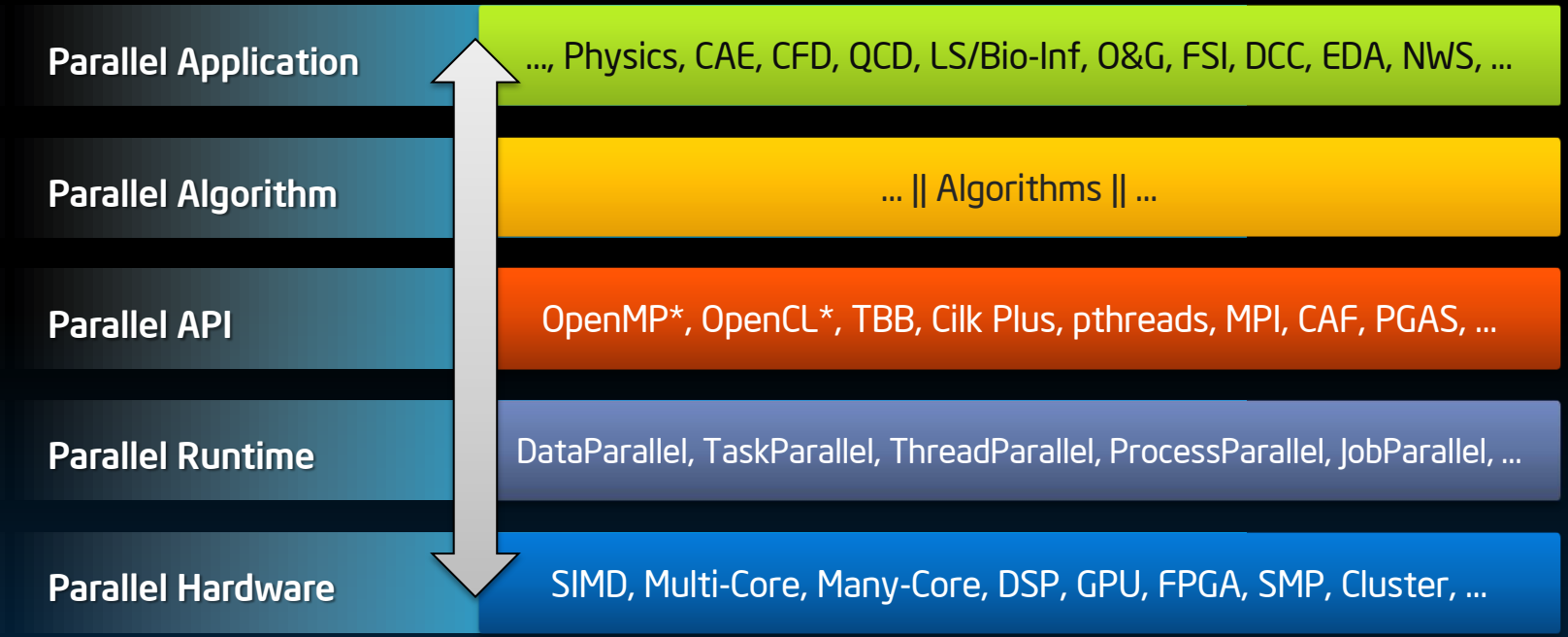
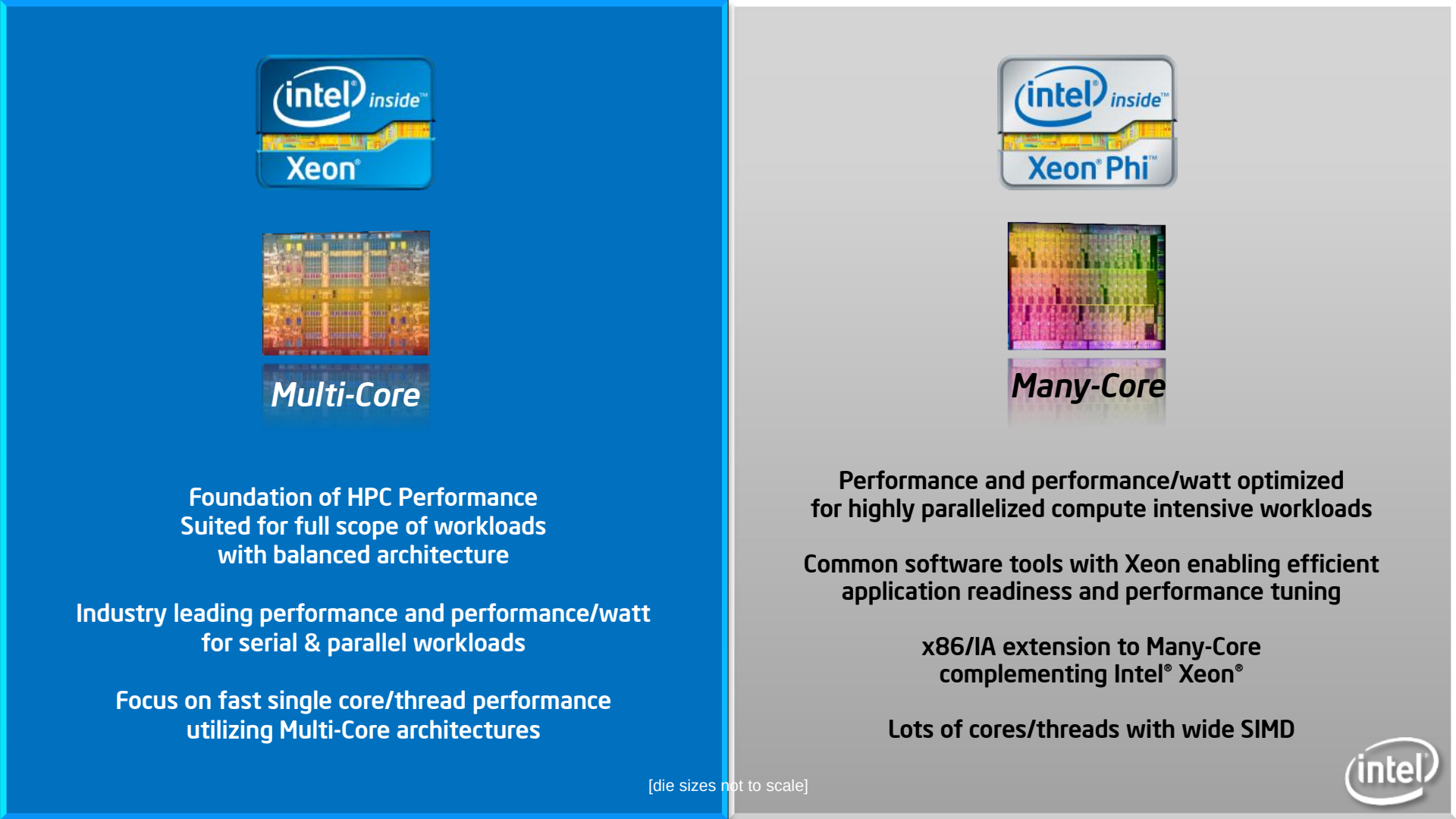
Parallel Computing & Programing




intel inside
Xeon
Multi-Core
Foundation of HPC Performance
Suited for full scope of workloads
with balanced architecture
Industry leading performance and performance/watt
for serial & parallel workloads
Focus on fast single core/thread performance
utilizing Multi-Core architectures
intel inside
Xeon Phi
Many-Core
Performance and performance/watt optimized
for highly parallelized compute intensive workloads
Common software tools with Xeon enabling efficient
application readiness and performance tuning
x86/IA extension to Many-Core
complementing Intel® Xeon®
Lots of cores/threads with wide SIMD
[die sizes not to scale]
intel

C/C++, FORTRAN, …

OpenMP, MPI, …

Same Comprehensive Set of SW Tools

Application Source Code Builds with a Compiler Switch

Established HPC Operating System

Offload and Native Autonomous Linux* Node

intel inside
Xeon

intel inside
Xeon Phi

[die sizes not to scale]

intel

Single Source Code

Compiler
Libraries
Parallel Models

intel Software

Intel Parallel Studio XE

Intel Cluster Studio XE

Multicore

Many-core

Cluster

Multicore CPU

Multicore CPU

Intel® MIC Architecture Co-processor

Multicore Cluster

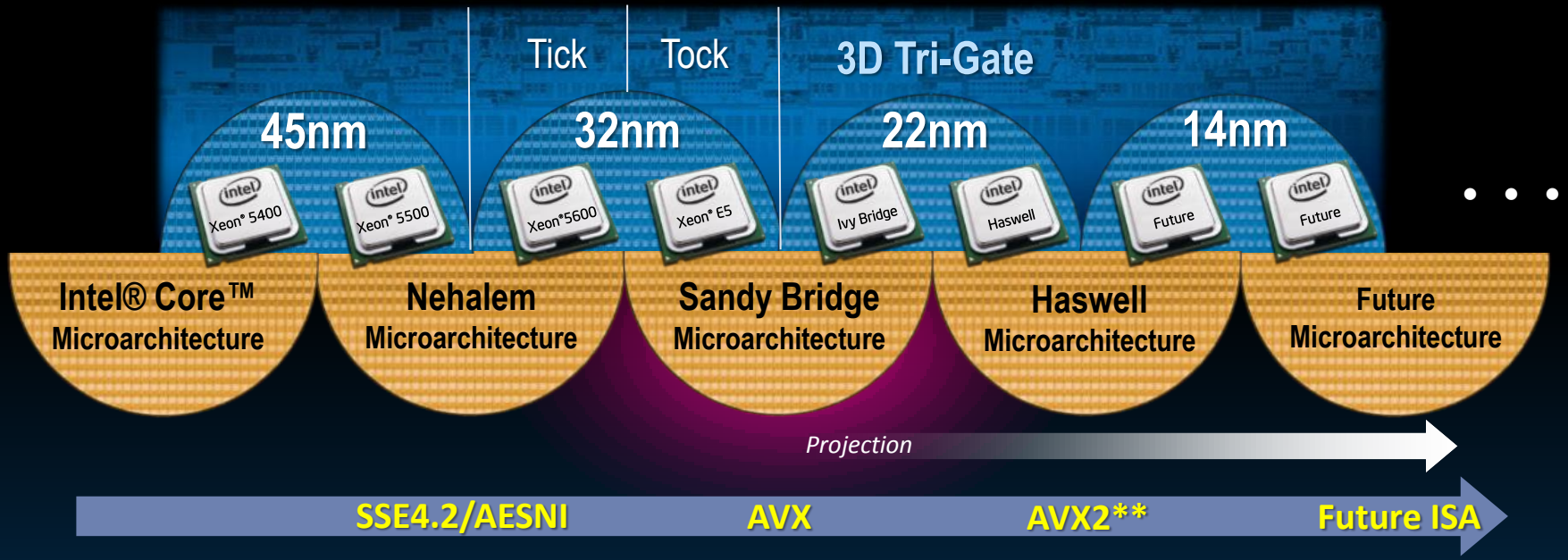
Multicore & Many-core Cluster

Eliminate Need for Dual Programming Software Architecture

For illustration only, potential future options subject to change without notice.

Tick-Tock Development Cycles

Integrate. Innovate.



**Intel® Architecture Instruction Set Extensions Programming Reference, #319433-012A, FEBRUARY 2012

Potential future options, subject to change without notice.

Intel® Xeon® E5-2600 Series Processors

Best combination
of high performance and
energy efficiency – optimizes HPC &
Cloud Solutions

Up to 8 Cores (16 Threads w/ HT)
AVX 256-bit SIMD Instructions
Up to 3.3GHz marked frequency
Turbo-Technology 2
Up to 20MB shared Cache

[data are per processor]

Virtualization (VT)
Trusted Execution (TXT)
AES New Instructions
Integrated PCI Express* 3.0 (x40)
Network Data Direct I/O (DDIO)

4 DDR3 Memory-Channel
(up to 1600MHz)
Up to 768GB memory
Intelligent Power Management

Continued Processor Technologies

- General Purpose programmable and balanced
- SIMD Processing continues as it is quite energy efficient
- Multi/Many-Core with even more Threads
- Fast and Efficient shared Cache/Memory Hierarchy

Potential future options and features are projections and targets, subject to change without notice.

SC'11 November 2011

1 TFLOPS DP-F.P.

(Early Silicon Architecture Demonstration)

MIC: Knights Corner

- In 22nm process technology
- >50 cores/die energy efficient
- 512 bit SIMD instructions
- Prototype Si delivers 1TFLOPS sustained on DGEMM as architecture capability demonstration
- Runs Linux
- Can be
  - a native network node (IP addressable, ssh in …)
  - used as an offload co-processor
- Common x86 programming models, techniques and tools
- Targeted by Intel compilers and SW-tools
- 3rd party software being enabled

Intel® Xeon Phi™ Product Family

based on Intel® Many Integrated Core Architecture

Many Cores compared to Multi-Core

- Many smaller lower power Intel processor cores
- Wider vector processing units for greater (generally) floating point performance/watt

Highly Parallel

- Higher aggregate performance**
- Supports Data Parallel, Thread Parallel, Process/Task Parallel
- Higher memory bandwidth**

Highly Programmable

- Standards-based: C/C++/FORTRAN
- Abstract: no requirement to program to the underlying hardware
- More than an accelerator: fully addressable, independent node in a cluster
- Full support by Intel® Parallel Studio XE and Intel® Cluster Studio XE

It's a Coprocessor, *not an Accelerator*

**Relative to multi-core Intel Xeon processors.

Intel® Xeon Phi™ Product Family

based on Intel® Many Integrated Core Architecture

Optimized, Highly Parallel

Intel® Xeon Phi™ **coprocessor**

(pairs with Intel® Xeon® processor host via PCIe)

Runs Complete Applications

IP Addressable

Open Source Linux OS

Common Source Code

Standard models of clustering

Builds on / Advances

State of the Art in Parallelism

Intel Software Developer tools

SMP on a chip!

The “Knights” Family

Future “Knights” Products

“Knights Corner”

1st Intel® MIC architecture based product

22nm process

>50 Intel Architecture cores

TFLOPS of Performance

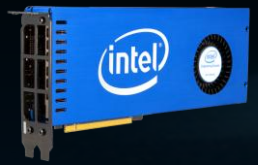
Energy Efficient

Offload Co-Processor and

Native Linux* Node Programming

“Knights Ferry”

Development Platform



“Programmed like a computer”

All dates, product descriptions, availability, and plans are preliminary forecasts and subject to change without notice.

Early Performance on Intel® Xeon Phi™ Coprocessor

(Codenamed Knights Corner)

Small cluster with Intel® Xeon® E5 processor based nodes with early Intel® Xeon Phi™ coprocessors

> 1 TFLOP

Linpack (HPL) on a node

118 TFLOPS

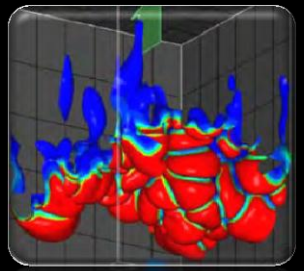
#150 on TOP500 (Jun'12)

In Production in 2012, Enabled by 22nm 3-D TriGate Transistors


Journey to Exascale

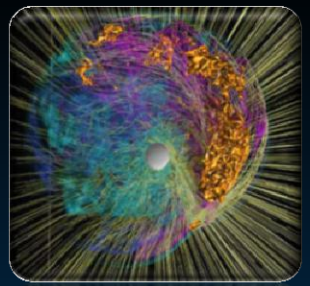
Assume Exascale Computing at 20MW …

New Forms of Energy

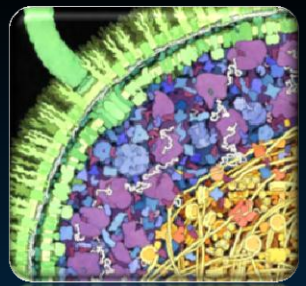


Ecological Sustainability

Space Exploration



Medical Innovation



And many others….

Data Center Sized Exascale System

Lower Volume
Higher Cost

20MW

Rack Sized Petascale System

"Mainstream"

20KW

Embedded Terascale System

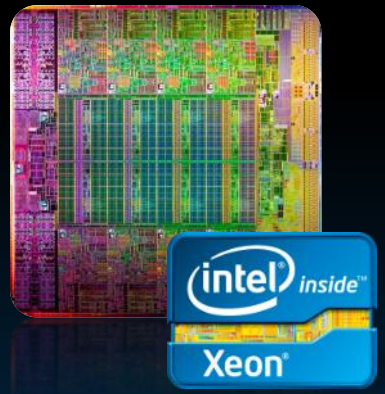
Higher Volume
Lower Cost

20W

For illustration and concept only.

HPC:
The Path to Exascale

Processors
Intel® Xeon® Processor



Co-Processor
Intel® Many Integrated Core

Fabrics

Software

HPC:
The Path to Exascale (cont.)

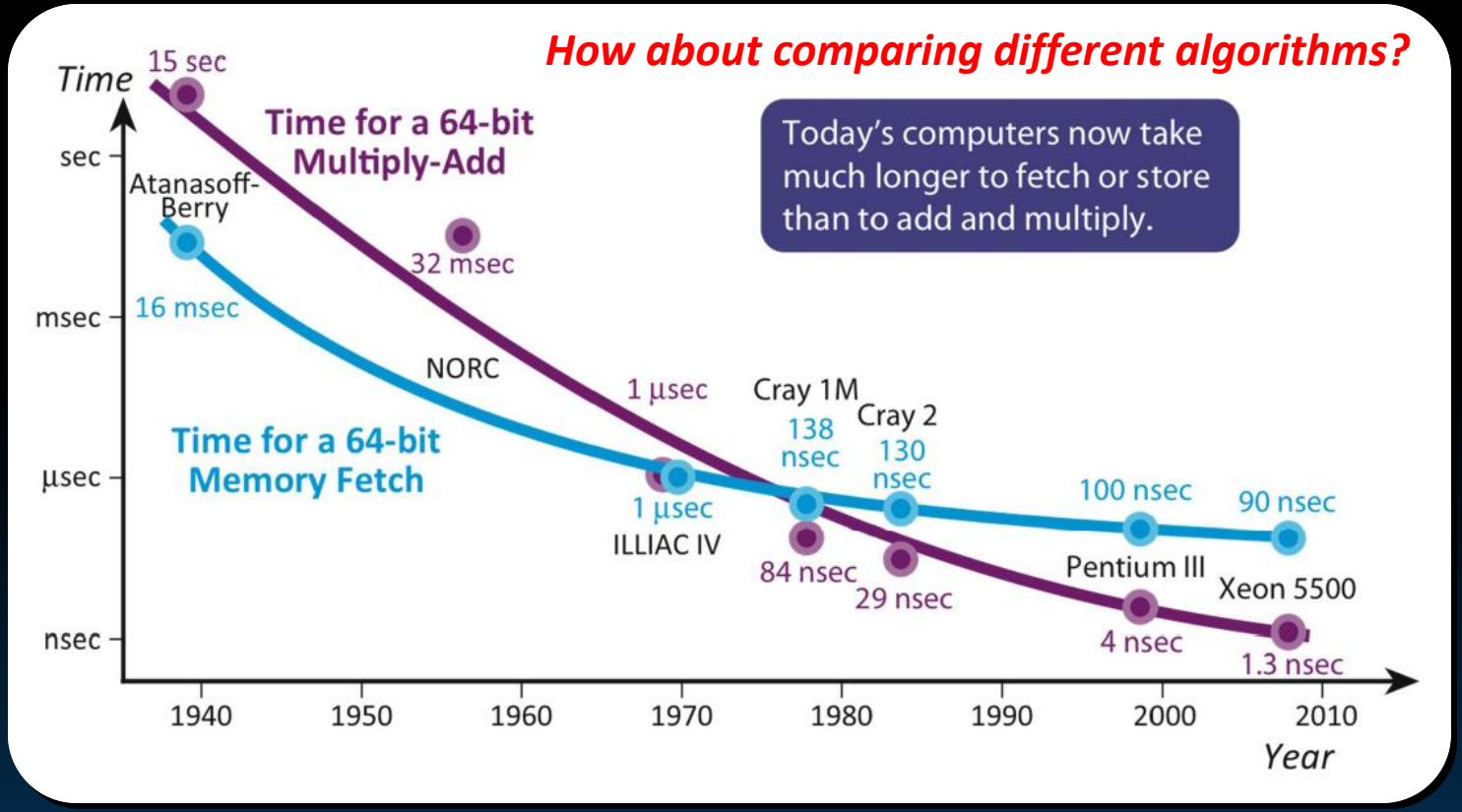
Memory & Storage

Networking

Reliability & Resiliency

Power Management

"The Memory Wall"

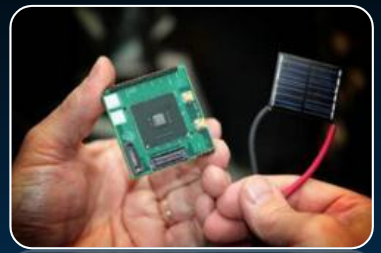


“ExtremeScale”

August 6, 2010

The Defense Advanced Research Projects Agency (DARPA*) has initiated the Ubiquitous High Performance Computing (UHPC) program to create an innovative, revolutionary new generation of computing systems that overcomes the limitations of current evolutionary approach. The goal of DARPA’s UHPC program is to re-invent computing. It plans to develop radically new computer architectures and programming models that are **100 to 1,000 times more energy efficient, with higher performance, and that are easier to program than current systems.**

Prototype UHPC systems are expected to be complete by **2018**. UHPC systems will need to deliver a petaflop of High Performance Linpack (HPL) in a single cabinet and achieve an energy efficiency of at least **50 gigaflops/watt**.

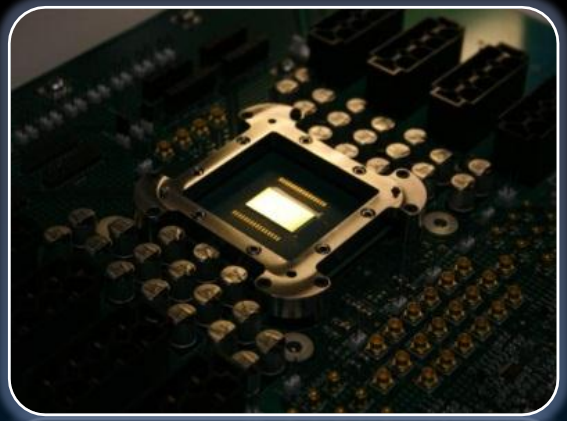


Intel [and others] and the Defense Advanced Research Projects Agency (DARPA) have entered into a collaborative research agreement to investigate revolutionary hardware and software technologies for extreme-scale computing systems.

e.g. using Near Threshold Voltage research IA processor (IDF Fall 2011)

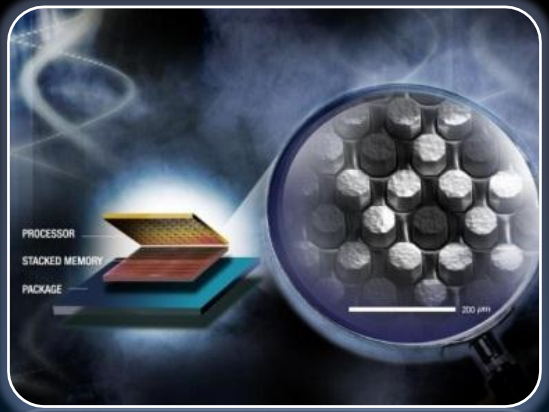
Intel TeraScale Research Areas

MANY-CORE COMPUTING



Teraflops
of computing power

3D STACKED MEMORY



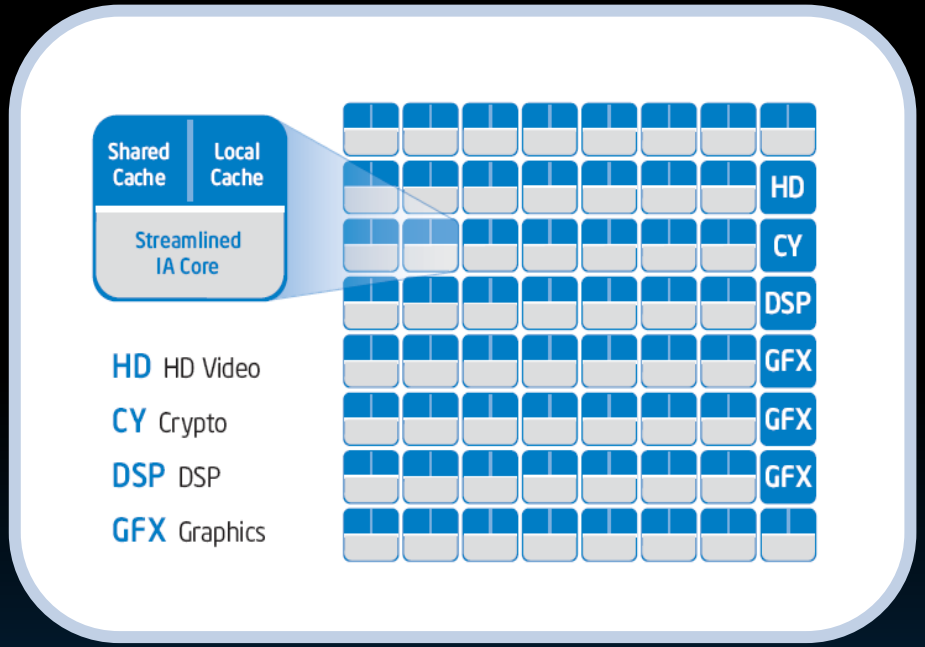
Terabytes
of memory bandwidth

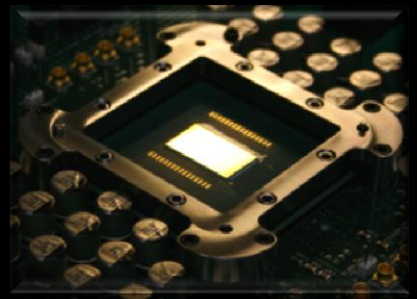
SILICON PHOTONICS

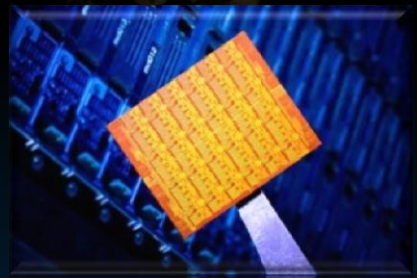
Terabits
of I/O throughput

Future vision, does not represent real products.

Many-Core Chip Research



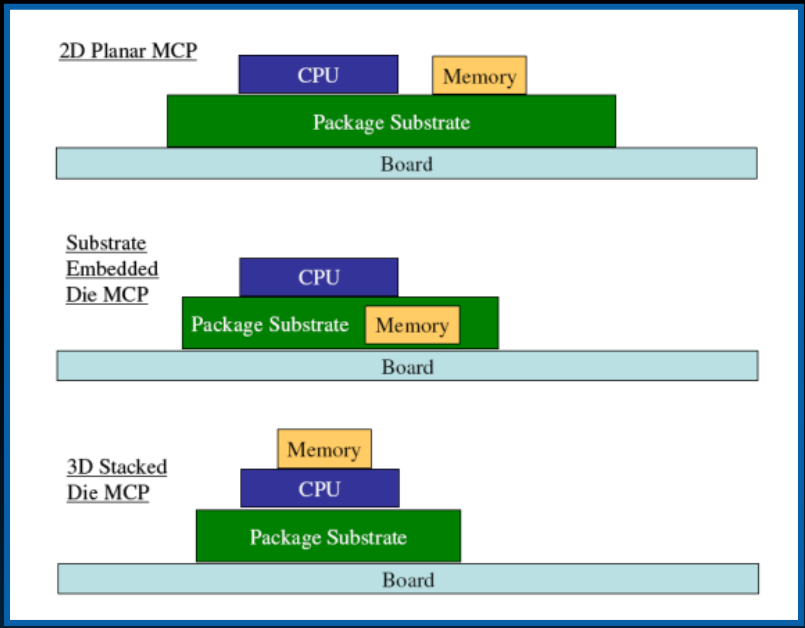

"Polaris": Experimental Research Test Chip

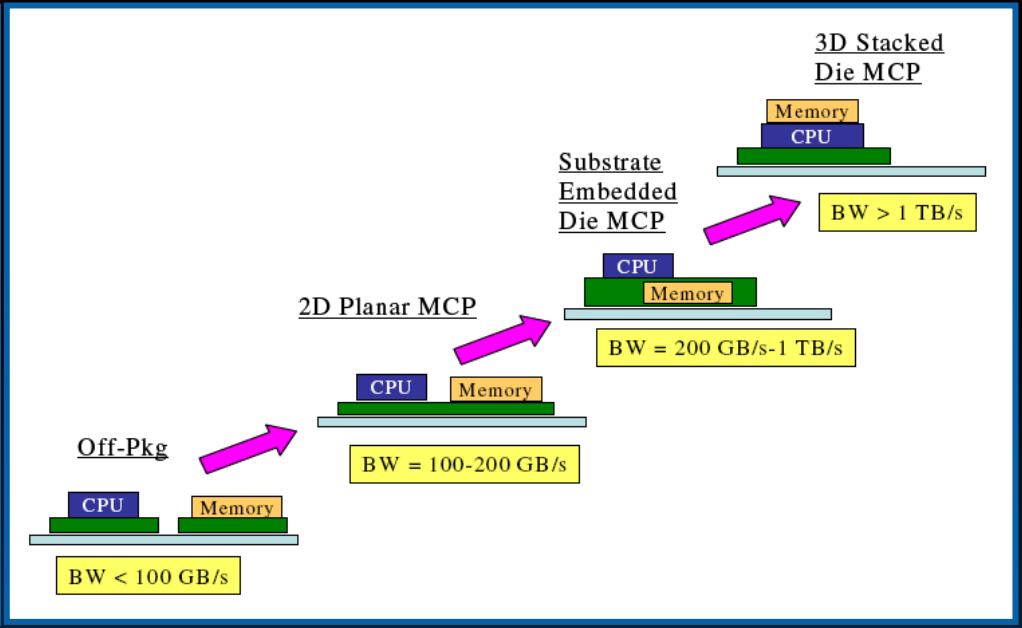

"SCC": Experimental Research Test Chip

Future tera-scale chips could use an array of tens to hundreds of cores with reconfigurable caches, as well as special-purpose hardware accelerators utilizing a scalable on-die interconnect fabric.

Potential future options, no indication of
actual product or development, subject to change without notice.

Memory and CPU Package Architectures for addressing Bandwidth Challenges - Research



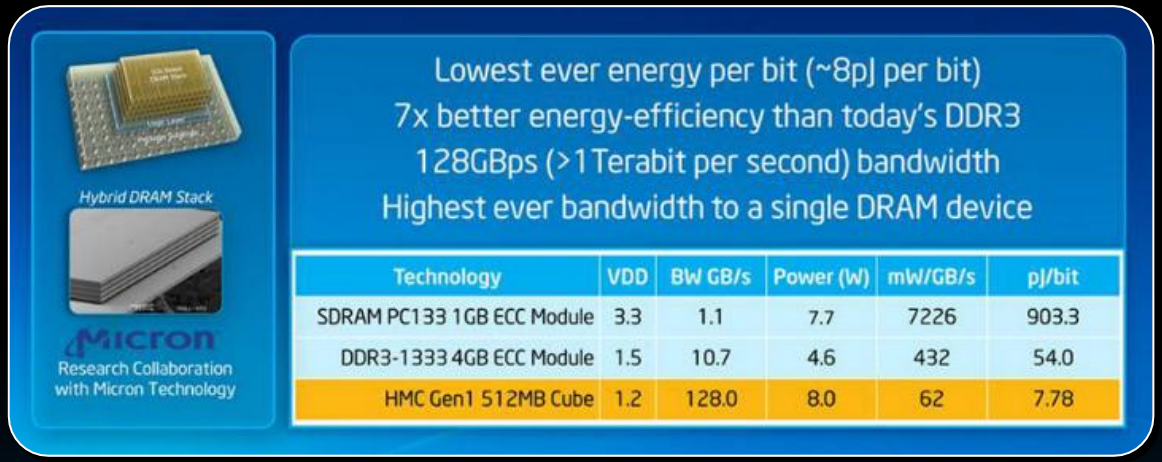


Package Technology to Address the Memory Bandwidth Challenge for Tera-scale Computing, Intel Technology Journal, Volume 11, Issue 3, 2007

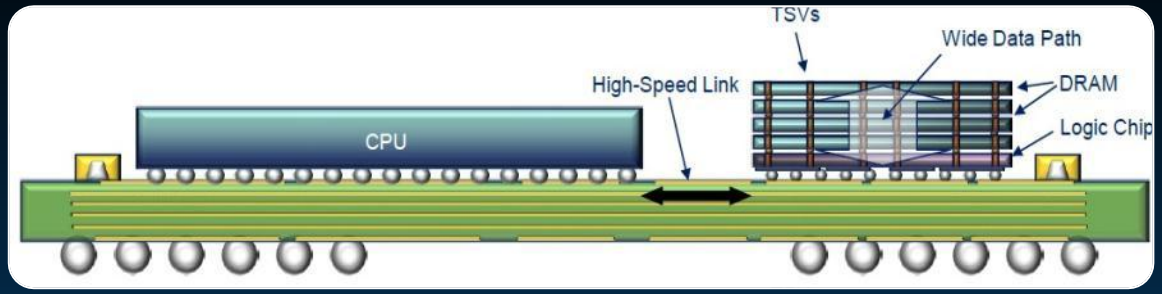
Potential future options, no indication of
actual product or development, subject to change without notice.

Hybrid Memory Cube: Experimental DRAM

Highest Performance and most Energy Efficient DRAM in the Industry



Technology	VDD	BW GB/s	Power (W)	mW/GB/s	pJ/bit
SDRAM PC133 1GB ECC Module	3.3	1.1	7.7	7226	903.3
DDR3-1333 4GB ECC Module	1.5	10.7	4.6	432	54.0
HMC Gen1 512MB Cube	1.2	128.0	8.0	62	7.78

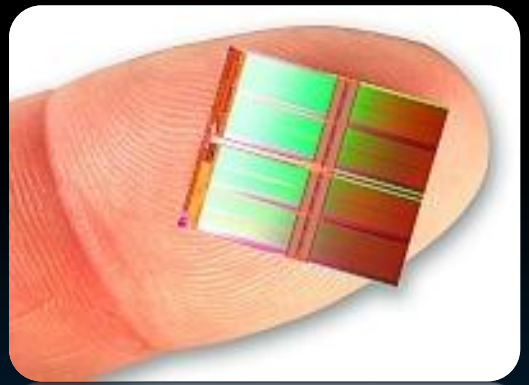


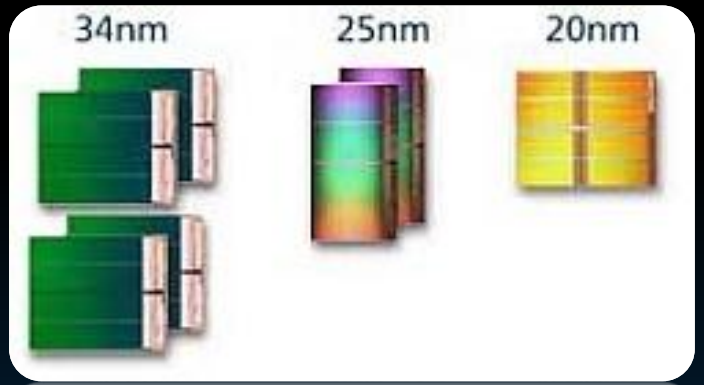
http://www.micron.com/innovations/hmc.html

Intel and Micron's Joint-Development Venture

IM Flash Technologies (IMFT)

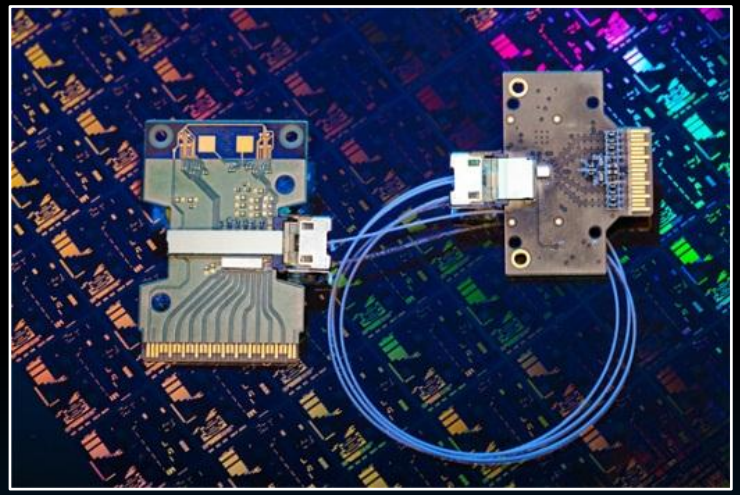
128 Gbit (16GB) NAND in 20nm





Pictures: Micron

Silicon Photonics Research



50Gbps Silicon Photonics Link
The transmit module (left) sends laser light from the silicon chip at the center of the green board, which then travels through optical fiber to the receiver module (right), where a second silicon chip detects the data on the laser and coverts it back into an electrical signal.

Terabits of I/O throughput potential

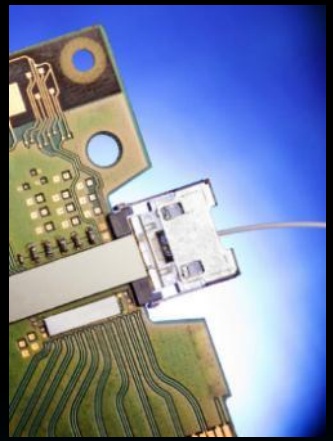
Controller chip for conversion from electricity to light and vice versa, using miniature lasers and photo detectors

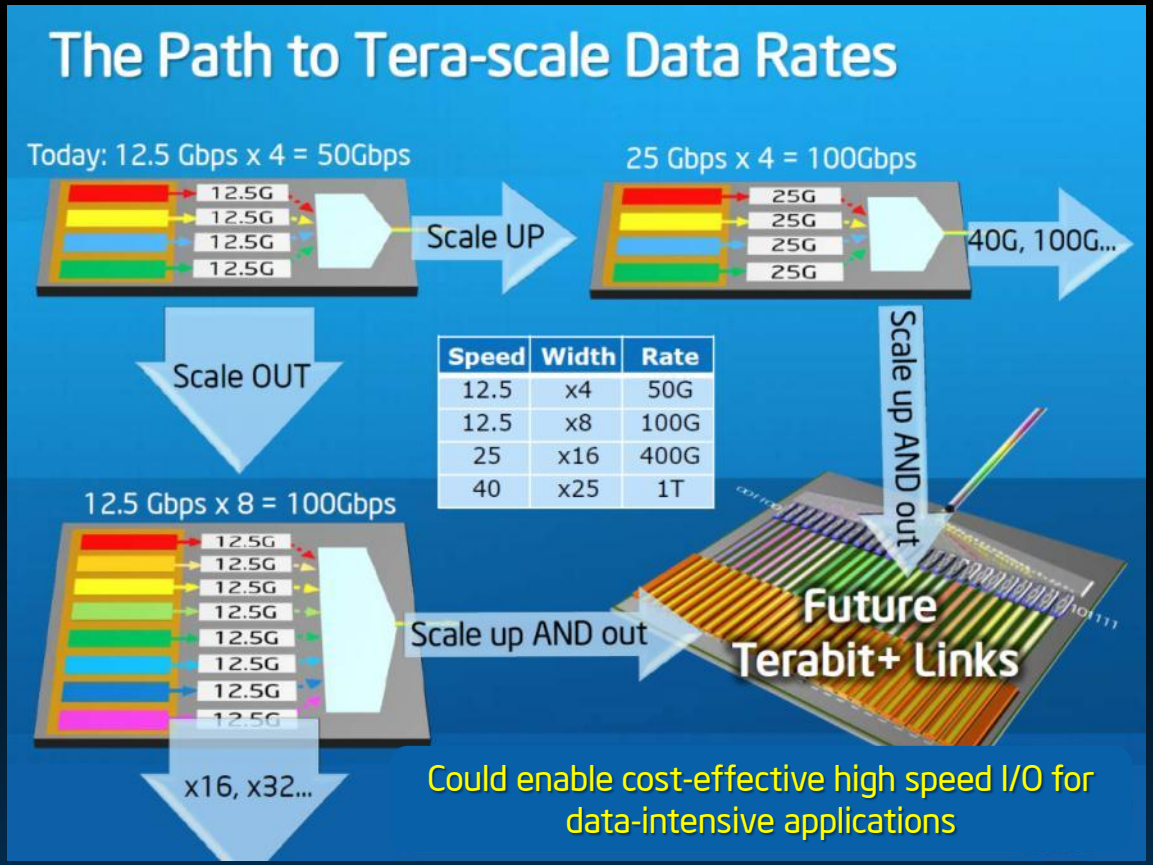
Chip-to-Chip
Board-to-Board
System-to-System

Provides substantial size, cost, and power savings over traditional optical communication solutions

Potential future options, no indication of
actual product or development, subject to change without notice.

Silicon Photonics





Speed	Width	Rate
12.5	x4	50G
12.5	x8	100G
25	x16	400G
40	x25	1T

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Access innovations … *in the formative stages*

Active Projects

Designing New Capabilities

- Adobe* Premiere® Pro/Premiere® Elements Encoder plug-in using Intel® Media SDK and Intel® Quick Sync Video Technology **New!**
- Intel Advisor Lite Now Part of Intel® Parallel Studio
- Intel® Web APIs **New!**
- Intel® Energy Checker SDK **Rev 2.0 Release**
- Intel® SOA Expressway XSLT 2.0 Processor
- Smoke - Game Technology Demo **Rev 1.2 Released**
- Isolated Execution
- Intel® Direct Ethernet Transport
- Intel® Software Development Emulator

Creating Concurrent Code

- **New!** Intel® Concurrent Collections for C++ Rev 0.7 Released
- Intel® Array Building Blocks
- **New!** Intel® Benchmark Install and Test Tool (Intel® BITT) Tools
- **New!** Intel® Cilk Plus Software Development Kit
- Intel® Cilk++ Software Development Kit

Math Libraries

- Intel® Adaptive Spike-Based Solver

Performance Tuning

- Intel® Performance Bottleneck Analyzer **4.0.1 Update Released**
- Intel® Software Autotuning Tool **New!**
- Intel® Software Tuning Agent
- Intel® Architecture Code Analyzer
- Intel® Performance Tuning Utility **4.0 Update 5 Released**
- Intel® Platform Modeling with Machine Learning

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Modern programming practices and computer languages (like .NET) tend to dynamically create...

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Just a quick post to let people know that they can now try SOA Expressway directly themsel...

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The Open Web Application Security Project (OWASP) maintains and publishes an oingoing list...

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Affiloblueprint 3.0 Review and Bonus
Affiloblueprint 3. is the latest product by super affiliate and affiliate marketing vetera...

Voice recognition for faster programming
Voice recognition for faster programming

PTU vs Amplifier...
Hi,Excuse my ignorance but is there a relationship between the Performance Tuning Utility ...

Querries related to Alpha software
wat acctually is a alpha software. how can it be utilized

More...

“One last thing …”

A Very Simple Arithmetic Example

using IEEE 64-bit DP-F.P.

X_1	X_2	X_3	X_4	X_5	SUM(X_1:X_5)
1.00E+21	-1.00E+21	17	-10	130	137.00 ✔

Source: Ulrich Kulisch, *Computer Arithmetic and Validity,* de Gruyter Studies in Mathematics 33 (2008), p. 250

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1.00E+21	-1.00E+21	17	-10	130	137.00	✓

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1.00E+21	17	-10	130	-1.00E+21	0.00	✗ ✗
1.00E+21	-10	-1.00E+21	130	17	147.00	✗
1.00E+21	-1.00E+21	17	-10	130	137.00	✓

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1.00E+21	-1.00E+21	17	-10	130	137.00	✓
1.00E+21	17	130	-1.00E+21	-10	-10.00	✗✗✗

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1.00E+21	17	-1.00E+21	-10	130	120.00	✗
1.00E+21	-10	-1.00E+21	130	17	147.00	✗
1.00E+21	-1.00E+21	17	-10	130	137.00	✓
1.00E+21	17	130	-1.00E+21	-10	-10.00	✗✗✗

Source: Ulrich Kulisch, *Computer Arithmetic and Validity,* de Gruyter Studies in Mathematics 33 (2008), p. 250

"Results can be satisfactory, inaccurate or completely wrong. Neither the computation itself nor the computed result indicate which one of the three cases has occurred."

Thank You.