

The SuperCDMS FPGA Trigger

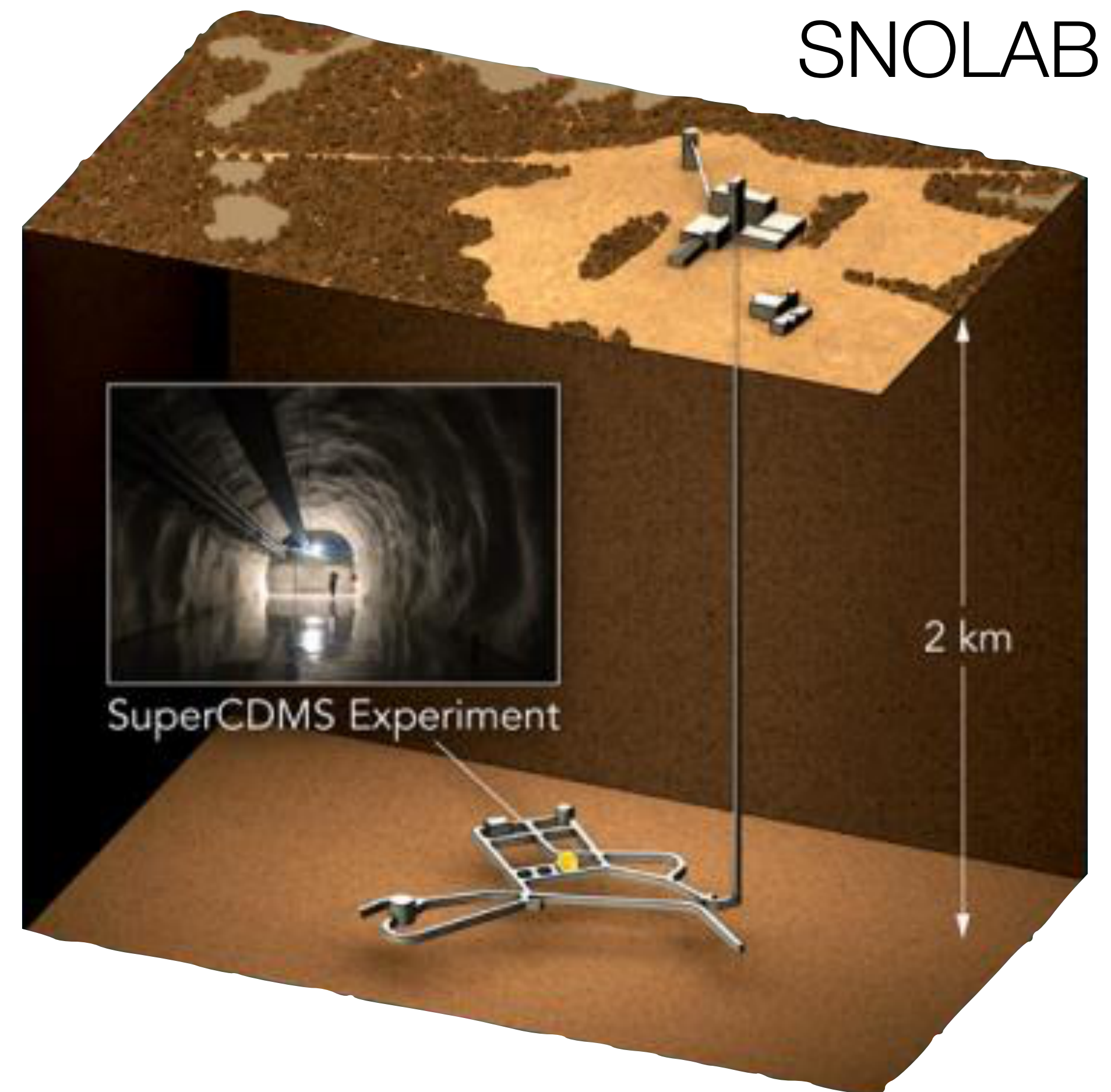


Hanno Meyer zu Theenhausen, Belina von Krosigk
University of Hamburg, Feb 18 '20

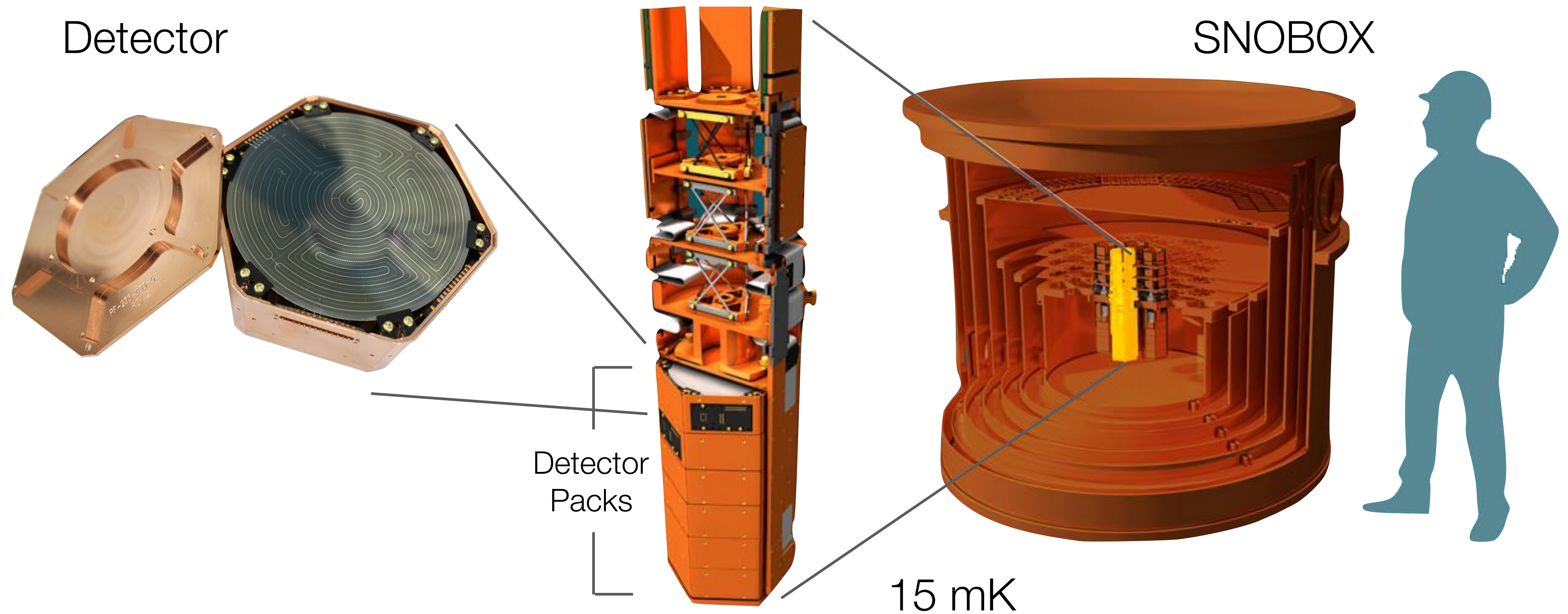


What is SuperCDMS?

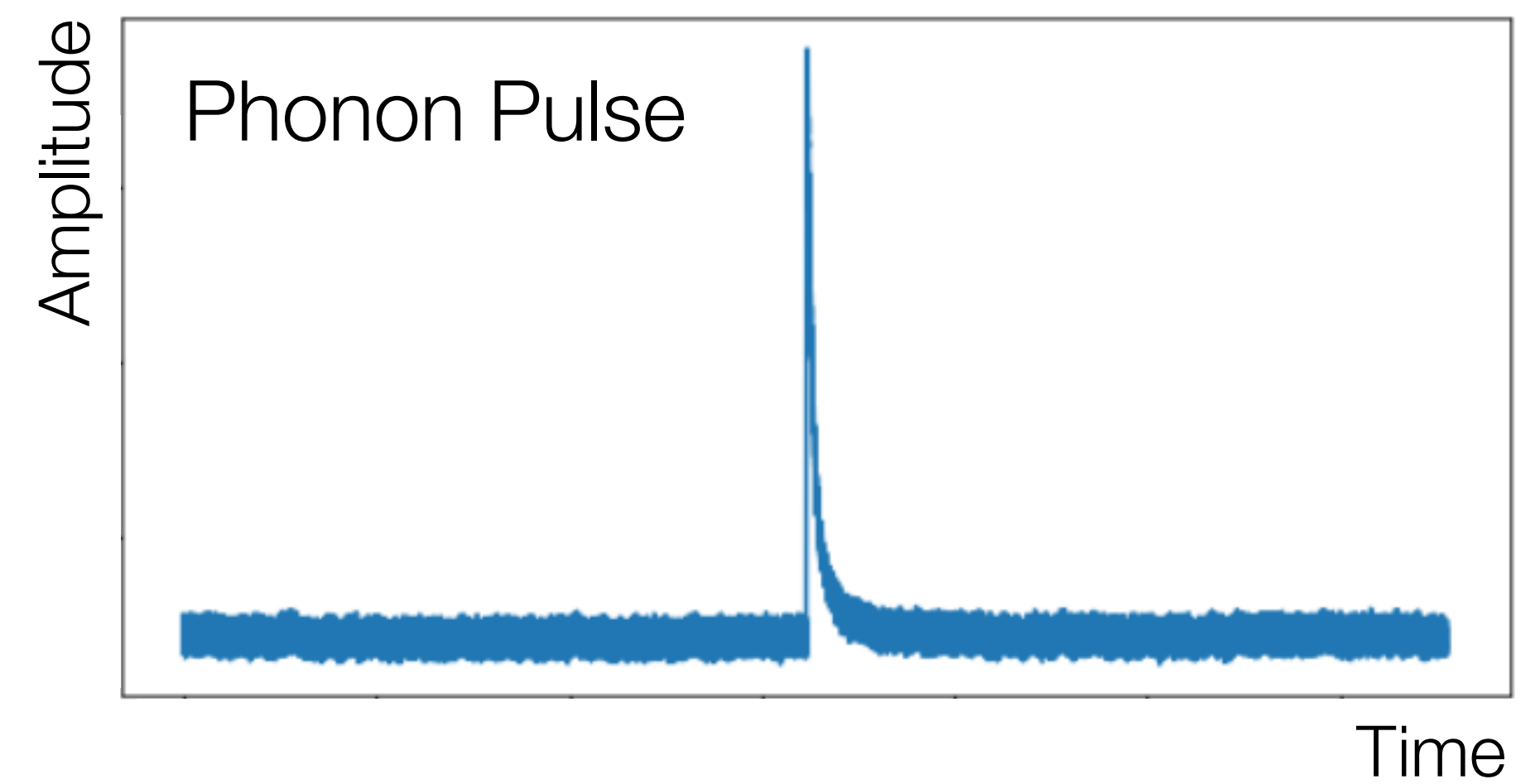
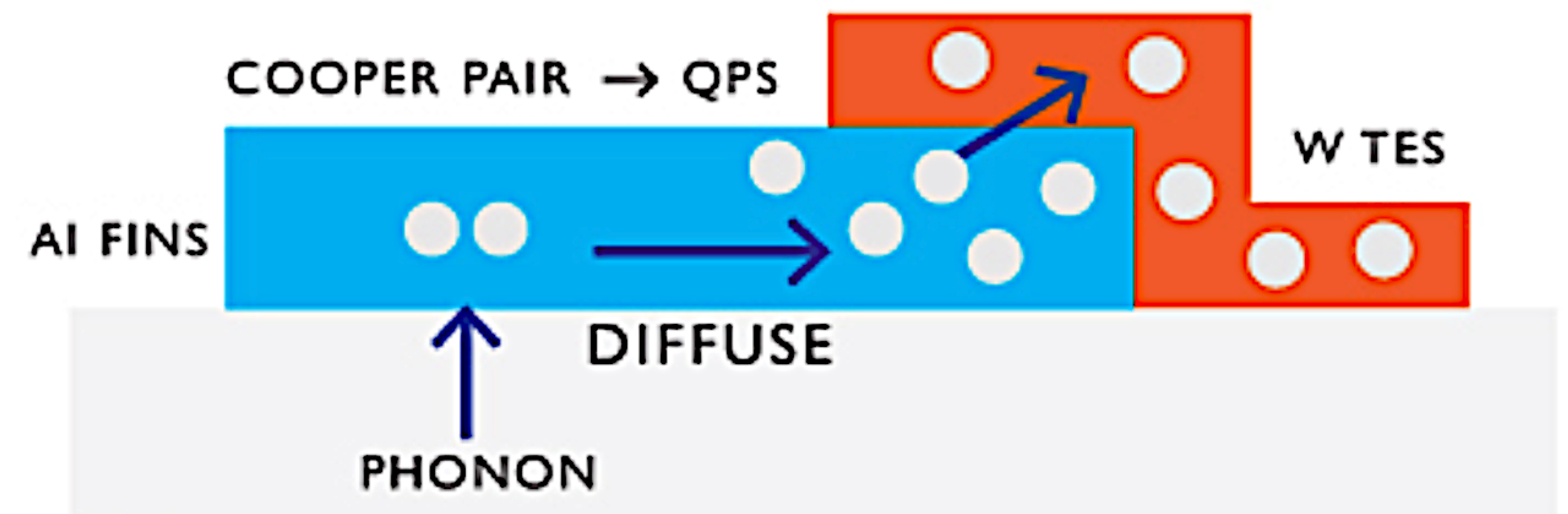
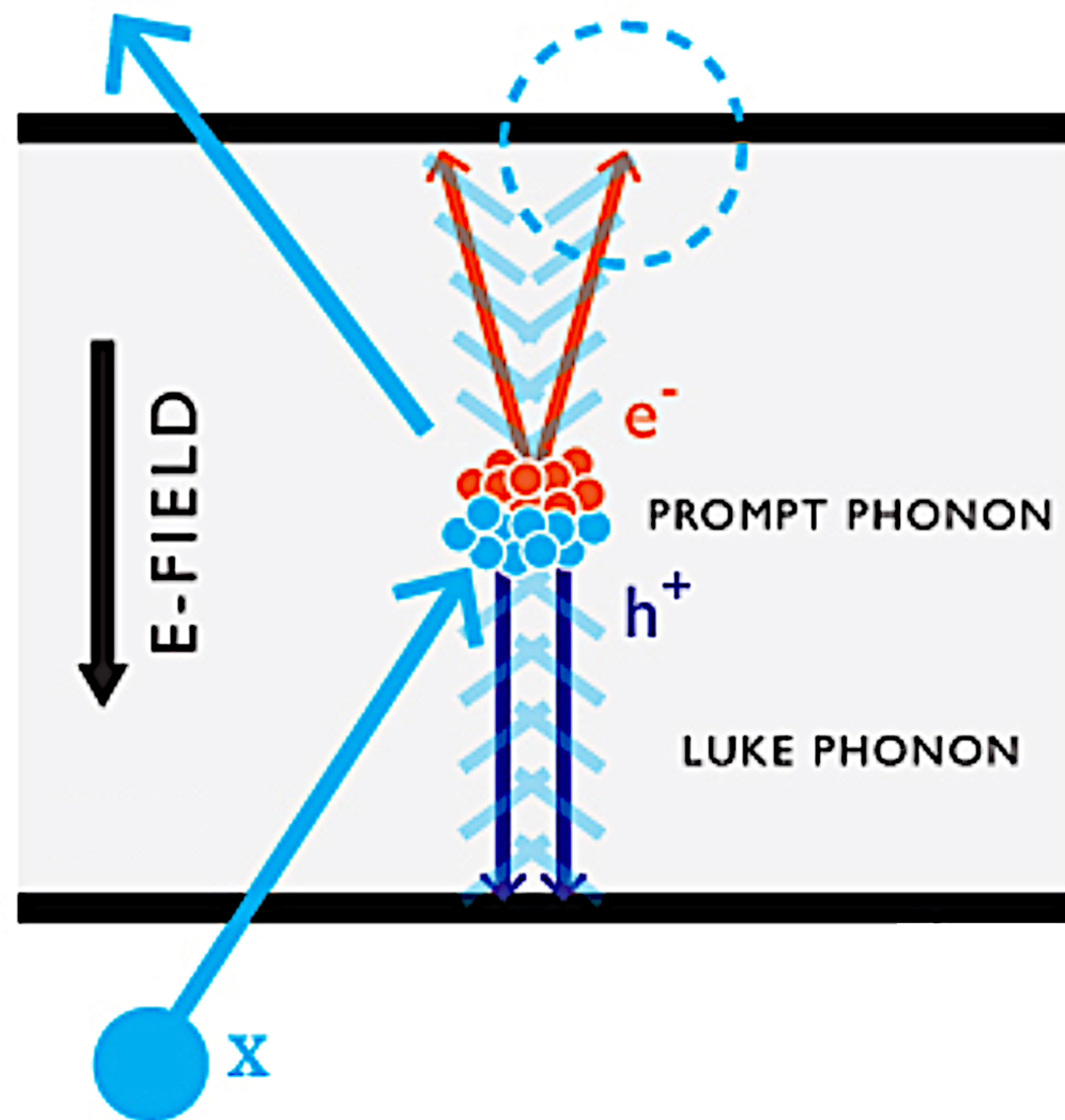
Cryogenic **D**ark **M**atter **S**earch



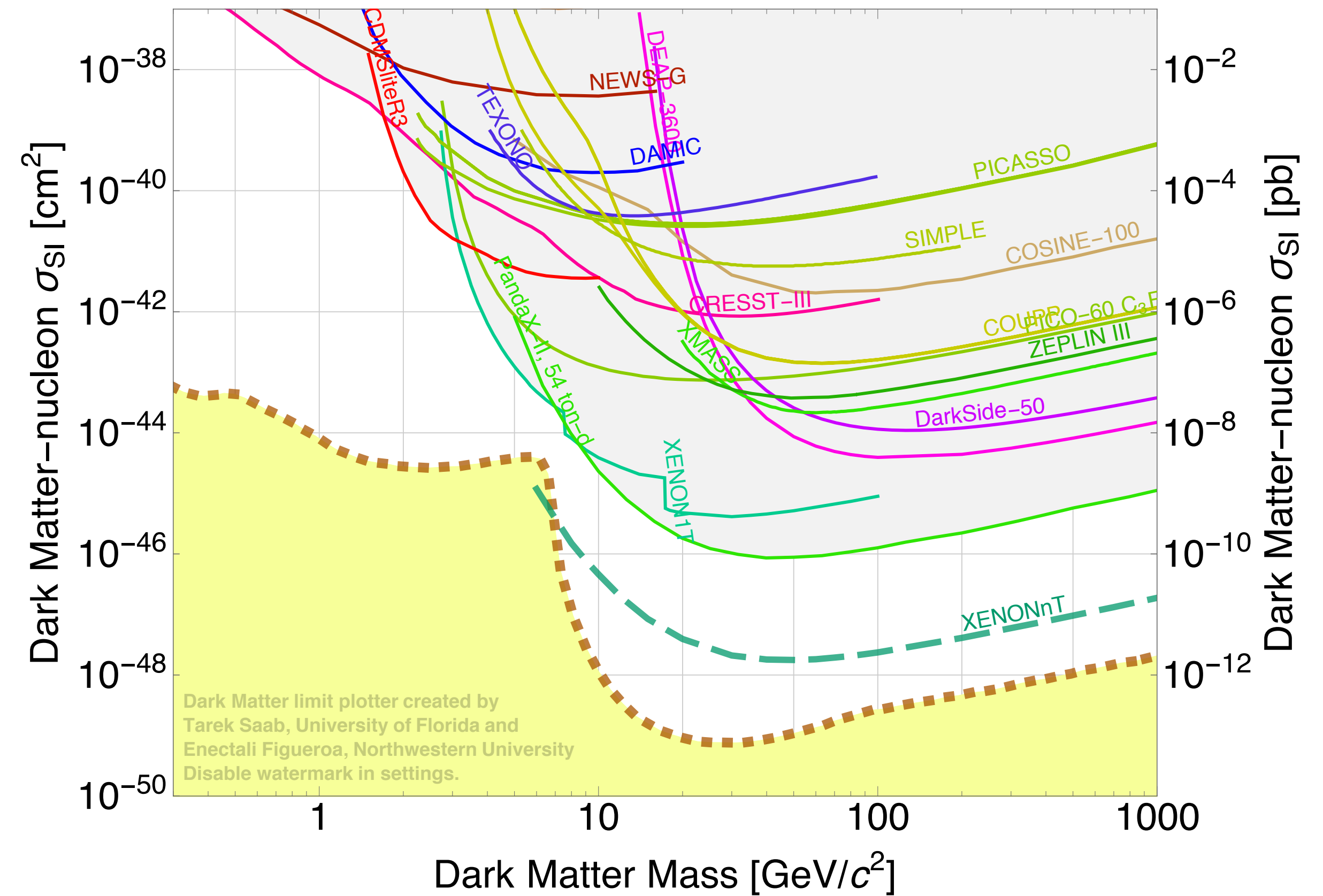
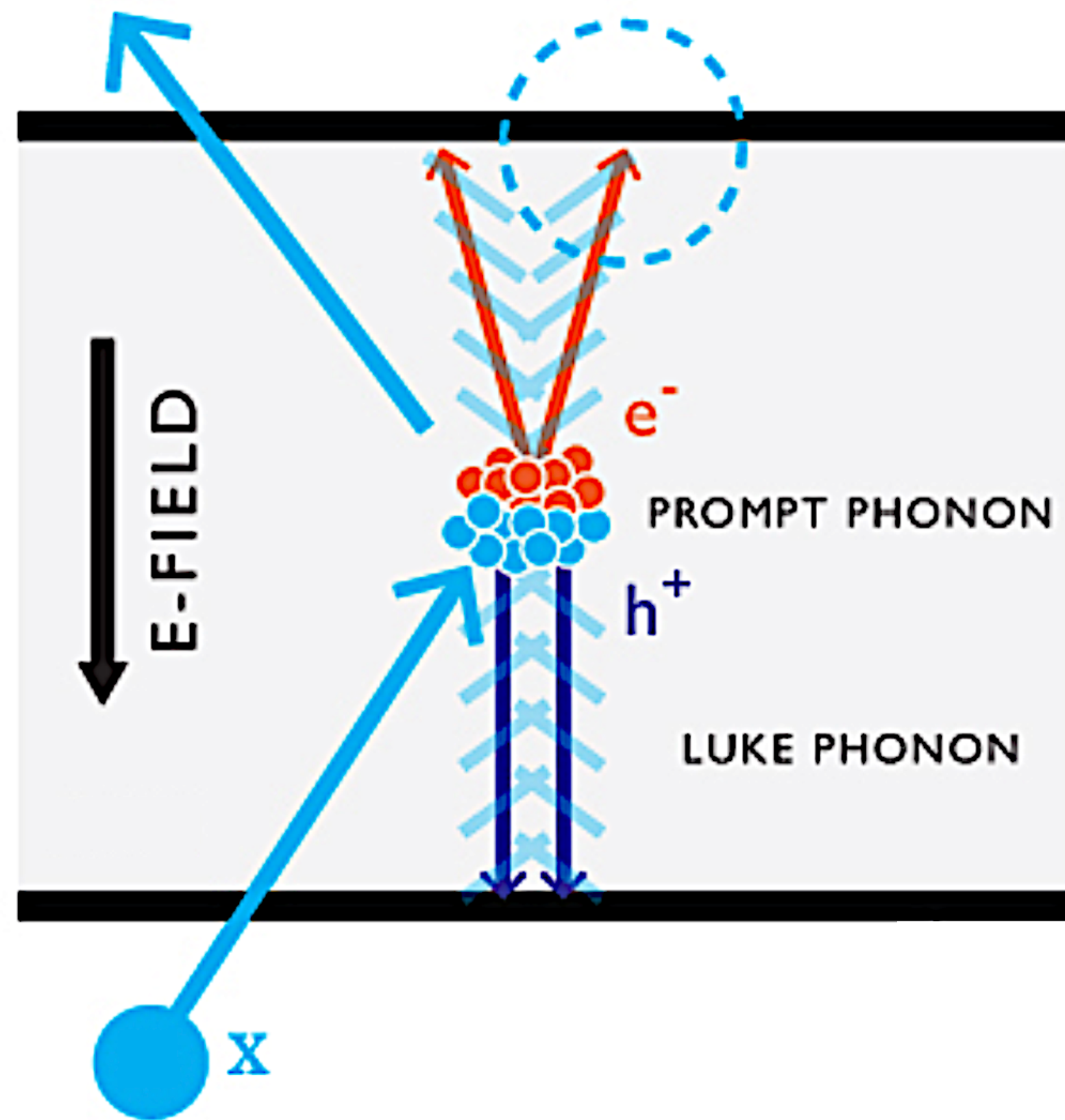
What is SuperCDMS?



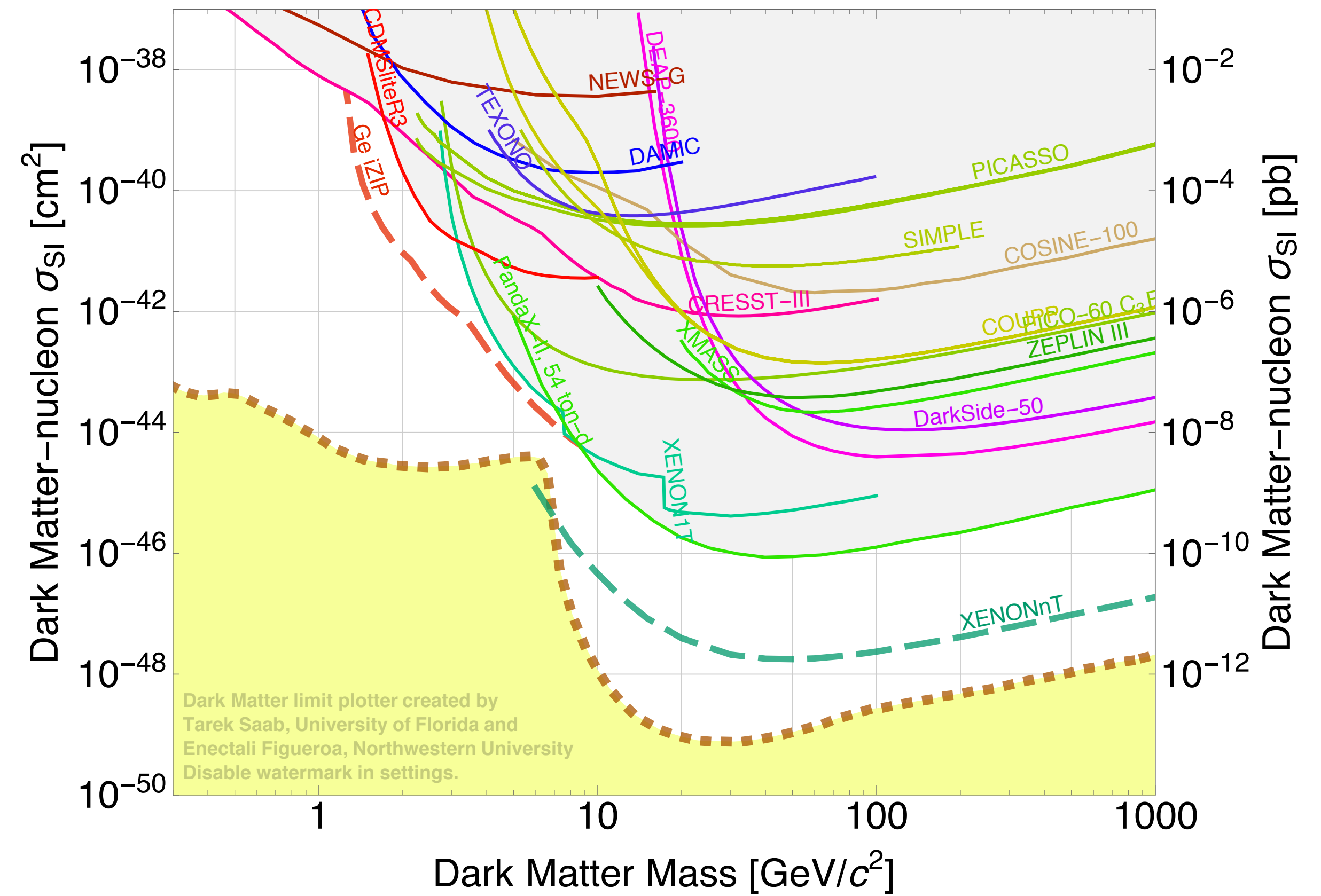
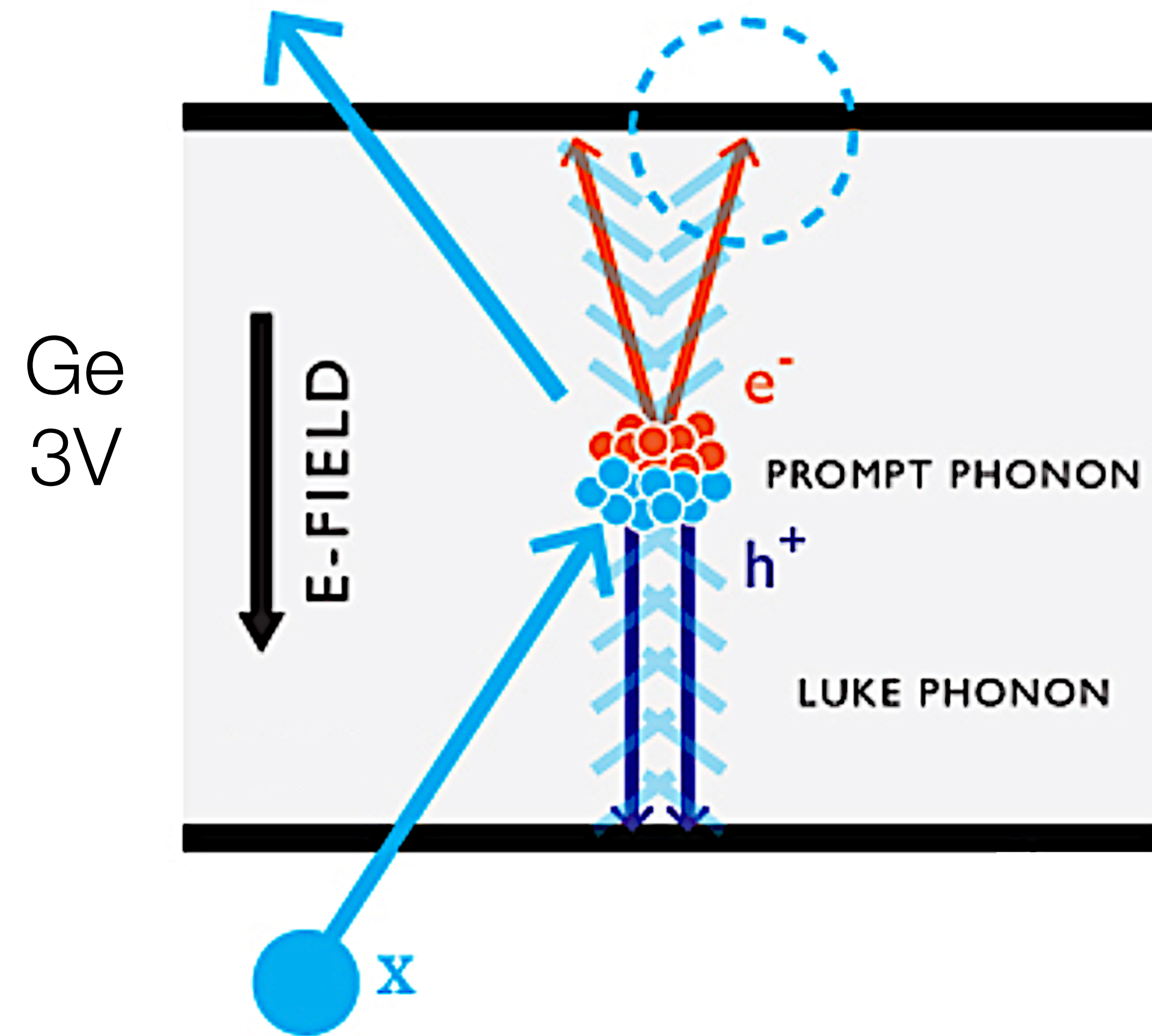
Detection Principle



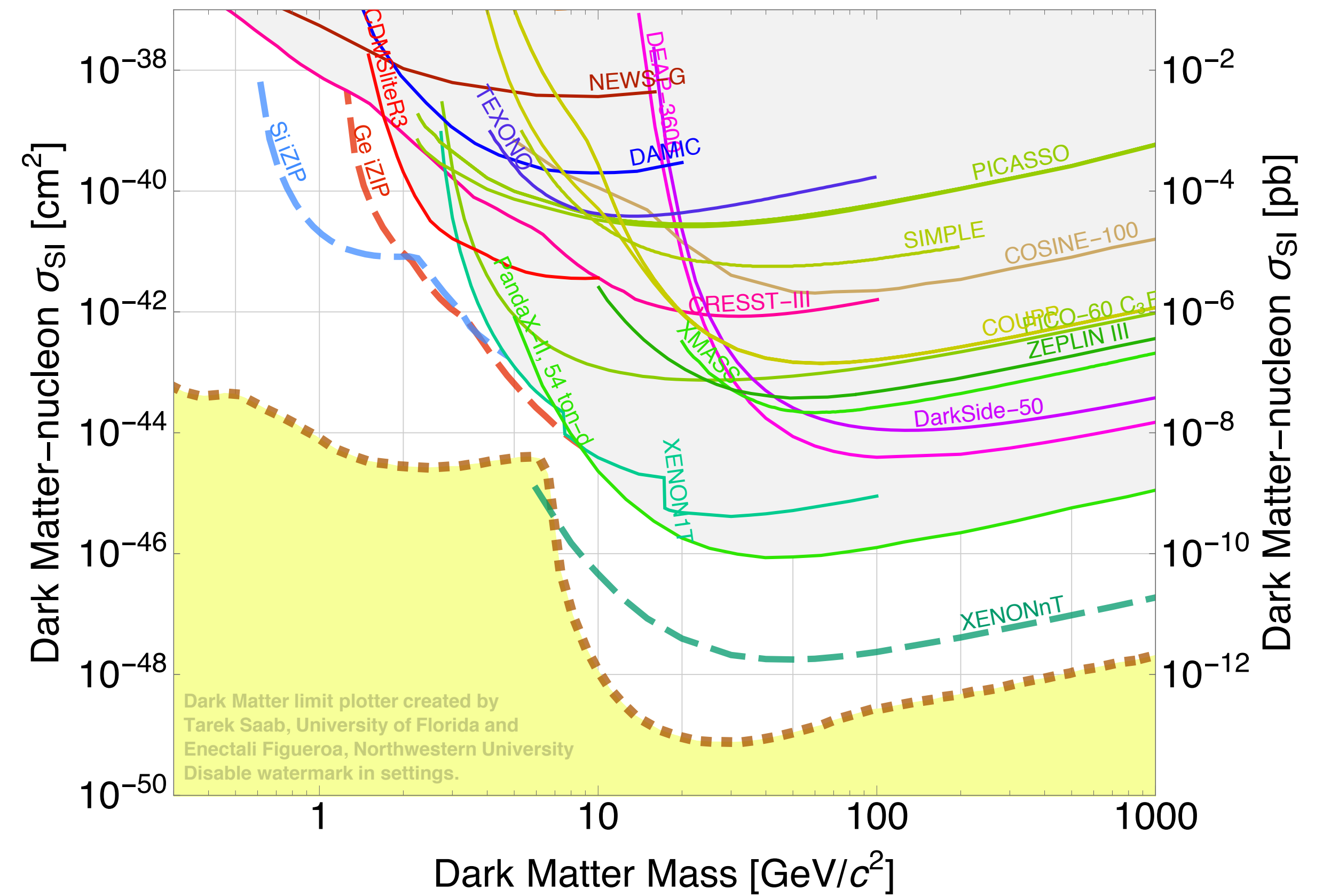
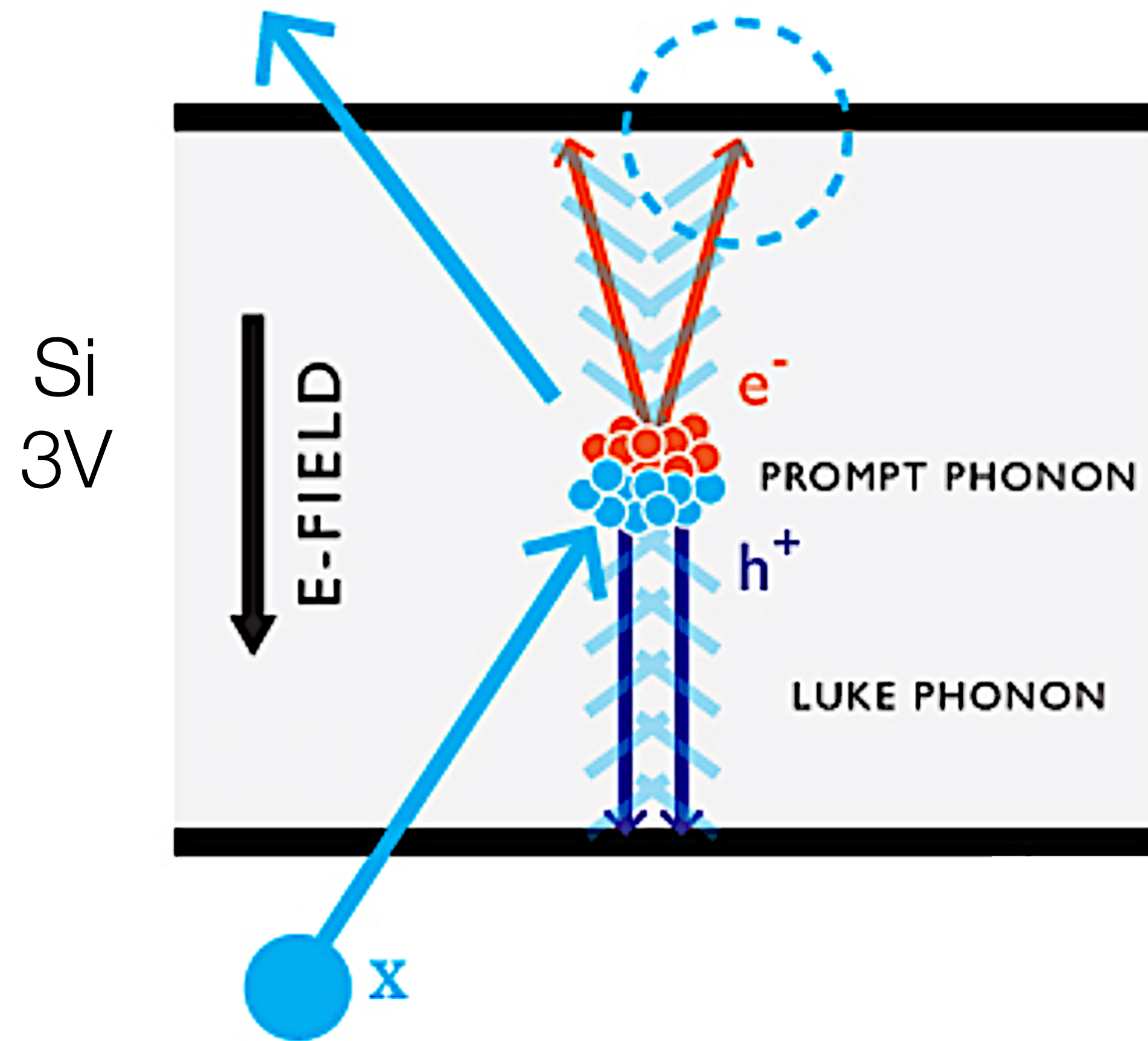
Detection Principle and Sensitivity



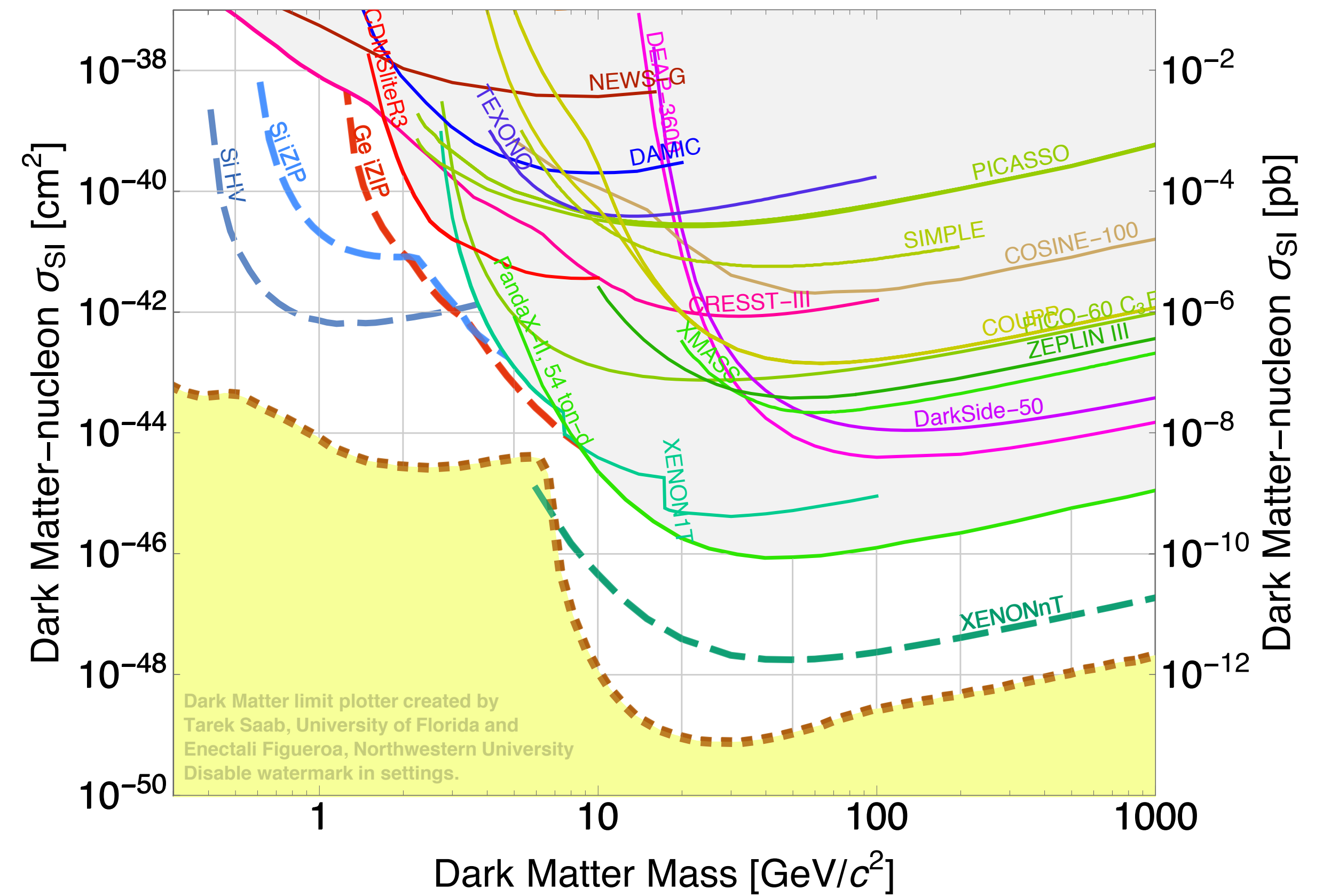
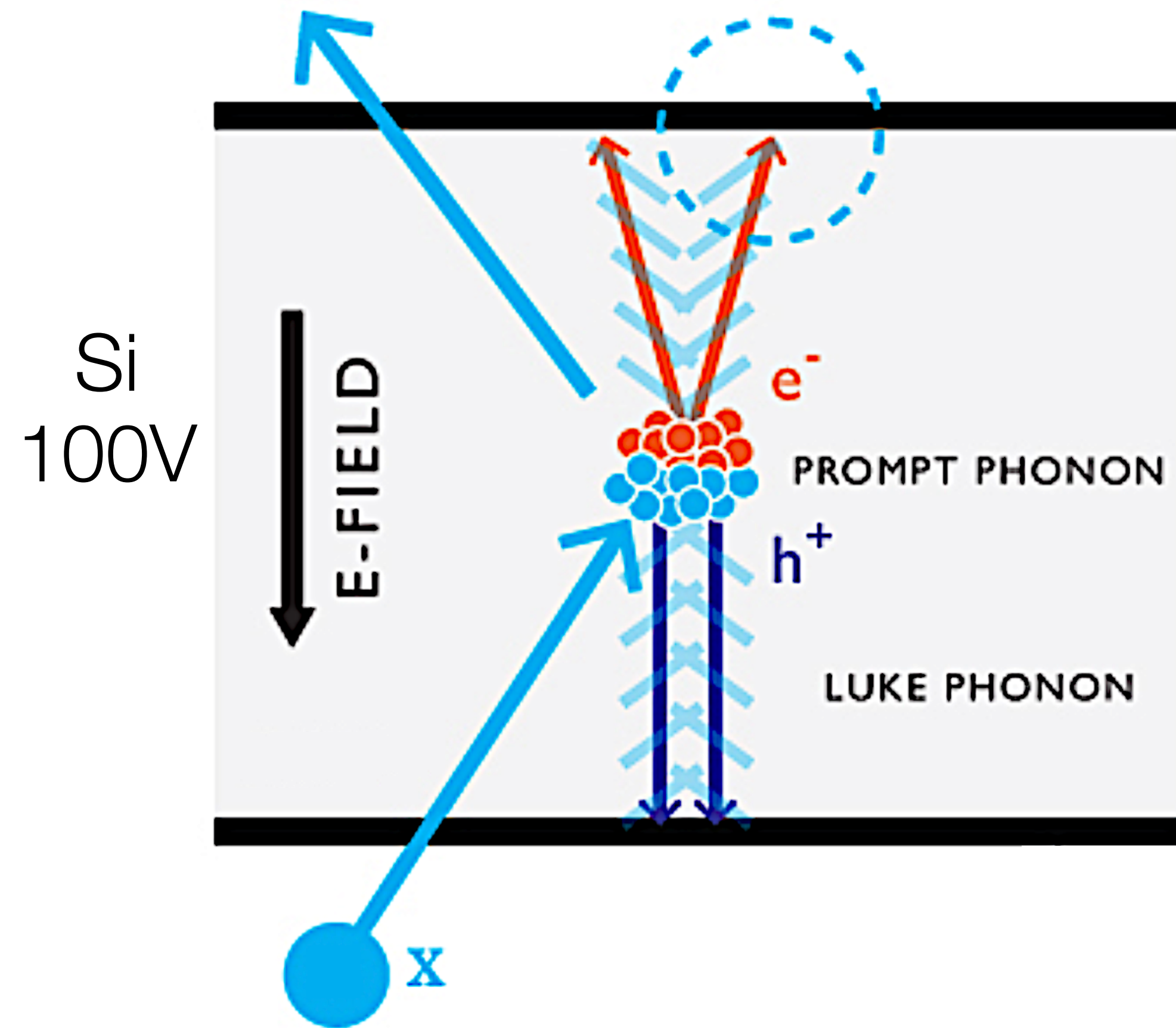
Detection Principle and Sensitivity



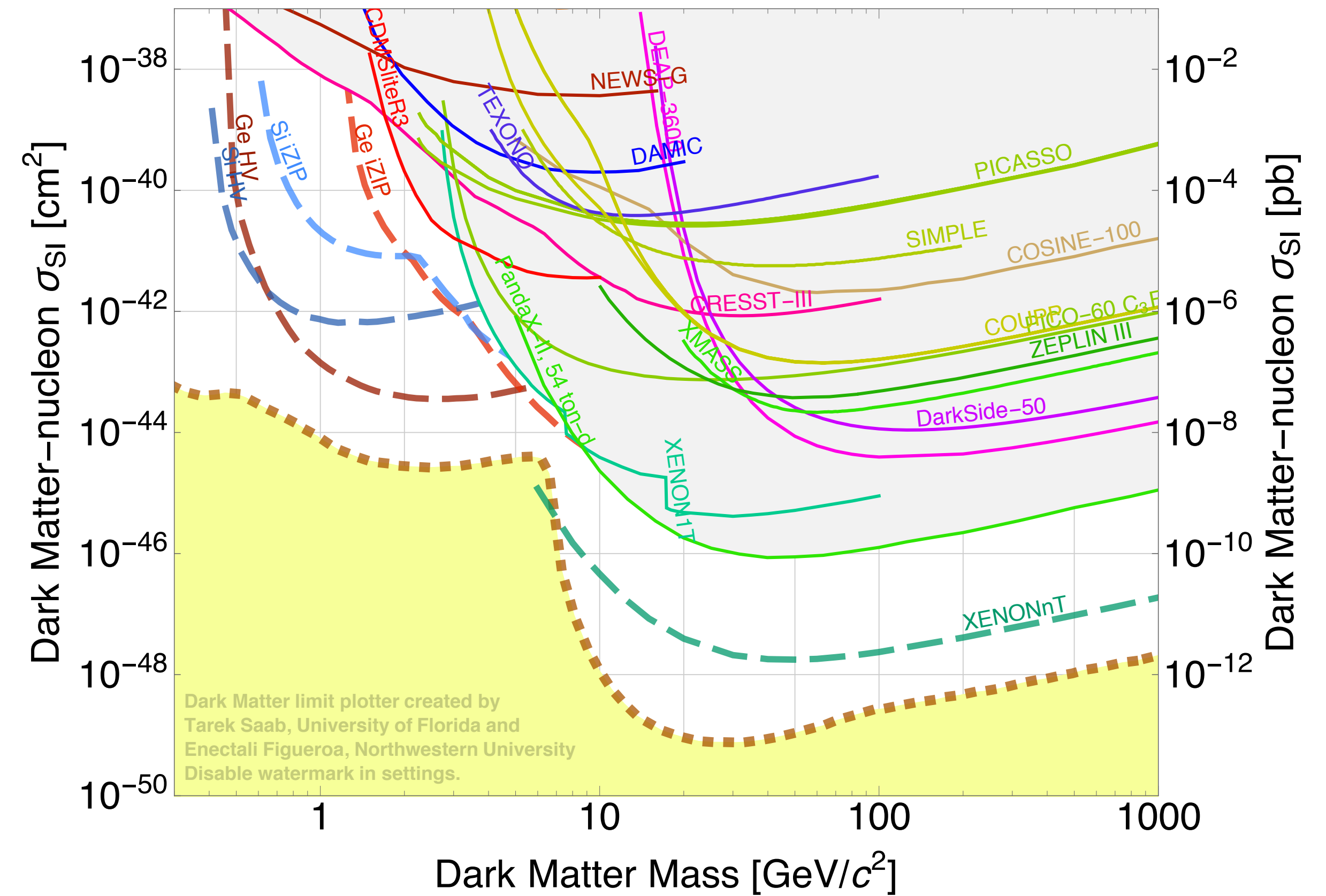
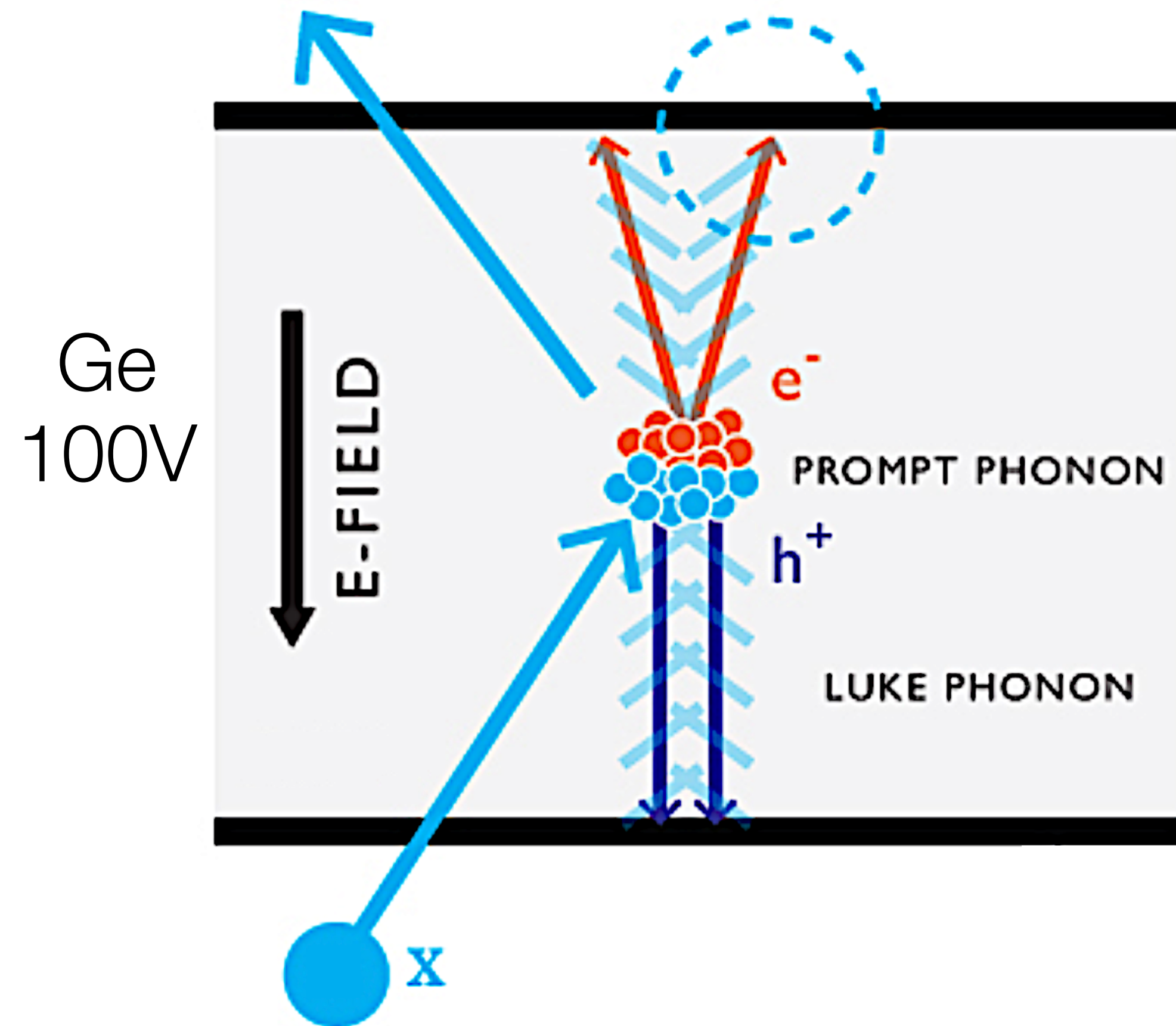
Detection Principle and Sensitivity



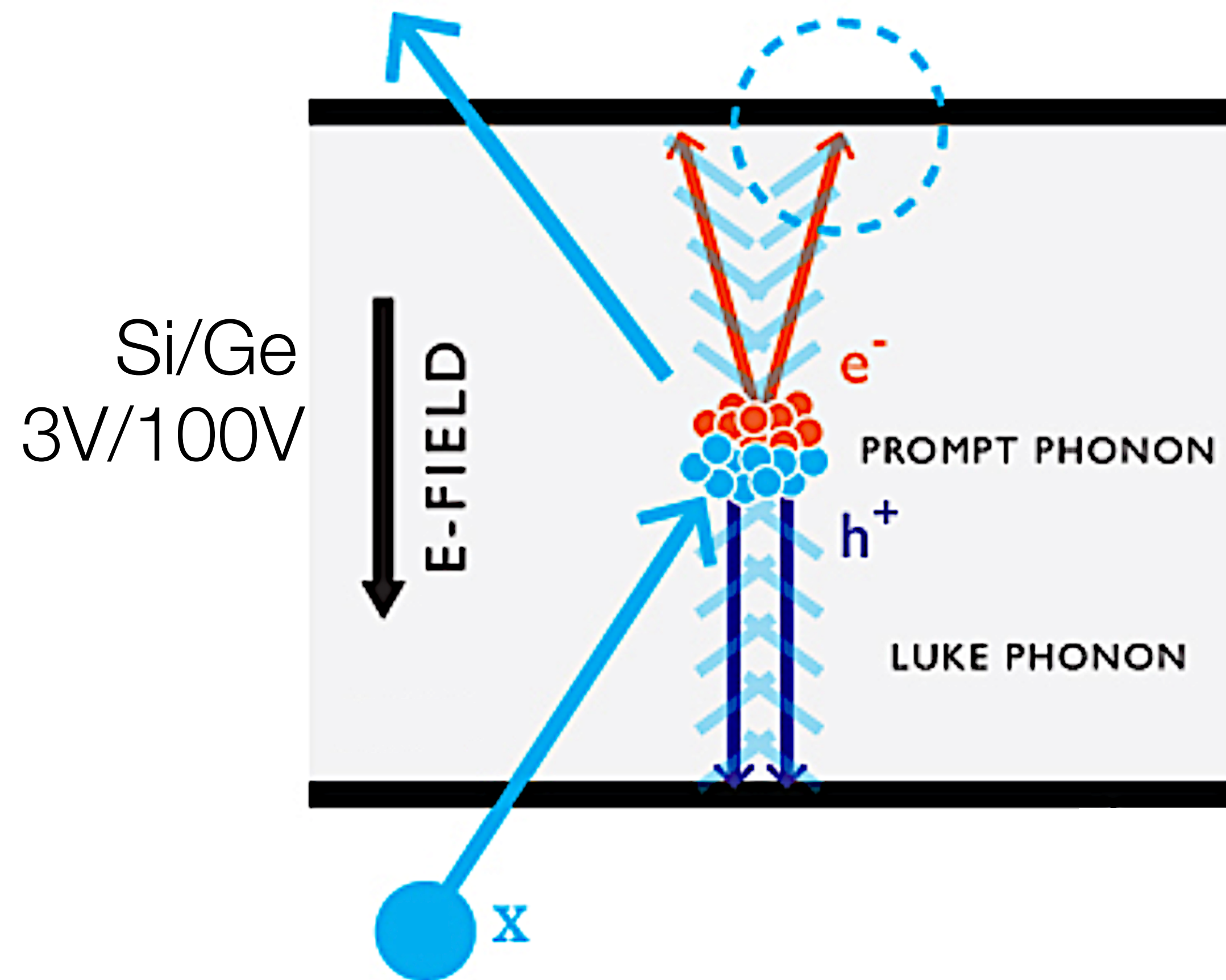
Detection Principle and Sensitivity



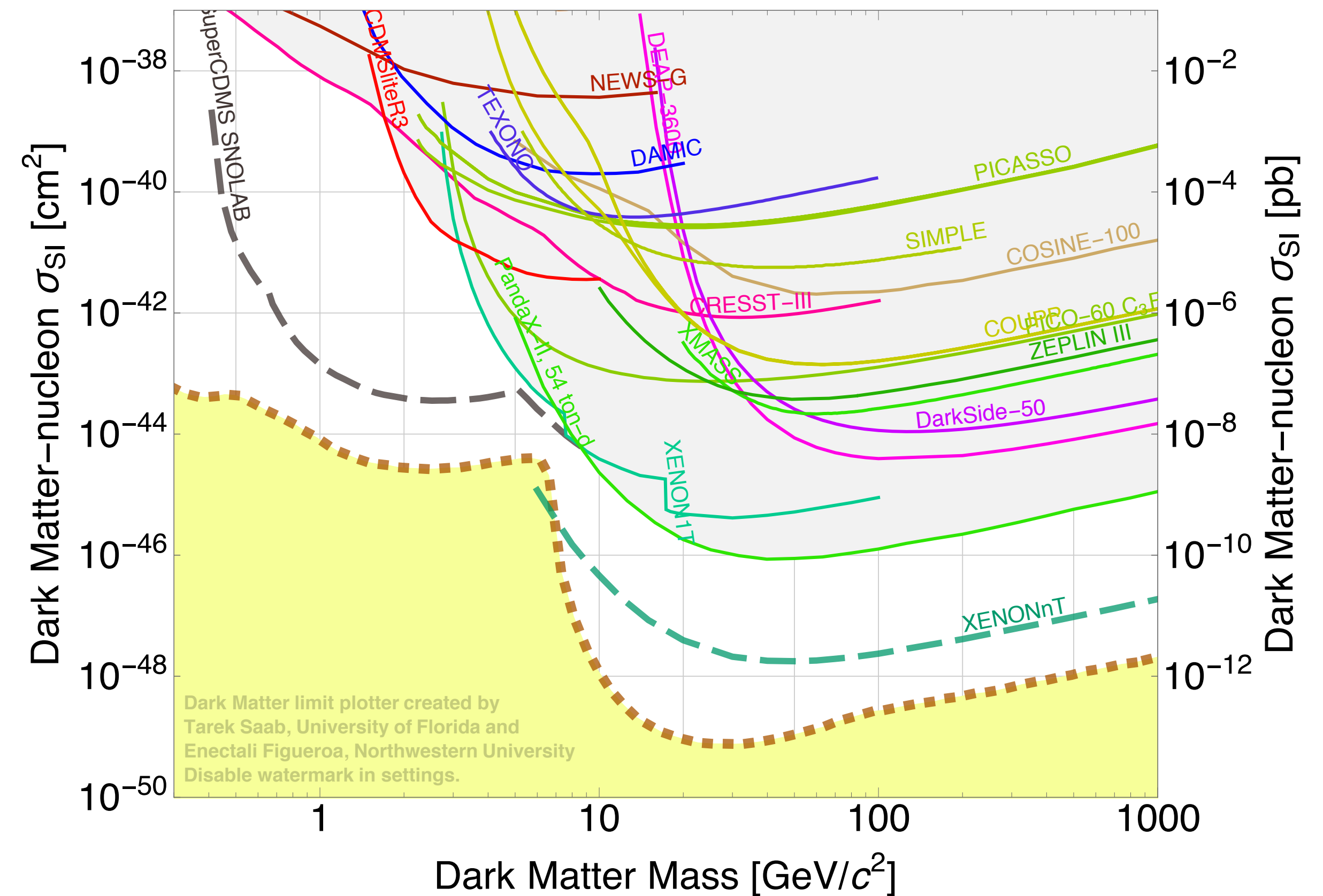
Detection Principle and Sensitivity



Detection Principle and Sensitivity

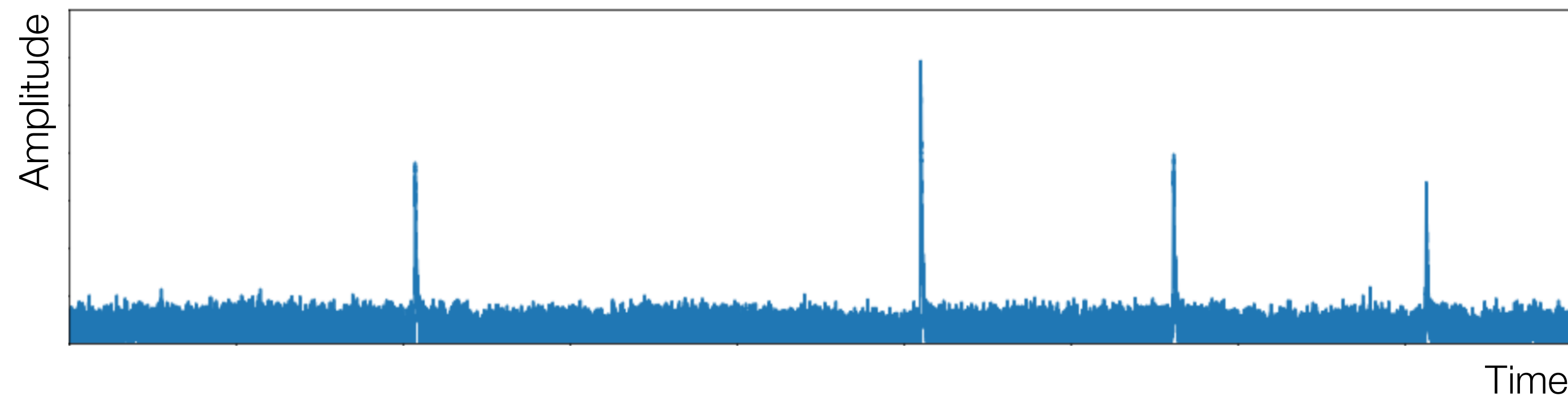


Low threshold experiment requires a good trigger



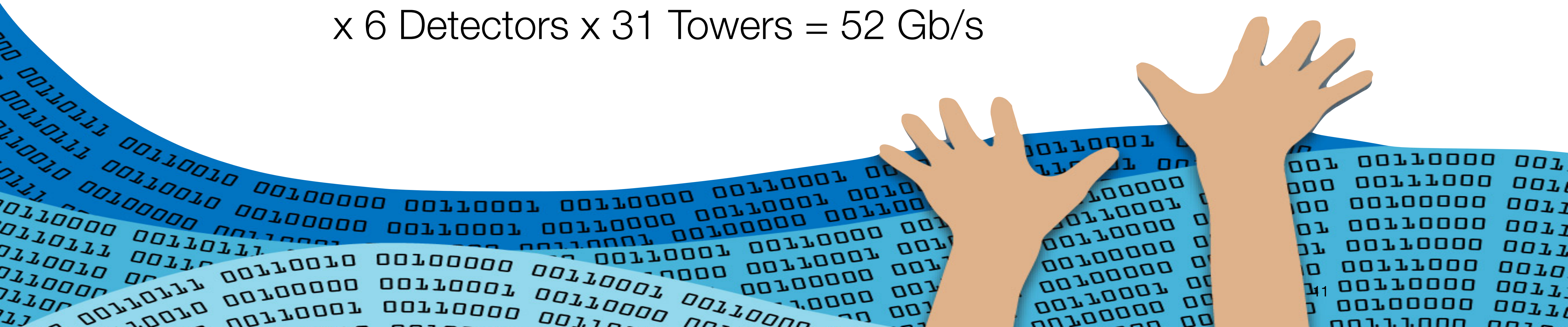
Why does SuperCDMS need a Trigger?

Assume: Continuous readout with up to 2.5 MHz sampling frequency



280 Mb/s per detector

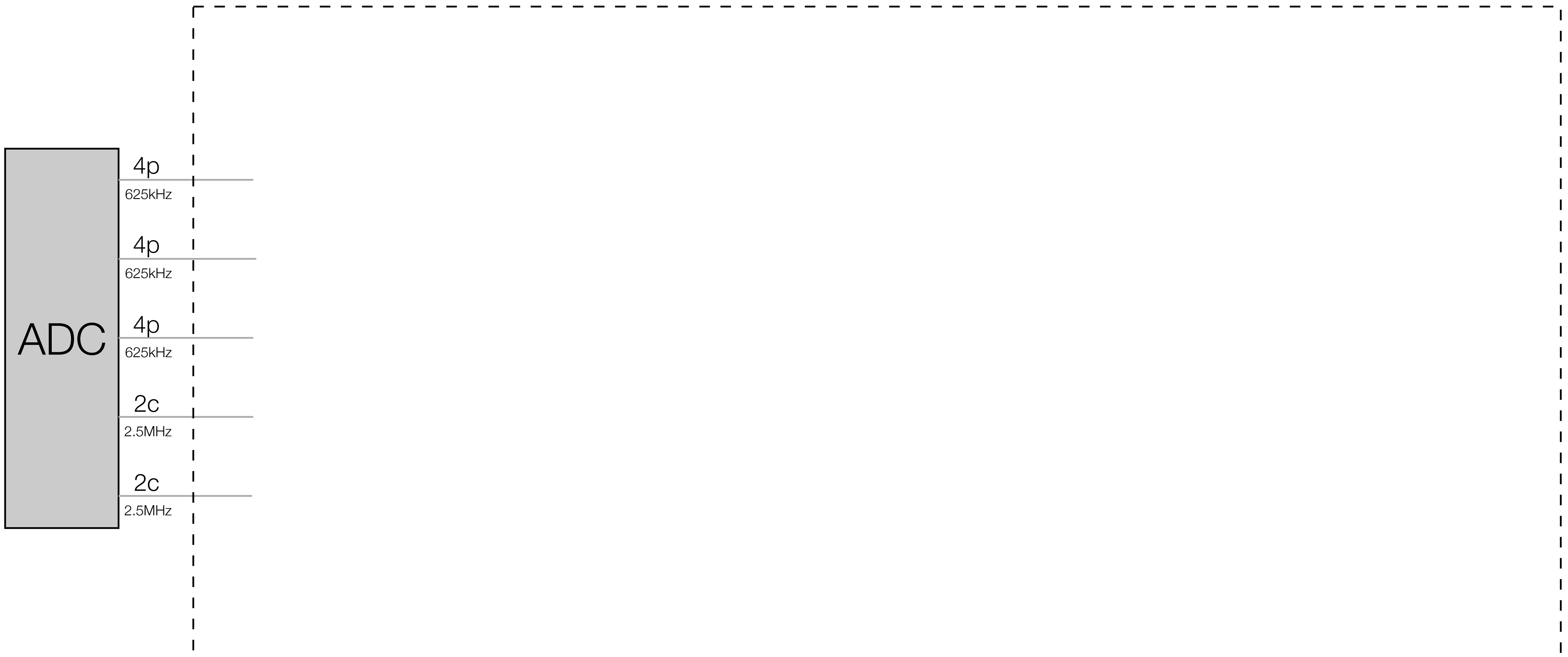
x 6 Detectors x 31 Towers = 52 Gb/s



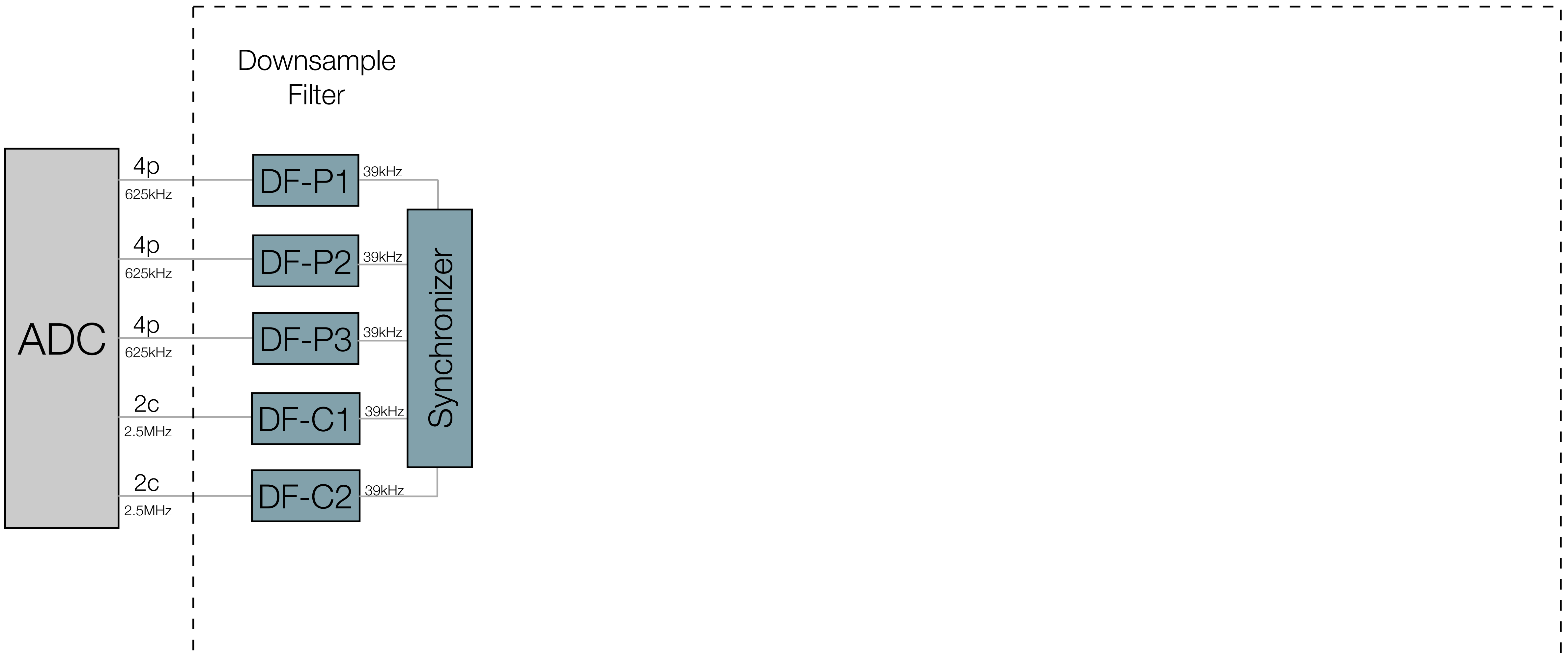
Detector Readout and Control Cards



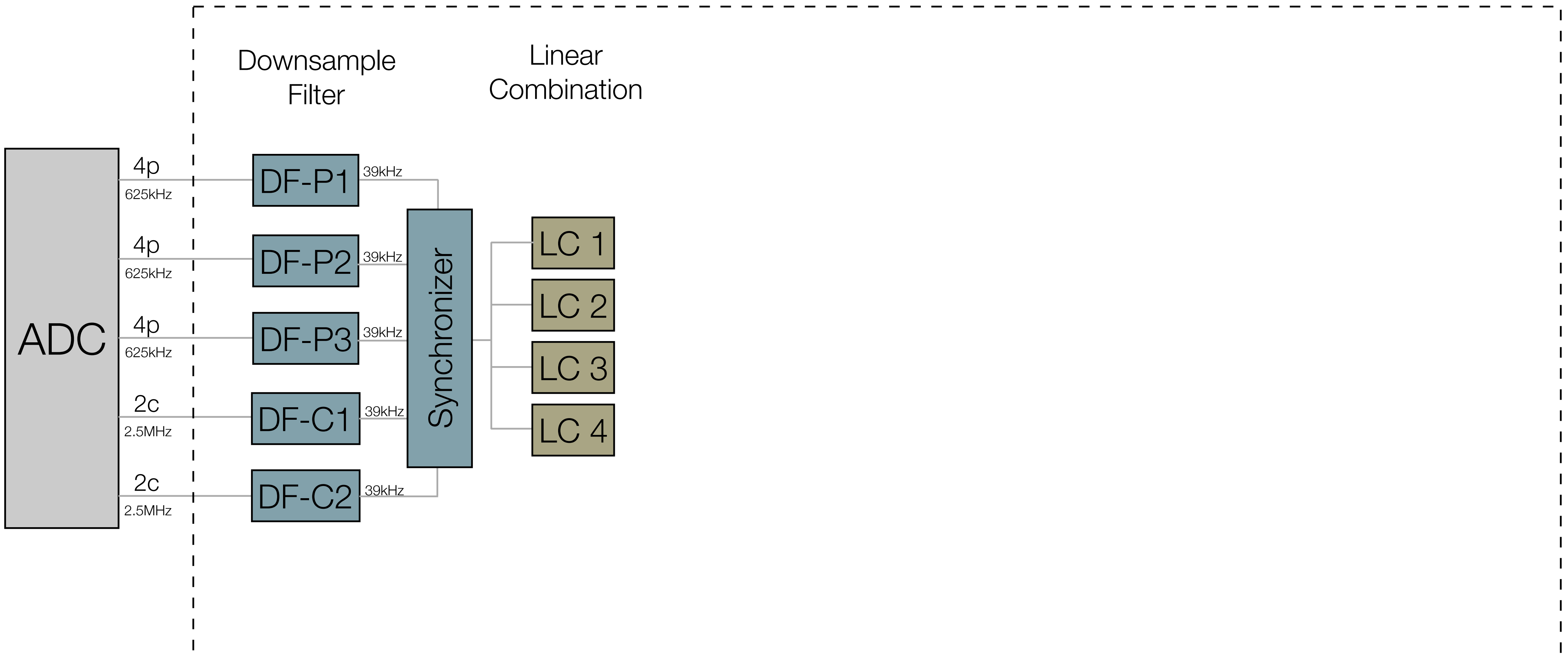
The L1 FPGA Trigger



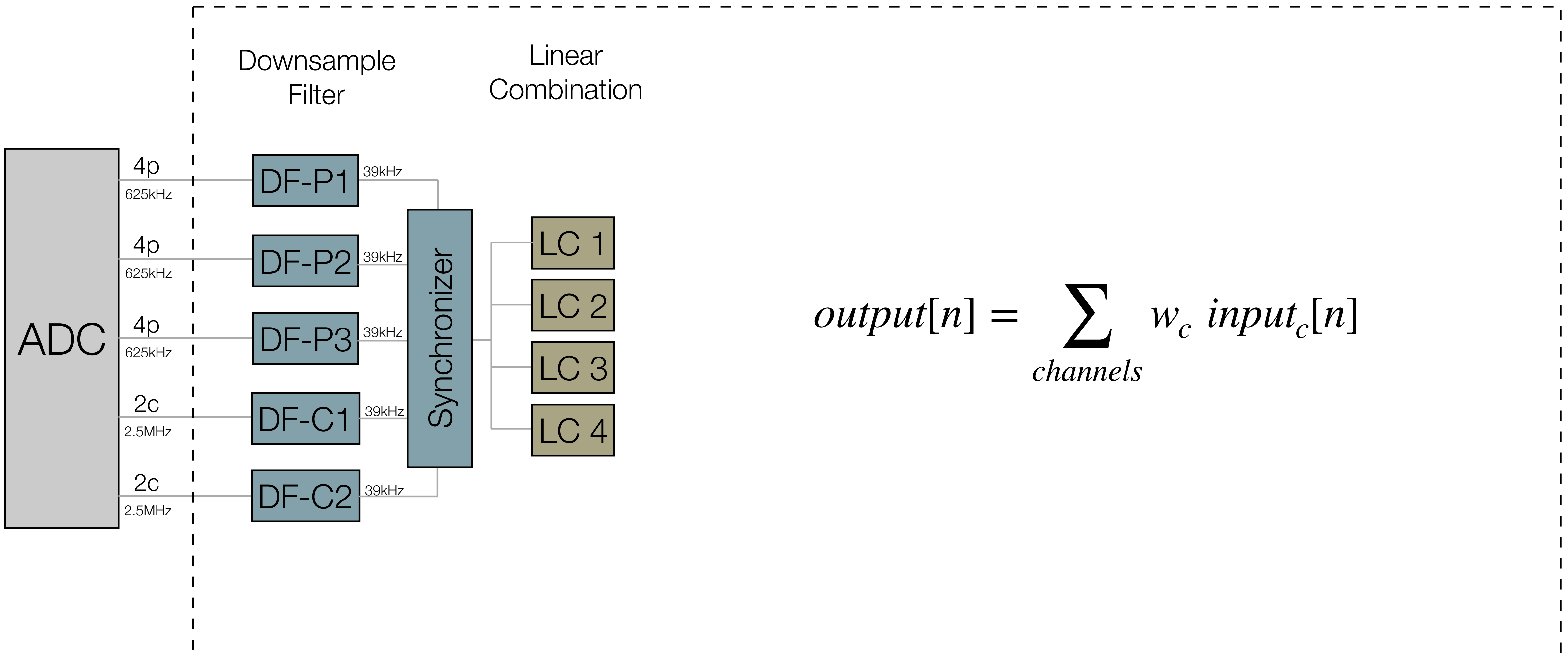
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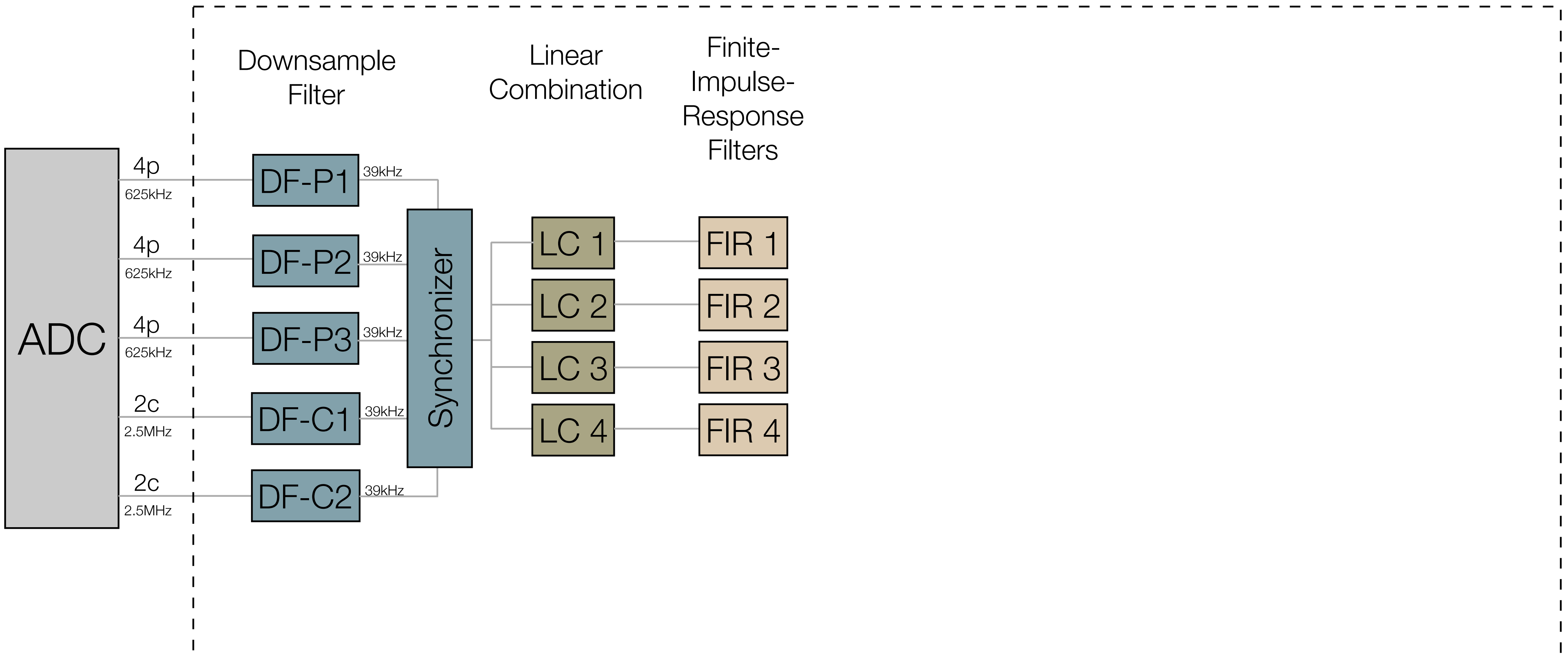


The L1 FPGA Trigger

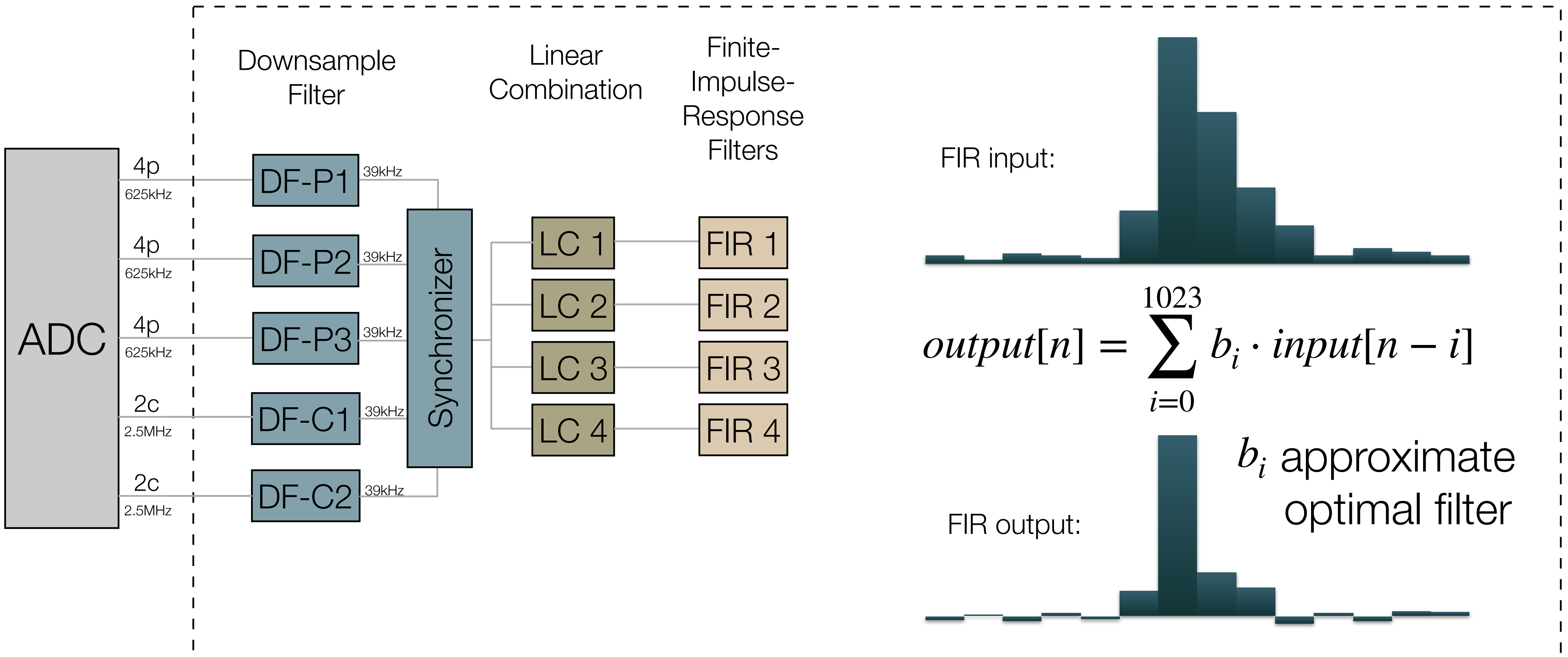


$$output[n] = \sum_{channels} w_c input_c[n]$$

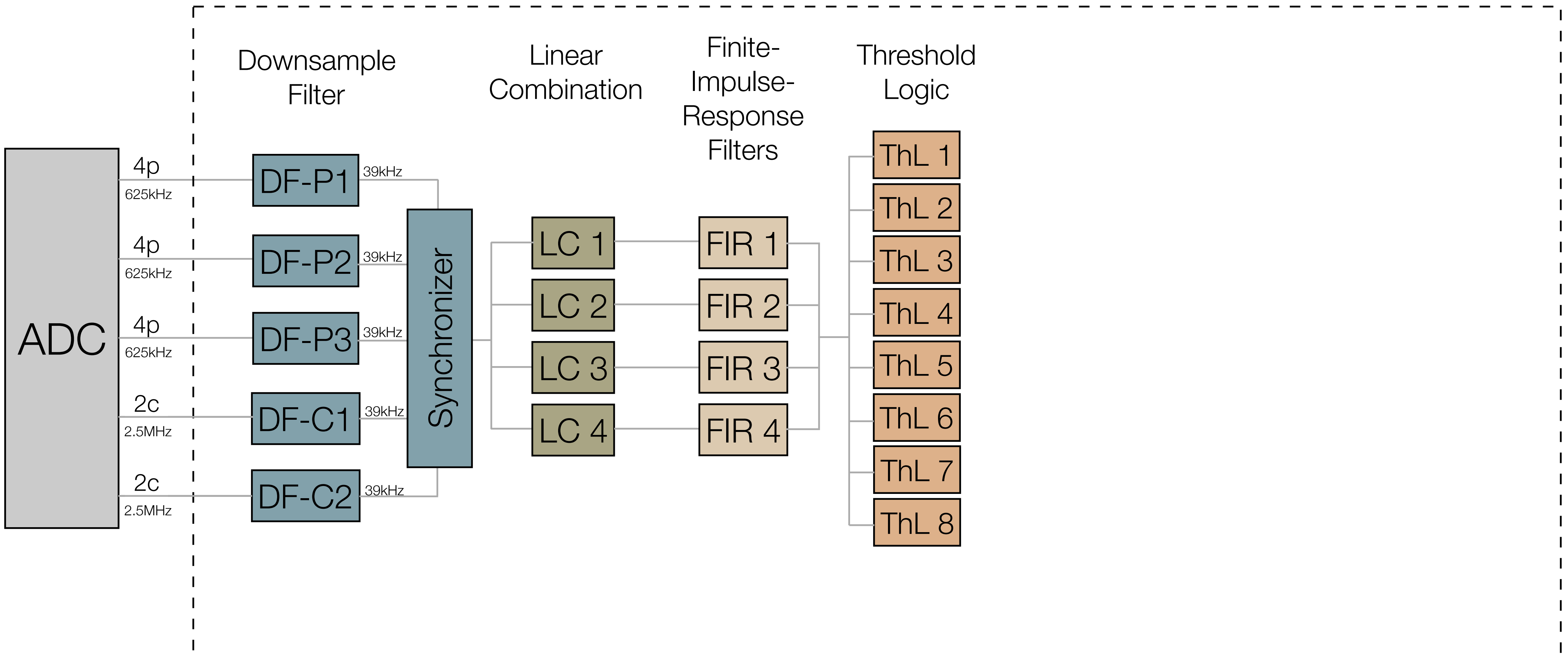
The L1 FPGA Trigger



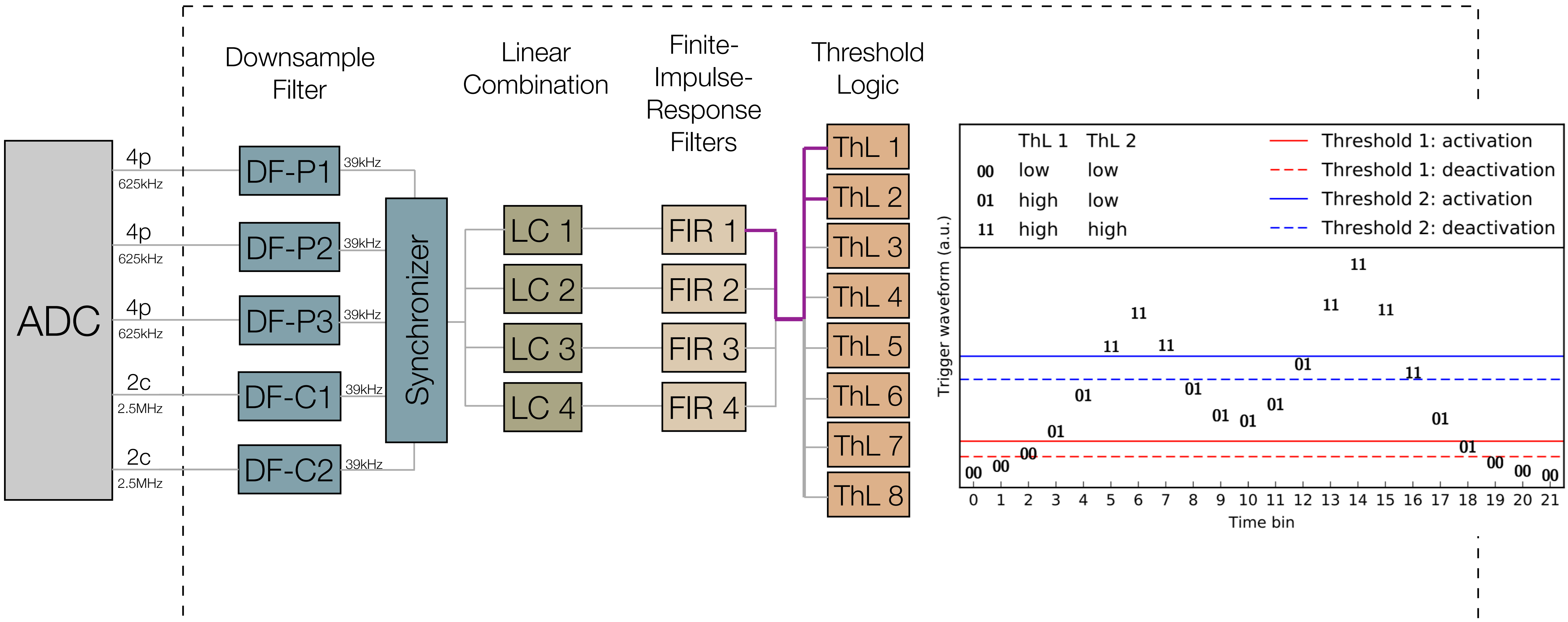
The L1 FPGA Trigger



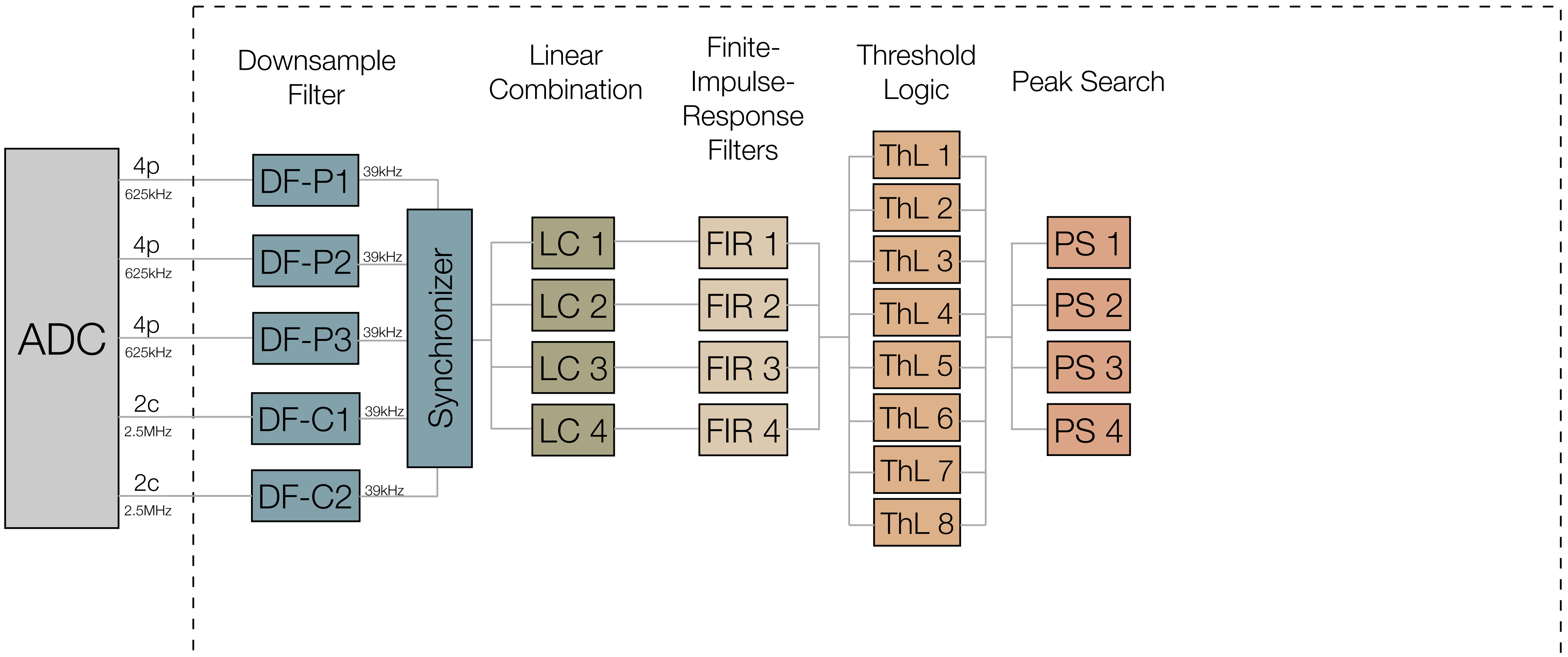
The L1 FPGA Trigger



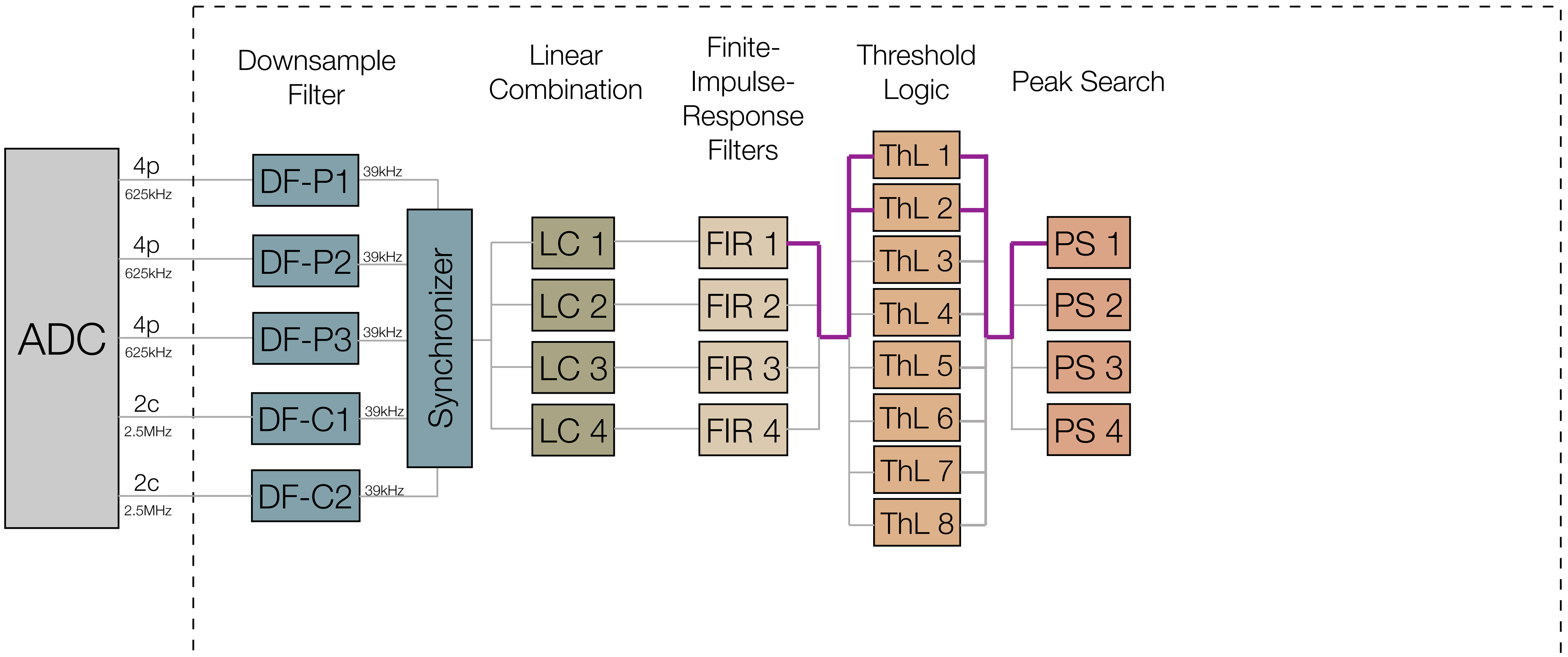
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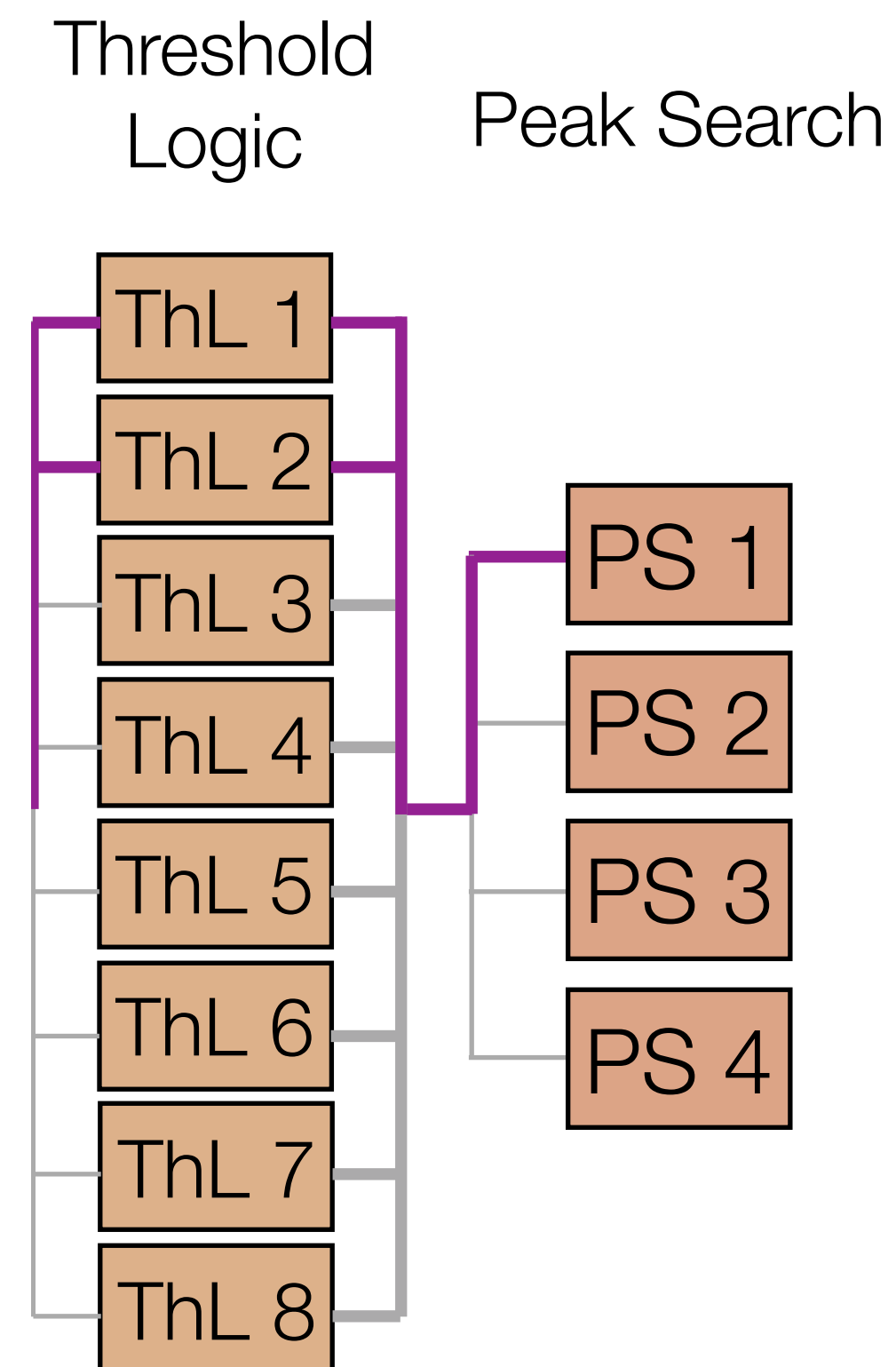
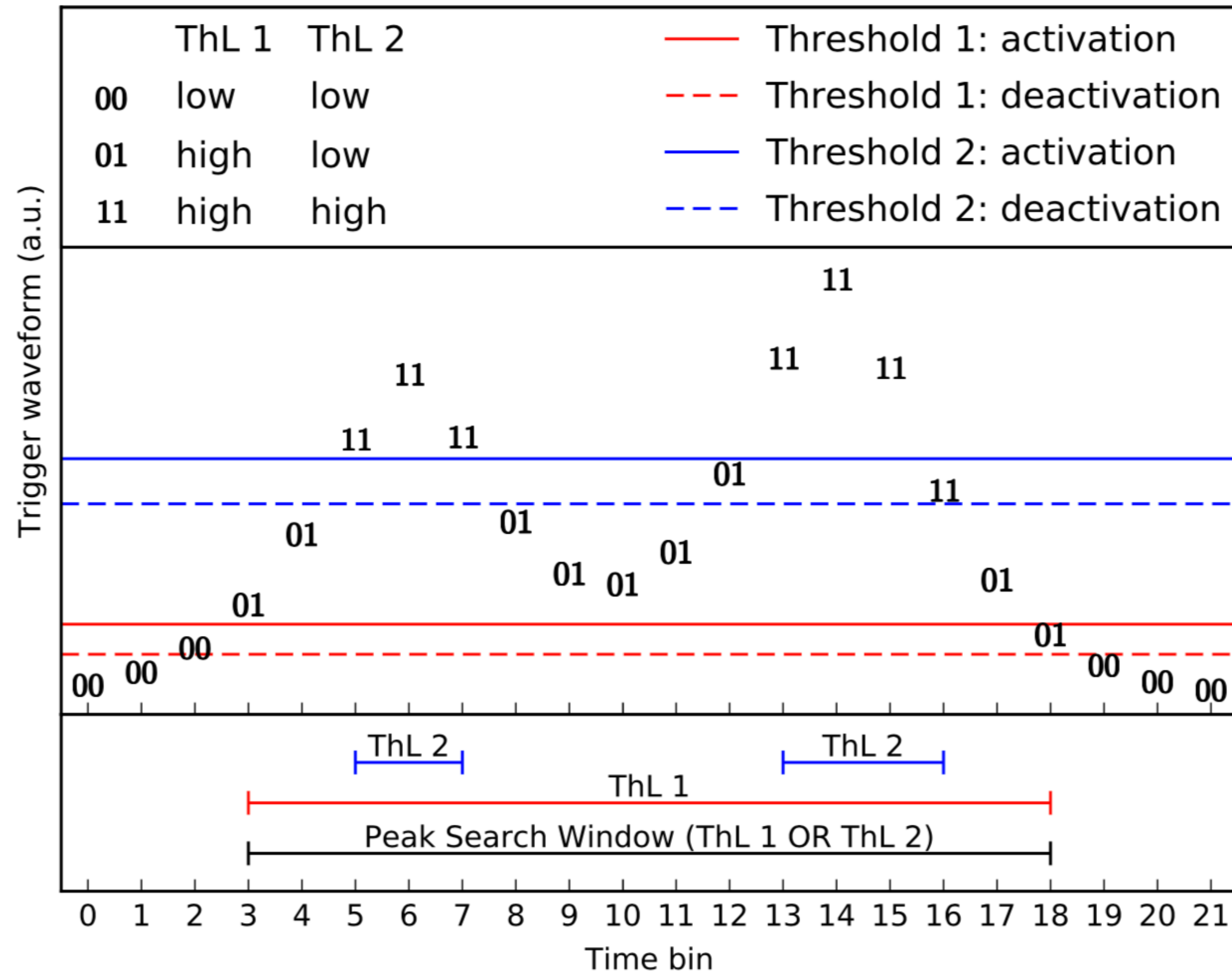
The L1 FPGA Trigger



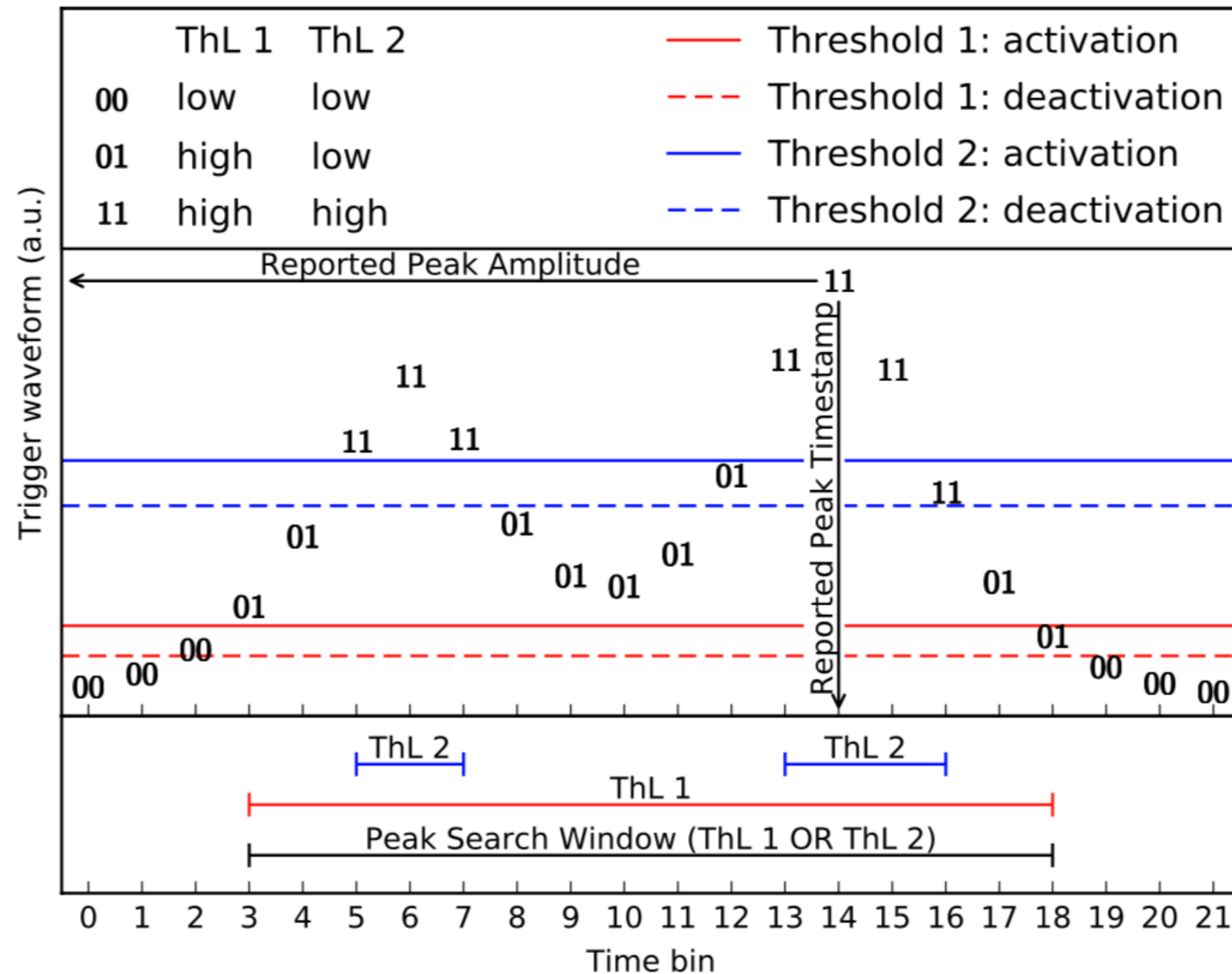
The L1 FPGA Trigger



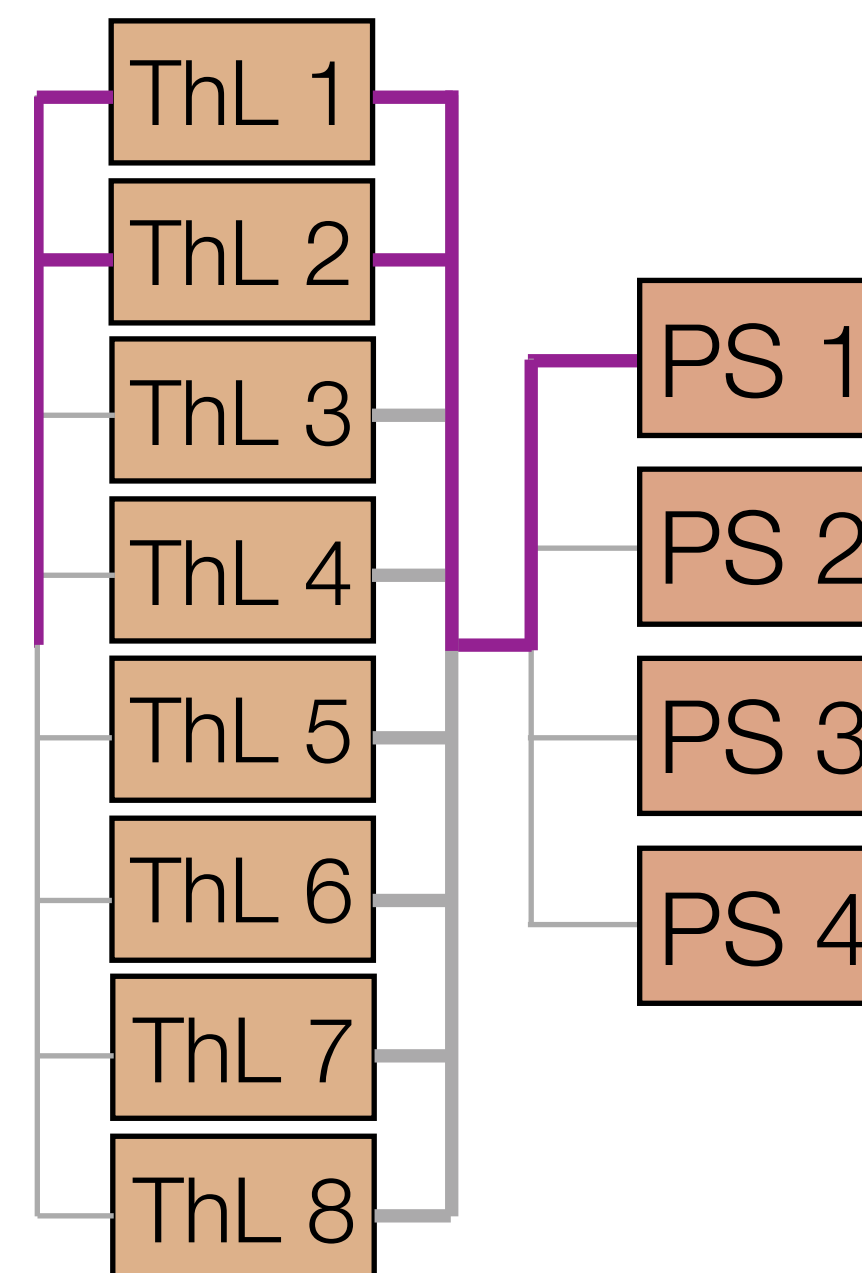
The L1 FPGA Trigger



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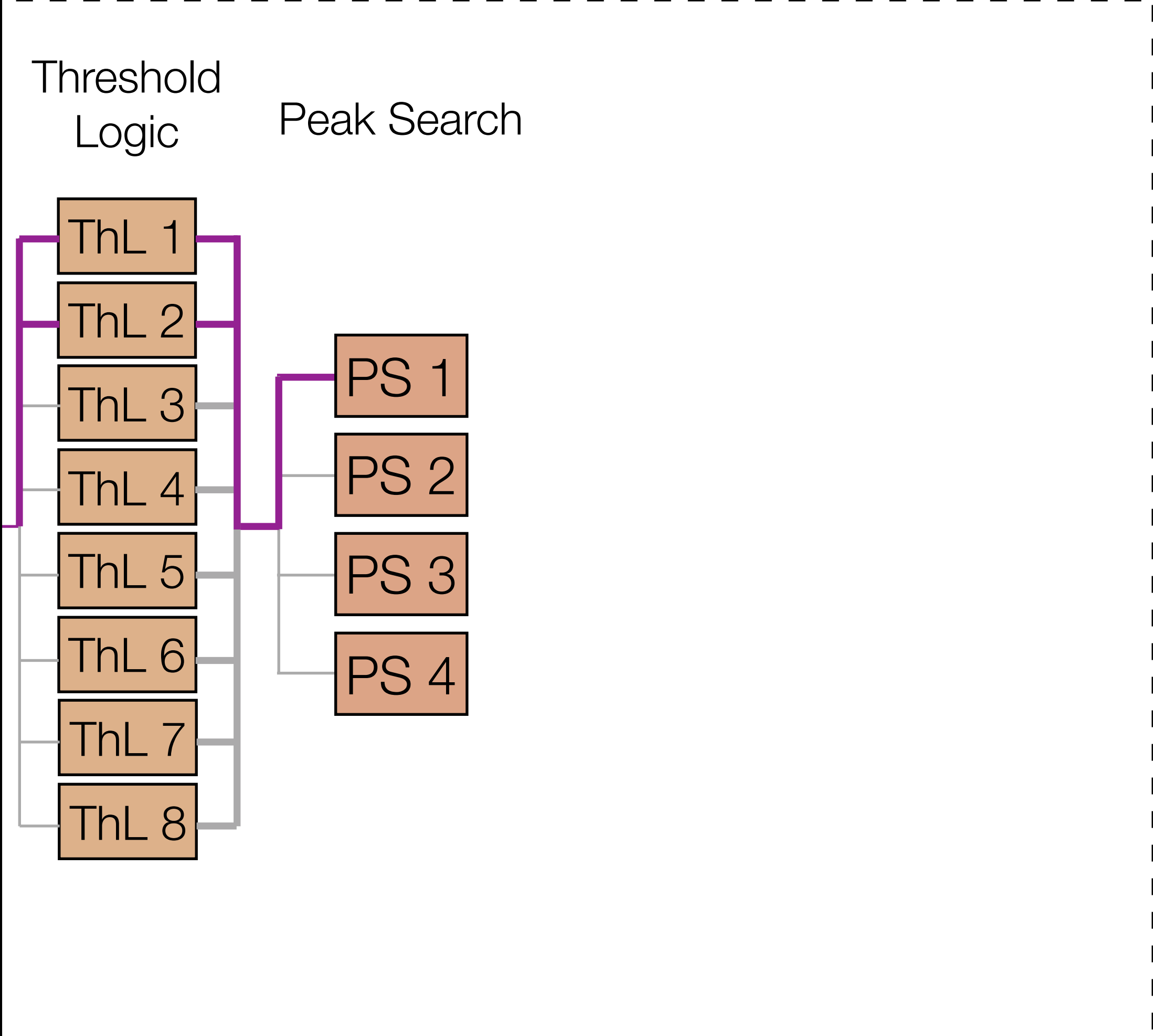


Threshold Logic Peak Search



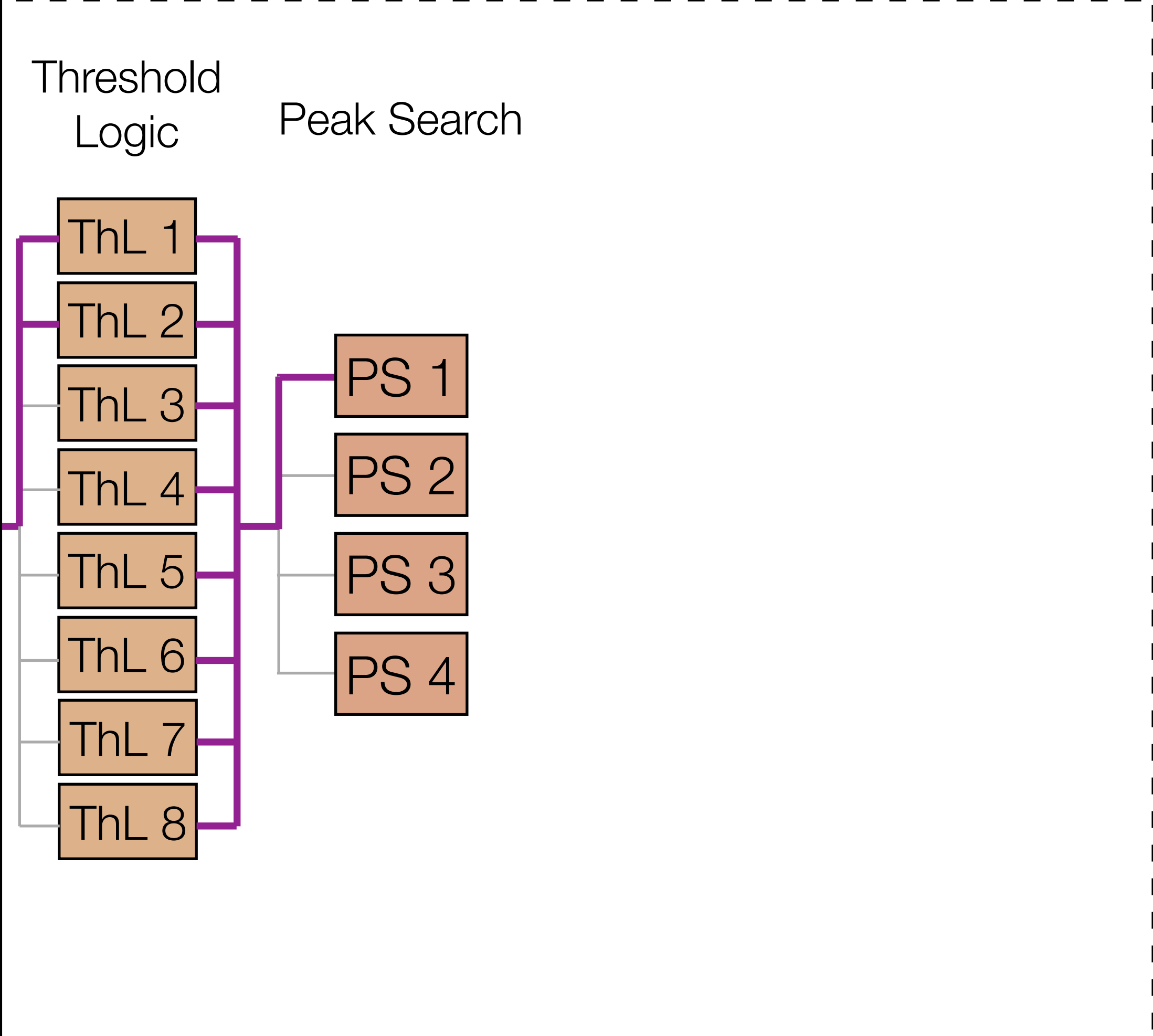
The L1 FPGA Trigger

ThL Selectors		0	0	1	1	1	2	2	3	Peak Search Window
Time bin	Trigger Waveform 0	ThL 1	ThL 2	ThL 3	ThL 4	ThL 5	ThL 6	ThL 7	ThL 8	
0	10	0	0	1	0	0	0	1	1	0
1	14	0	0	1	0	0	0	1	1	0
2	22	0	0	0	0	0	0	1	1	0
3	36	1	0	0	0	0	0	1	1	1
4	70	1	0	0	0	0	0	1	1	1
5	91	1	1	0	0	0	0	1	1	1
6	113	1	1	0	0	0	0	1	1	1
7	92	1	1	0	0	0	0	0	1	1
8	64	1	0	0	0	0	0	0	1	1
9	47	1	0	0	0	0	0	0	1	1
10	43	1	0	0	0	0	0	0	1	1
11	54	1	0	0	0	1	0	0	1	1
12	80	1	0	0	0	1	1	0	1	1
13	118	1	1	0	0	1	1	0	1	1
14 (peak)	145	1	1	0	0	1	1	0	0	1
15	115	1	1	0	0	1	1	0	1	1
16	74	1	1	0	0	1	1	0	1	1
17	45	1	0	0	0	0	1	0	1	1
18	26	1	0	0	0	0	1	0	1	1
19	16	0	0	0	0	0	1	0	1	0
20	11	0	0	1	0	0	1	0	1	0
21	8	0	0	1	0	0	1	0	1	0
At-peak trigger word		1	1	0	0	1	1	0	0	
During-window trigger word		1	1	0	0	1	1	1	1	

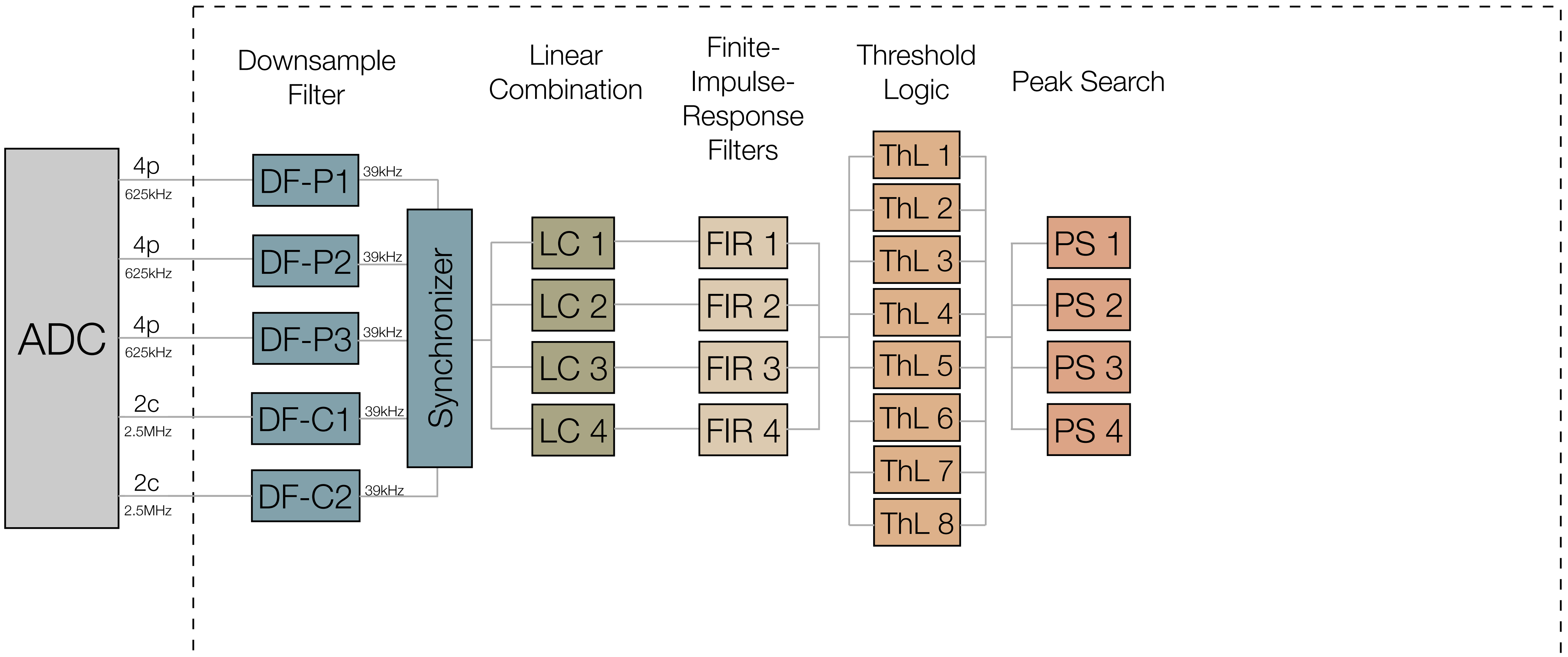


The L1 FPGA Trigger

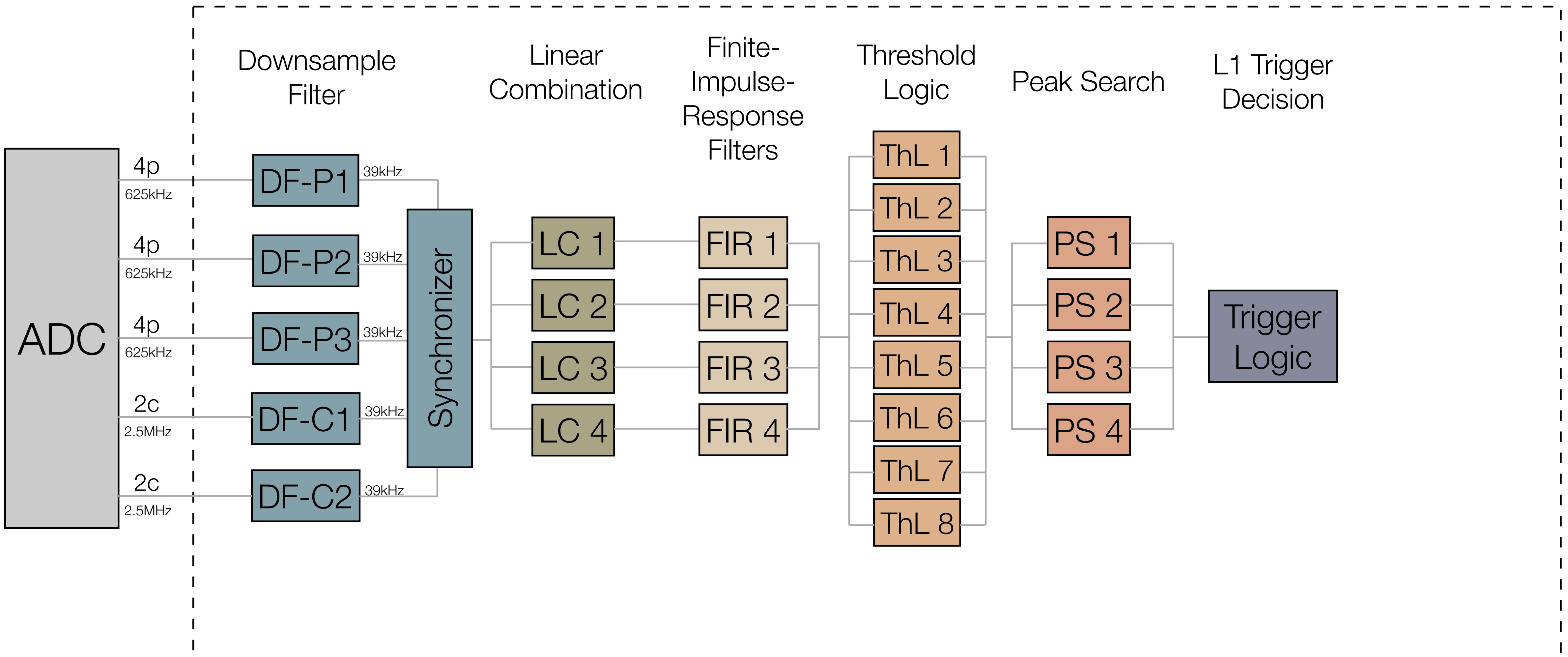
ThL Selectors		0	0	1	1	1	2	2	3	Peak Search Window
Time bin	Trigger Waveform 0	ThL 1	ThL 2	ThL 3	ThL 4	ThL 5	ThL 6	ThL 7	ThL 8	
0	10	0	0	1	0	0	0	1	1	0
1	14	0	0	1	0	0	0	1	1	0
2	22	0	0	0	0	0	0	1	1	0
3	36	1	0	0	0	0	0	1	1	1
4	70	1	0	0	0	0	0	1	1	1
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9	47	1	0	0	0	0	0	0	1	1
10	43	1	0	0	0	0	0	0	1	1
11	54	1	0	0	0	1	0	0	1	1
12	80	1	0	0	0	1	1	0	1	1
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19	16	0	0	0	0	0	1	0	1	0
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At-peak trigger word		1	1	0	0	1	1	0	0	
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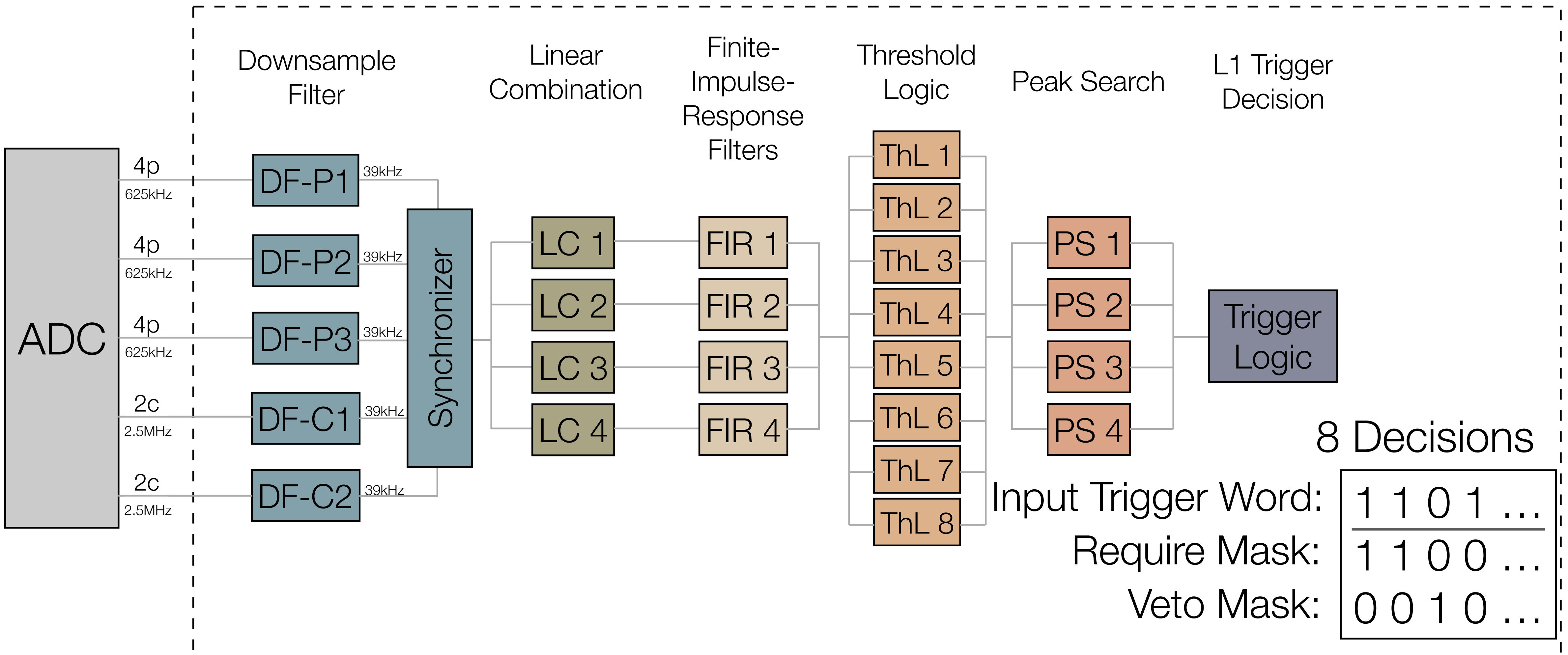
The L1 FPGA Trigger



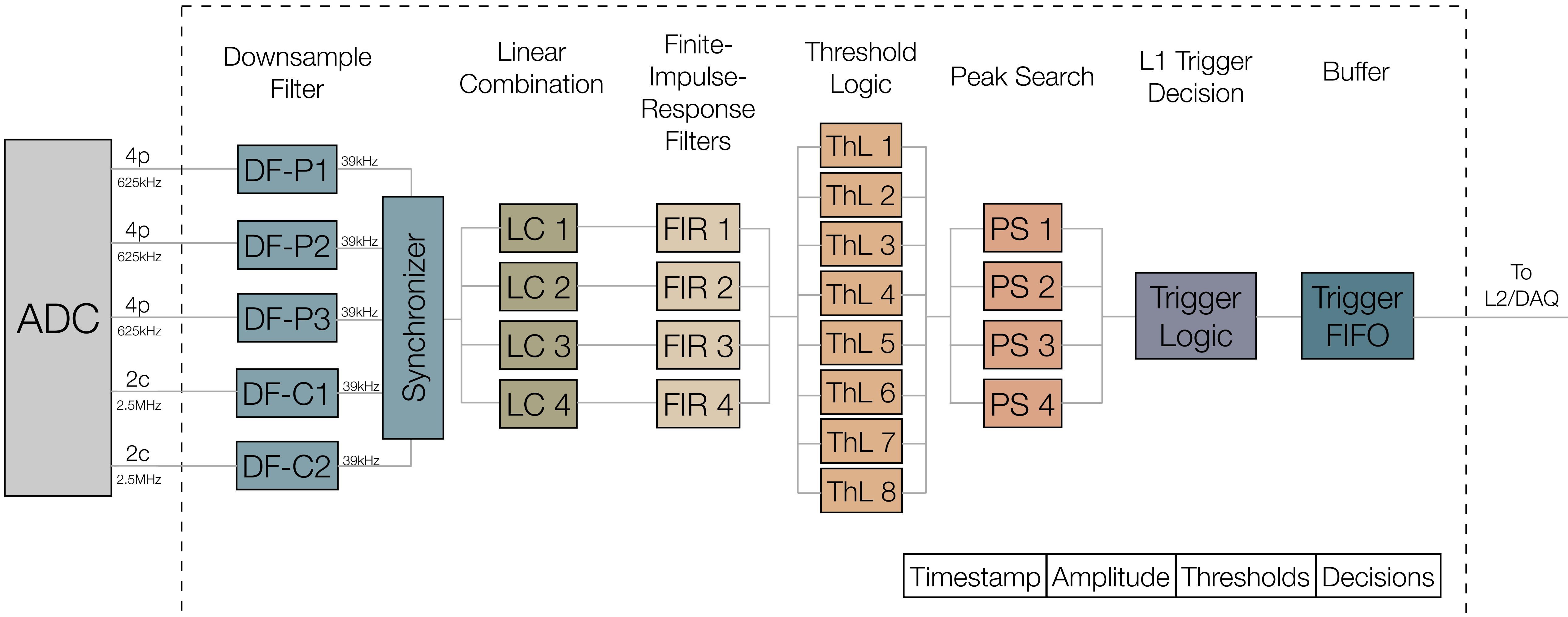
The L1 FPGA Trigger



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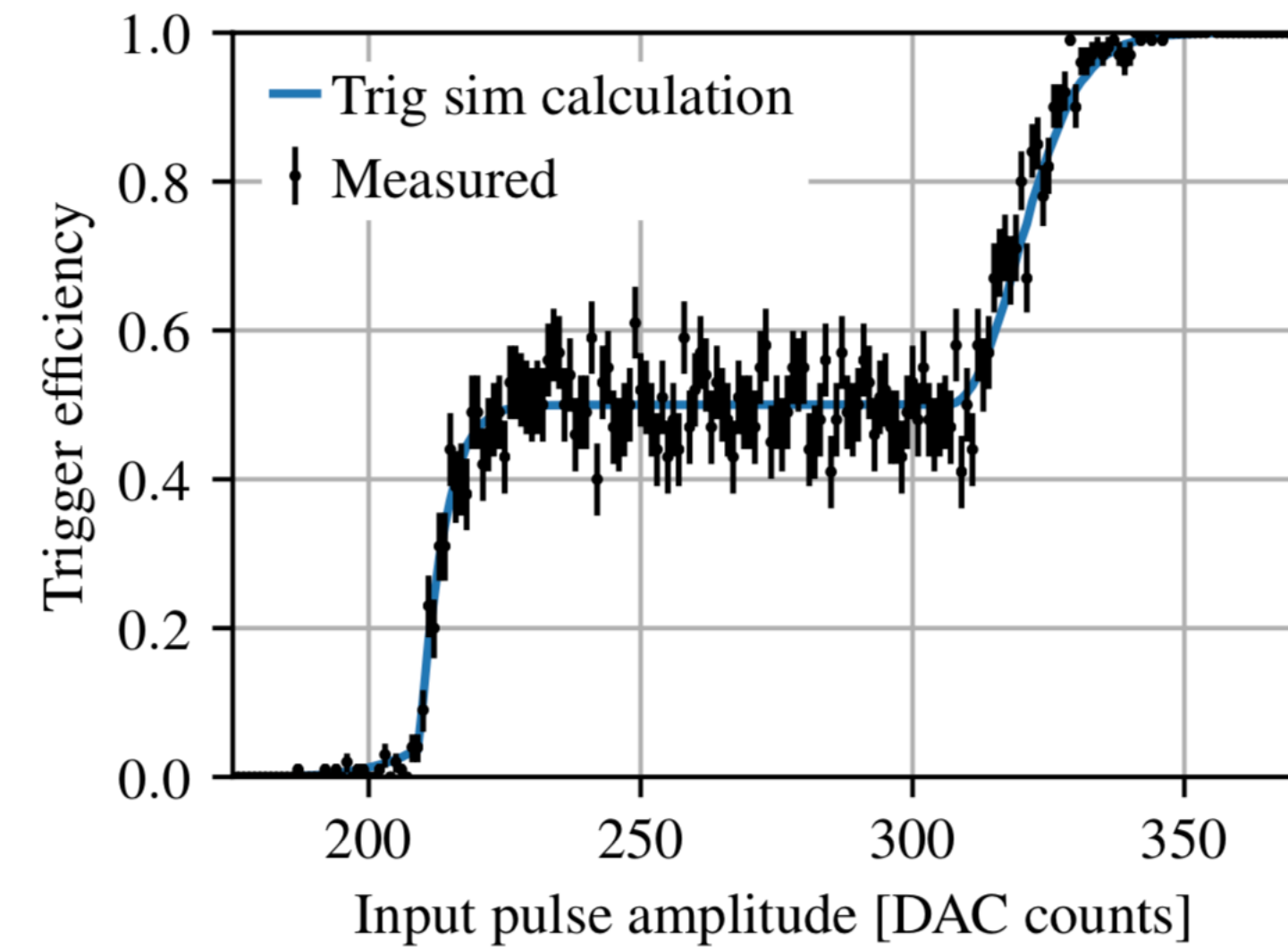
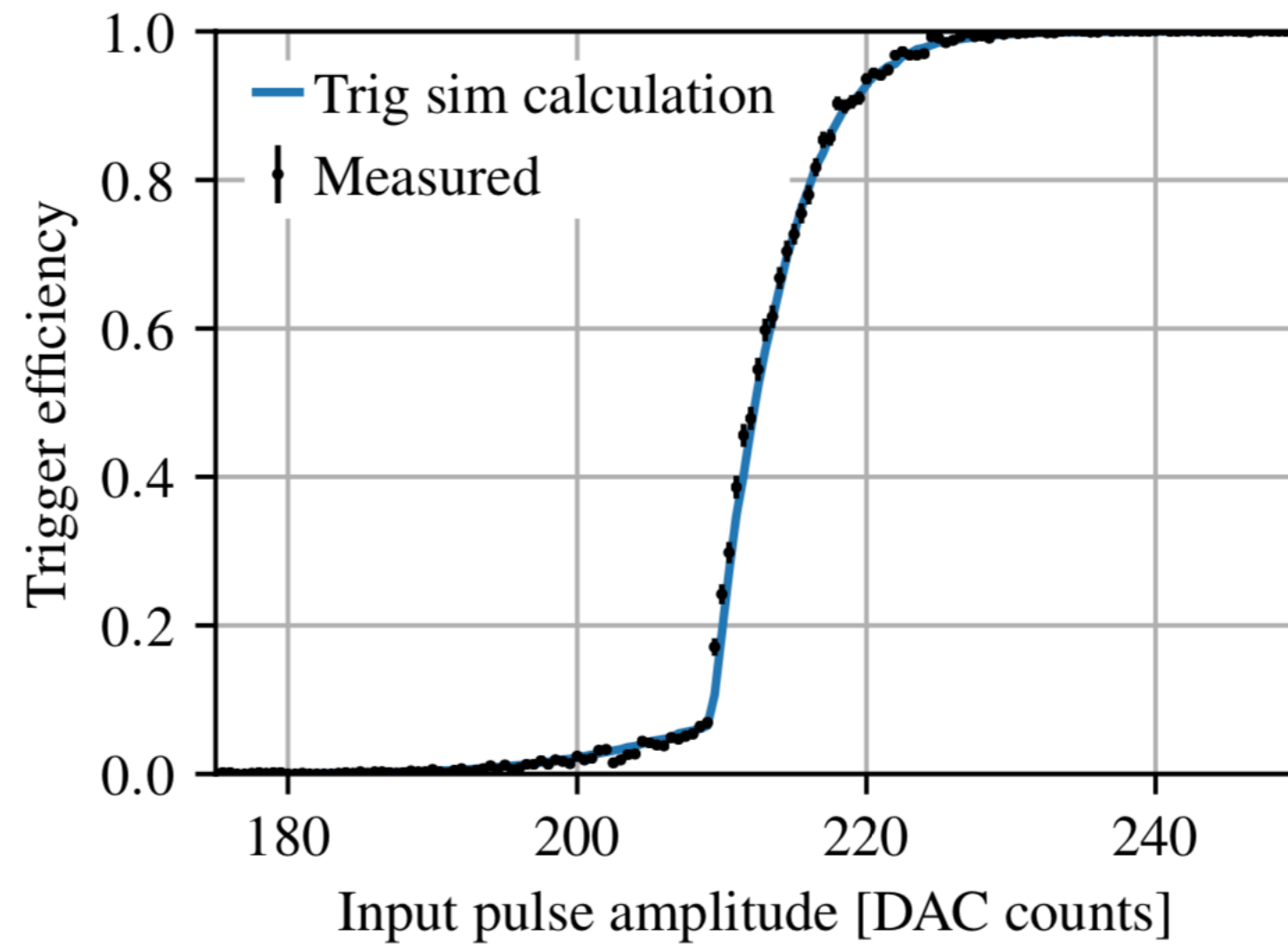


The L1 FPGA Trigger



Trigger Performance

Single threshold

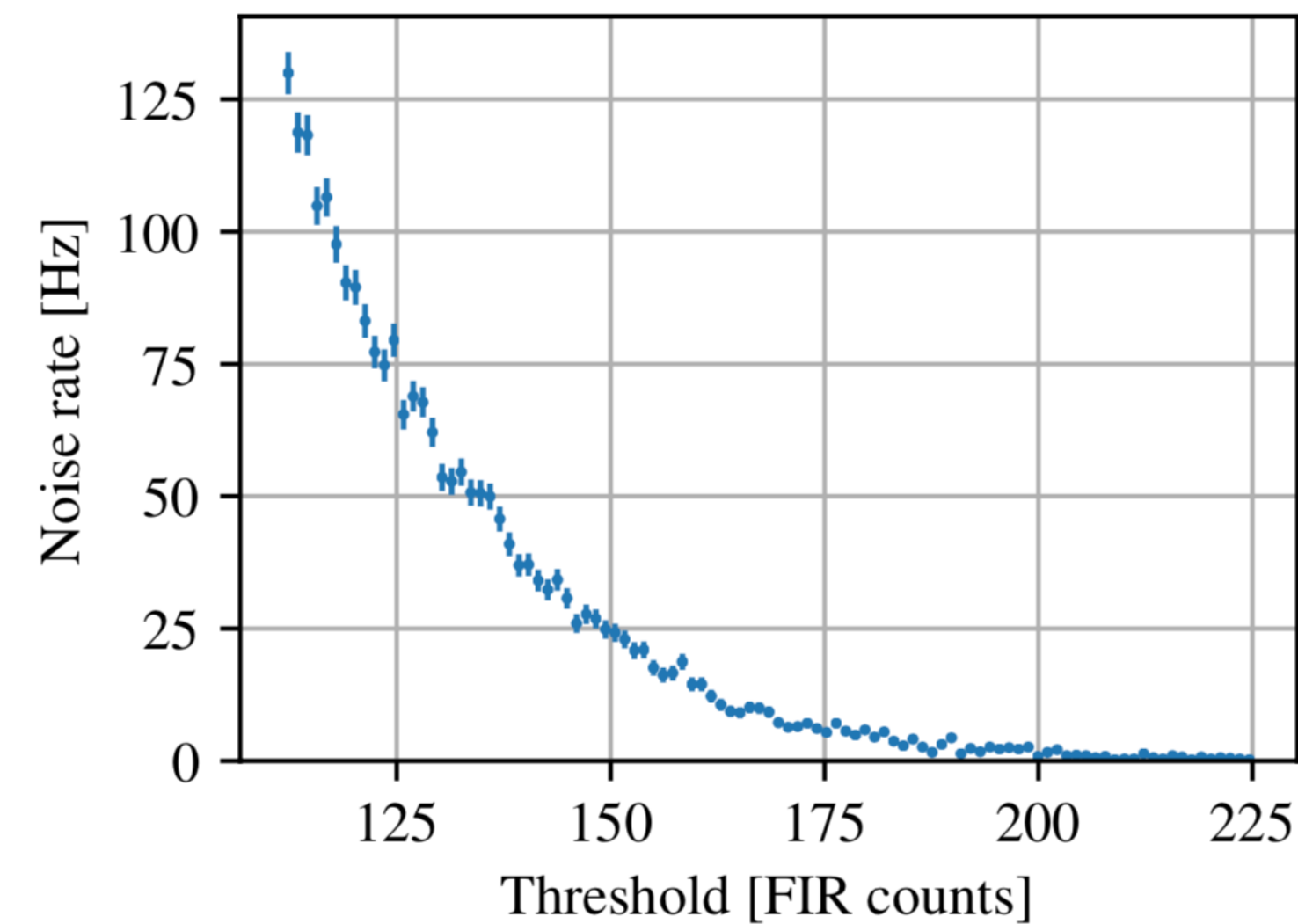
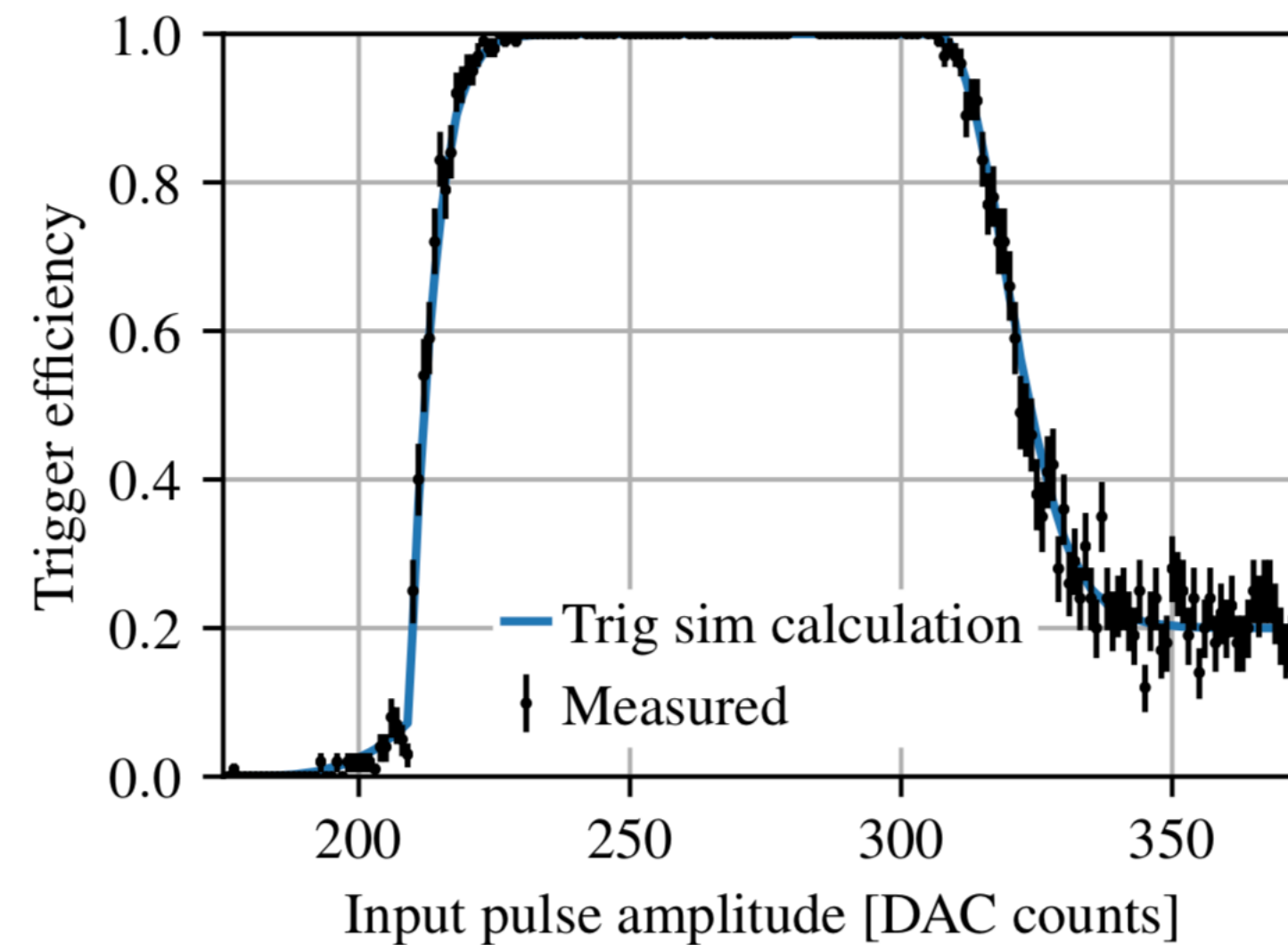


Low threshold
50% prescaled

High threshold
Unprescaled

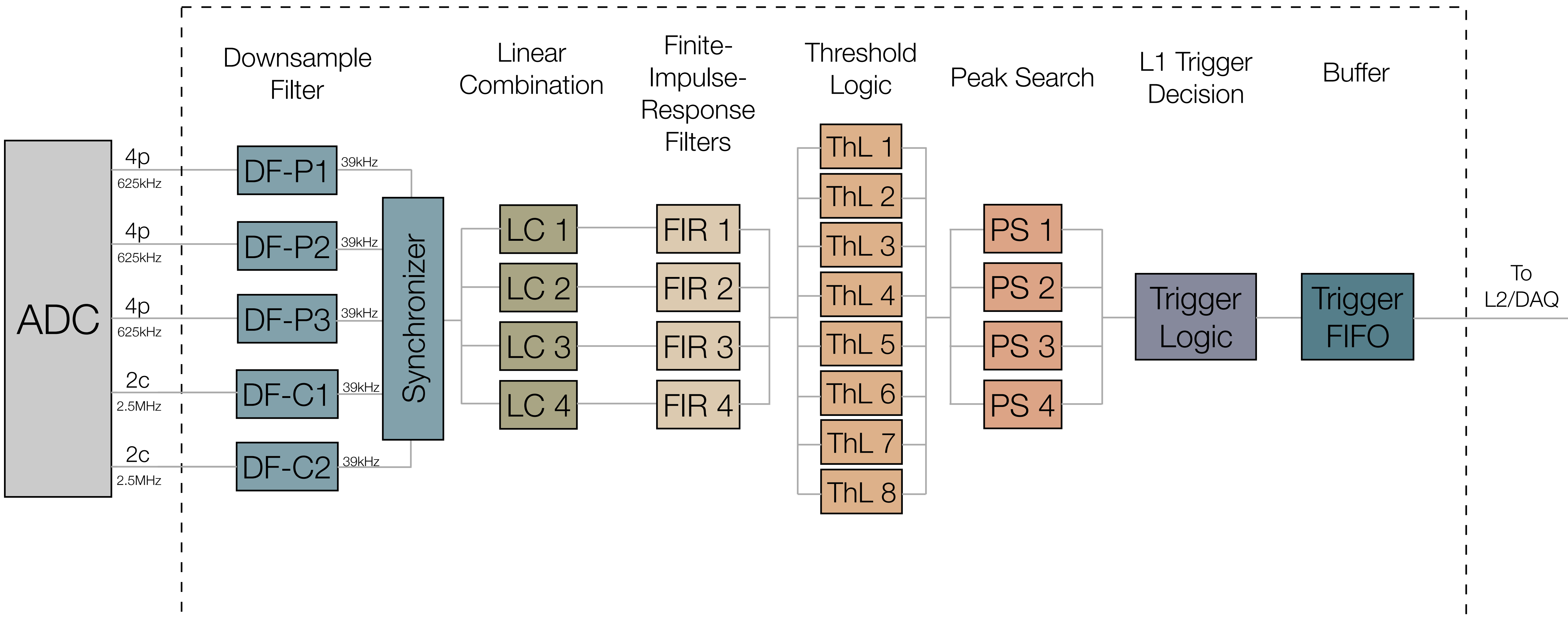
Low threshold
unprescaled

High threshold
vetoed

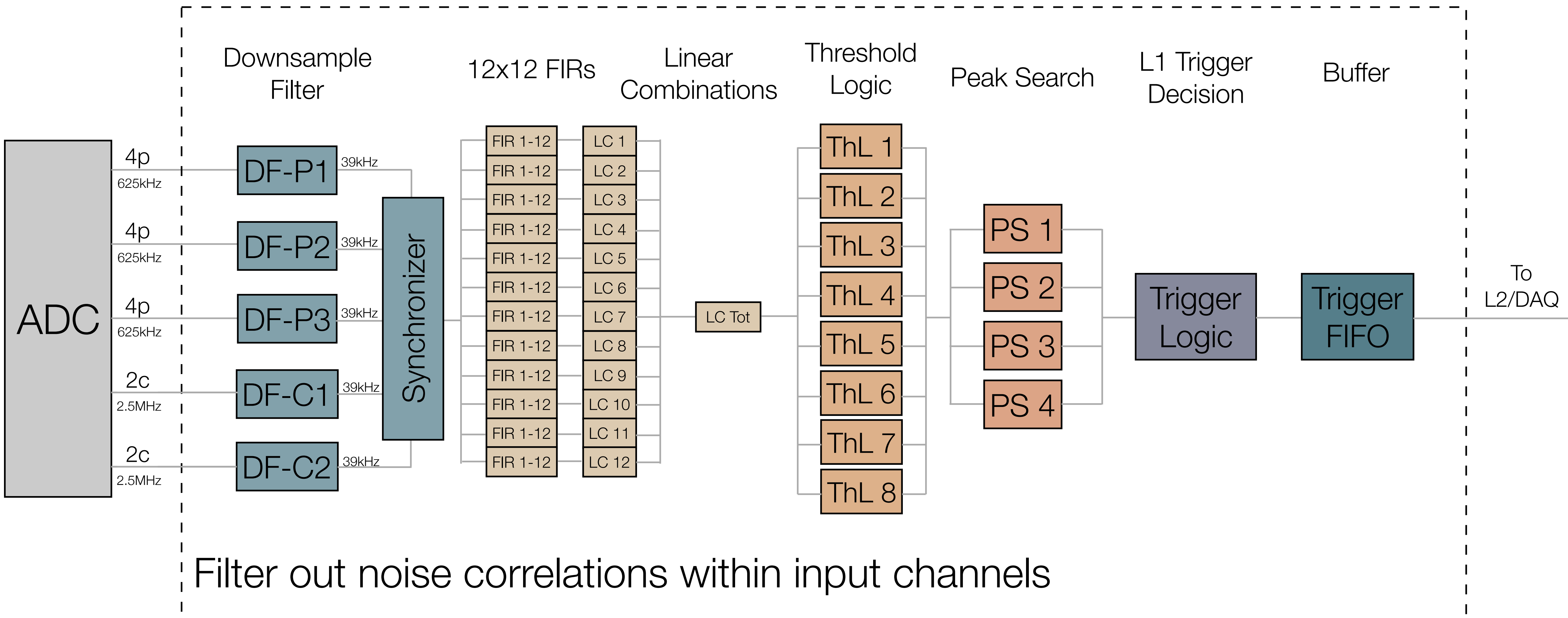


Noise dependence

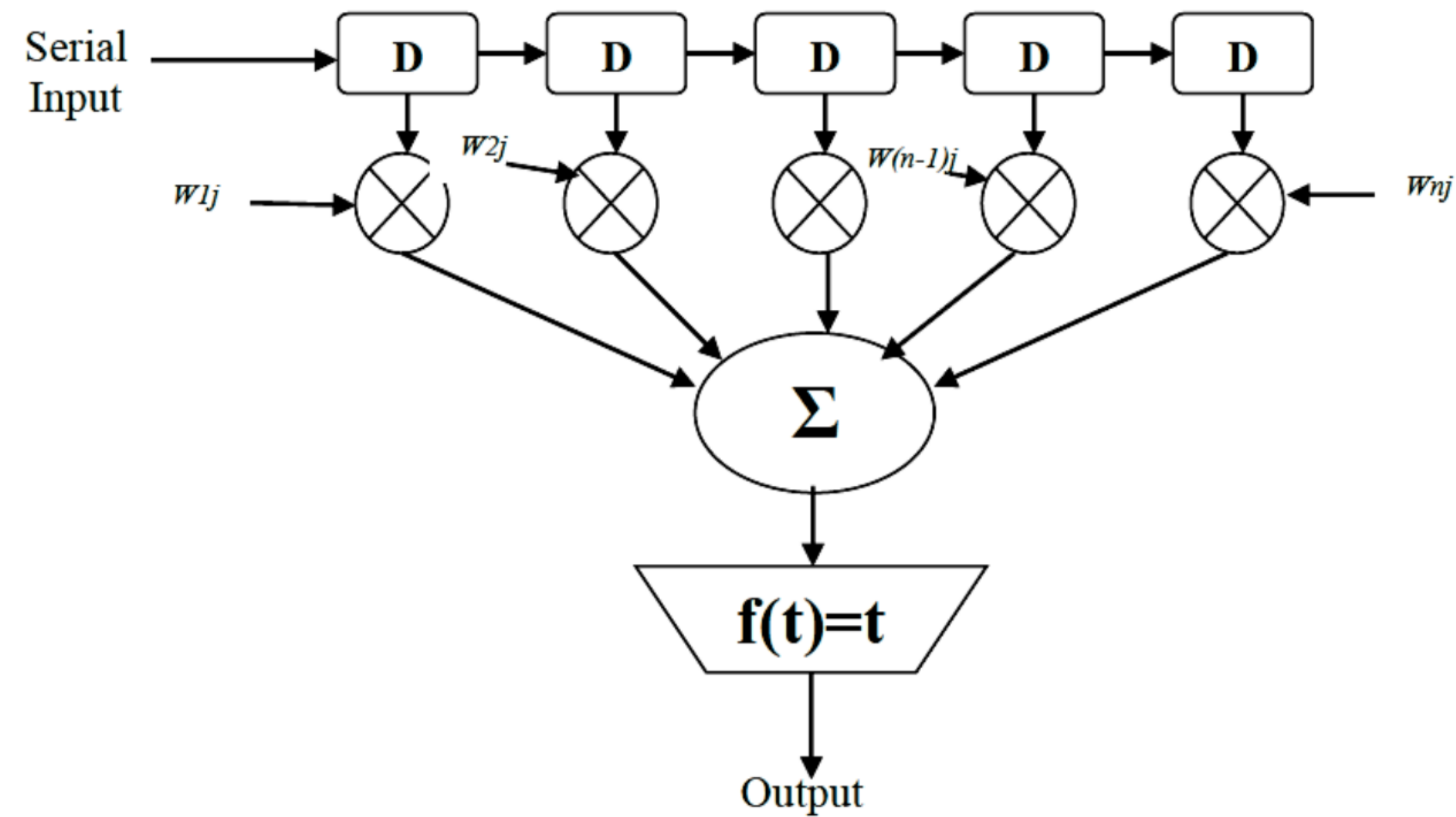
Future Improvement: NxM Correlated Optimal Filter



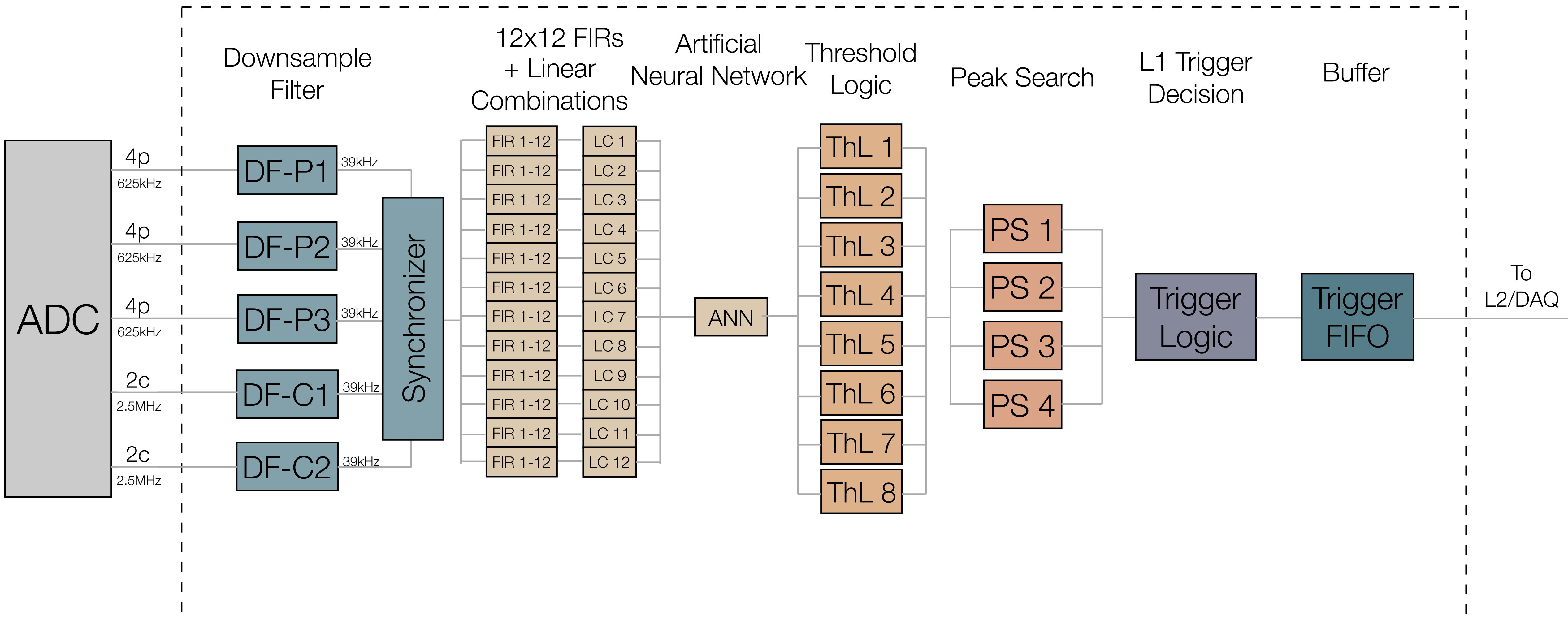
Future Improvement: NxM Correlated Optimal Filter



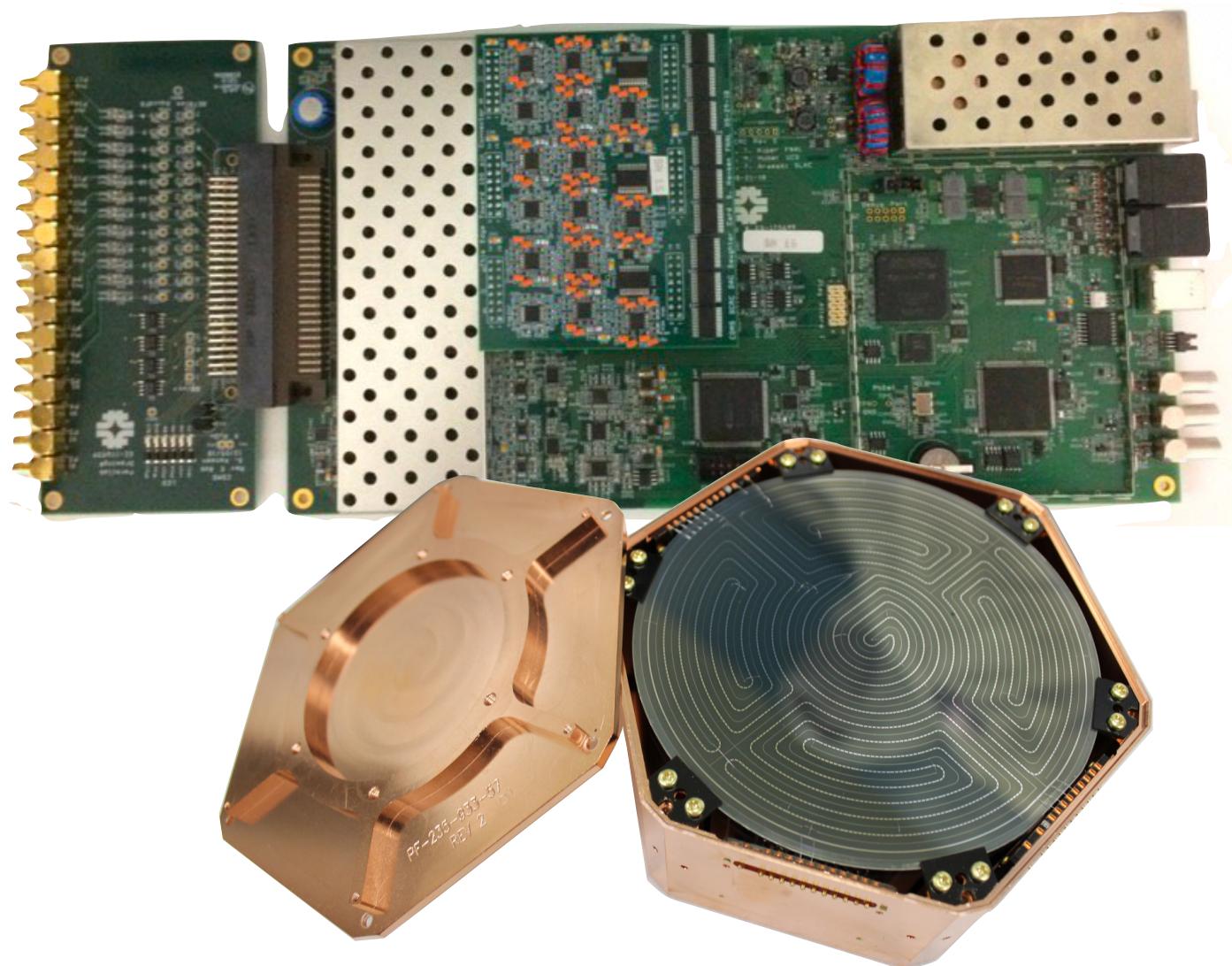
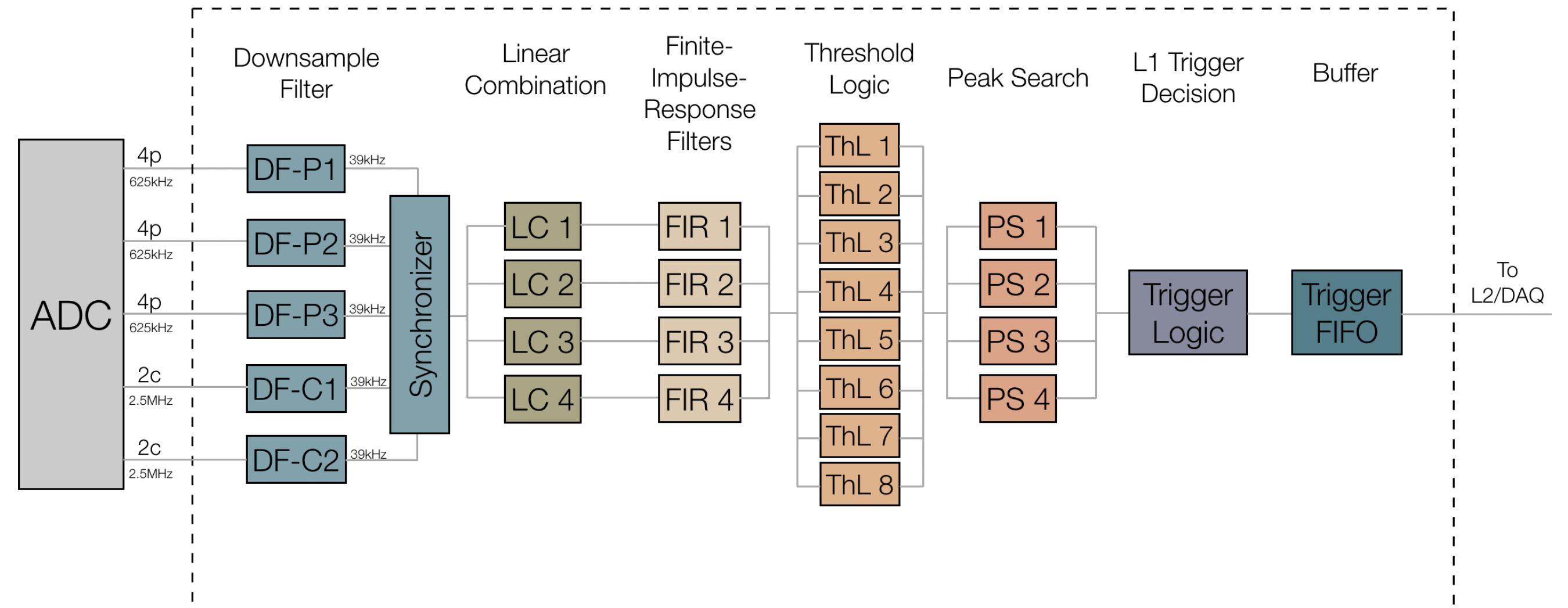
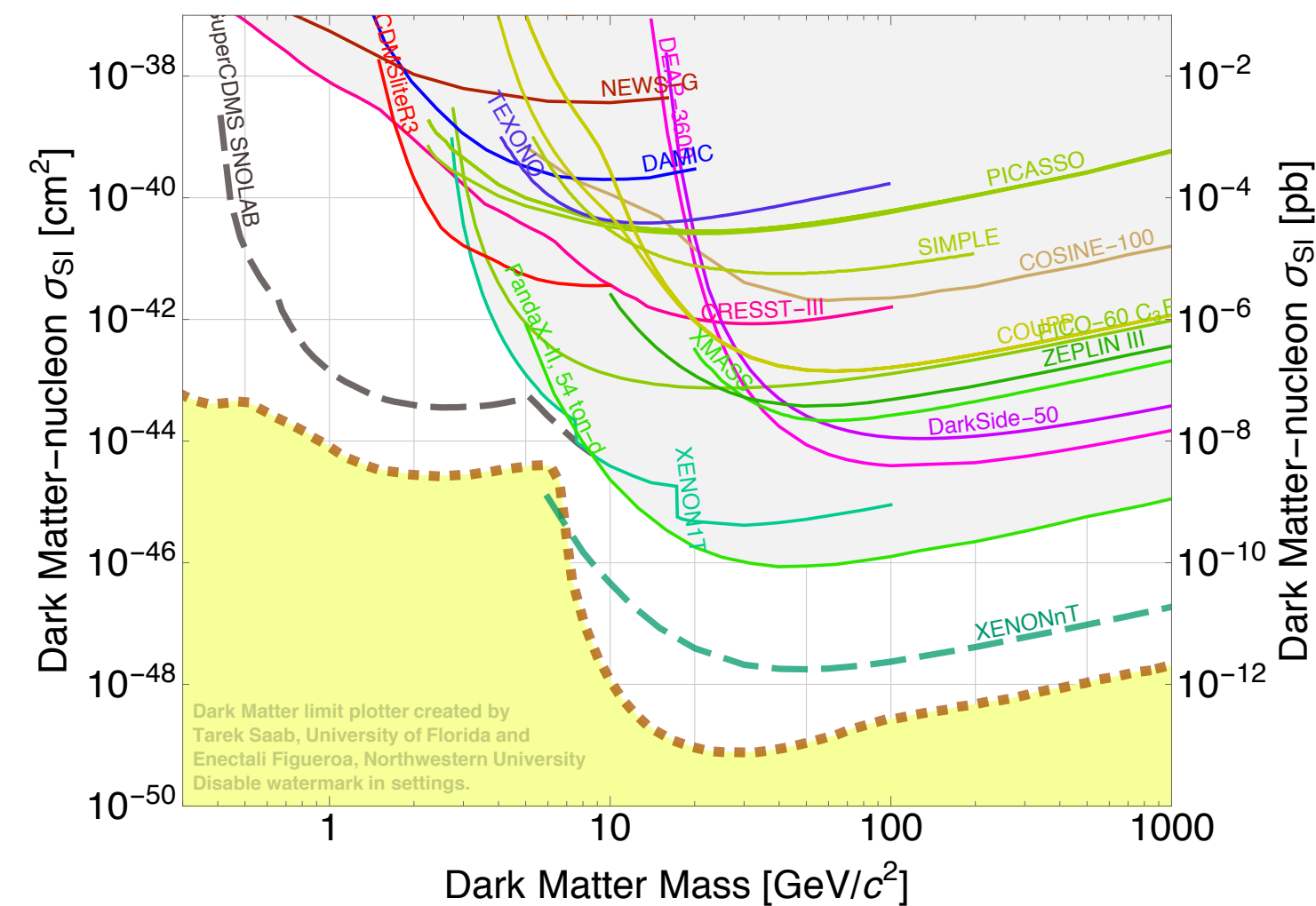
Future Improvement: Machine Learning on FPGA



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Thanks for your attention!



Two cross-disciplinary open positions:

SuperCDMS (Postdoc):

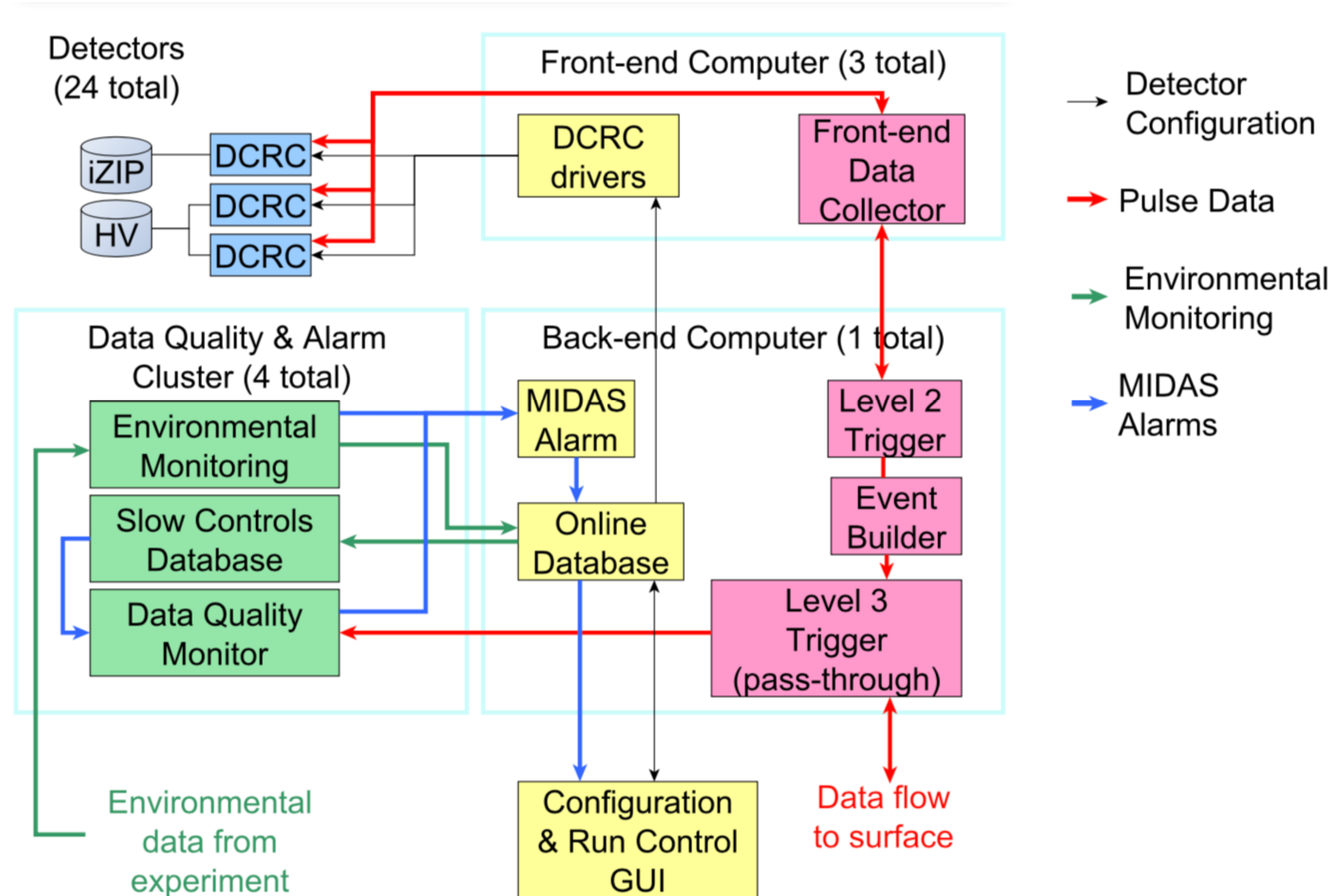
<https://www.uni-hamburg.de/uhh/stellenangebote/wissenschaftliches-personal/exzellenzcluster-quantum-universe-qu1/29-02-20-19-en.pdf>

Belle II (PhD):

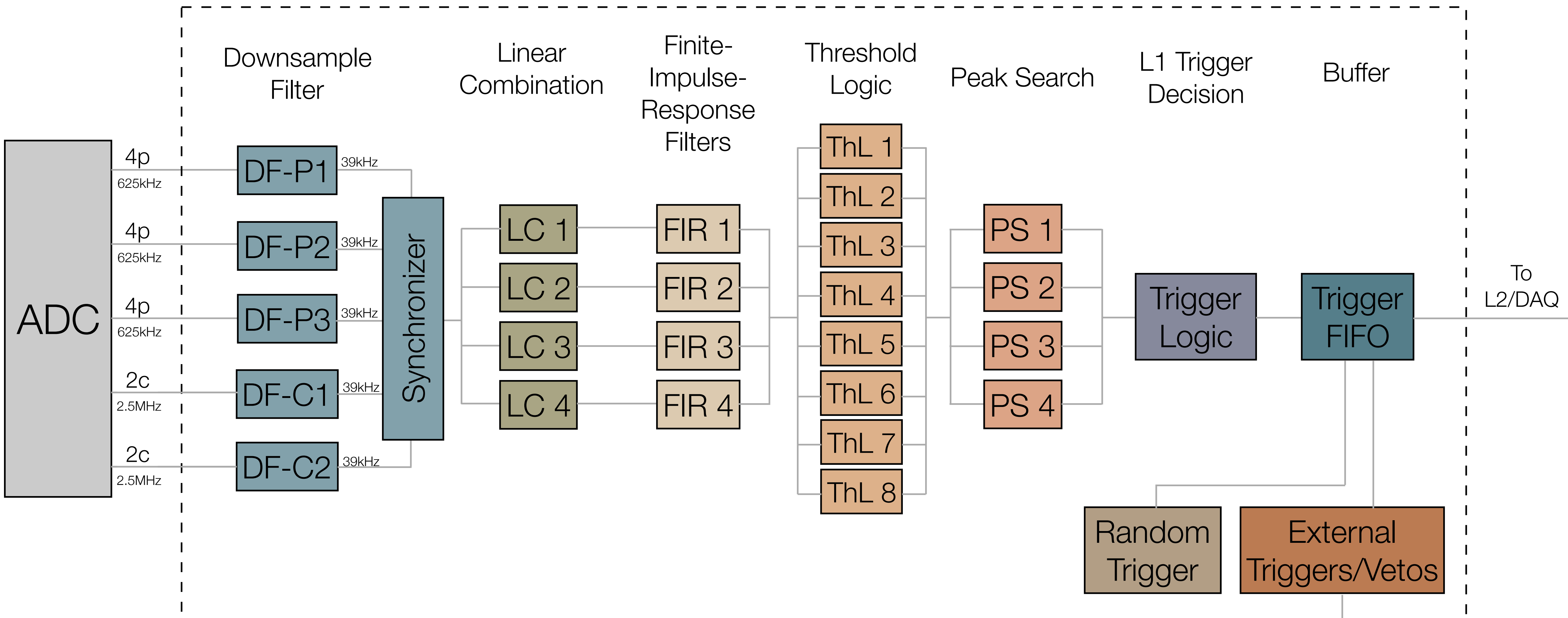
http://www.desy.de/career/job_offers/index_eng.html?joboffer=99930



Backup: The SuperCDMS DAQ System



Backup: Randoms and External Triggers/Vetos



Backup: Signal Vs Background Trace

