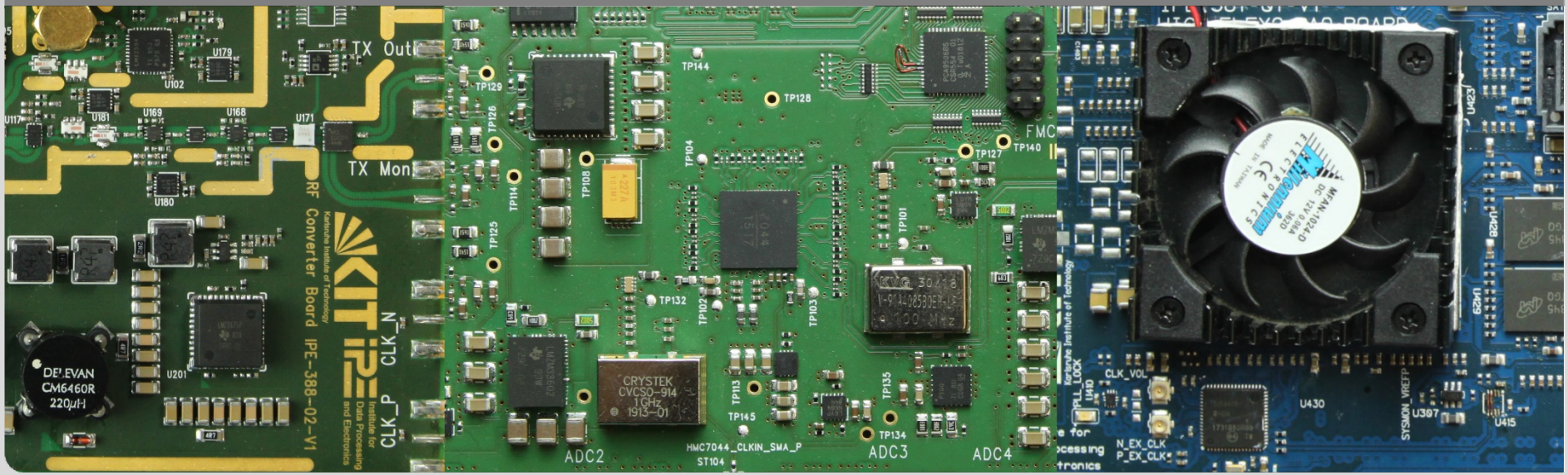
Karlsruhe Institute of Technology

Wideband Readout System for Microwave-Resonator Multiplexed Sensors

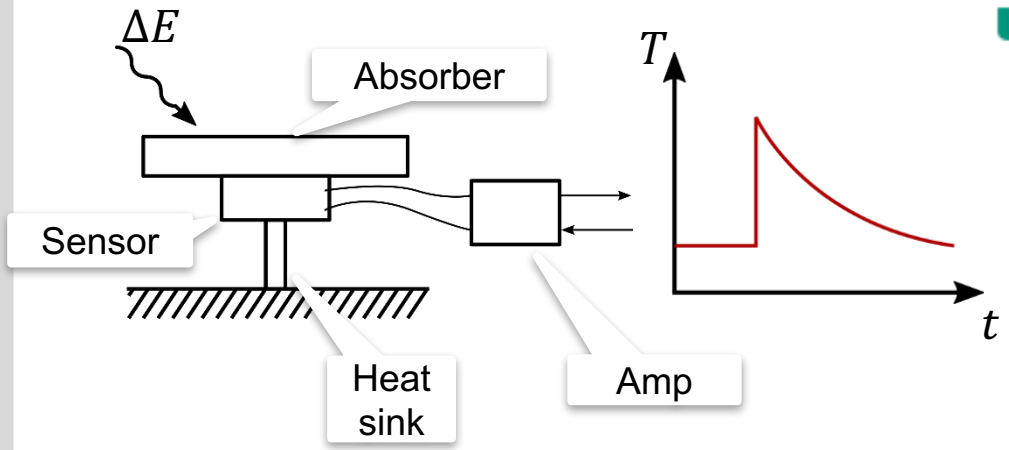
Nick Karcher

KSETA Plenary Workshop 19. – 21.2.2020

Institute for Data Processing and Electronics (IPE) – Embedded Parallel Systems (EPS)

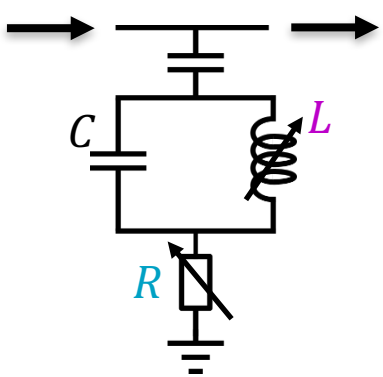


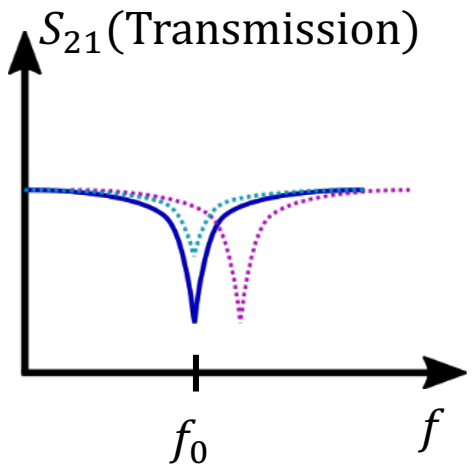
Cryogenic Calorimetry Sensors



- Cryogenic calorimeters
  - Measure single photons
  - Operated << 1K
  - Resolution 1.58 eV @ keV

- Scaling sensor quantity
  - 2 – 10 Connections per sensor
  - Wiring complexity + costs

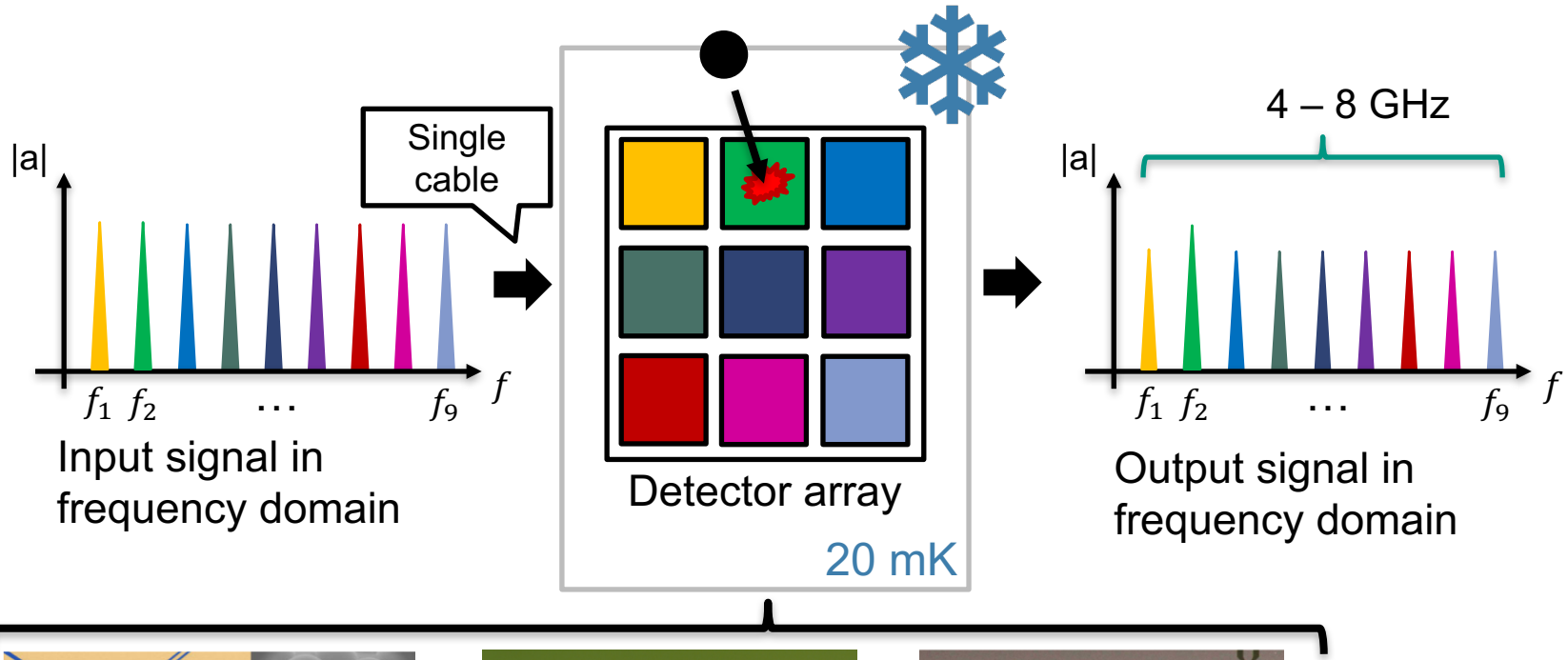


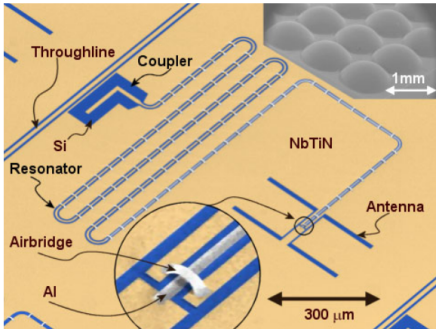


- Microwave resonators
  - Couple to resonance circuit
  - Resonance dip at f_0

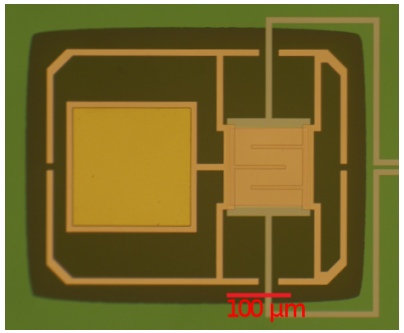
→ **Frequency Multiplex possible**

Frequency Division Multiplex Readout of Cryogenic Sensors

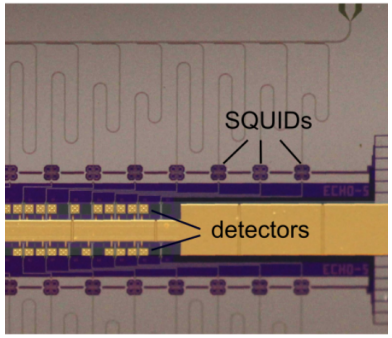




Microwave Kinetic Inductance Detectors[1]



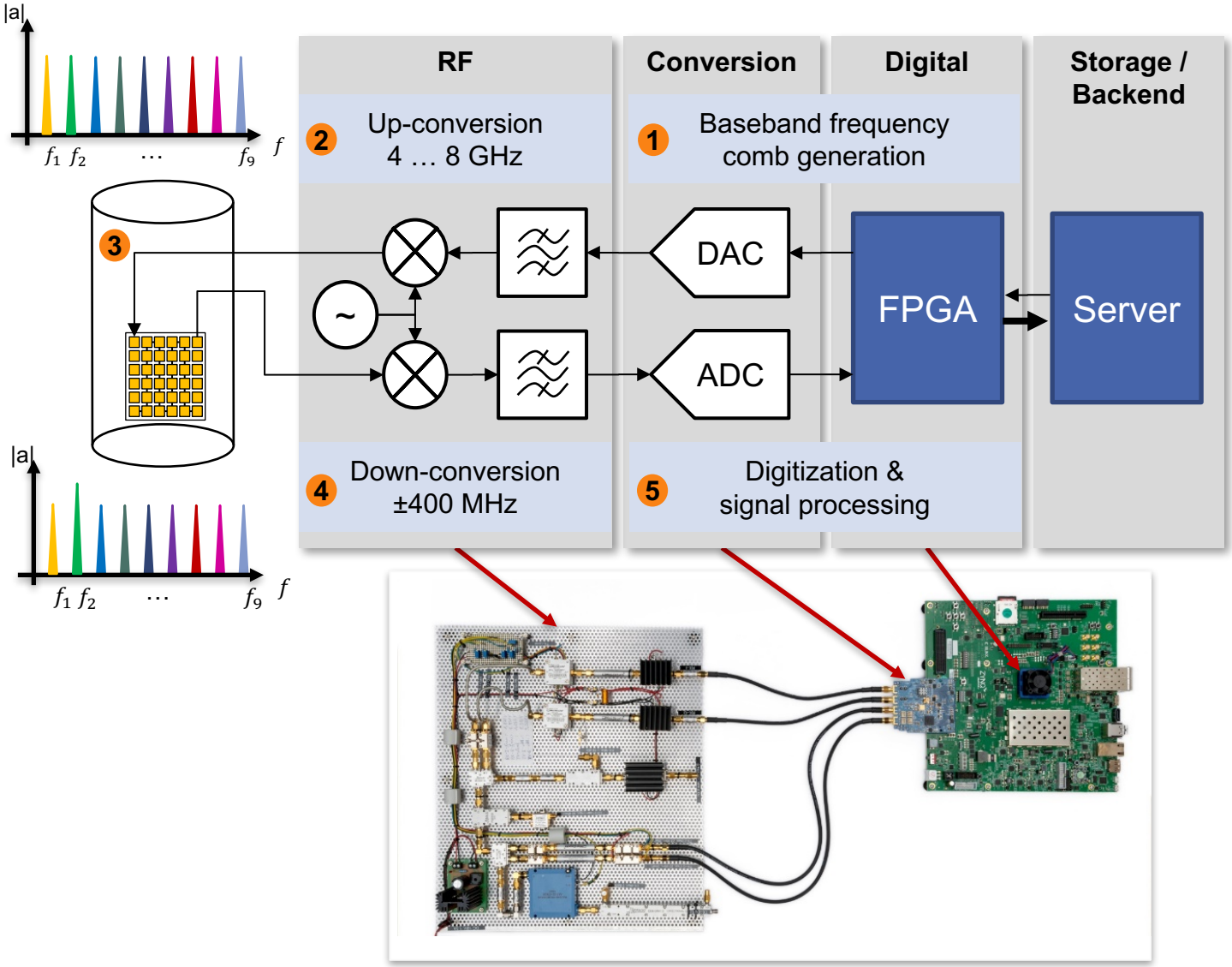
Transition Edge Sensors[2]



Metallic Magnetic Calorimeters[3]

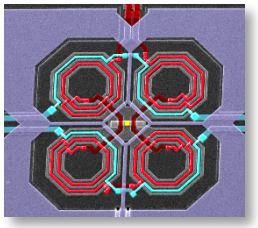
[1] Yates et al., arXiv: 1107.4330
[2] Giachero et al., arXiv: 1612.03947
[3] Kempf et al., AIP Advances, 2017

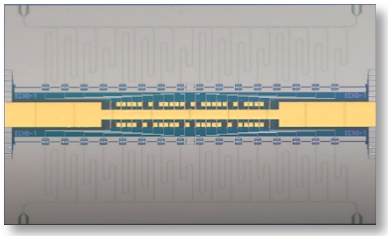
Readout Electronics Setup

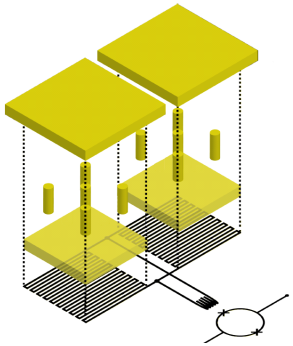


Electron Capture ^{163}Holmium experiment

The **E**lectron **C**apture ^{163}**Ho**lmium experiment **ECHo**[1] will investigate the electron neutrino mass by analyzing the energy spectrum in the electron capture process of ^{163}Ho using metallic magnetic calorimeters. The project aims to reach sub-eV sensitivity.



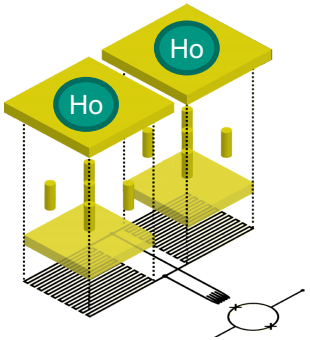


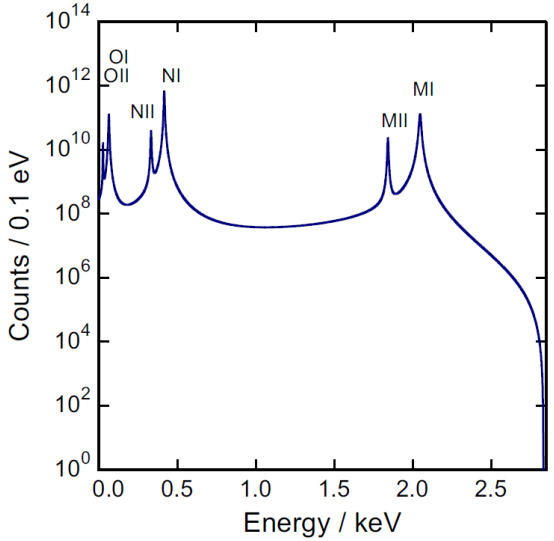


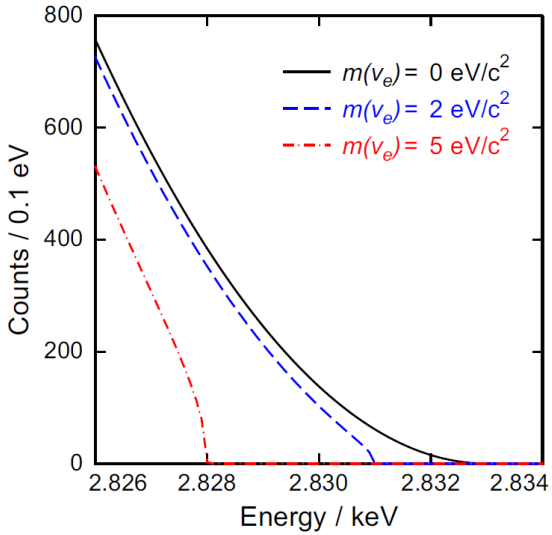
[4] Gastaldo et.al., Eur. Phys. J. Special Topics **226**, 1623–1694 (2017)

^{163}Ho Decay Process

$$^{163}Ho + e^- \rightarrow {}^{163}Dy^* + \nu_e$$
$$\hookrightarrow {}^{163}Dy + E_c$$







- Holmium Electron Capture
  - Electron-Neutrino is emitted
  - Dysprosium in excited state
- Available energy:
  $Q_{EC} = 2833$ eV
- Measured decay energy
  - Neutrino is not measured directly
  - De-excitation energy forms continuous spectrum
  - **Rare events at end-point & small mass of neutrino → high statistics → high resolution**

[1] Gastaldo et.al., Eur. Phys. J. Special Topics 226, 1623–1694 (2017)

ECHo Requirements

ECHo targeted activity

- 120k events/s, 10 Bq activity
- 12k sensors
- 6000 resonators

Frequency multiplex

- 4 – 8 GHz HEMT amplifier
- 1.6 MHz channel bandwidth
- 10 MHz spacing

Device specification

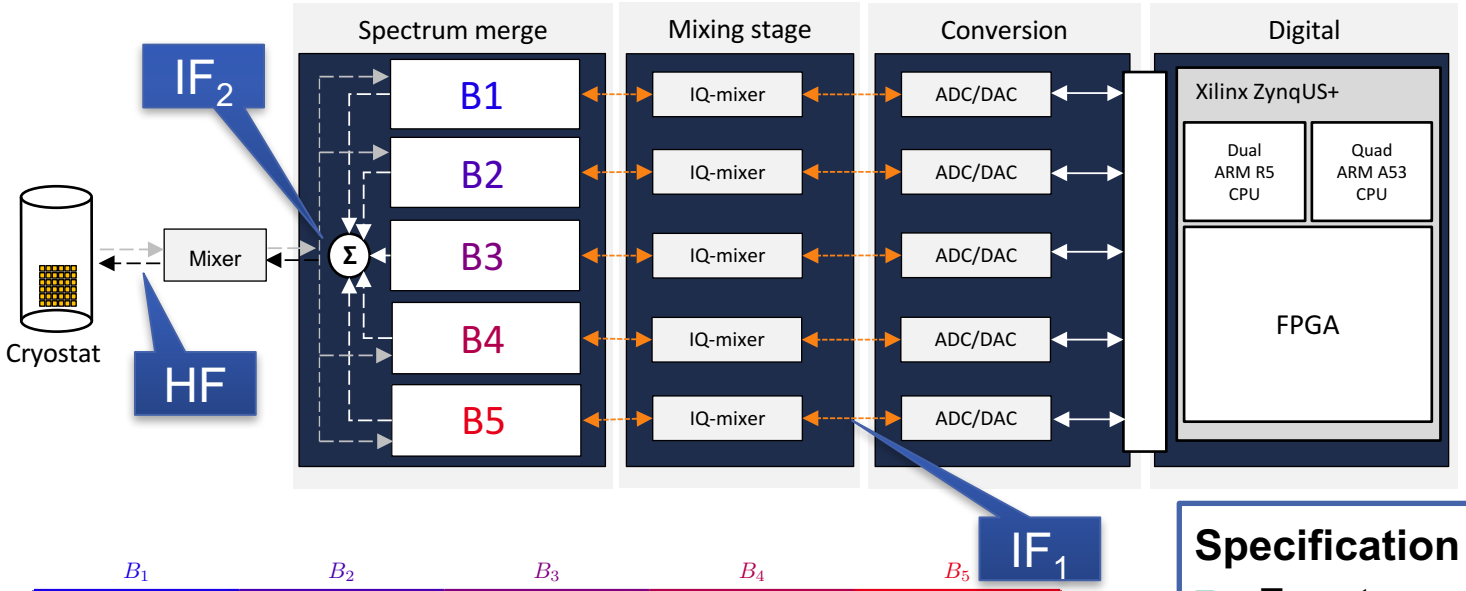
- **15 devices**
- 400 resonators per device
- **4 GHz real-time bandwidth**
  - **Generation & acquisition**

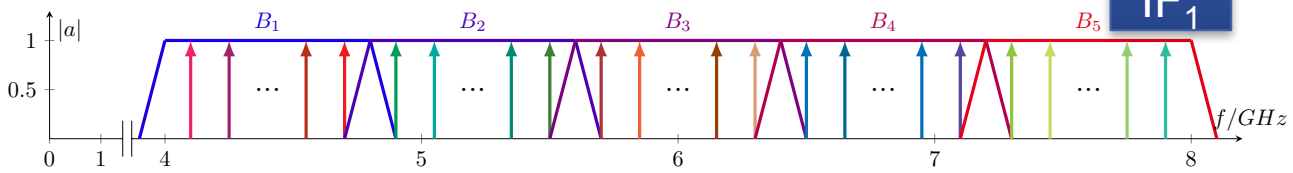
R&S® FSW, 5 GHz BW spectrum analyzer

Price: ~200 k€

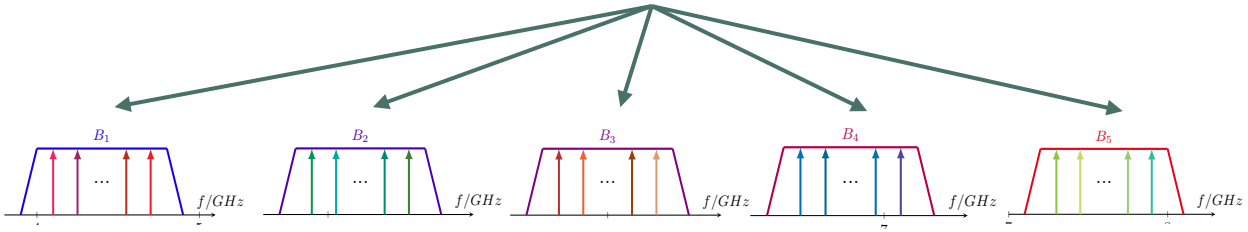
Total: 3 M€

Software-defined Radio (SDR) system architecture





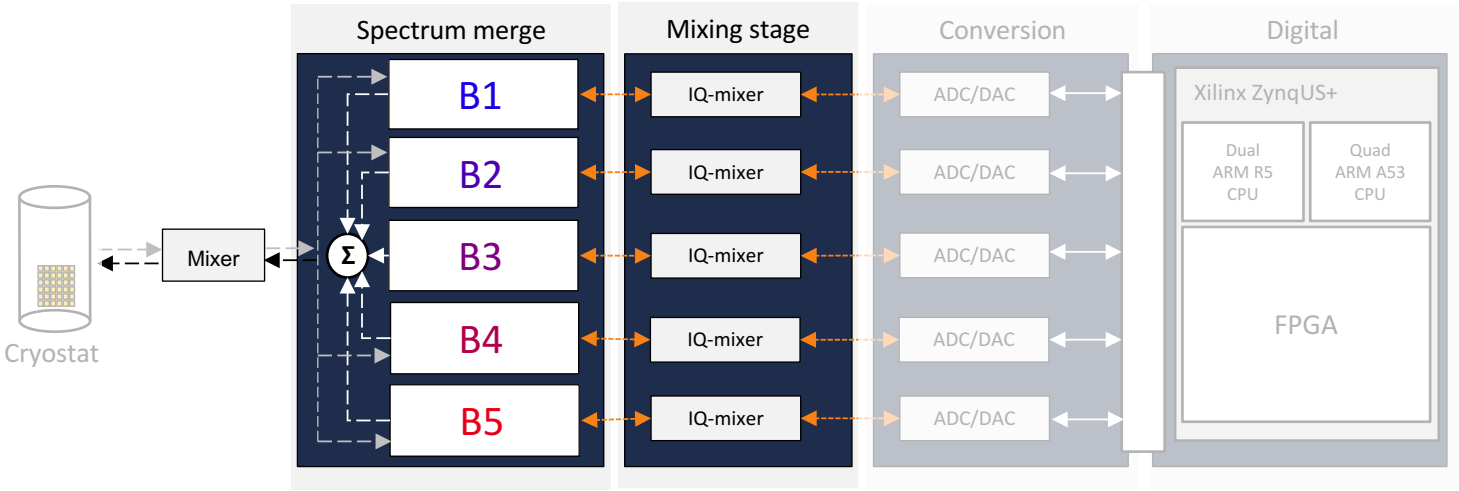
Spectrum of one single transmitter/receiver-pair (HF)



Five sub-band spectra in intermediate frequency (IF_1)

Specification

- Two stage mixing
- 2 x 5 x IQ mixers IF_1 to common IF_2 800 MHz each
- IF_2 from 0.5 – 4.5 GHz
- 2 x 2 Real mixers mixes IF_2 to HF band (4 – 8 GHz)
- Local oscillators integrated on board


Spectrum merge
Mixing stage
Conversion
Digital
B1
B2
B3
B4
B5
IQ-mixer
IQ-mixer
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ADC/DAC
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ADC/DAC
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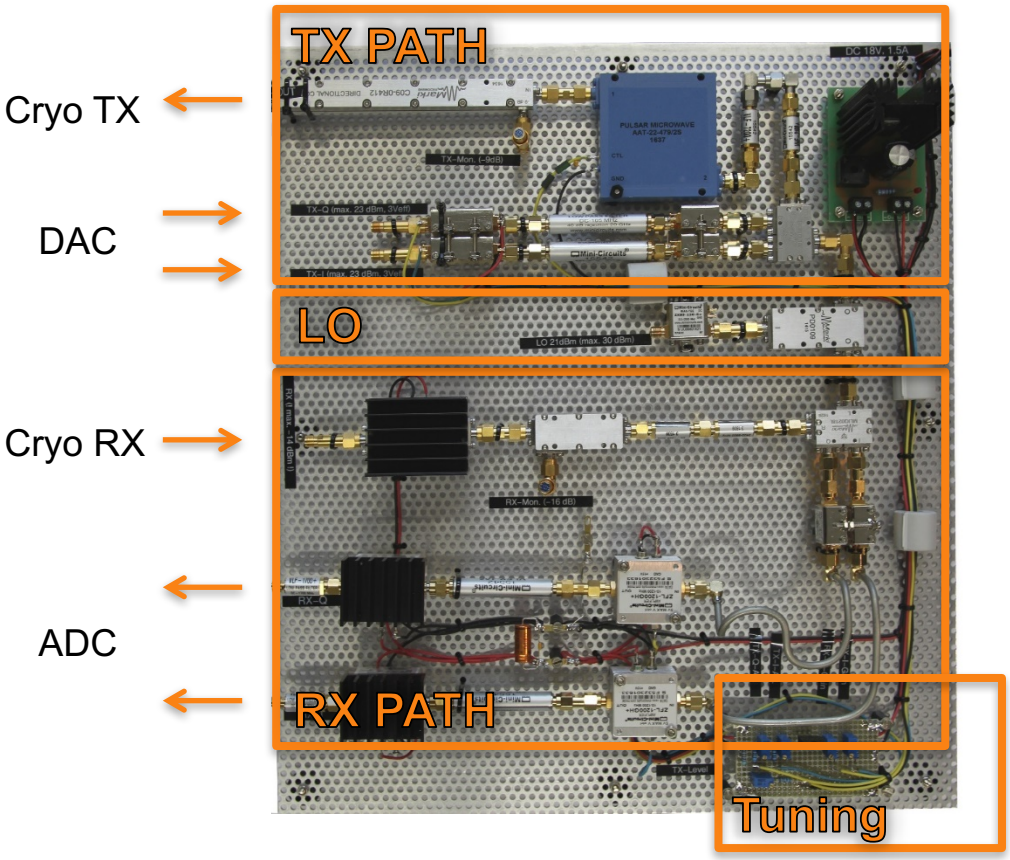
Xilinx ZynqUS+
Dual ARM R5 CPU
Quad ARM A53 CPU
FPGA
Σ
Mixer
Cryostat

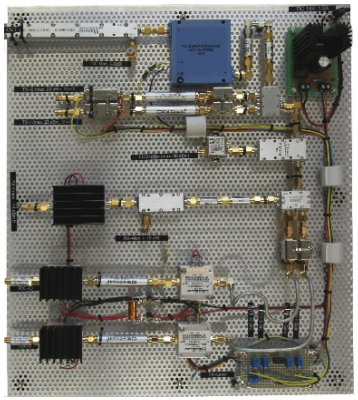
RF conversion V1.0



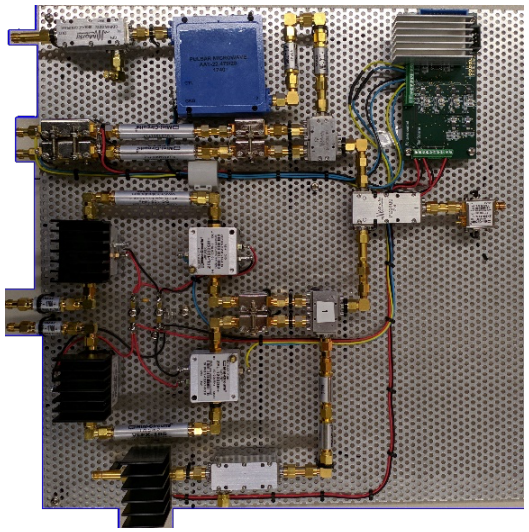
- RF band (single stage)
  - IQ-Mixers (2 – 18 GHz)
  - Filters 4 – 8 GHz
- Base band
  - 0 – 2 GHz
  - Filters 230 MHz (460 MHz IQ bandwidth)
  - 29 dB sideband suppression
- Power supply
- Variable attenuation and amplification (Manual Tuning)
- Monitoring
- External RF signal source (LO)

[5] O. Sander, N. Karcher, O. Krömer et al. PoS TWEPP17 2017

Evolution of RF conversion

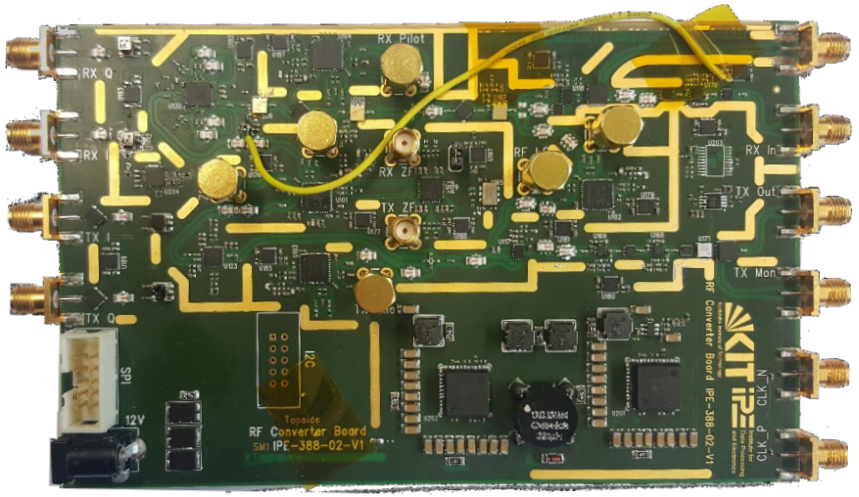


Version 1.0



Version 1.1

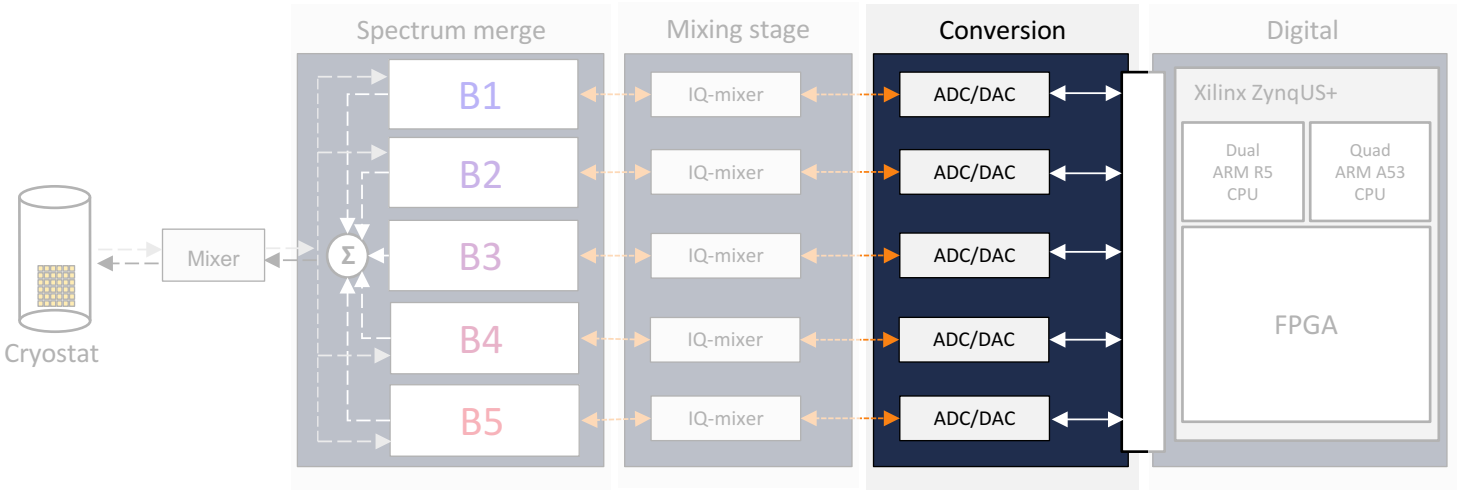
+ Low noise supply
+ Digitally controllable (I^2C)



Version 3.0

+ Integrated on PCB
+ Two stage mixing (one channel)
+ Integrated rf sources
+ Digitally controllable (SPI)
+ Pilot tones for calibration
+ Cost efficient

*Version 2.0 build for readout of Qubits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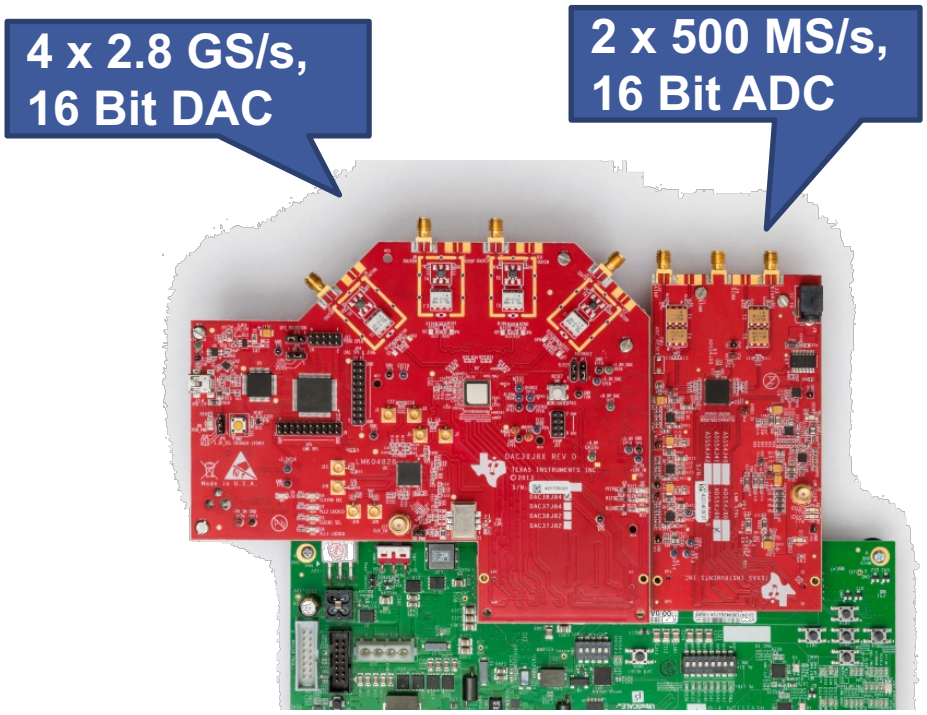
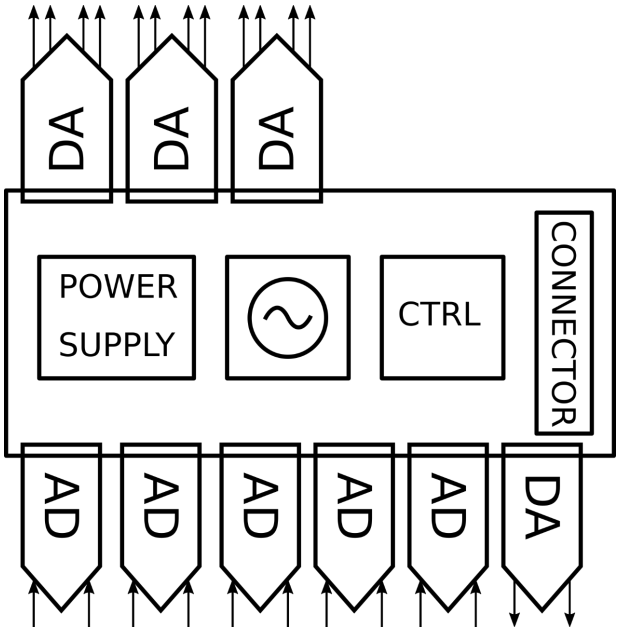
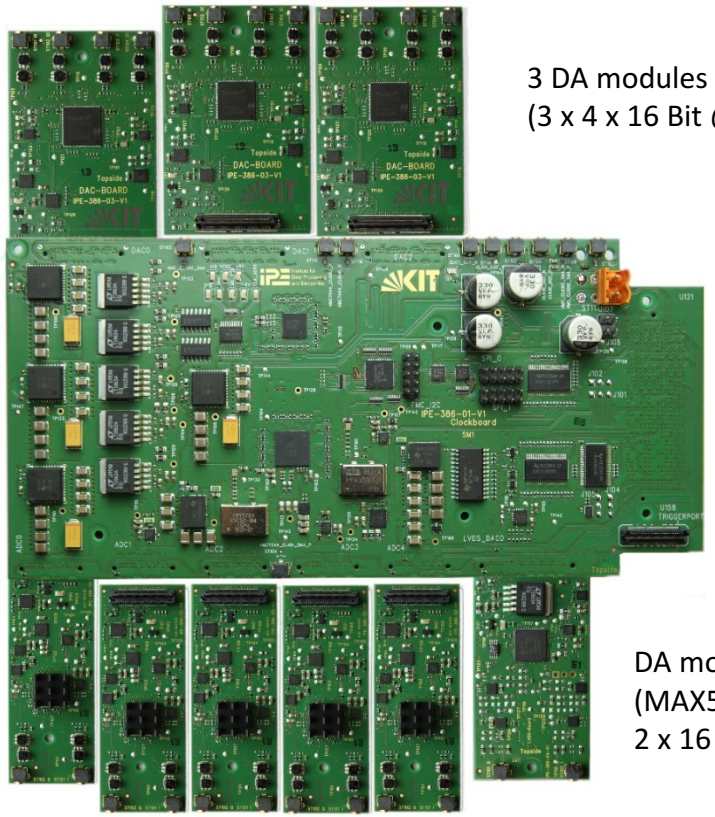
ECHo single channel AD/DA conversion



- Two independent evaluation boards from Texas Instruments
- FMC connectors for FPGA
- Single channel of the concept
- Offers bandwidth of < 500 MHz
  → 4 GHz required

Modular Conversion Board





3 DA modules (AD9144)
(3 x 4 x 16 Bit @ 2.8 GS/s)

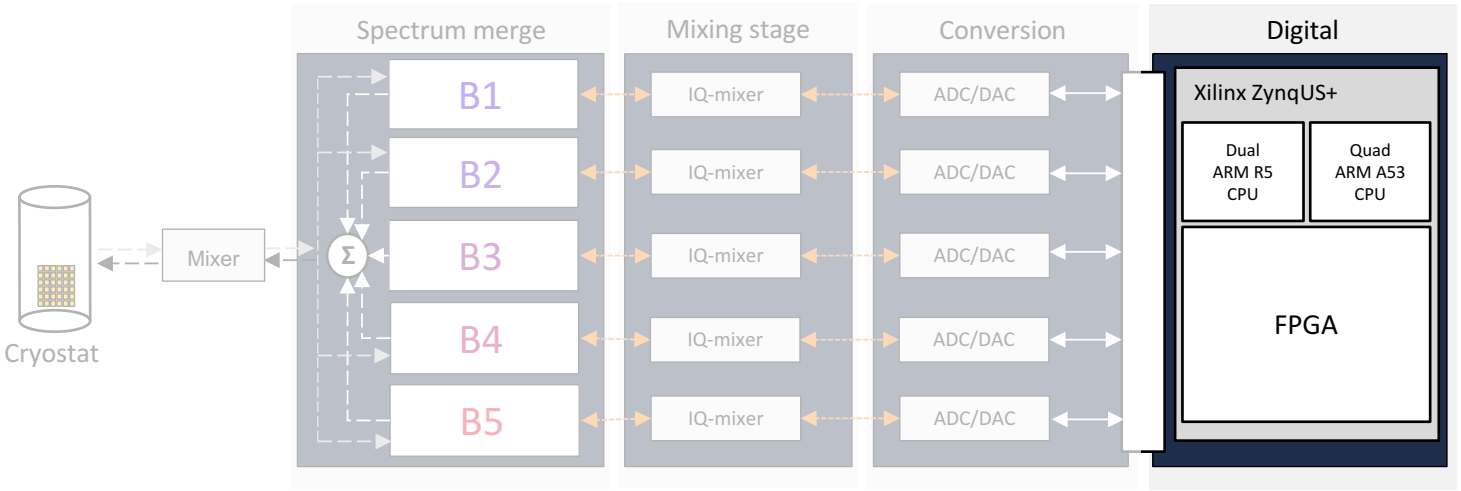
DA module
(MAX5898)
2 x 16 Bit

5 AD modules (AD9680)
(5 x 2 x 14 bit@ 1 GS/s)

- Common clock domain
- Channelization trough digital down conversion in AD converter
- FMC+ connector for FPGA

Data rate of 20 GB/s (bidirectional)

[6] O. Sander, N. Karcher et. al. IEEE TNS 2019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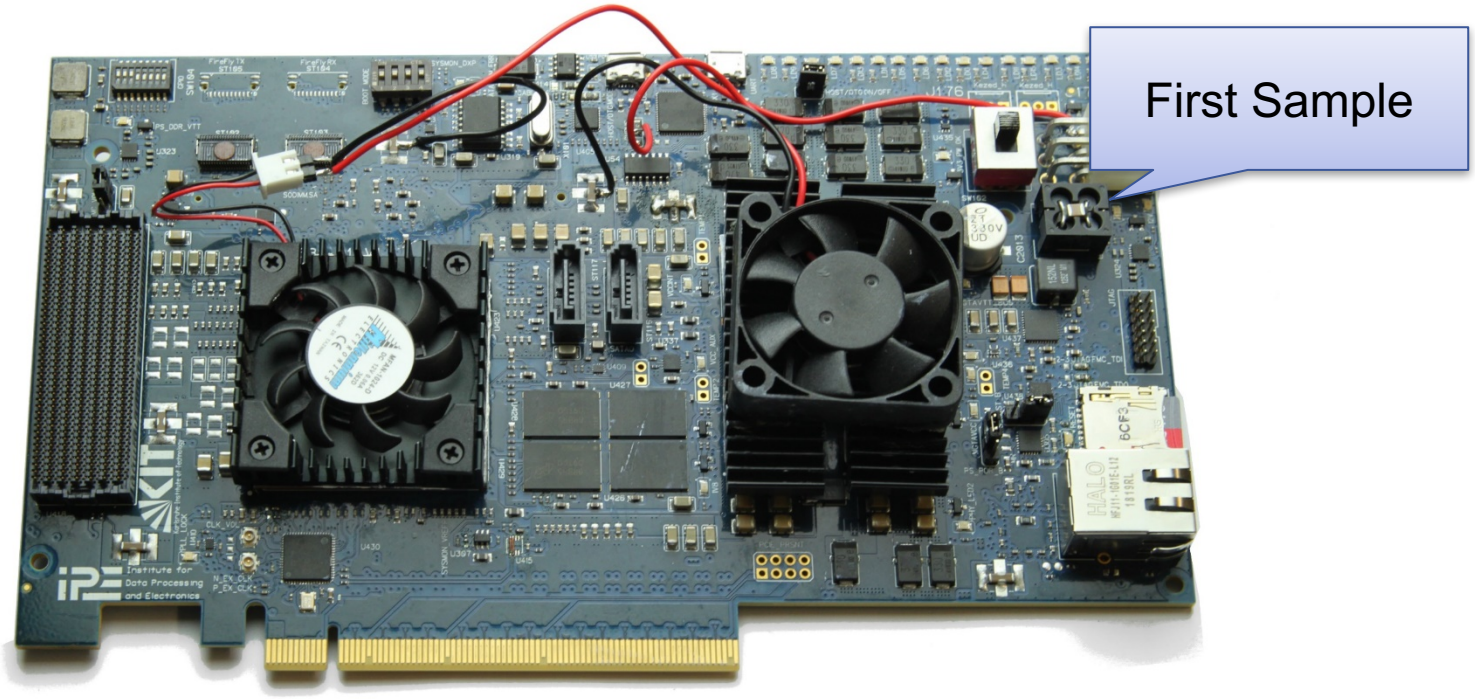
Processing Platform – IPE HiFlex2

Xilinx Zynq Ultrascale+ 11EG

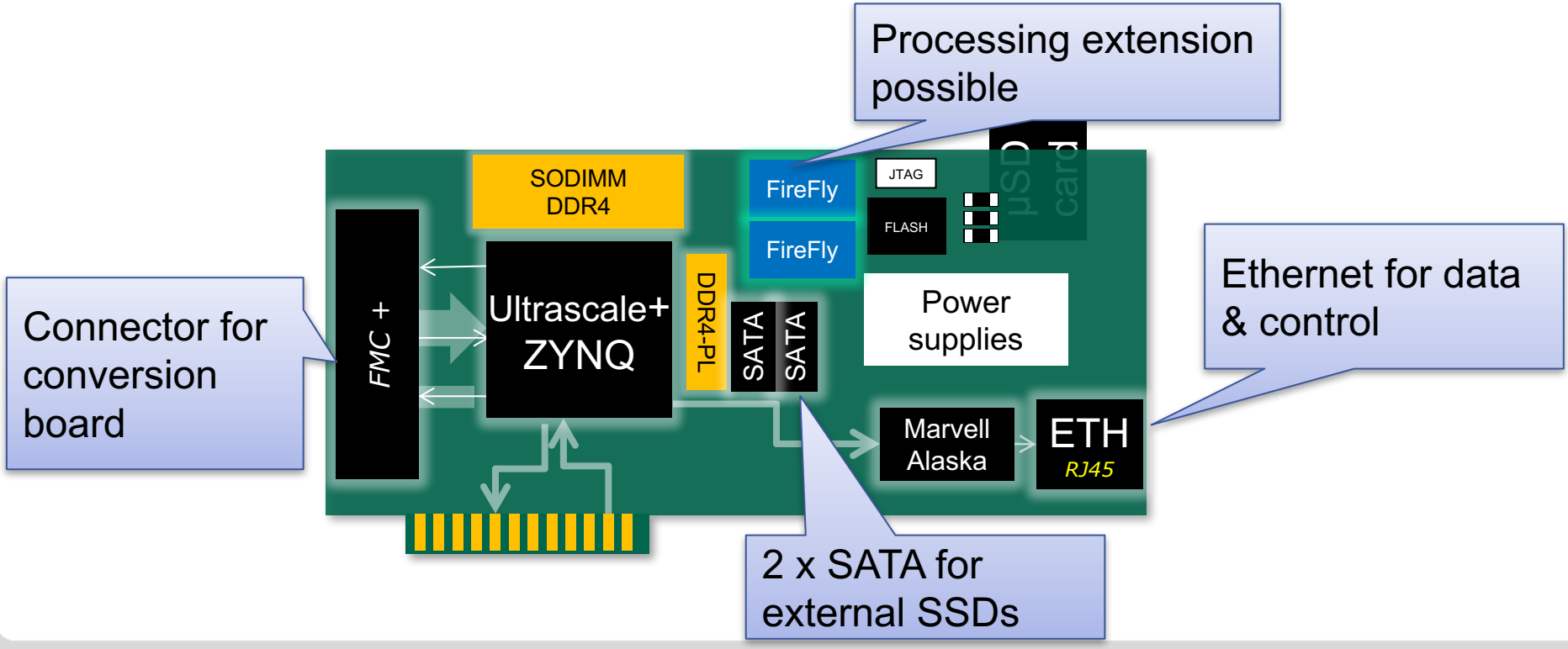
- 4-core ARM Cortex-A53 processor for light processing and control
- 2-core ARM Cortex R5 real-time processor for system management
- Second largest Field Programmable Gate Array (FPGA) in class



Processing Platform – IPE HiFlex2

Xilinx Zynq Ultrascale+ 11EG

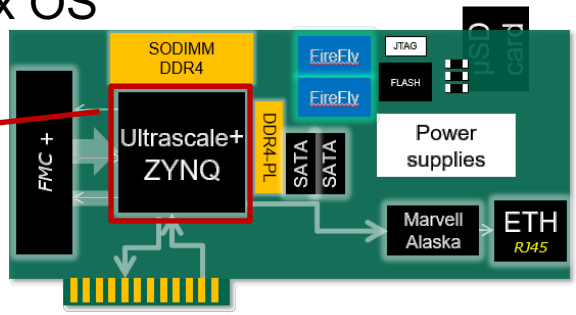
- 4-core ARM Cortex-A53 processor for light processing and control
- 2-core ARM Cortex R5 real-time processor for system management
- Second largest Field Programmable Gate Array (FPGA) in class

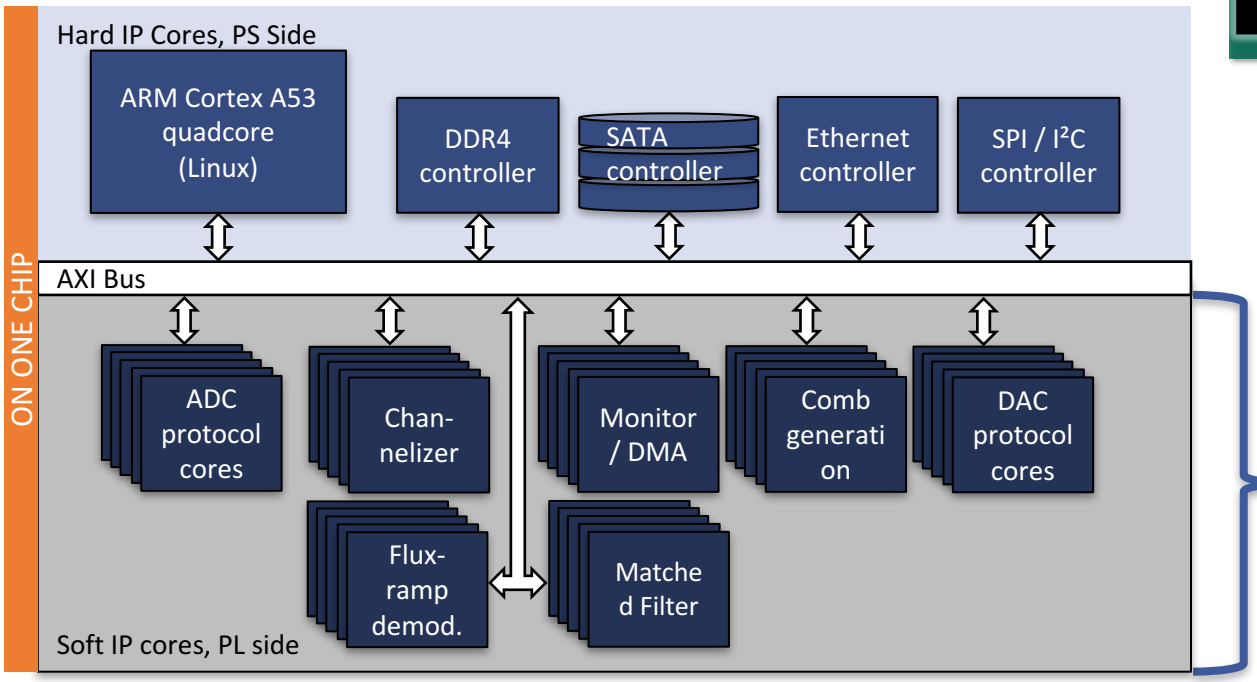


IPE HiFlex2 for ECHo

Xilinx Zynq Ultrascale+ 11EG

- Splits in processing and FPGA side
- All processing cores are controlled directly with Linux OS



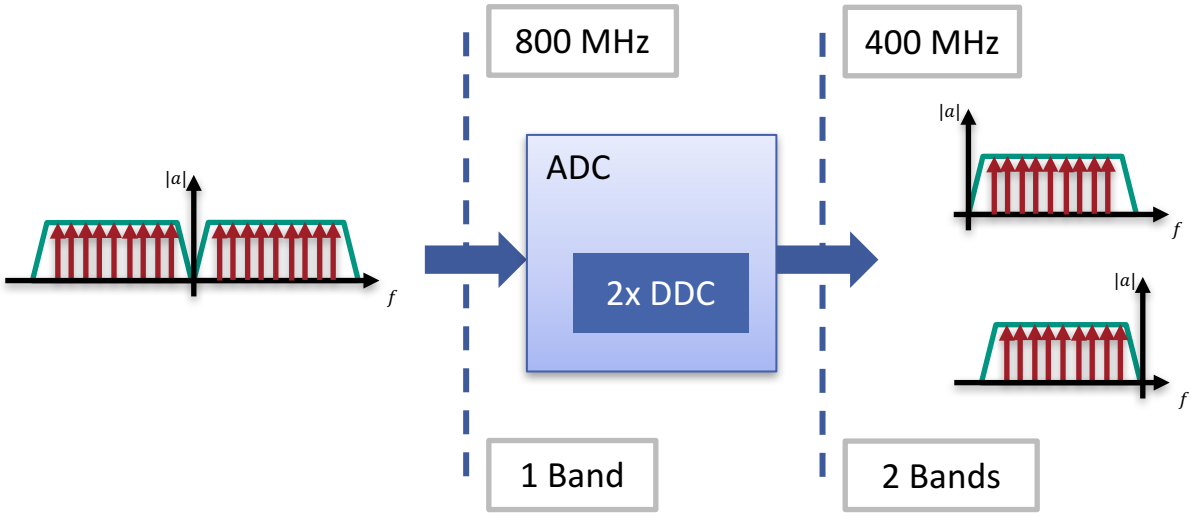


Signal processing modules and infrastructure for converters and data

[6] O. Sander, N. Karcher et. al. IEEE TNS 2019

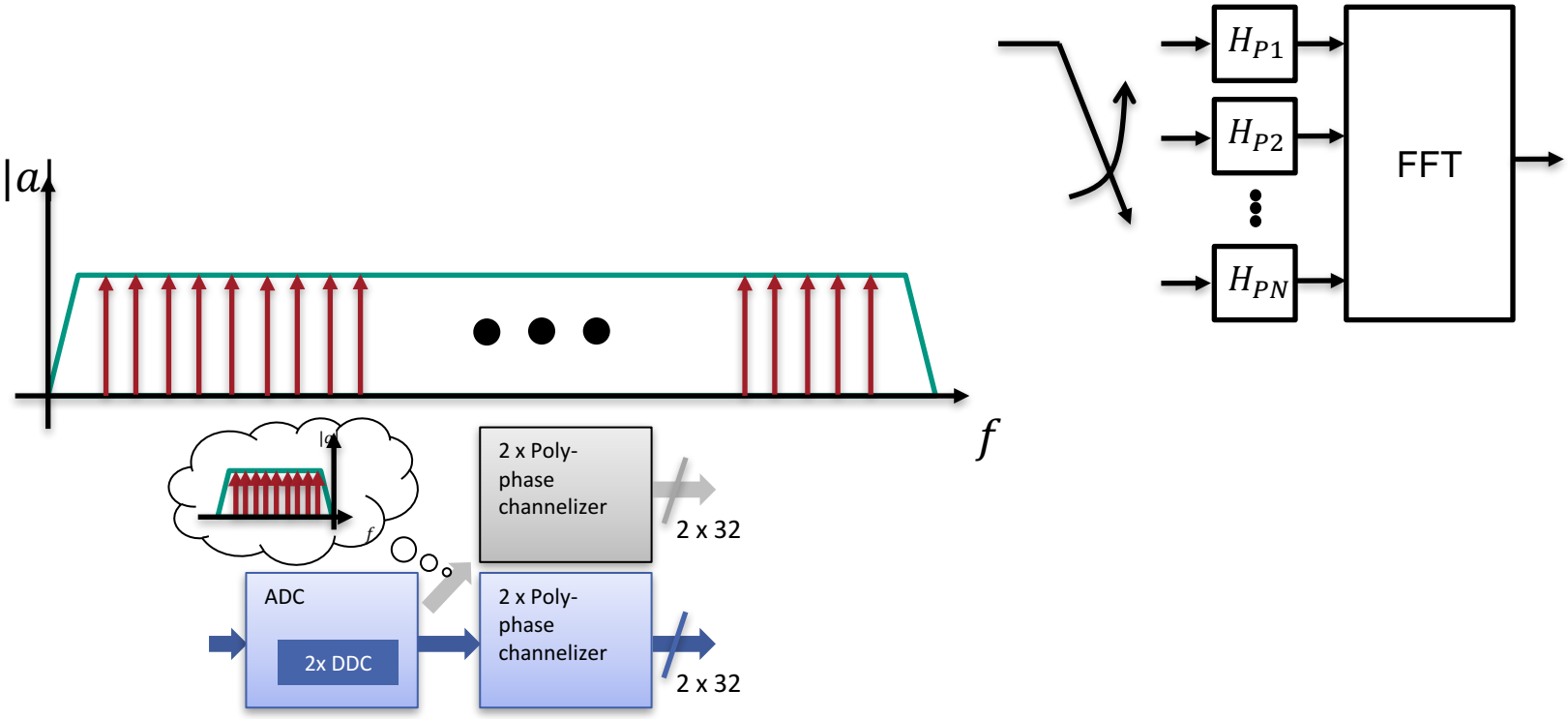
Channelization – spectrum split DDC

- ADC input: 800 MHz signal bandwidth (1 GS/s)
- Splits spectrum in upper and lower sideband with 400 MHz BW
- Digital down conversions (DDC) on ADC



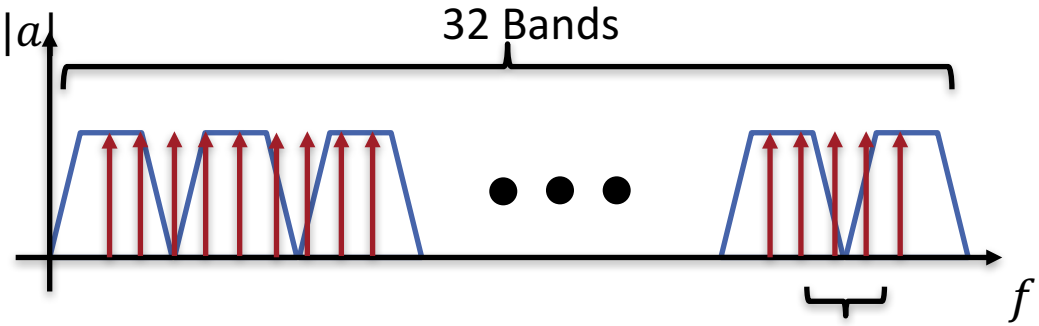
Channelization – poly-phase channelizer

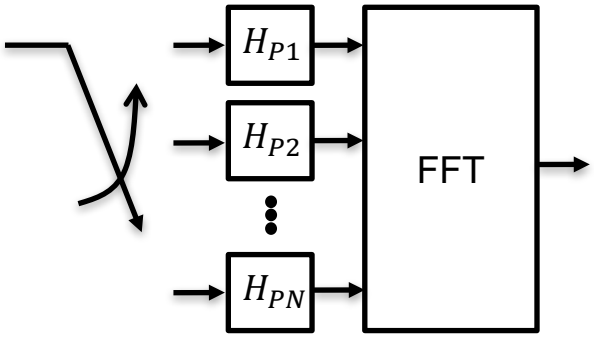
- One channelizer pair for upper, one pair for lower sideband

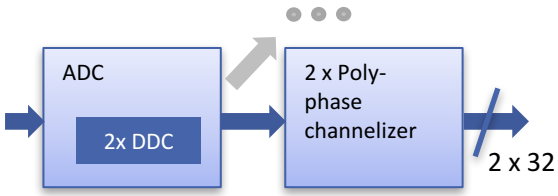


Channelization – poly-phase channelizer

- One channelizer pair for upper, one pair for lower sideband
- Decimates sampling frequency to 15.625 MHz, filters and down converts signal
- 11 MHz sub-band contains 1-2 resonators

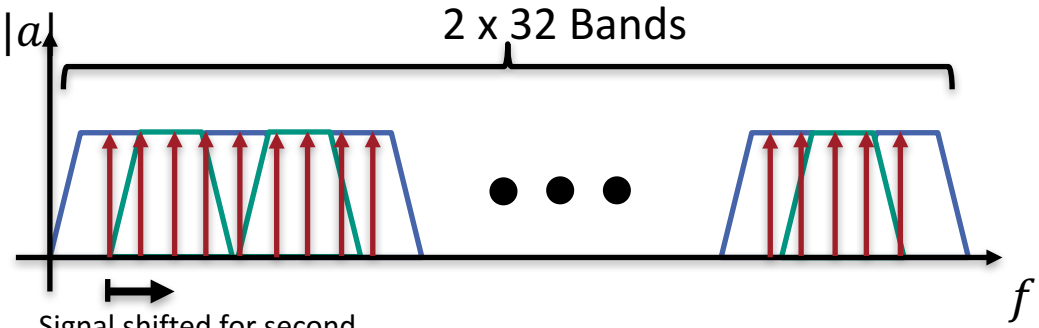


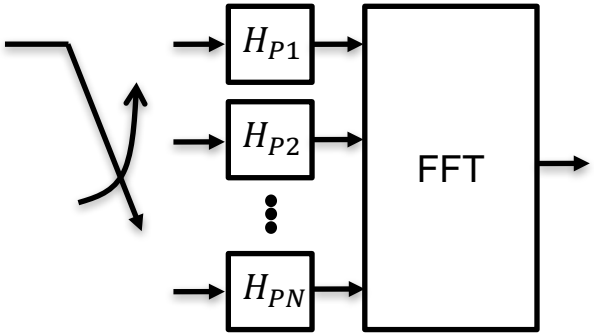


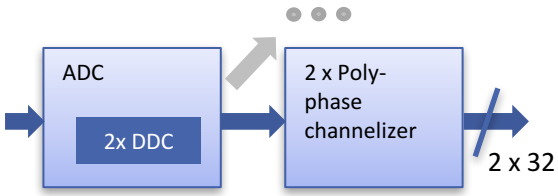


Channelization – poly-phase channelizer

- One channelizer pair for upper, one pair for lower sideband
- Decimates sampling frequency to 15.625 MHz, filters and down converts signal
- 11 MHz sub-band contains 1-2 resonators
- 2 x 32 overlapping sub-bands

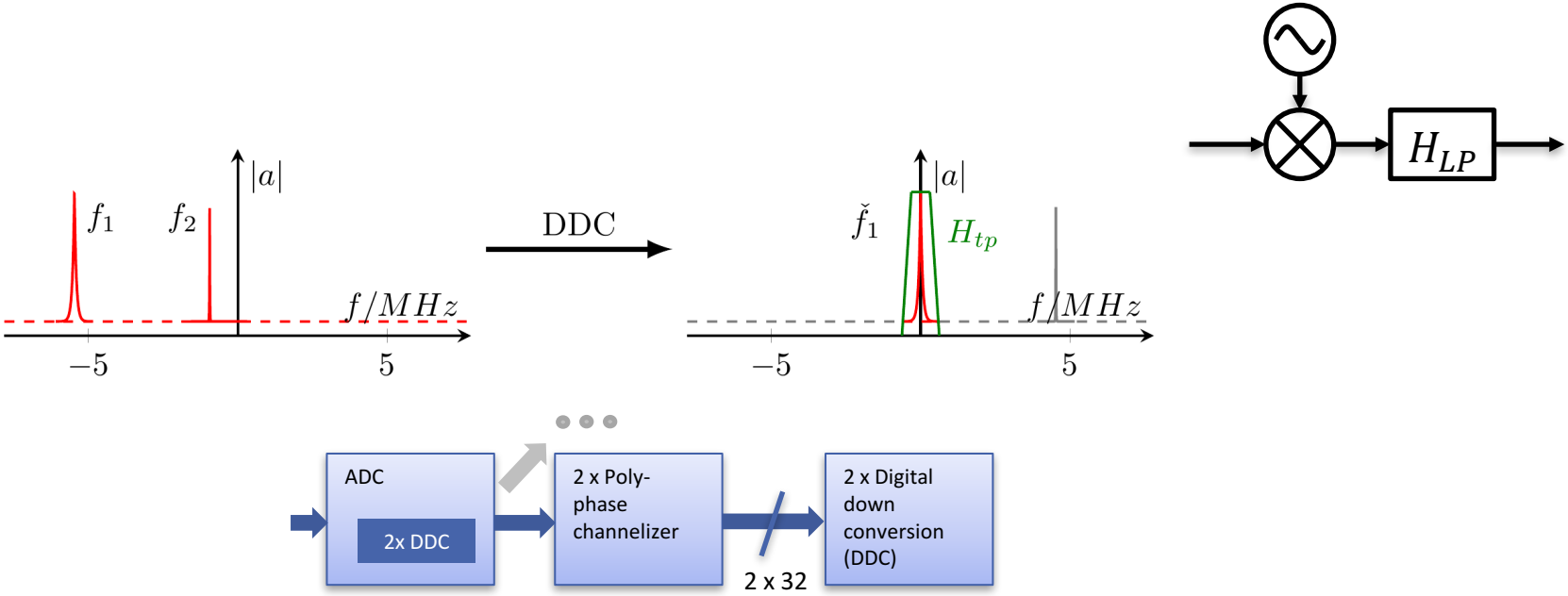




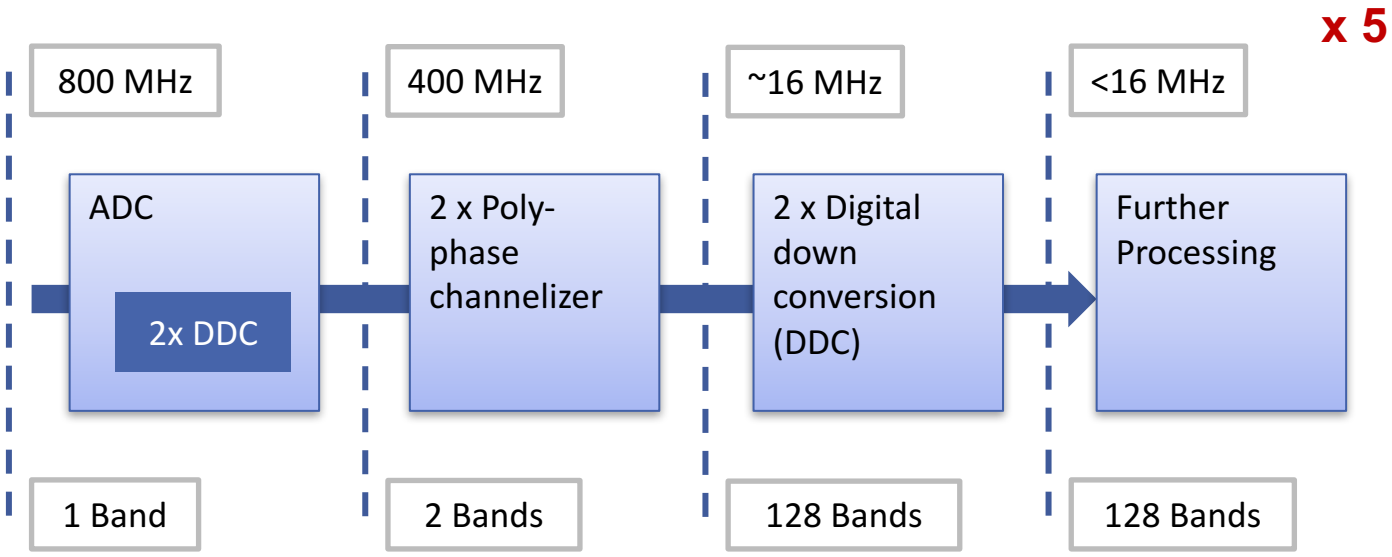


Channelization – demodulation DDC

- Multi channel DDC for amplitude and phase demodulation
- Low-pass filter to cancel other channels
- 32 channels processed in one data cycle
- Output: Individual resonator signals with 1 MHz bandwidth



Channelization – cascade overview



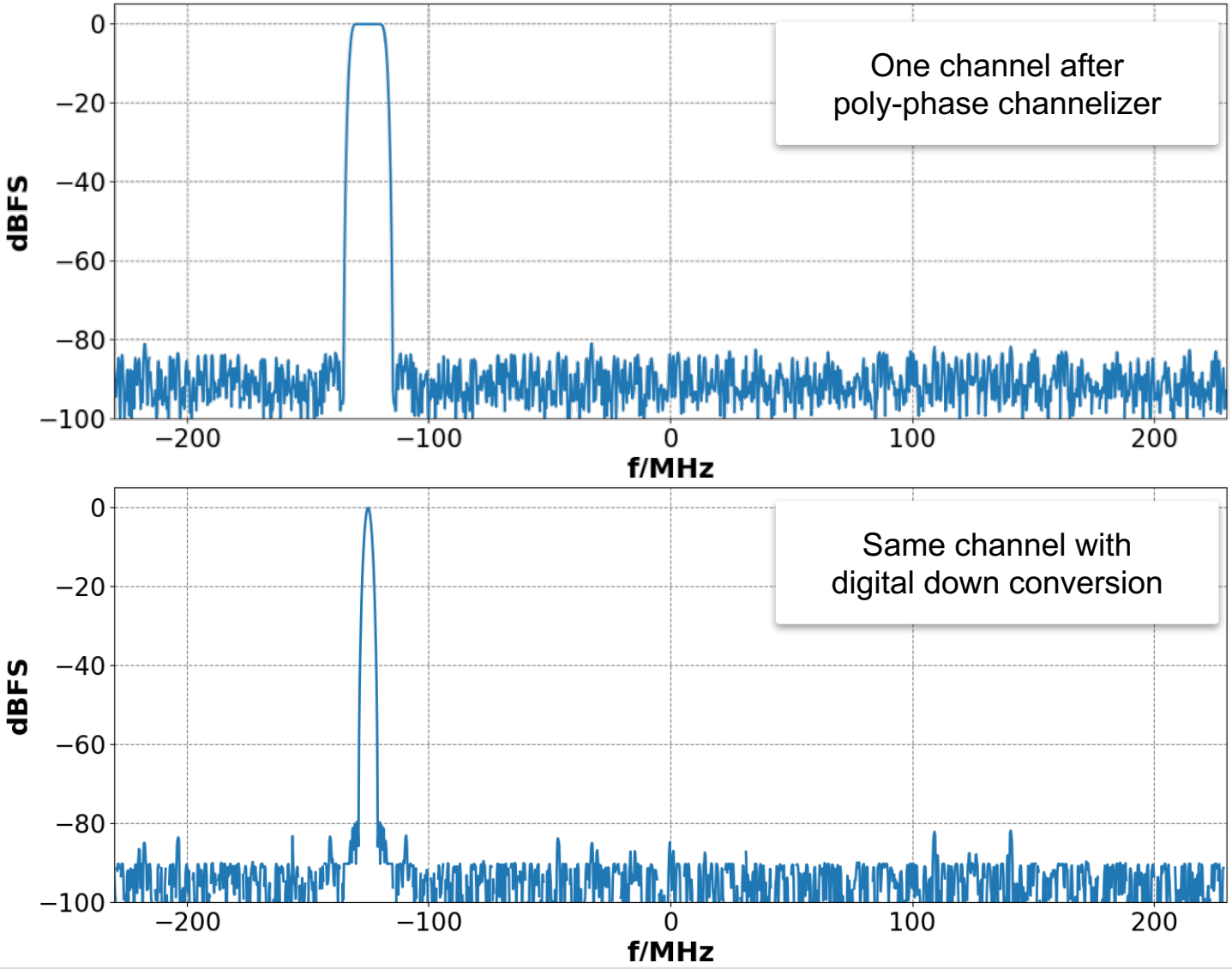
- Optimized digital down conversion with multirate filters
  - 19 DSP / Channel
  - 2 36k-BRAM / Channel

x 8.5 efficiency

- Resources cascade with poly-phase channelizer
  - 2.22 DSP / Channel
  - 0.04 36k-BRAM / Channel

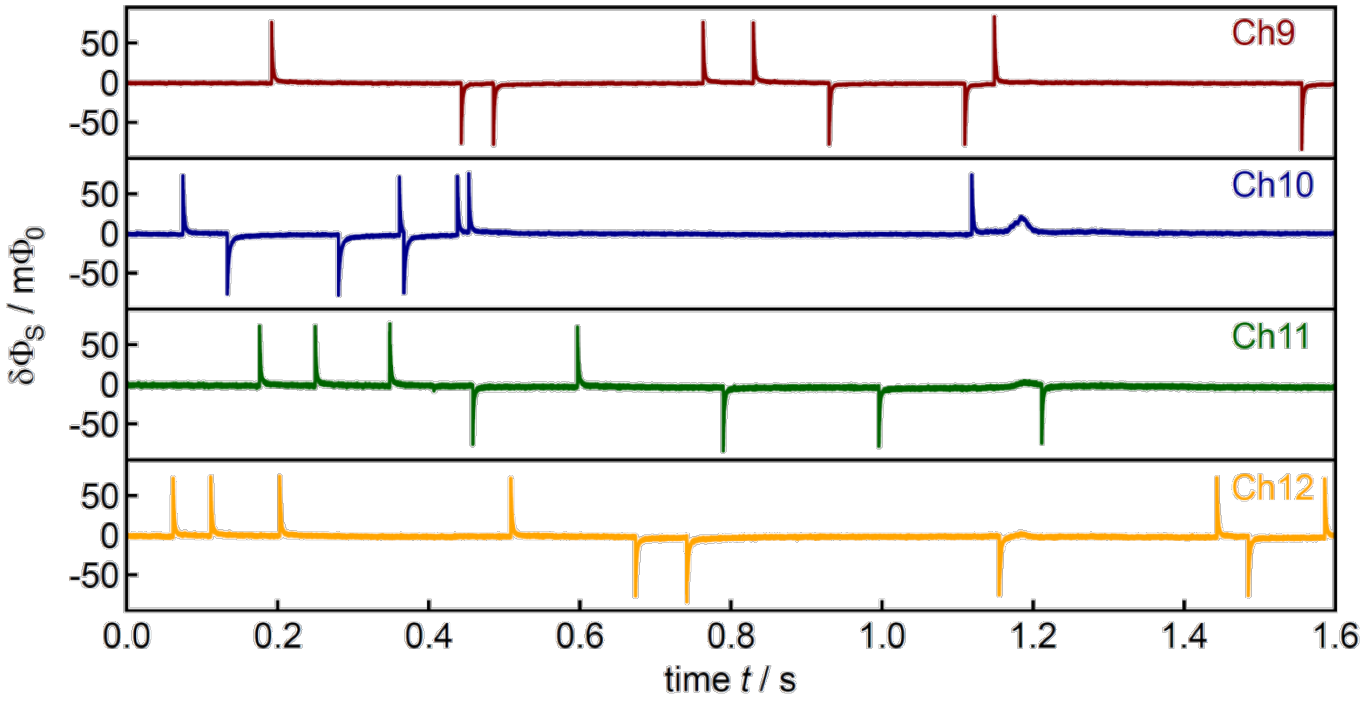
DSP: Digital Signal Processor
BRAM: Block RAM

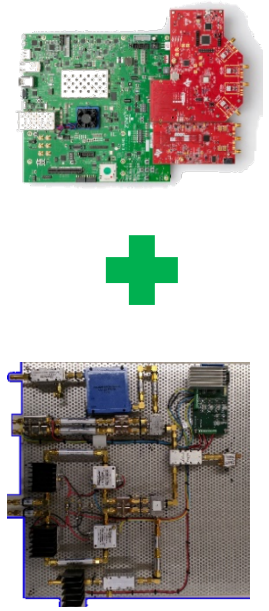
Filter Frequency Response



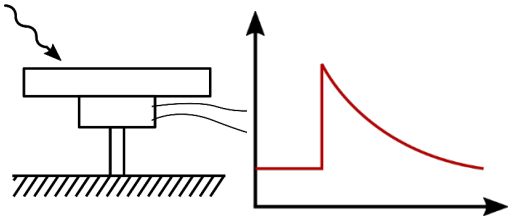
Multiplexed readout – 4 channels / 8 sensors

use of full muxing system including SDR electronics
(missing firmware modules replaced by offline software analysis, restriction to four channels)

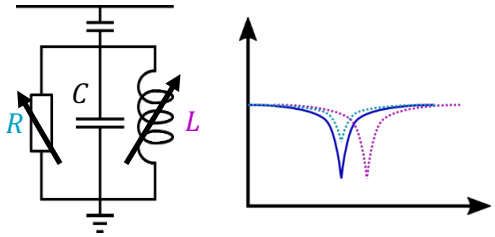




Summary

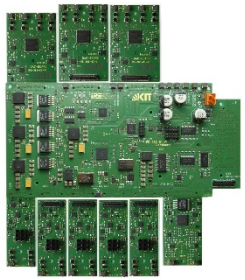


Precise cryogenic calorimeters

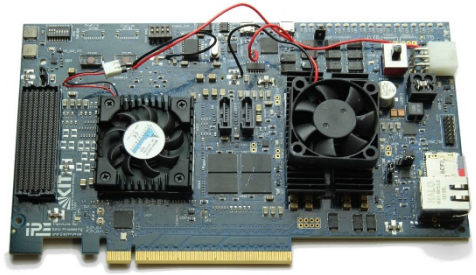


Multiplex through microwave resonators

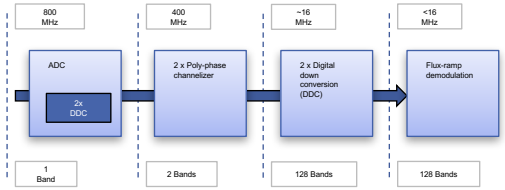
Conversion between MHz and GHz



Broadband AD/DA conversion

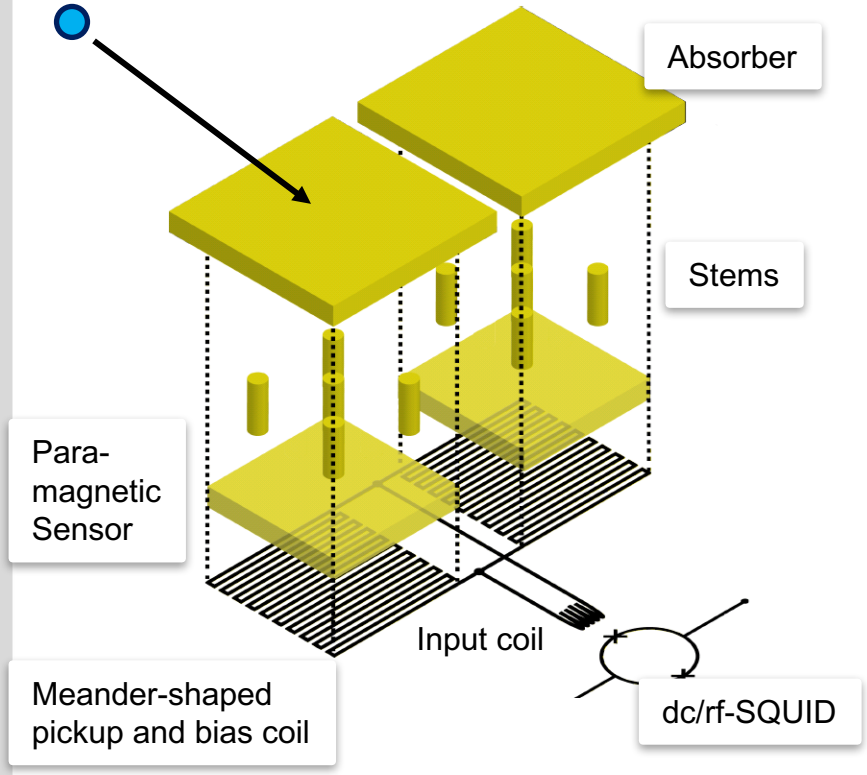


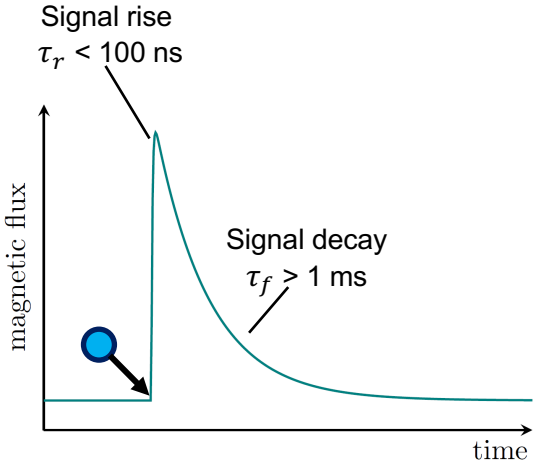
SoC-FPGA perfoms digital processing



Digital channelizer for demultiplex

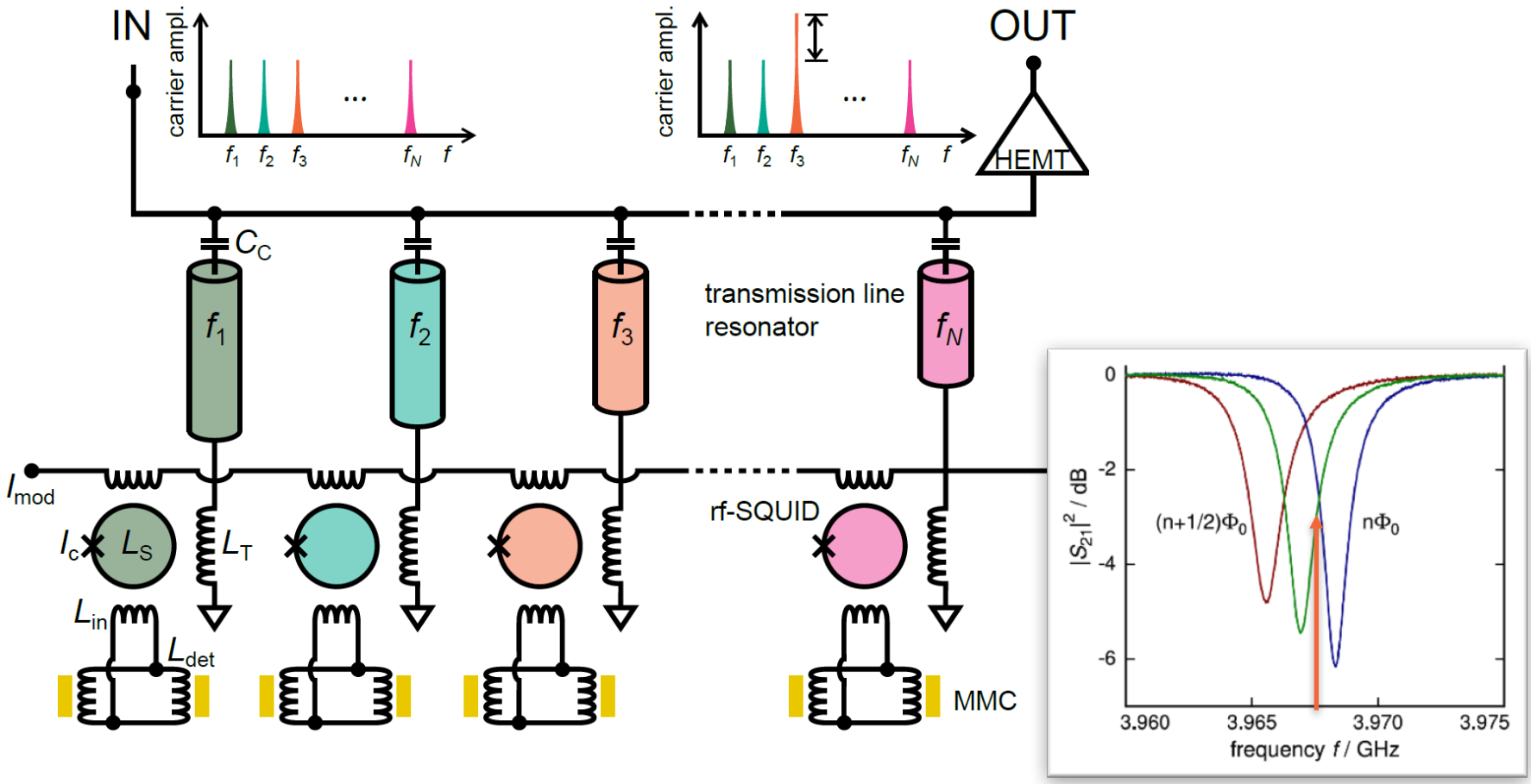
Metallic Magnetic Calorimeters (MMCs)



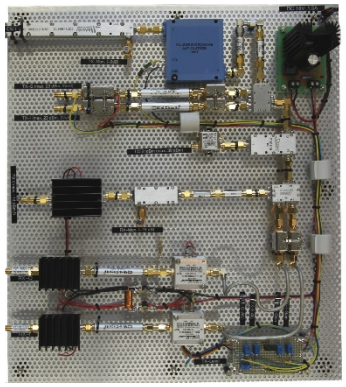


Fast signal rise time:	τ_r < 100 ns
Very good energy resolution:	ΔE_{FWHM} = 1.6 eV @ 6 keV
Large energy bandwidth:	eV to 100 keV
Excellent linearity:	5.9 % @ 60 keV

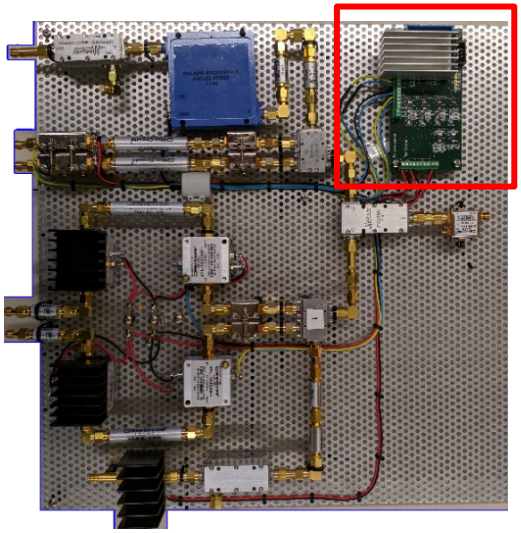
Resonator Frequency Multiplex



Evolution of RF conversion

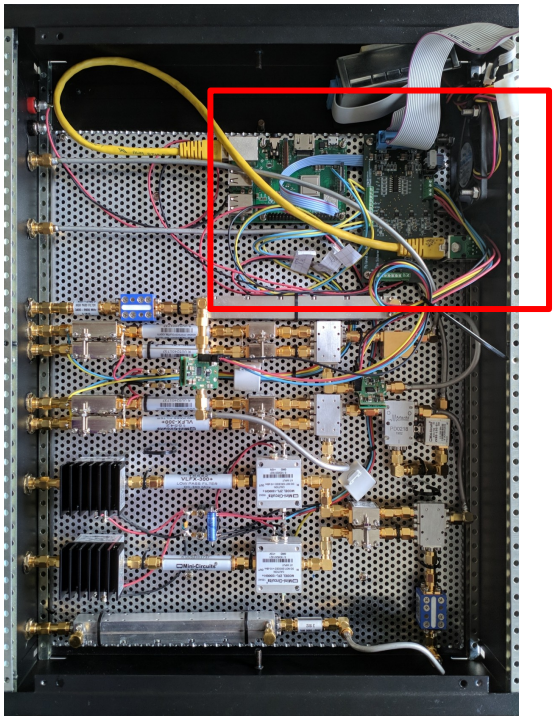


Version 1.0



Version 1.1

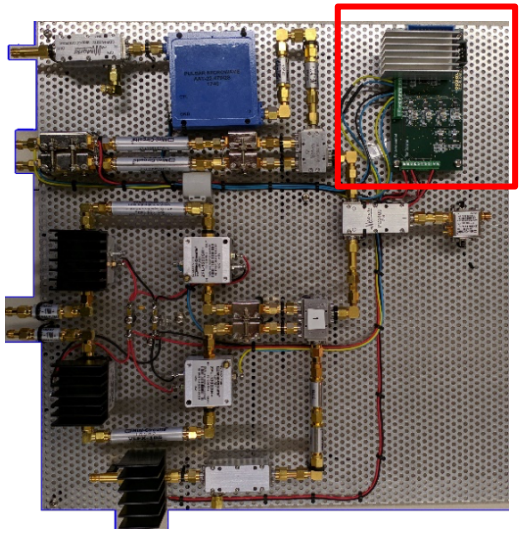
+ Low noise supply
+ Digitally controllable (I^2C)



Version 2.0 (for quantum bits)

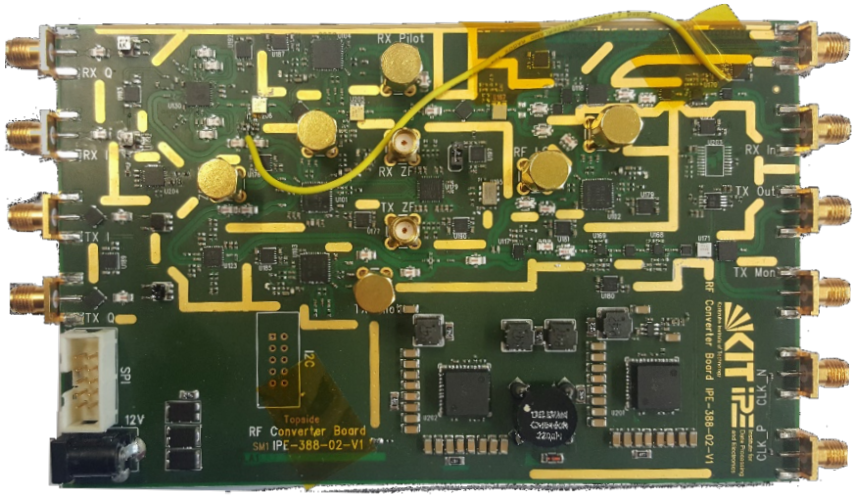
+ Second up-conversion path
+ Digitally controllable (Ethernet)

Evolution of RF conversion



Version 1.1

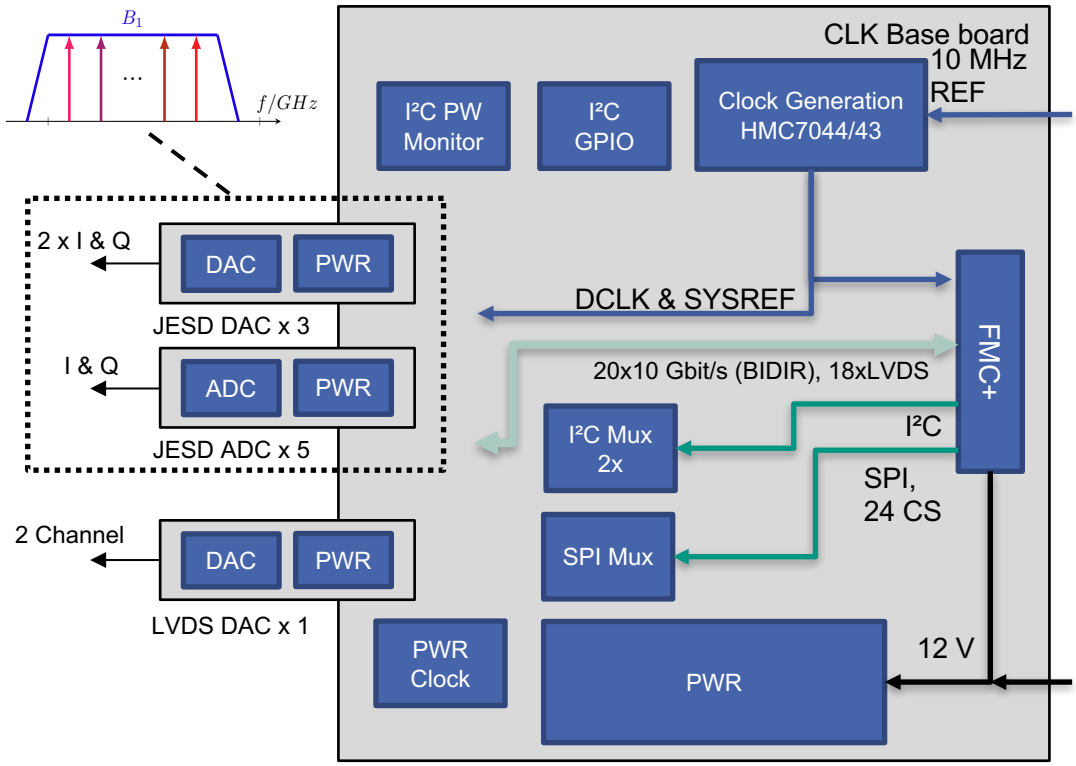
+ Low noise supply
+ Digitally controllable (I^2C)



Version 3.0

+ Integrated on PCB
+ Two stage mixing (One Channel)
+ Integrated rf sources
+ Digitally controllable (SPI)
+ Pilots for calibration
+ Cost efficient

Modular Conversion Board



Clock generation

- HMC7044
  - 2 stage PLL
  - ~55 fs @ 12k – 20MHz BW
  - ~115 fs total
- HMC7043 repeater
- Optional HF crystal for jitter below 100 fs

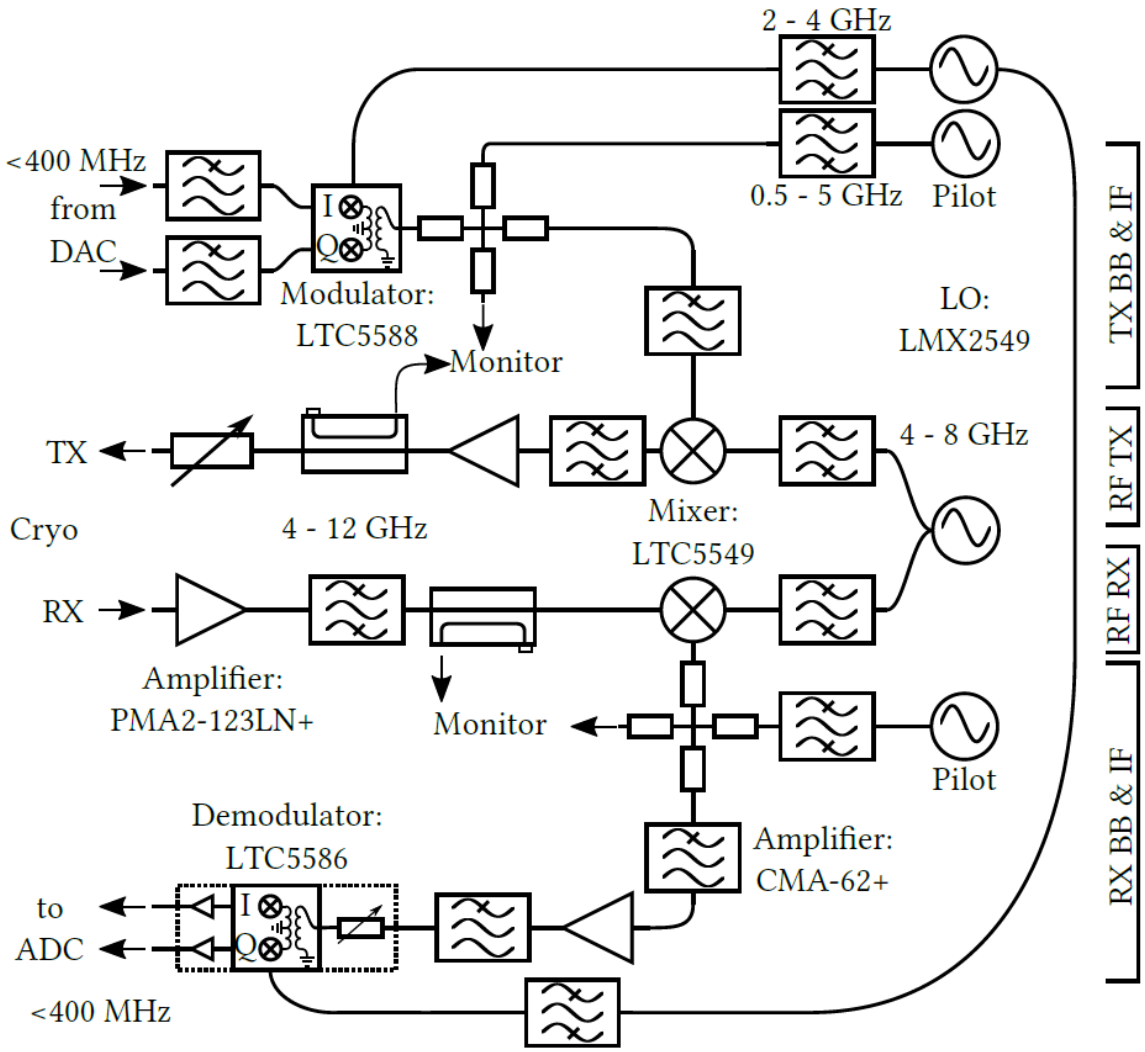
Converters (BW < 400 MHz)

- ADC – AD9680 (JESD204b)
  - 2 x 14 Bit @ 1 GS/s
  - 4 digital down conversions
- DAC – AD9144 (JESD204b)
  - 4 x 16 Bit @ 2.8 GS/s

Flux-ramp generation (BW < 30 MHz)

- DAC – MAX5898 (LVDS)
  - 2 x 16 Bit @ 500 MS/s
- Current or voltage source

HF Schematic



Channelization – Cascade Overview

- High data rate, five ADCs
- Time and space parallel execution
- Decimation required