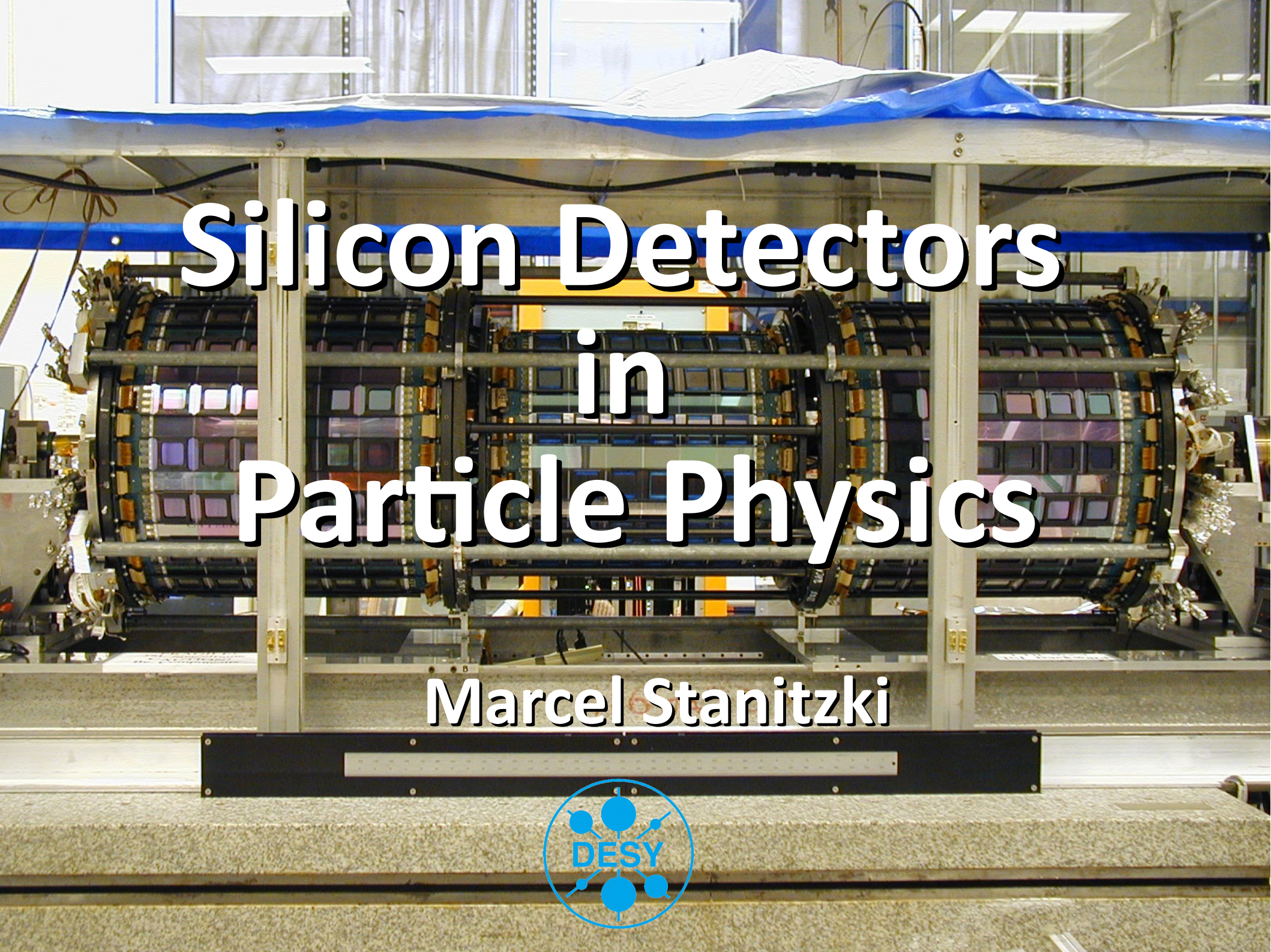
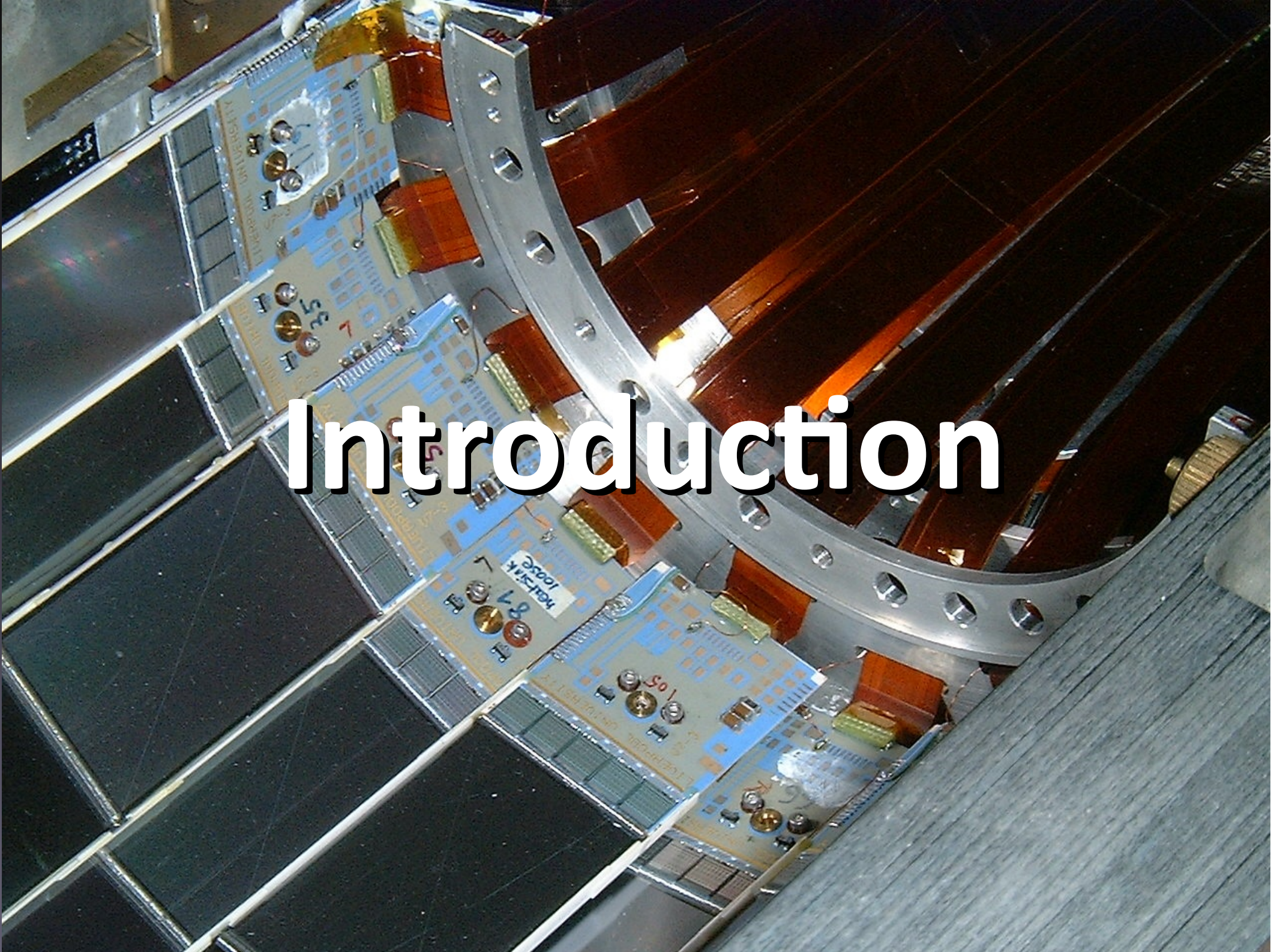


Silicon Detectors in Particle Physics

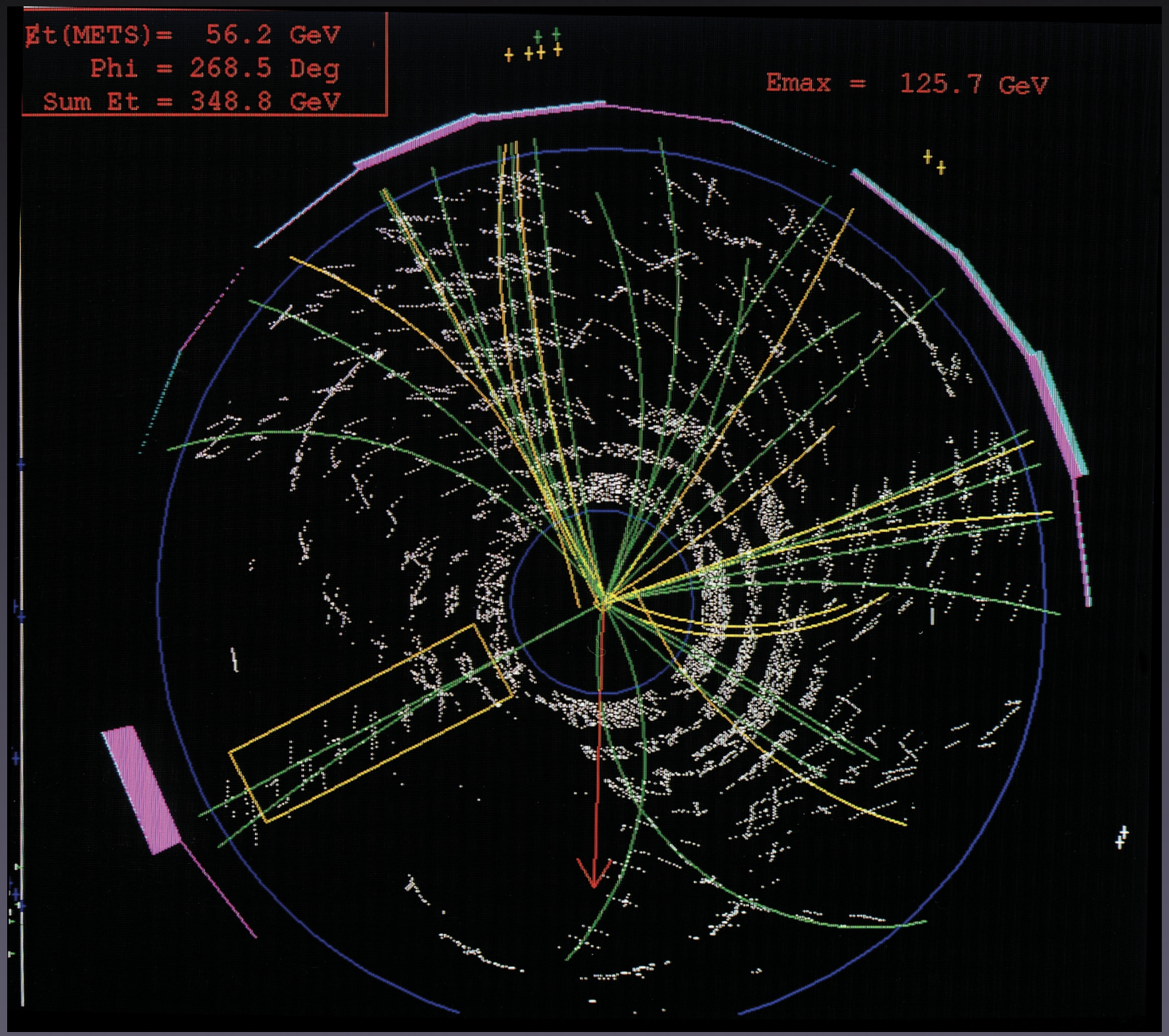
Marcel Stanitzki

DESY

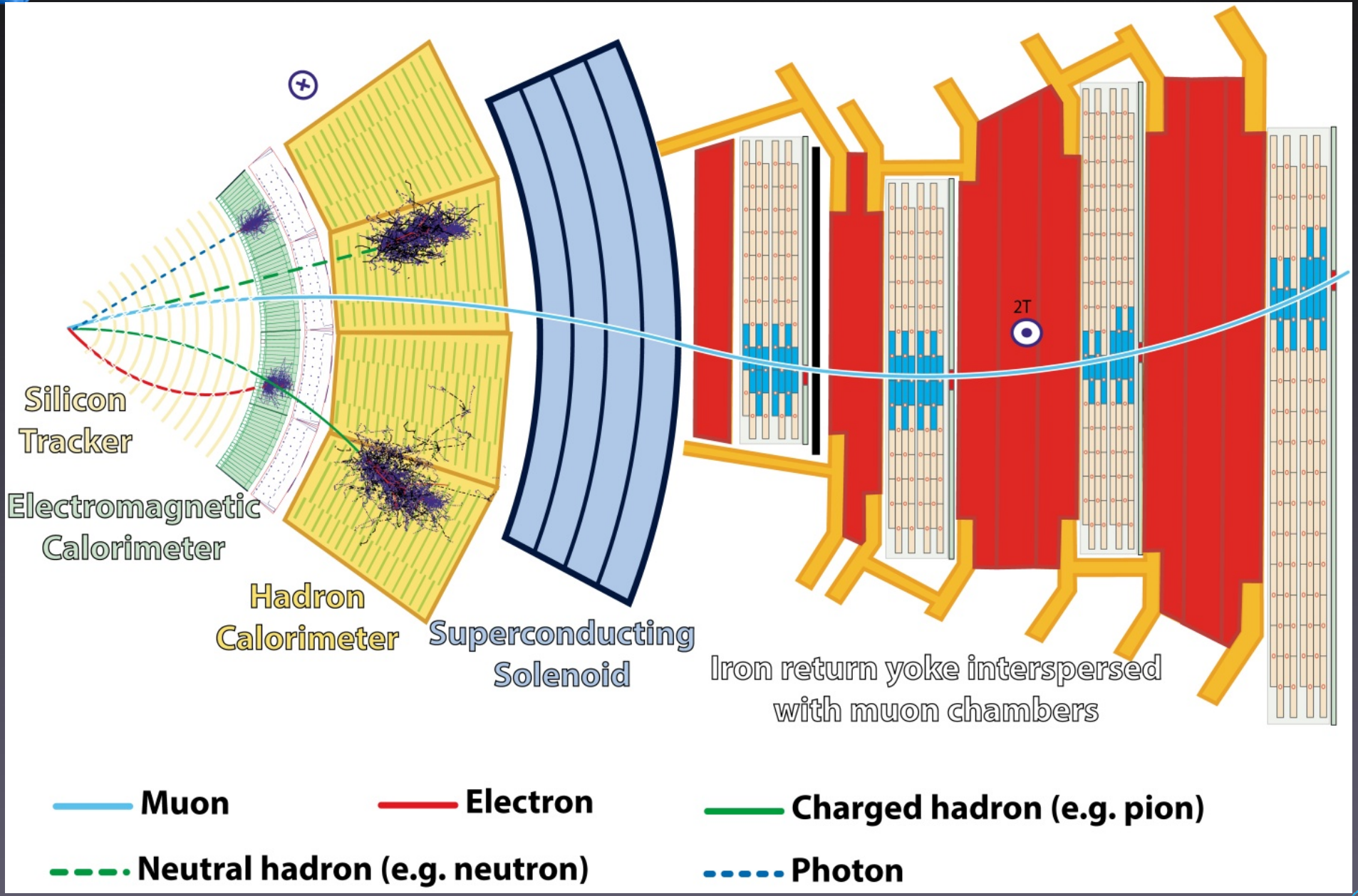

Introduction

Tracking Basics

And in Particle Physics

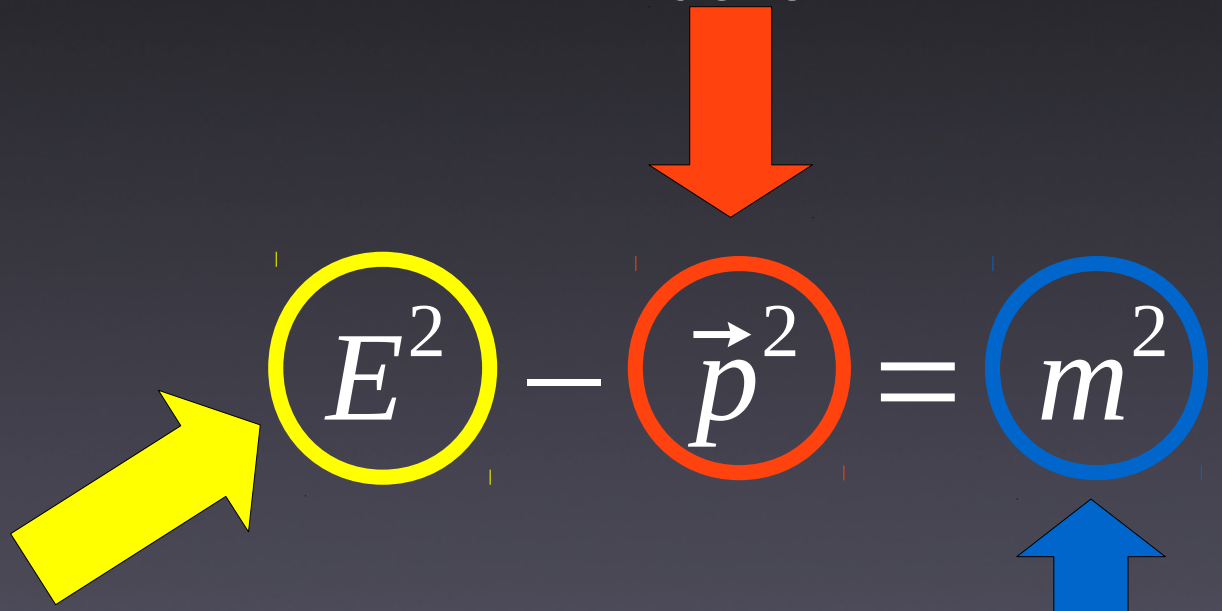


A typical particle physics detector



Reconstructing Particles

Momentum of charged particles measured with the Tracker

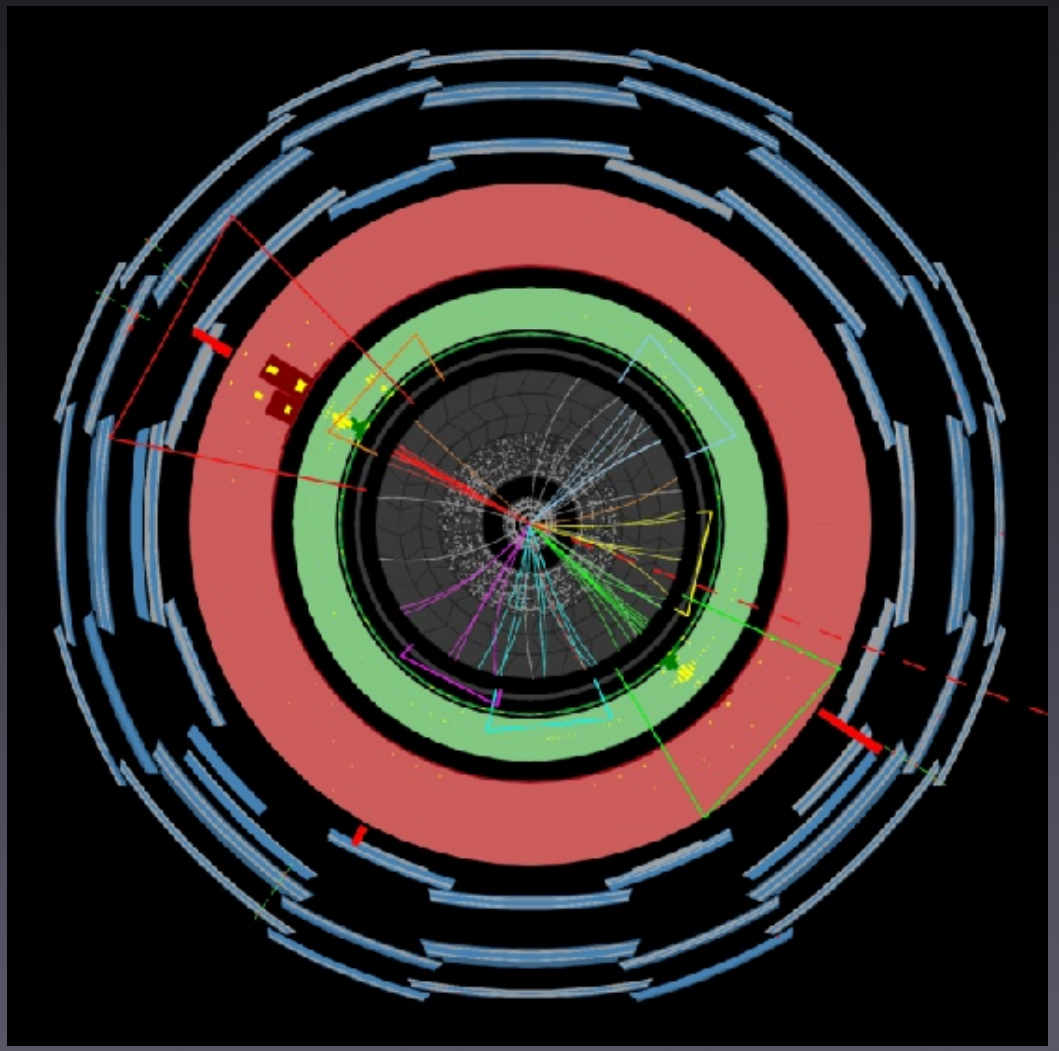


Energy of particles, measured with the Calorimeter

Particle mass Inferred from Particle ID

Tracking in Particle Physics

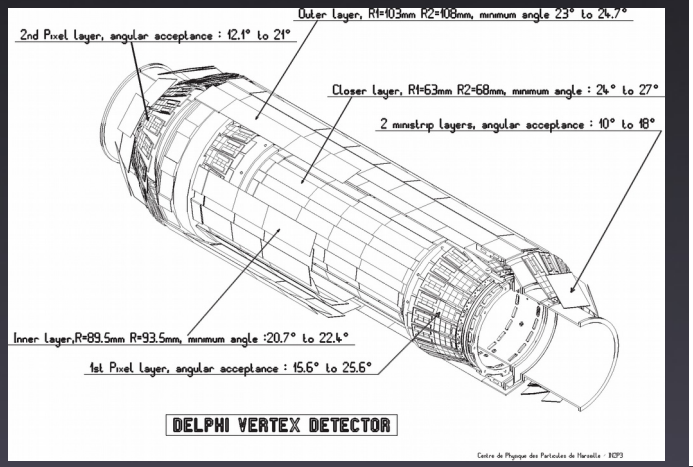
- Basic idea
  - Bend charged particle tracks in magnetic field
  - Add Position-sensitive detectors in the volume inside the magnet
  - Record a few hits
  - Reconstruct the helices
- That's where silicon detectors enter the game
  - Low mass and high resolution

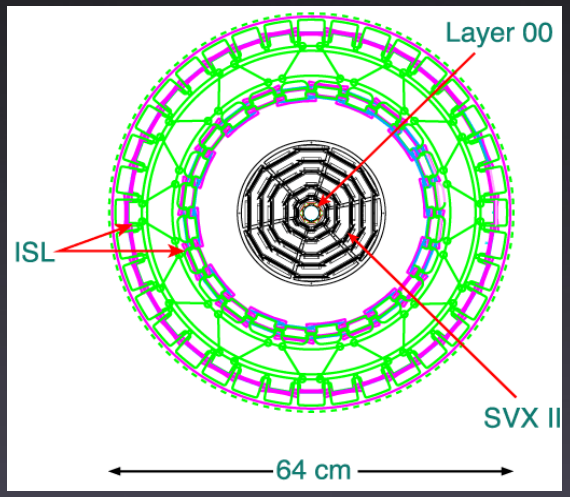


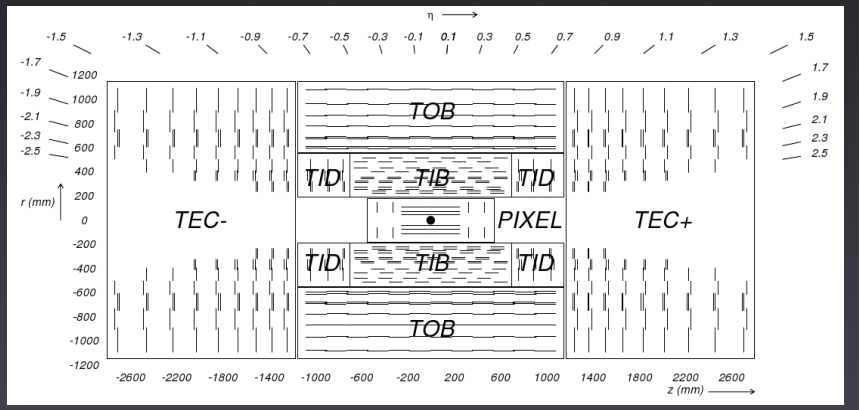
Tracking resolution

- Ultimately Tracking resolution driven by
  - Single Point Resolution
  - Multiple-Scattering
- Hence
  - $$\sigma_{Track} = \sqrt{\sigma^2_{Hit} + \sigma^2_{MS}}$$
- Notes
  - Multiple Scattering dominates at low momenta (~ < 10-20 GeV)
  - At higher momenta the single-point resolution becomes the limiting factor (~ > 50 GeV)

Silicon trackers – A bit of history







DELPHI
O(1m²)

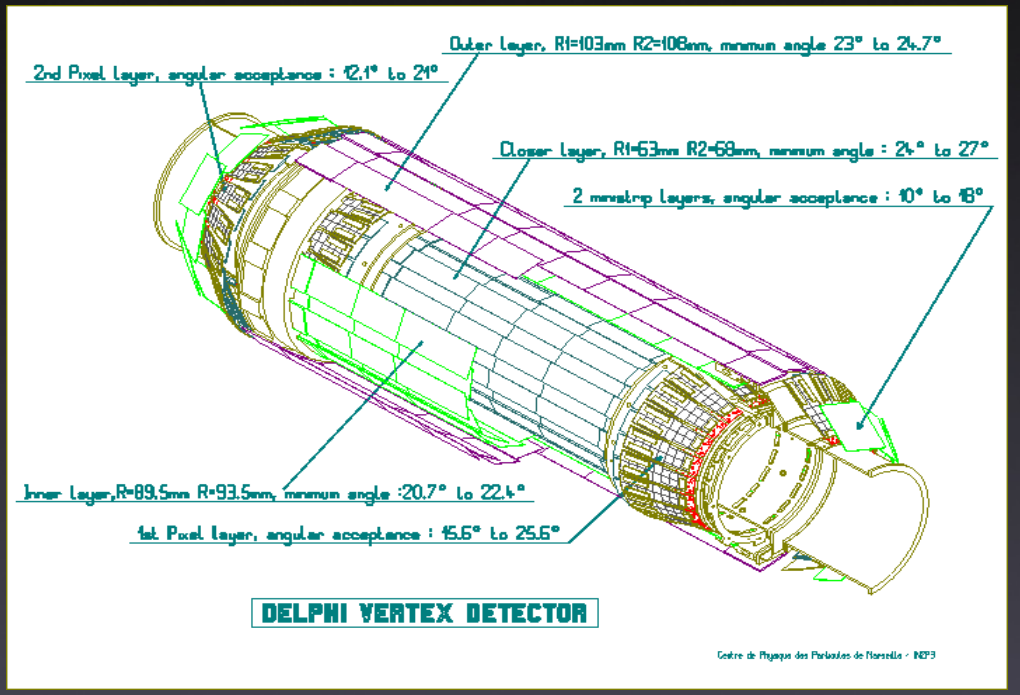
CDF
O(10m²)

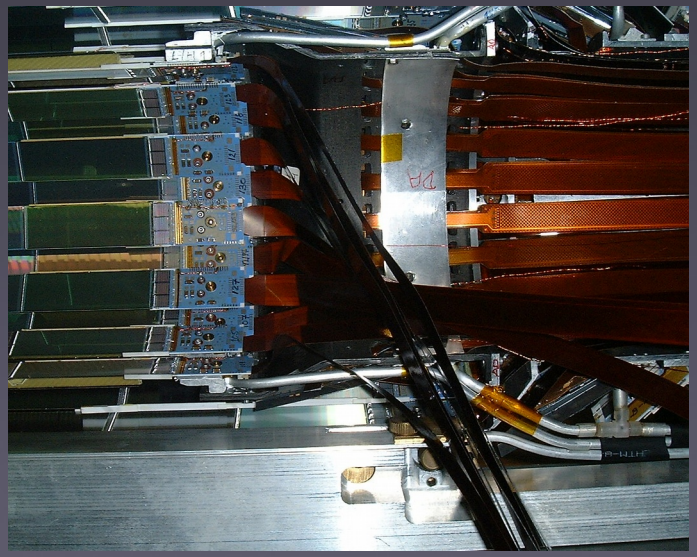
CMS
O(100m²)

1997 → **2008**

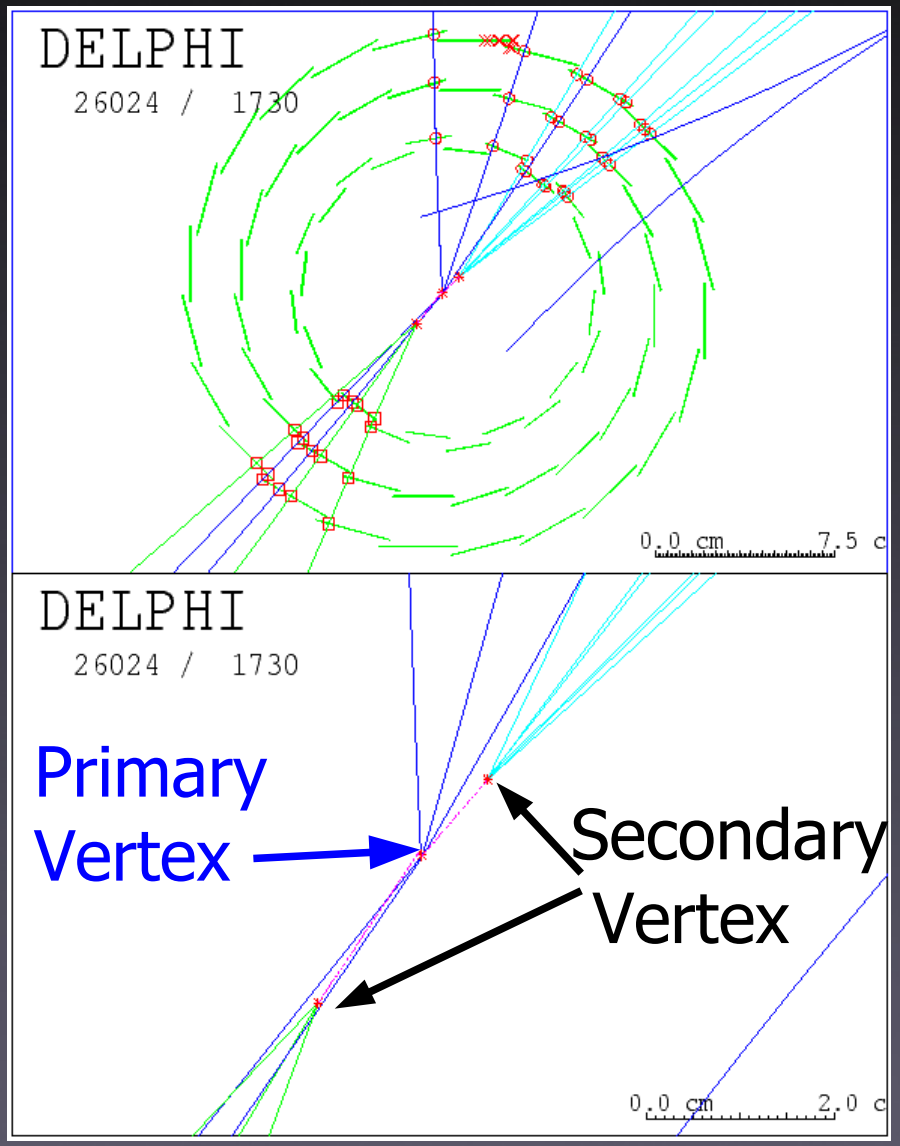
DELPHI Vertex Detector

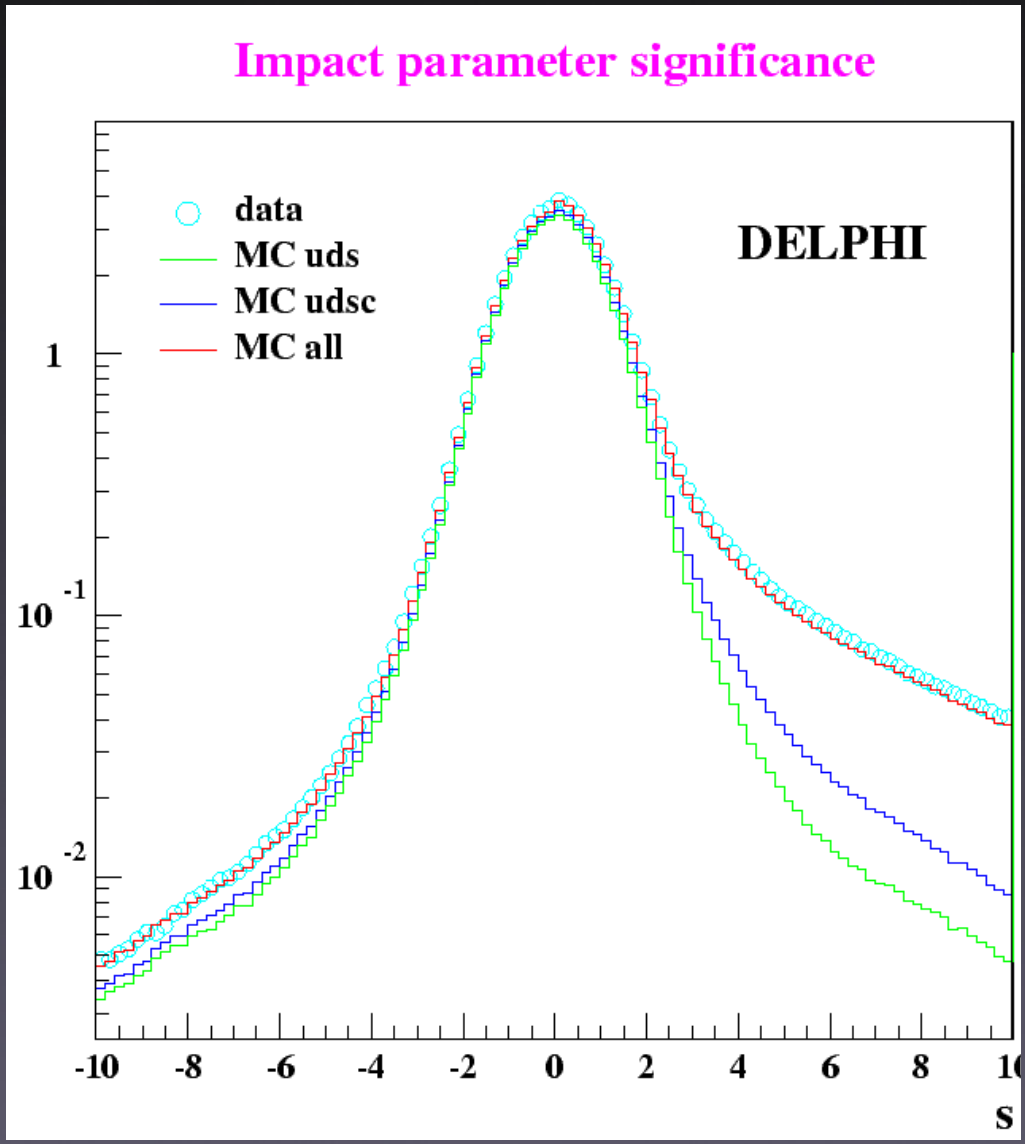
- DELPHI Experiment
  - 1989-2000 @ LEP
- Silicon Vertex Detector
  - Finalized 1997
  - Largest at the time
- Three layers
  - r=63 mm, 90 mm and 109 mm
  - Forward pixels
  - 3D Hits
- Intended for precision vertexing





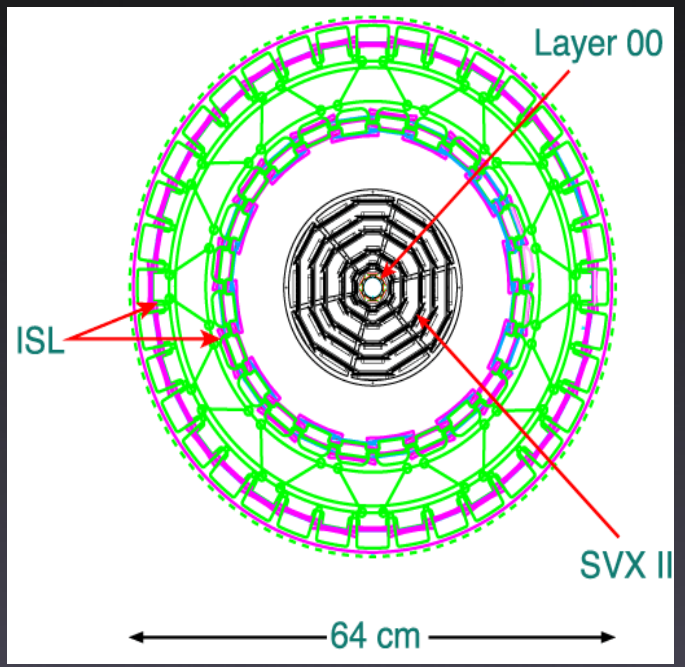
First Application : Vertexing

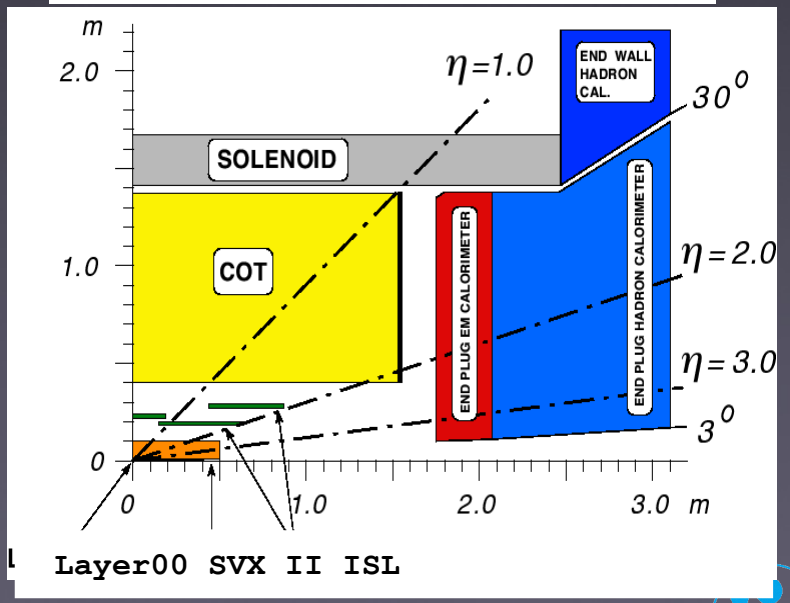




The CDF Silicon Detector

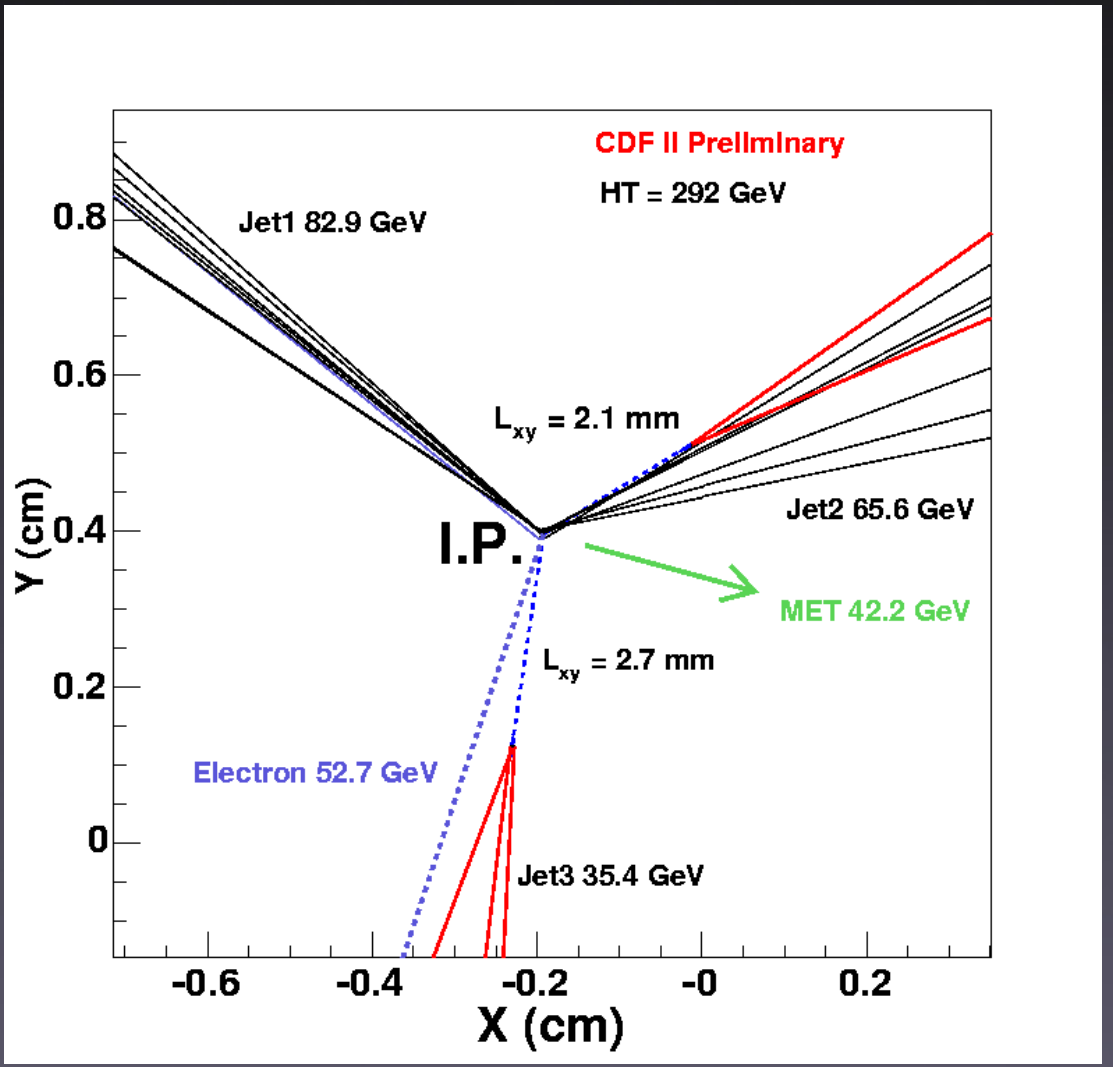
- CDF Detector
  - Teavtron @ Fermilab
- Design Goals (compared to Run-I)
  - Increased acceptance
  - Silicon data for L2 Trigger (unique)
  - Higher resolution for vertices (~ 30 µm)
- Requires versatile Silicon detector
  - Three Components: SVX II, ISL, L00
  - 7-8 layers, 722432 readout channels
  - 3D Hit information



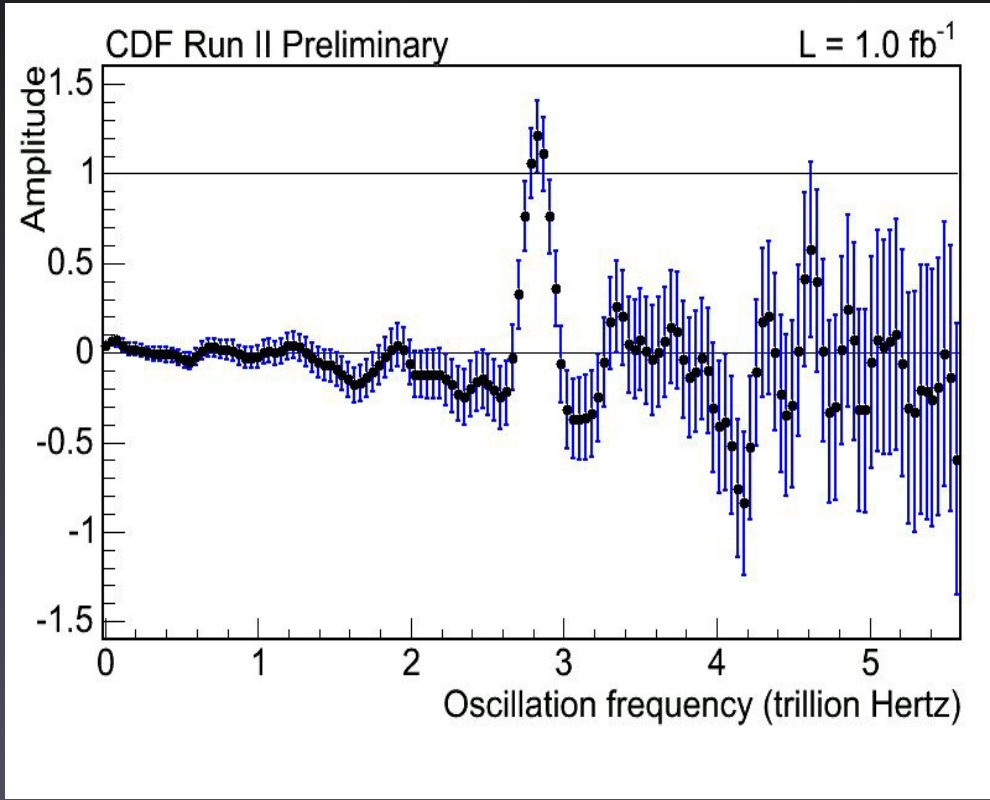


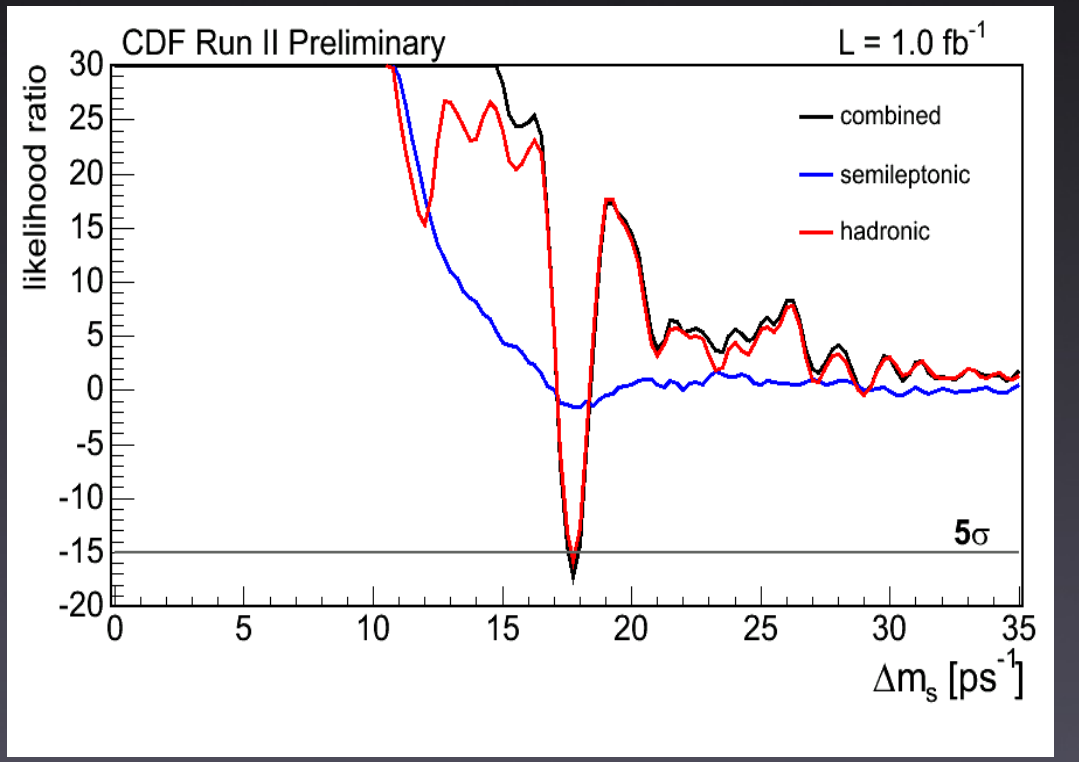
Triggering

- Triggers are essential at a hadron collider like the Tevatron
  - Bandwidth-limited, not event limited
- Idea: Trigger on secondary vertices
  - Larger and pure b-physics sample
- Requires
  - Silicon detector to be part of the trigger readout (very fast readout)
  - Track reconstruction in hardware



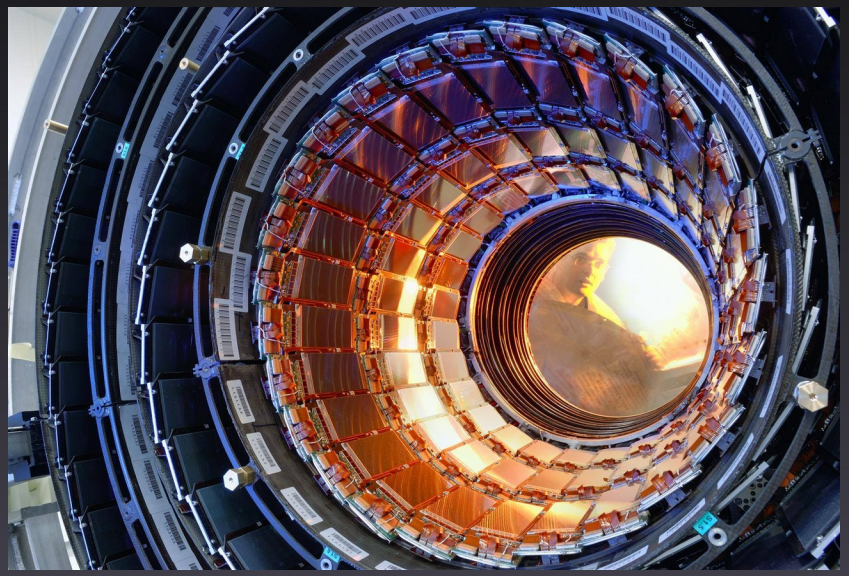
B_s Oscillations

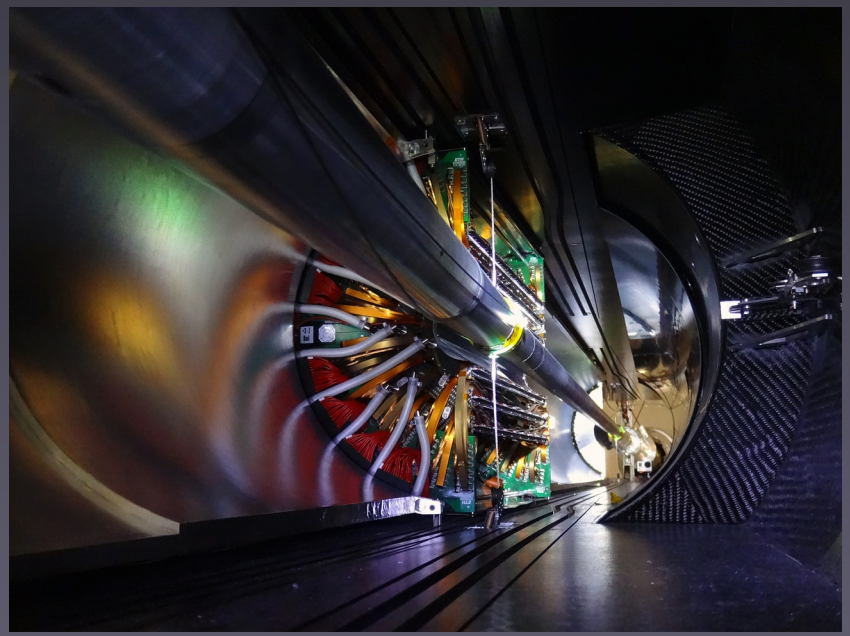




$\Delta m_s = 17.77 \pm 0.10(\text{stat}) \pm 0.07(\text{sys})$

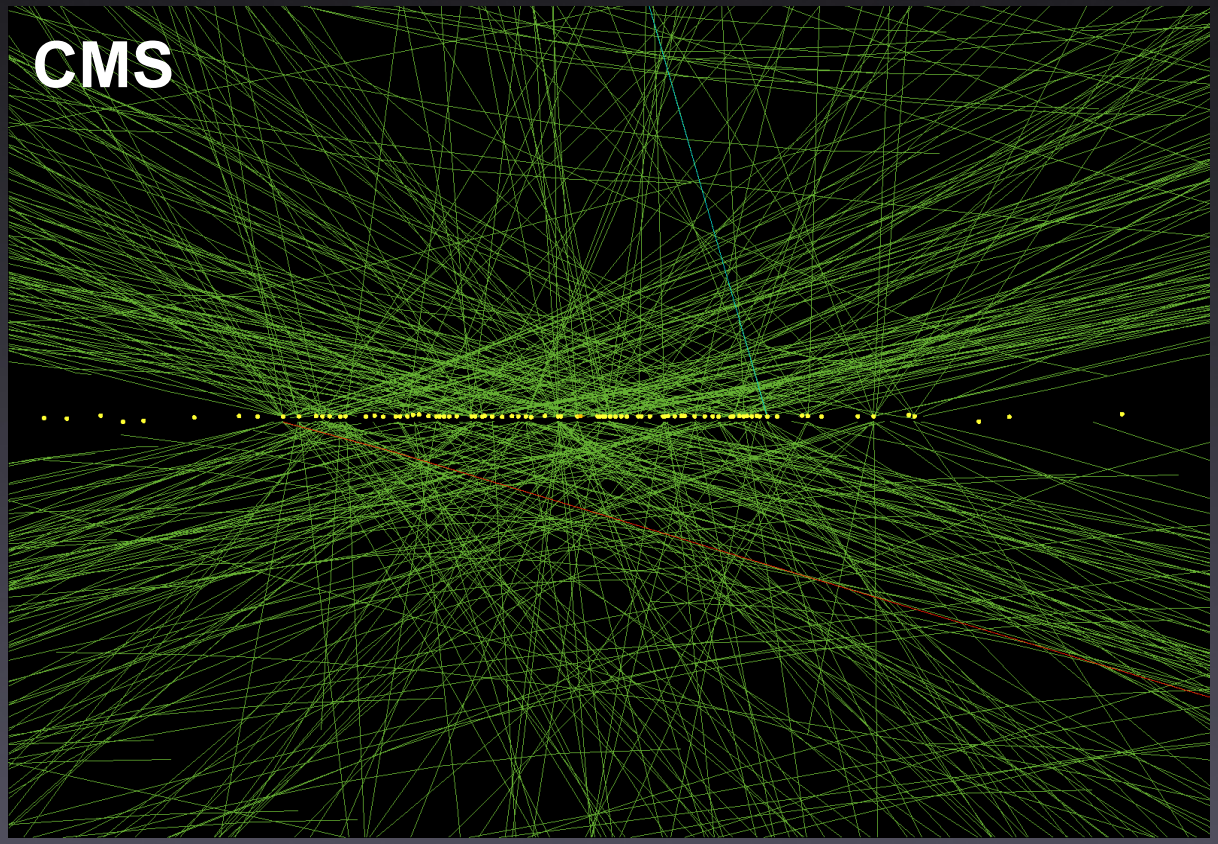
CMS All-Silicon Tracker

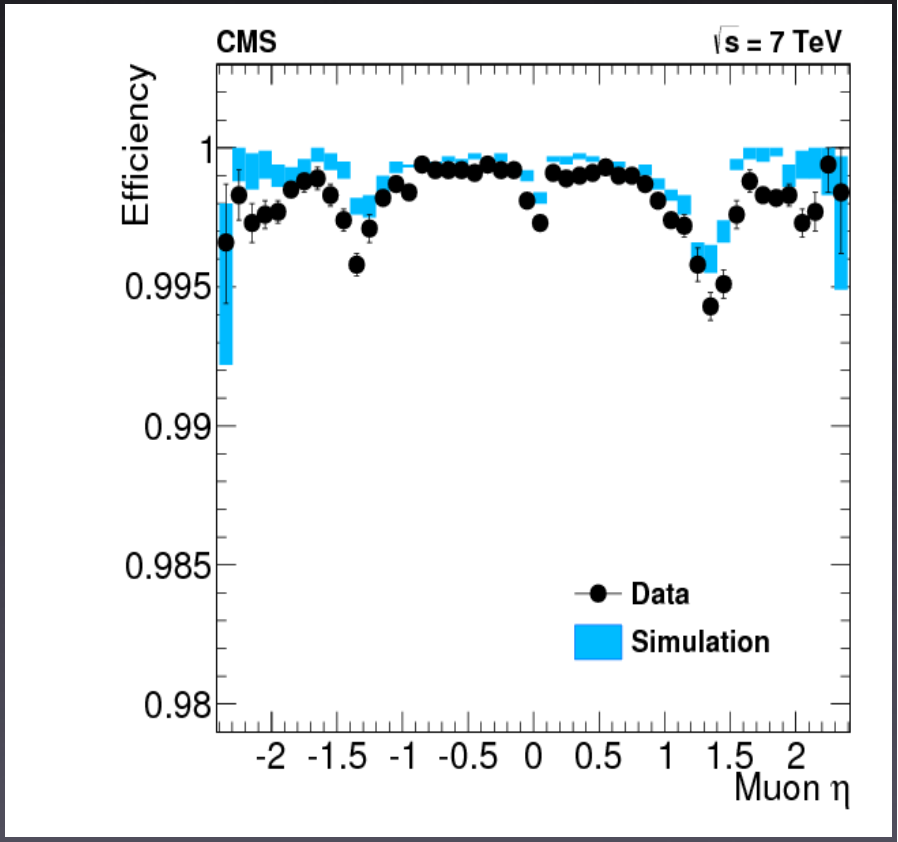




- CMS pixel detector,
  - 65 million pixels
  - Three cylindrical layers at 4 cm, 7 cm and 11 cm and disks
- CMS Tracker
  - 4 inner barrel (TIB) layers
  - 2 inner endcaps (TID) with3 small discs each
  - 6 outer barrel (TOB) layers
  - Two endcaps (TEC) with 9 discs each
  - 15,200 highly sensitive modules
  - Total of 200 m^2 with 10 million detector strips read by 80,000 microelectronic chips
- First All-silicon tracker ever
  - Data taking started in 2008

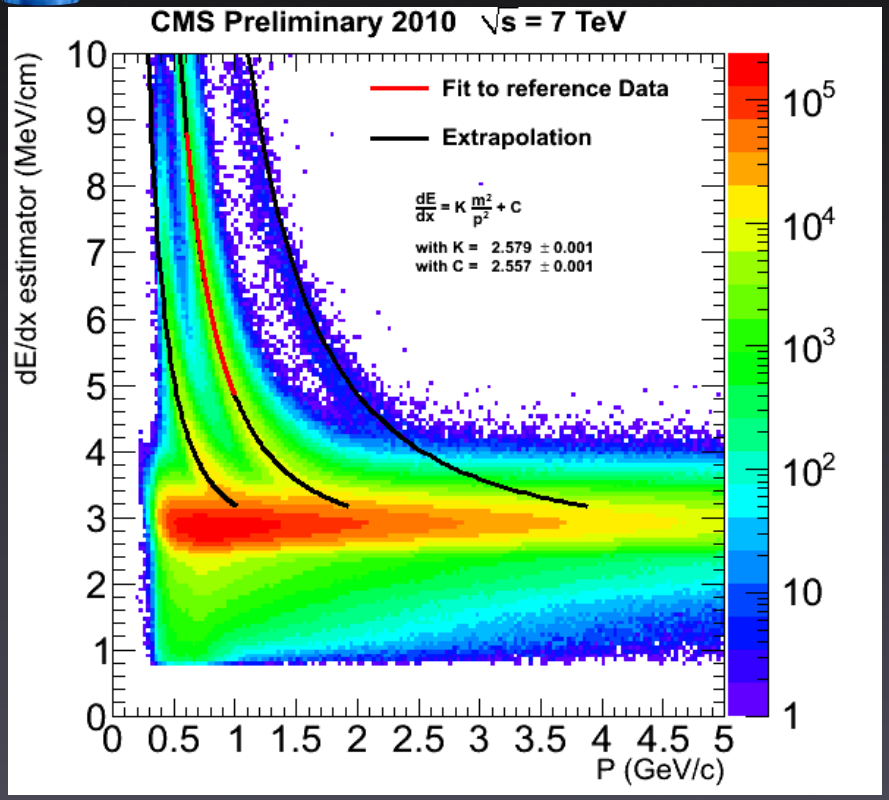
Full-Silicon tracking

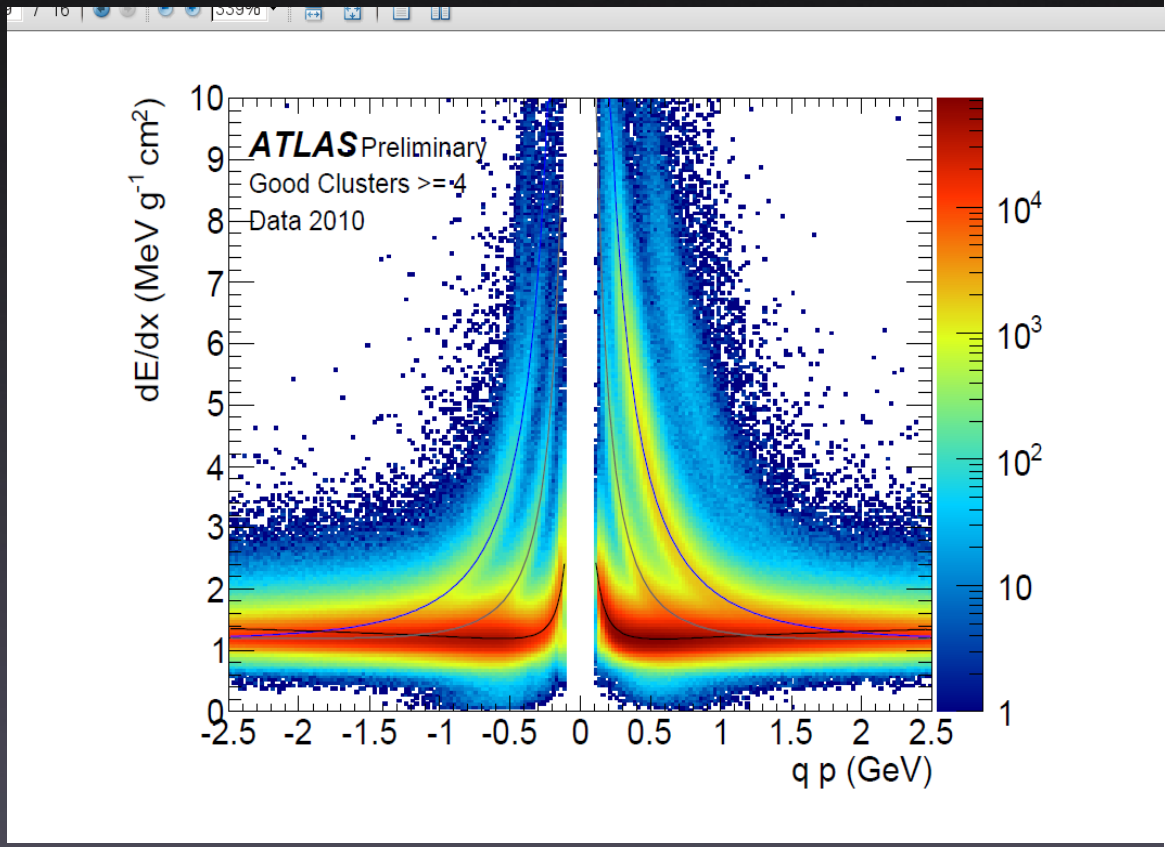




- Full Silicon Stand-alone Tracking
  - A first in HEP
  - No seeding from a tracking chamber anymore

Particle ID using dE/dx





- The folklore
  - Can't do dE/dx with silicon tracker
  - ATLAS and CMS have shown otherwise (with "low resolution" front-ends)

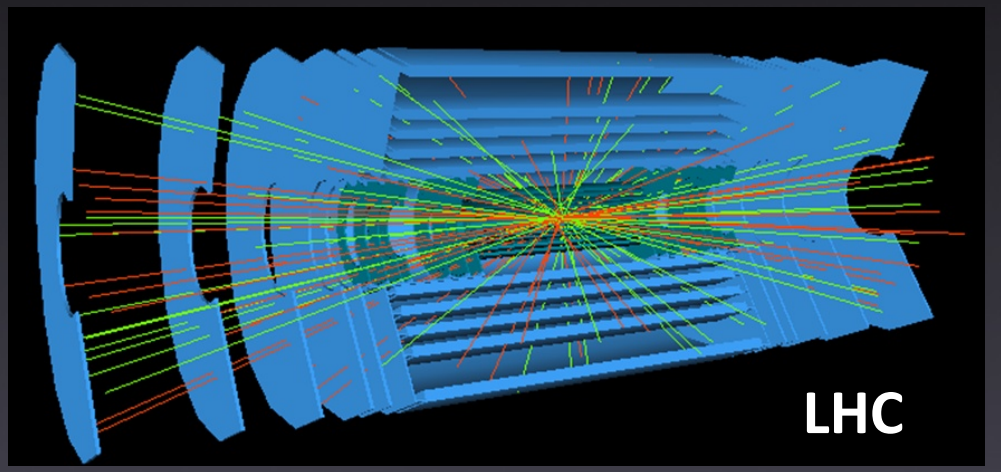

Todays Challenges
From HL-LHC to ILC

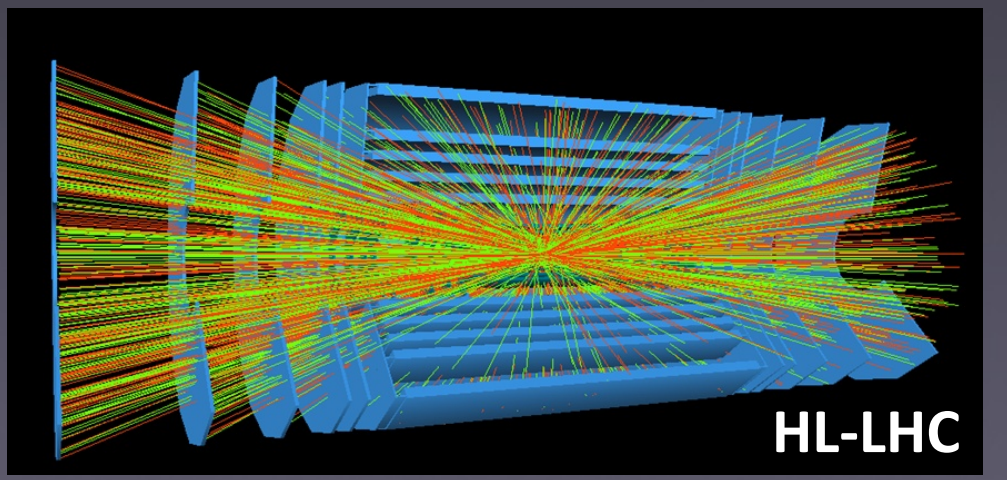
Upcoming Challenges

- HL-LHC Upgrade at CERN
  - pp collisons at 13 TeV
  - Start Data taking in 2025
  - Approved project
- ILC
  - e^+e^- collision at 500 GeV
  - TDR delivered, currently in the approval process
  - Start Data Taking ~ 2030
- Some other proposals
  - On the 2030-2040+ timescale

HL-LHC Upgrade

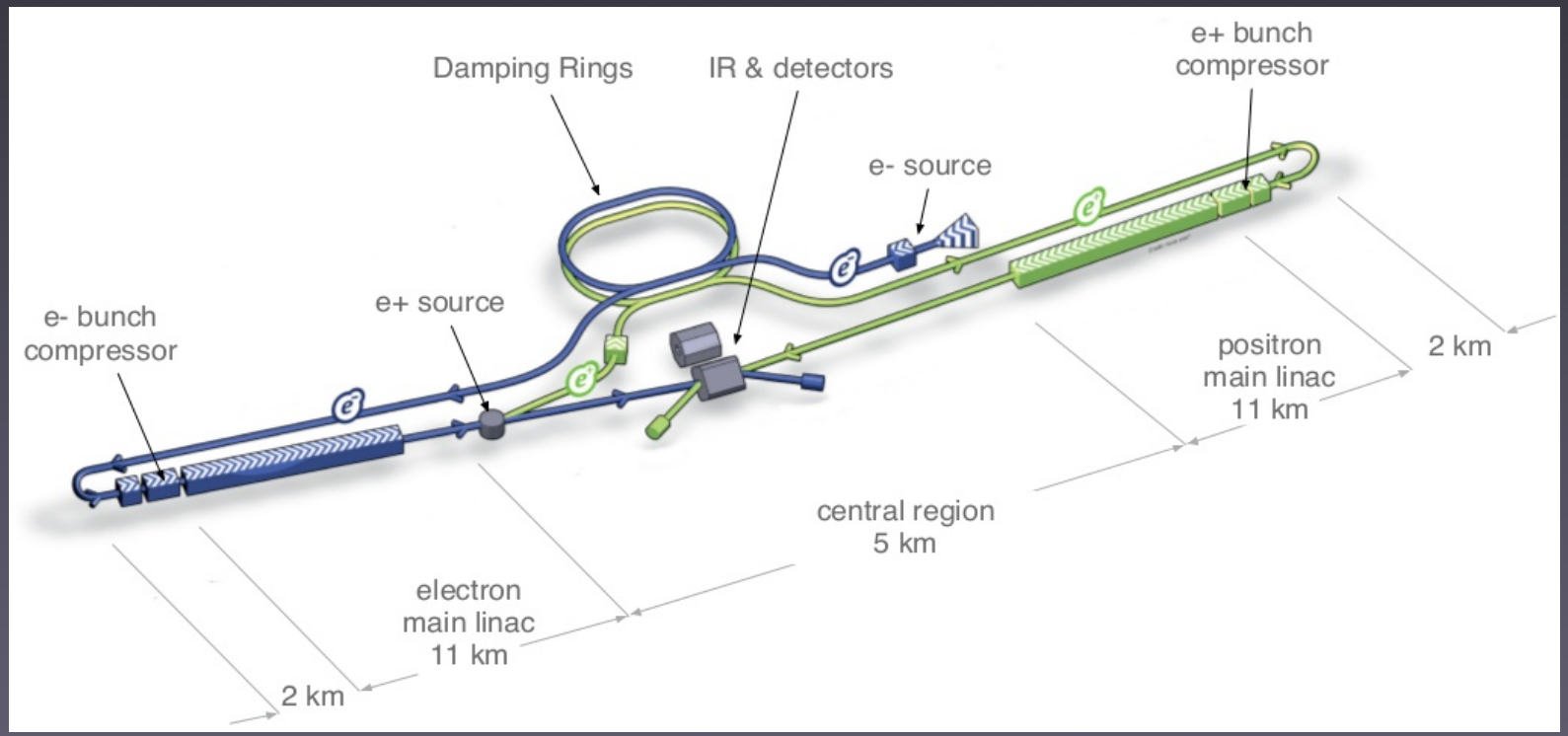
- Start of HL-LHC
  - a.k.a Phase-II
- Compared to Nominal LHC
  - Factor 5 initial luminosity
  - Luminosity leveling
  - Number of interactions 55 → 140
- Radiation damage is an issue
  - 1E16/1E15 neq



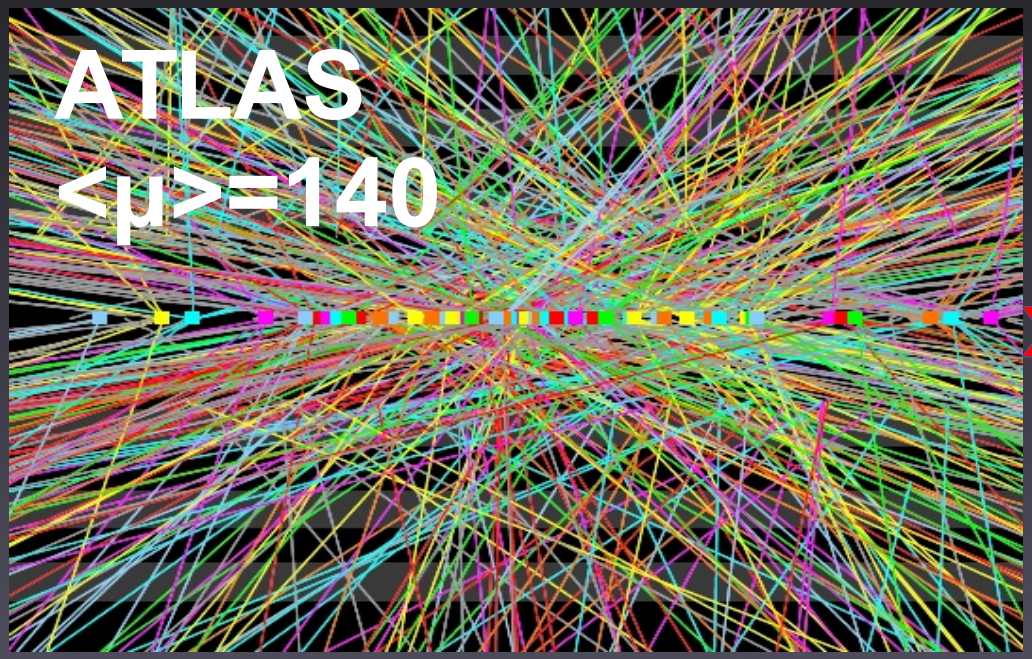


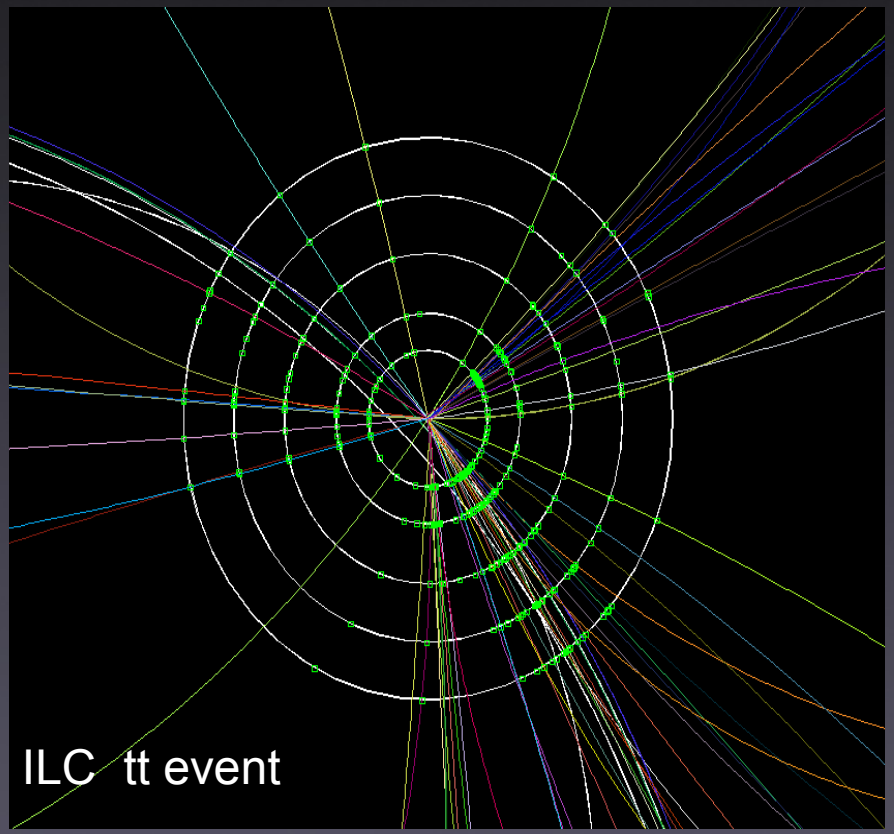
The ILC Project

- The ILC (International Linear Collider) in Japan
  - A 500 GeV (baseline) GeV e+e- Linear Collider
  - Clear Upgrade Path to 1 TeV
  - Beam Polarization
- Interaction Region with two detectors



HL-LHC vs ILC



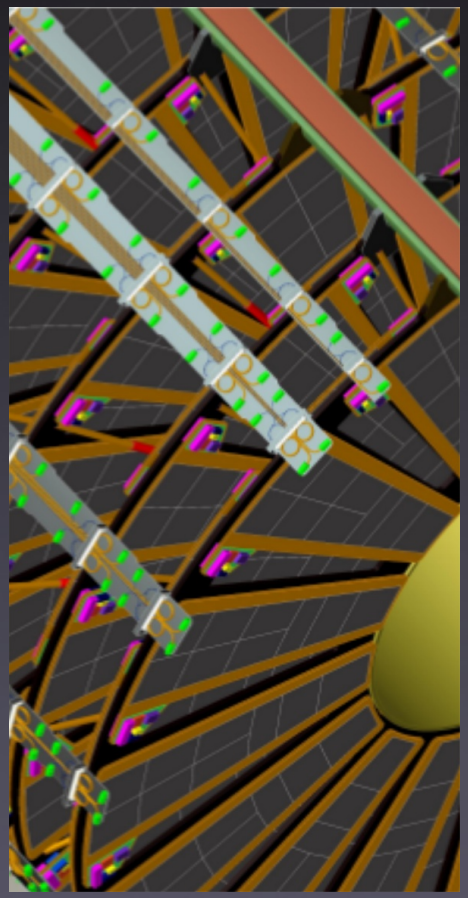


Moving from 140 interactions per 25 ns crossing to ~1 event/train
Tracker design is also machine-driven

Common Challenges

Physics and wishes Requirements

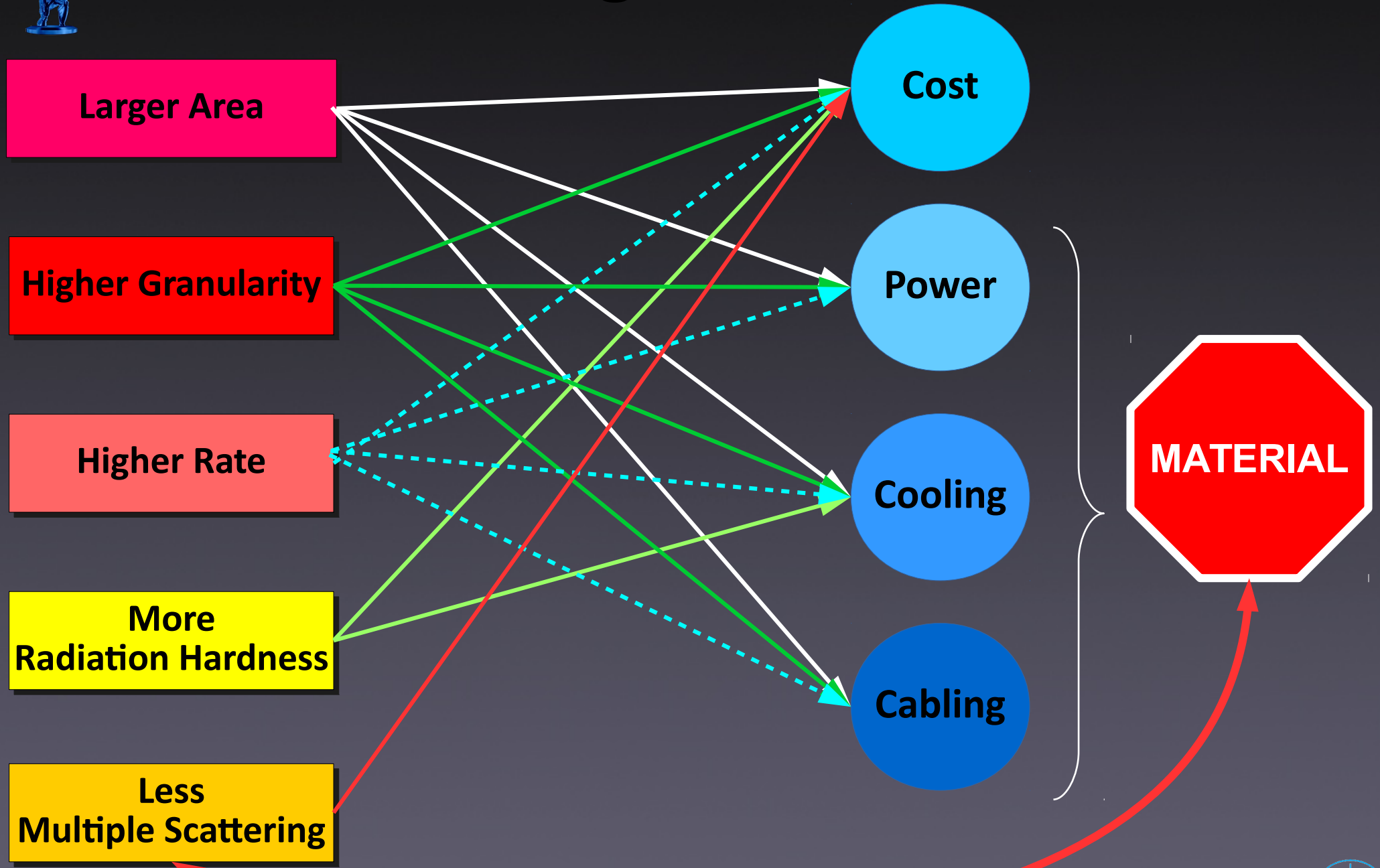
- Higher granularity
- Larger Coverage
- Higher Rate
- Higher Luminosity
- Less Multiple Scattering



Silicon sensors can deliver the performance needed!

Need to change “basic design paradigms” to reduce material

Design Matrix



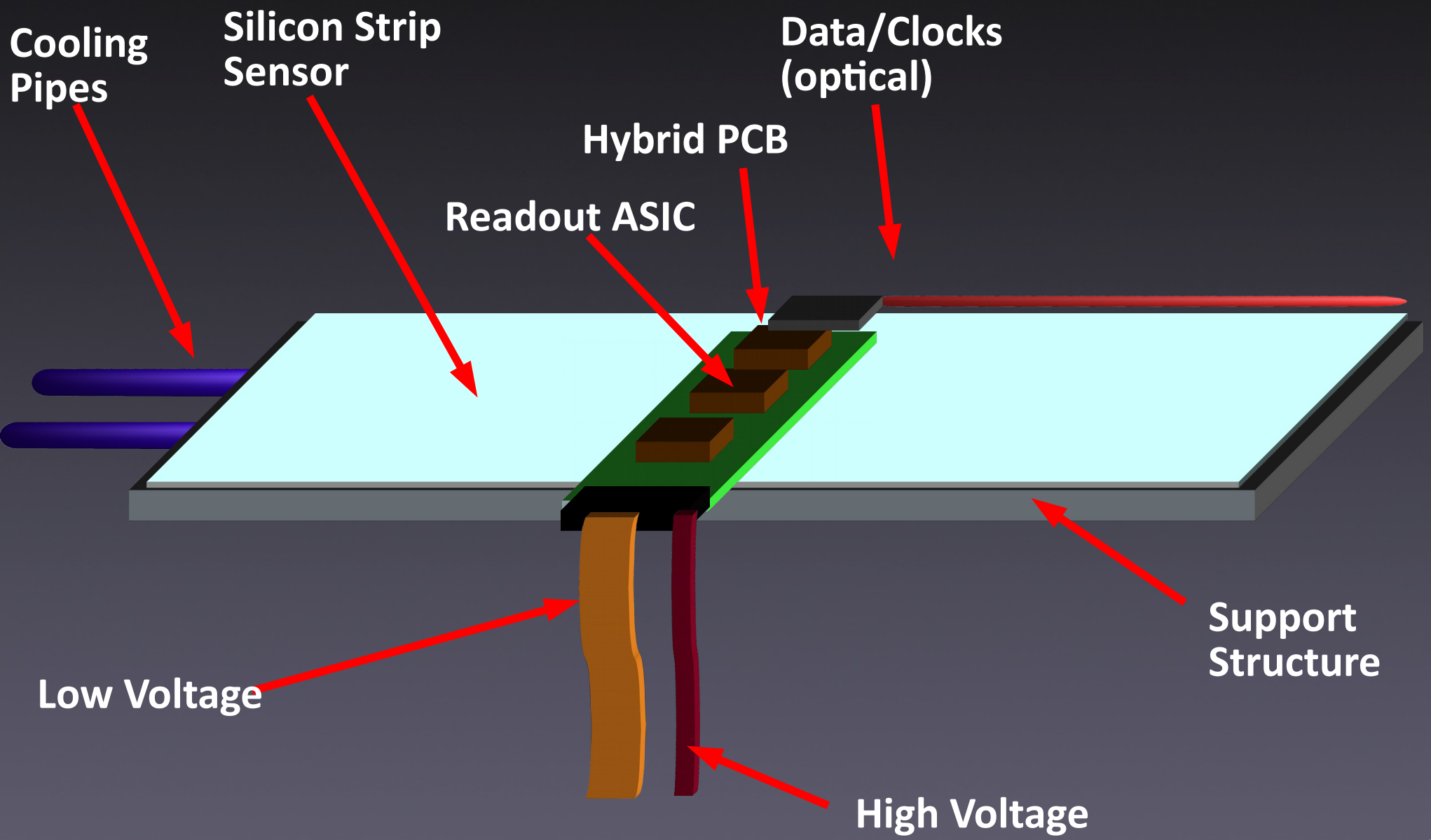
Cost considerations

- Increasing Area and Granularity
  - Number of Channels increases
- Present day and time

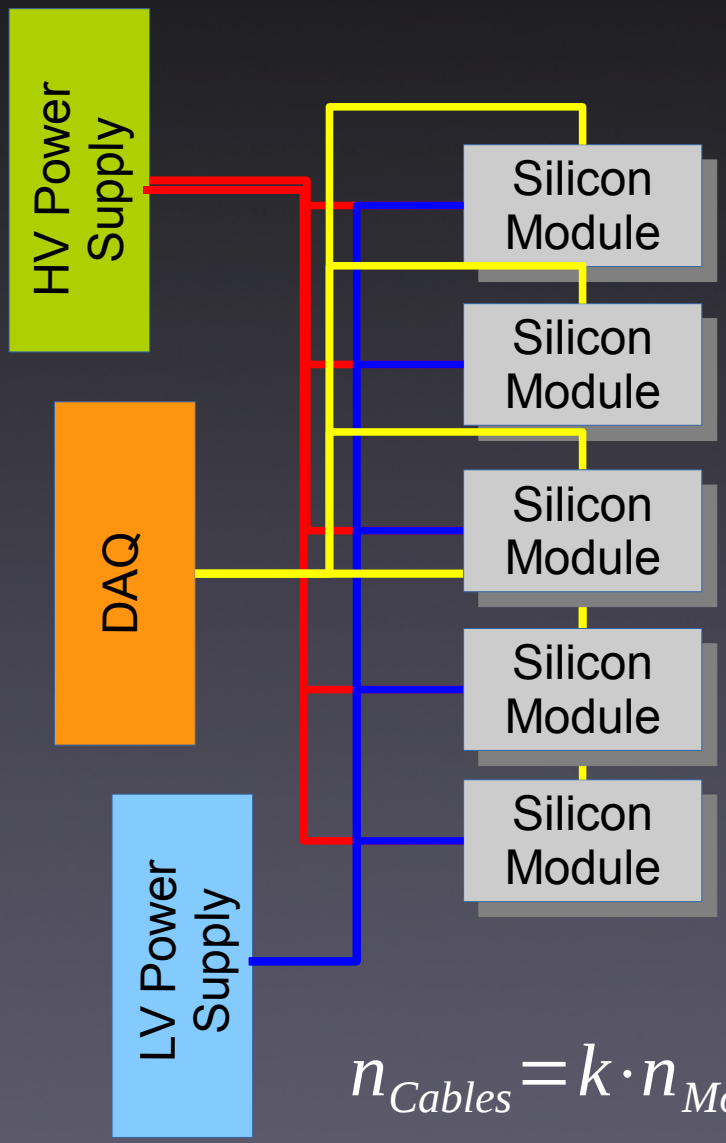
$$Detector\ Cost = N_{Channels} \cdot Cost_{per\ Channel} = const$$

- Reducing Cost per channel is essential
- How ?
  - Using industry-standard technologies wherever possible
  - Move away from hand-made sensors and hand-crafted modules

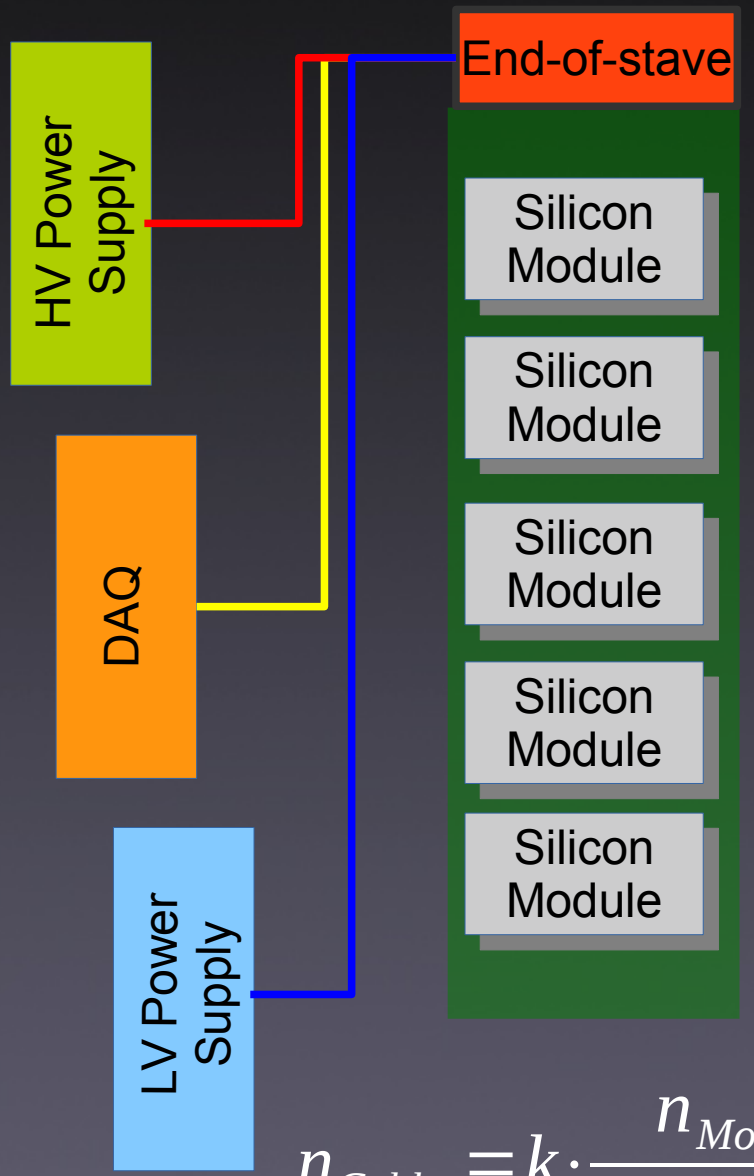
A “typical” Silicon Tracker Module



From Modules to Staves



$$n_{Cables} = k \cdot n_{Modules}$$



$$n_{Cables} = k \cdot \frac{n_{Modules}}{n_{Modules,\,Stave}}$$

ASIC designs

- The main power driver is LV consumption
  - ASICS, data links,
- Example ATLAS Phase-II Upgrade
  - ATLAS Barrel Hybrid with 2560 channels
- Switched from IBM 250 nm to IBM 130 nm technology
  - ABCN25 chip: IBM 250 nm 128 channels
  - ABC130 chip: IBM 130 nm 256 channels
- Benefits for a barrel hybrid
- ~ 20 W using ABCN25
- ~ 3W using ABC130

LV Powering Schemes

- Current LV needs
  - Chunky cables to transport 3.3V/1.5V with several amps
  - Loads of them
- Two ways out
  - Daisy-chaining
  - High Voltage-in, local conversion
- Both ideas have successfully been pursued

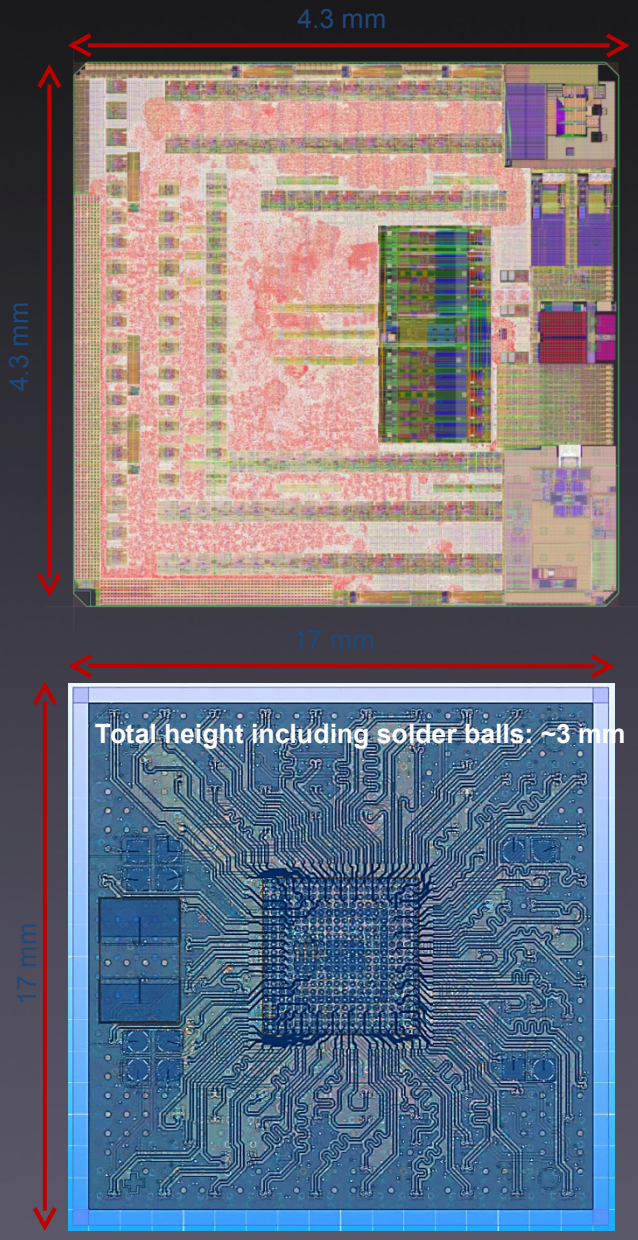
- Serial Powering
  - Every module on a stave is daisy-chained
  - Reliability worries
- DC-DC converters
  - Input 10 V
  - Output 1.5 V
  - Industry standard
    - But not for rad-had & Multi-Tesla field application

HV Multiplexing

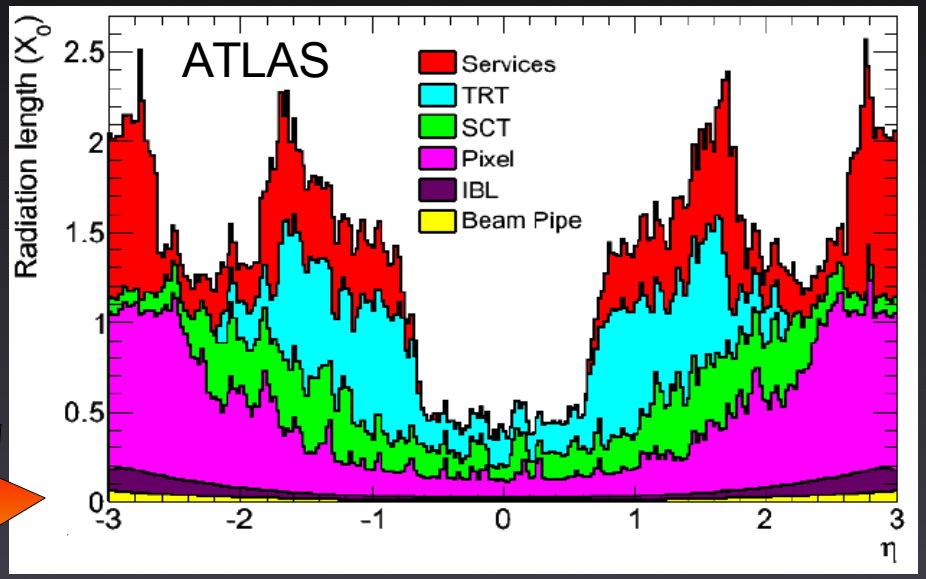
- A similar idea for distributing HV to each sensor
- Instead one common HV “bus” with individual switches per module
  - Retain capability to bias individual modules
  - Requires rad-hard High-Voltage transistors that can switch 500V +
  - Active R&D to qualify circuits
- HV distribution is a lot easier
- Drawback
  - All Modules need to use same bias voltage in the simplest approach

Optical Links

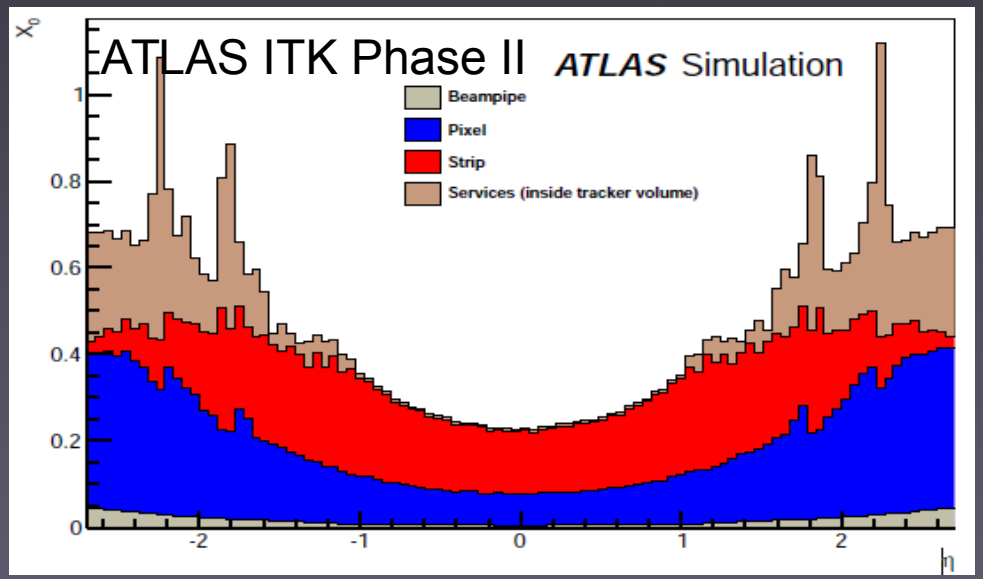
- Rad-Hard High speed optical links are key for HL-LHC
  - Common HL-LHC wide development (“GBT”)
- Versatile Link
  - Rad-Hard optical link with up to 10 Gbps
- GBT
  - Driver chip providing multiplexing, error correction, etc
- Eliminates a lot of individual links



Material Budget

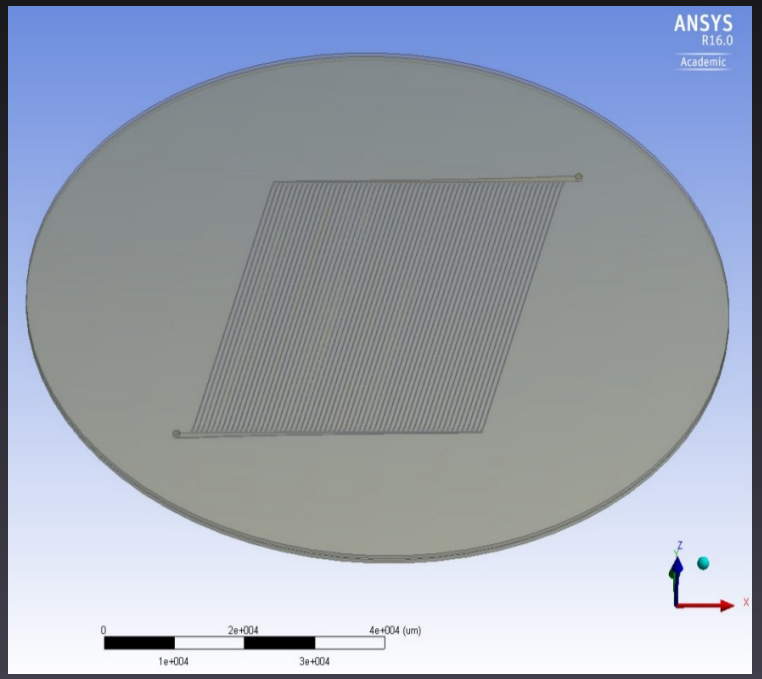


R&D on Services, Mechanics, Cooling

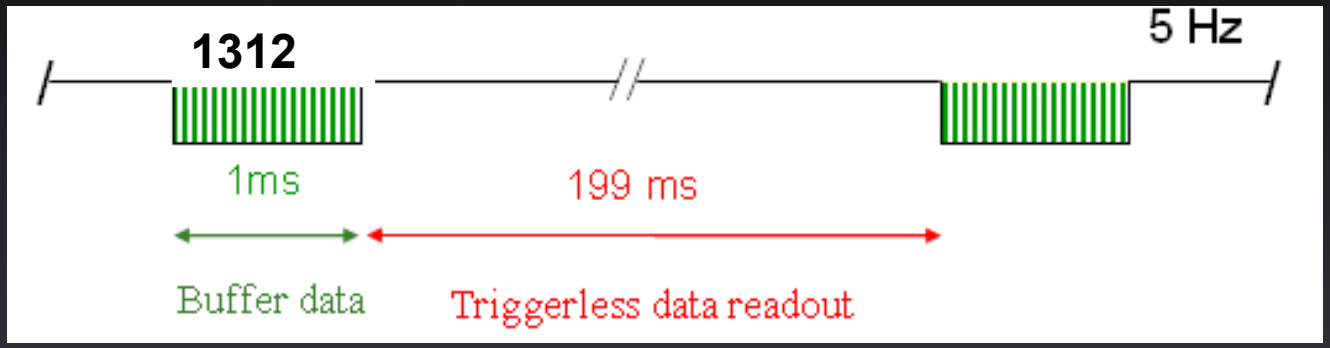


Micro-Channel Cooling

- Idea
  - Instead cooling the mechanical structure
  - Cool sensor directly
  - Higher efficiency → Less material
- Prototype :Microchannels etched into 4” silicon wafer
  - Sixty 100 µm x 100 µm channels connected via manifolds



Power Pulsing (I)



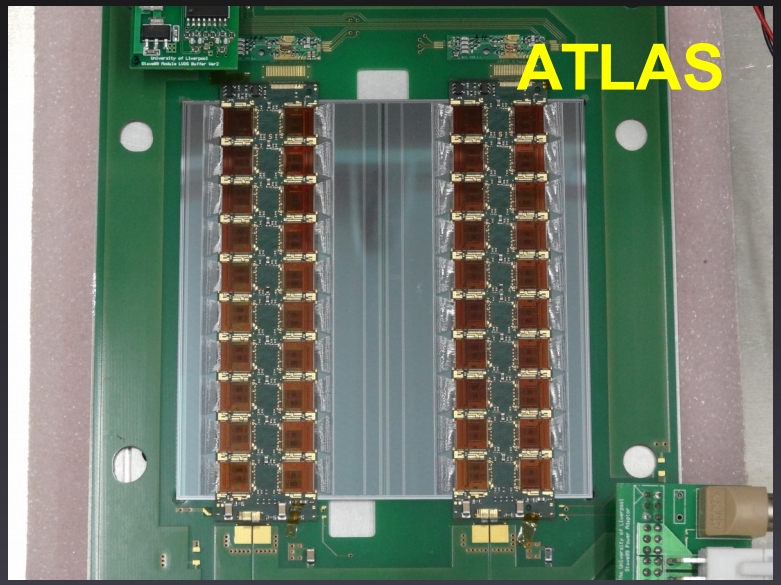
- ILC environment is very different compared to the LHC (or any other synchrotron)
  - Bunch spacing of ~ 554 ns (baseline)
  - 1312 bunches in 1 ms
  - 199 ms quiet time
- Readout during quiet time is possible
- In the idle time, power off electronics
- Big Impact on detector design

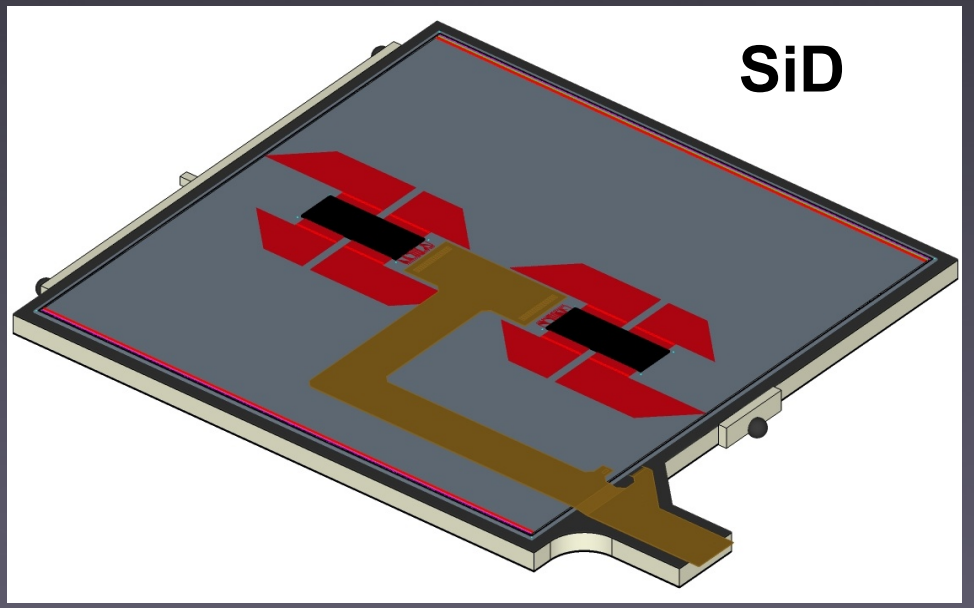
Power Pulsing (II)

- With a duty cycle of 1:200
  - Assume a factor 100 power reduction
- This is a major gain
  - Eliminate a dedicated cooling system
  - Gas cooling for a Tracker can be sufficient
- Technically no problem to shut down the power-hungry front-end
  - Has been demonstrated with several ASICS
  - System questions remain, what happens if one power-pulses a few thousand chips...

Eliminating Hybrids

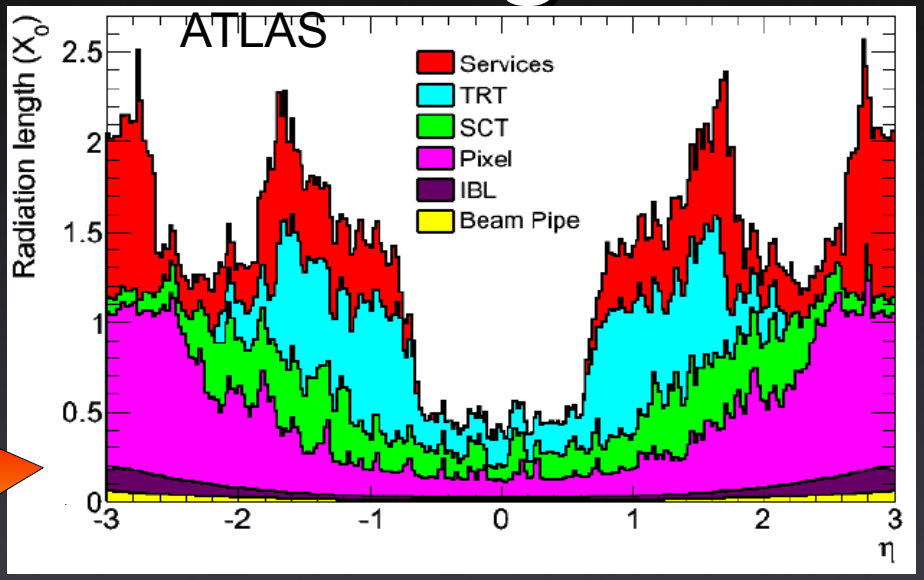
- Hybrid PCBS hosting the readout ASICS
  - Wire-bonding strips to the ASICS
  - Significant amount of material
- Alternative
  - Bump-Bonding the ASICS directly to the strips
  - Double-metal layers for the routing

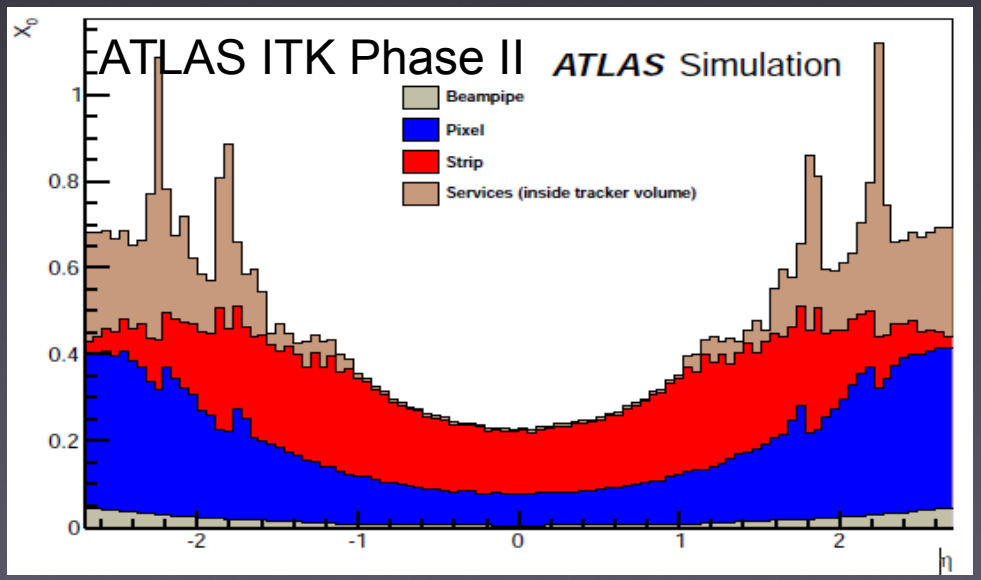




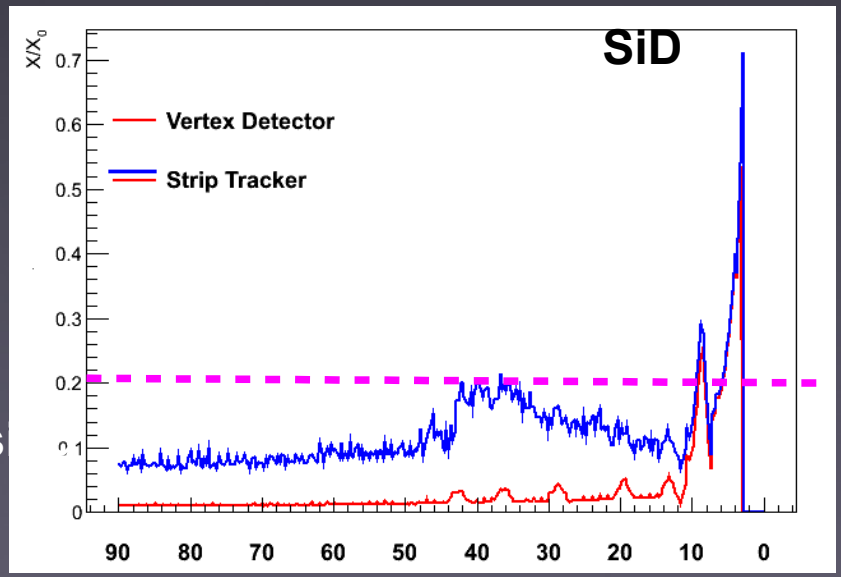
Material Budget

R&D on Services, Mechanics, Cooling





Power puls
No cooling

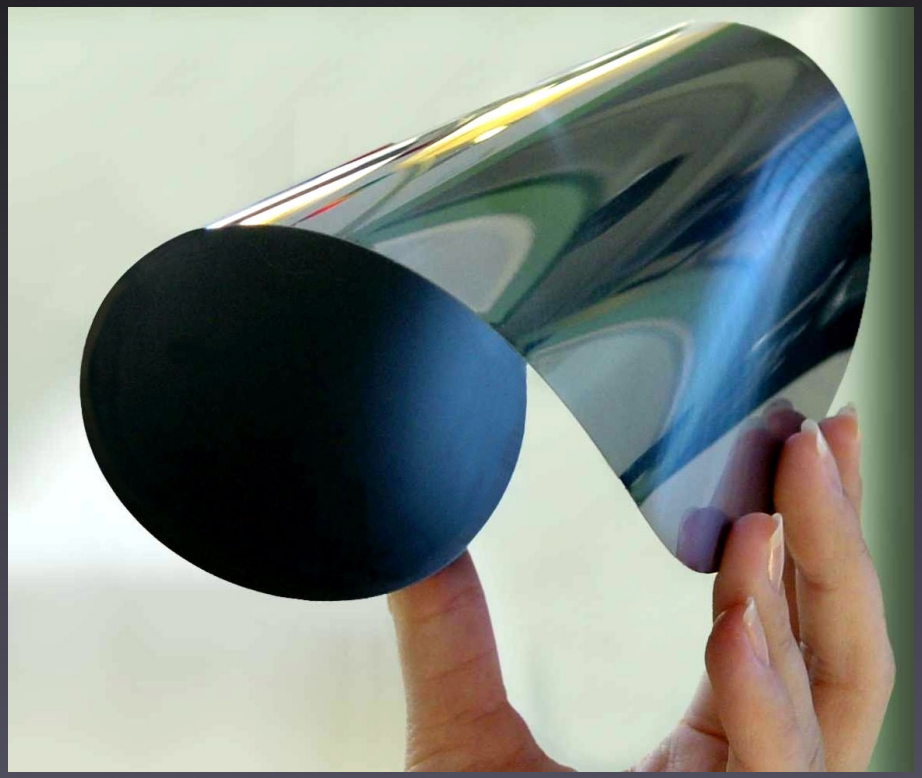


Up to now

- Hard work on the “Services”
  - Significant gains through-out
- But as always no free lunch
  - Losing granularity in detector control
  - More complexity
- But
  - Still 300 micron Silicon sensors (need two for a “3D space point”
  - 0.7 % X_0
- Next stop on our “reduce material” tour

Sensor Thinning

- Obvious Idea
  - Make the sensor thinner
- But unfortunately
  - Signal ~ thickness
  - Below 50 micron silicon becomes floppy
- LHC Upgrades
  - 200 micron seems a good number
  - 33 % less material

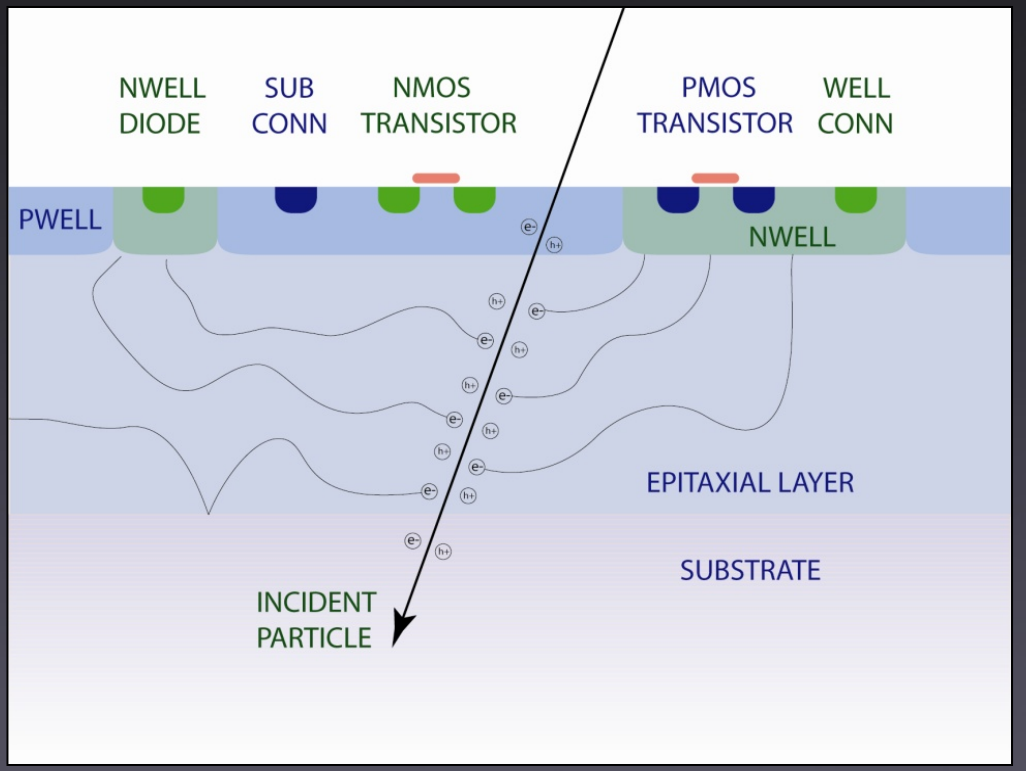


From Strips to Strixels and pixels

- "Classic" Silicon trackers
  - Based on strip sensors
  - Excellent rϕ resolution (20 micron or less) and mediocre z resolution driven by strip length
- For a 3D space point
  - Either double-sided sensors (rϕ and rz strips)
  - Small-Angle-Stereo configurations (usually two sensors)
- Obvious way out
  - Very short strips (strixels)
  - Pixels right away

Monolithic Active Pixel Sensors

- CMOS
  - Standard industry processes
- Baseline: Charge is collected by diffusion
  - Slow > 100 ns
- Readout is fully integrated
  - Standard MAPS limited to NMOS
- Thin Active layers
  - 20 microns
- Basic MAPS cell→The 3T array



Overcoming limitations

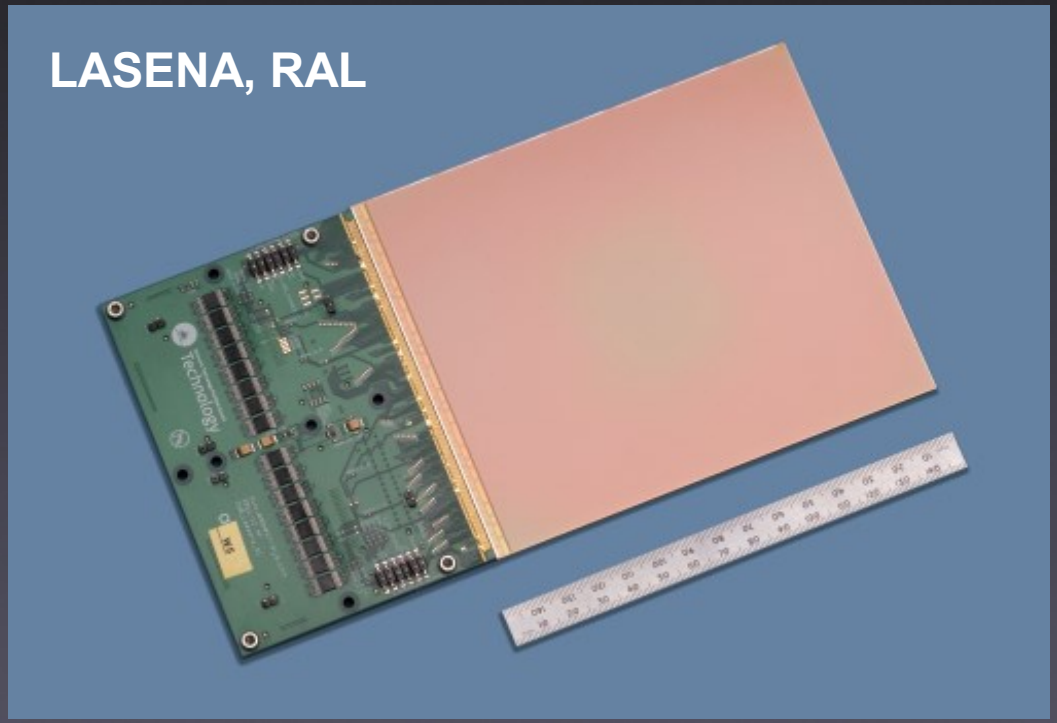
Full CMOS Capability

- Baseline MAPS limited by NMOS only
  - Full CMOS highly desirable
- Solution
  - Encapsulating the PMOS with a deep p-implant
- By now established technology

Charge collection

- Diffusion is inherently slow and radiation soft
- Need to make MAPS that collect charge by drift
  - Using high-resistivity epi-layers and or High Voltage
- Both HR-CMOS and HV-CMOS are considered as options for HL-LHC Phase-II upgrades

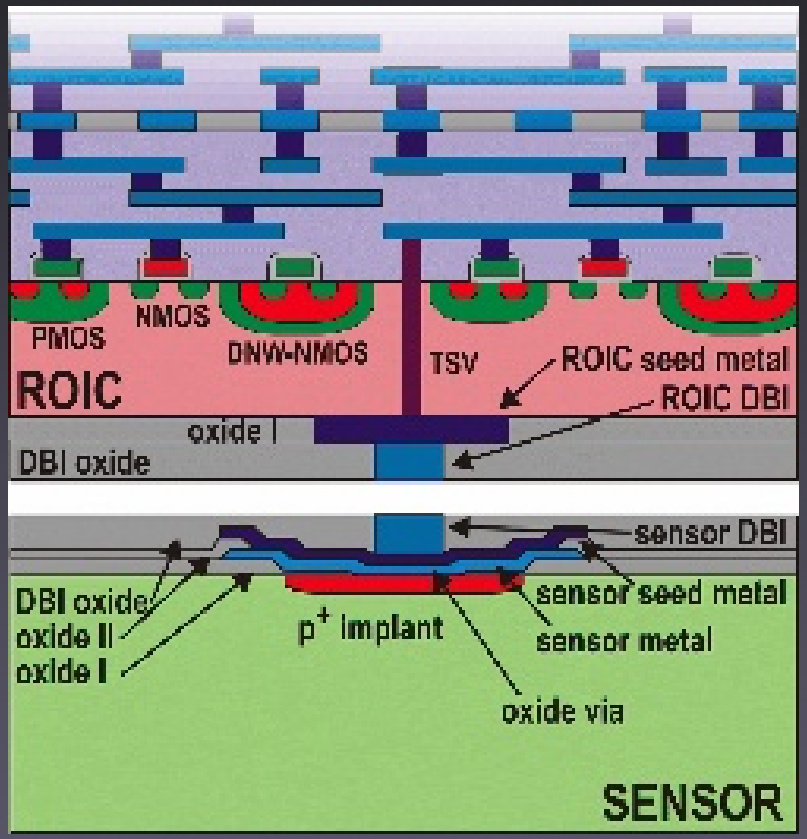
Wafer-scale devices



- MAPS sizes used to be limited to the Reticule size
  - 2.5 x 2.5 cm approx
- Stitching sensors has become possible now
  - Wafer size is now the limited
  - CMOS is typically using 300 mm wafers

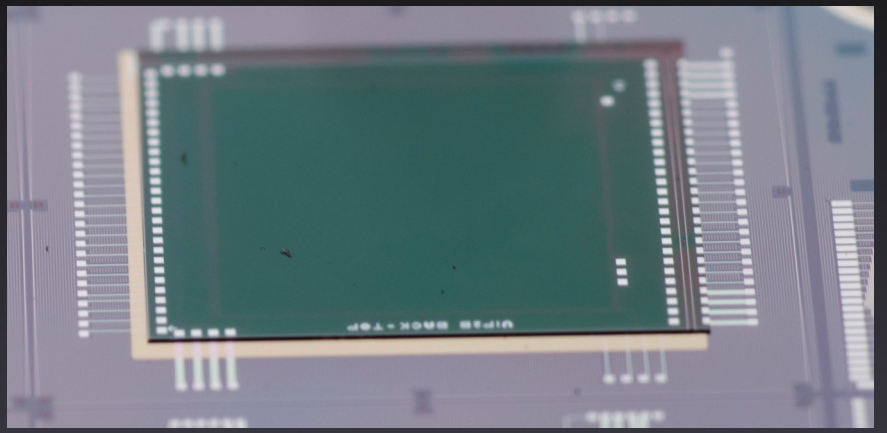
3D Technologies

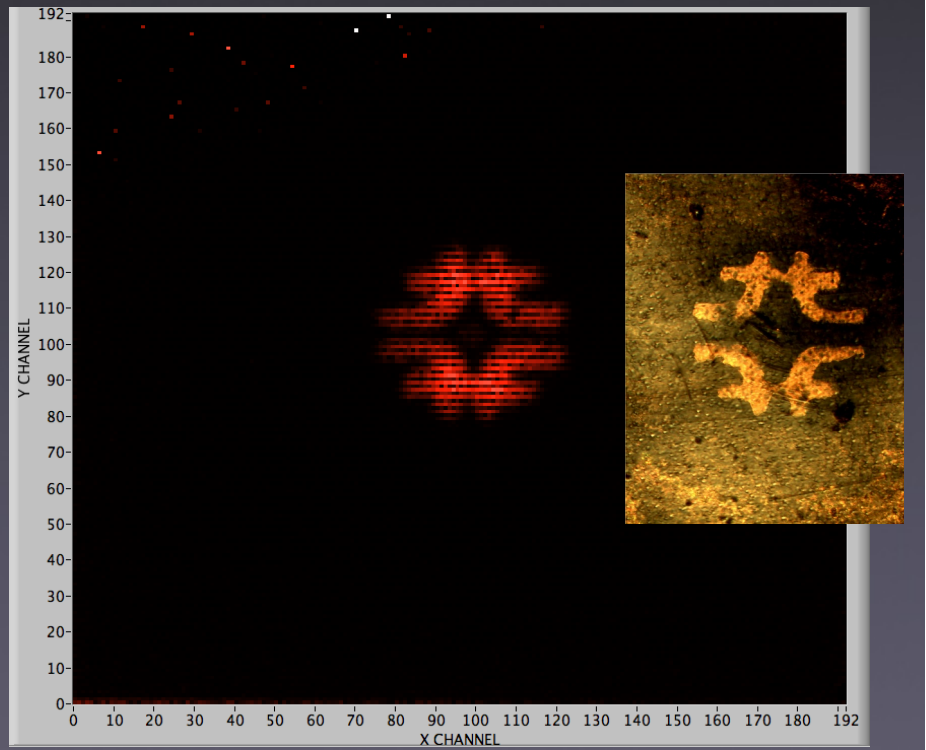
- Component Technologies
  - Through Silicon Vias (TSV)
  - Bonding: Oxide-, polymer-, metal-, or adhesive , Wafer-Wafer, Chip-Wafer or Chip-Chip
  - Wafer thinning
  - Back-side processing: metalization and patterning
- Three Chips made by Fermilab
  - VIP(ILC), VICTR(CMS), and VIPIC(X-Ray)



VIP for ILC

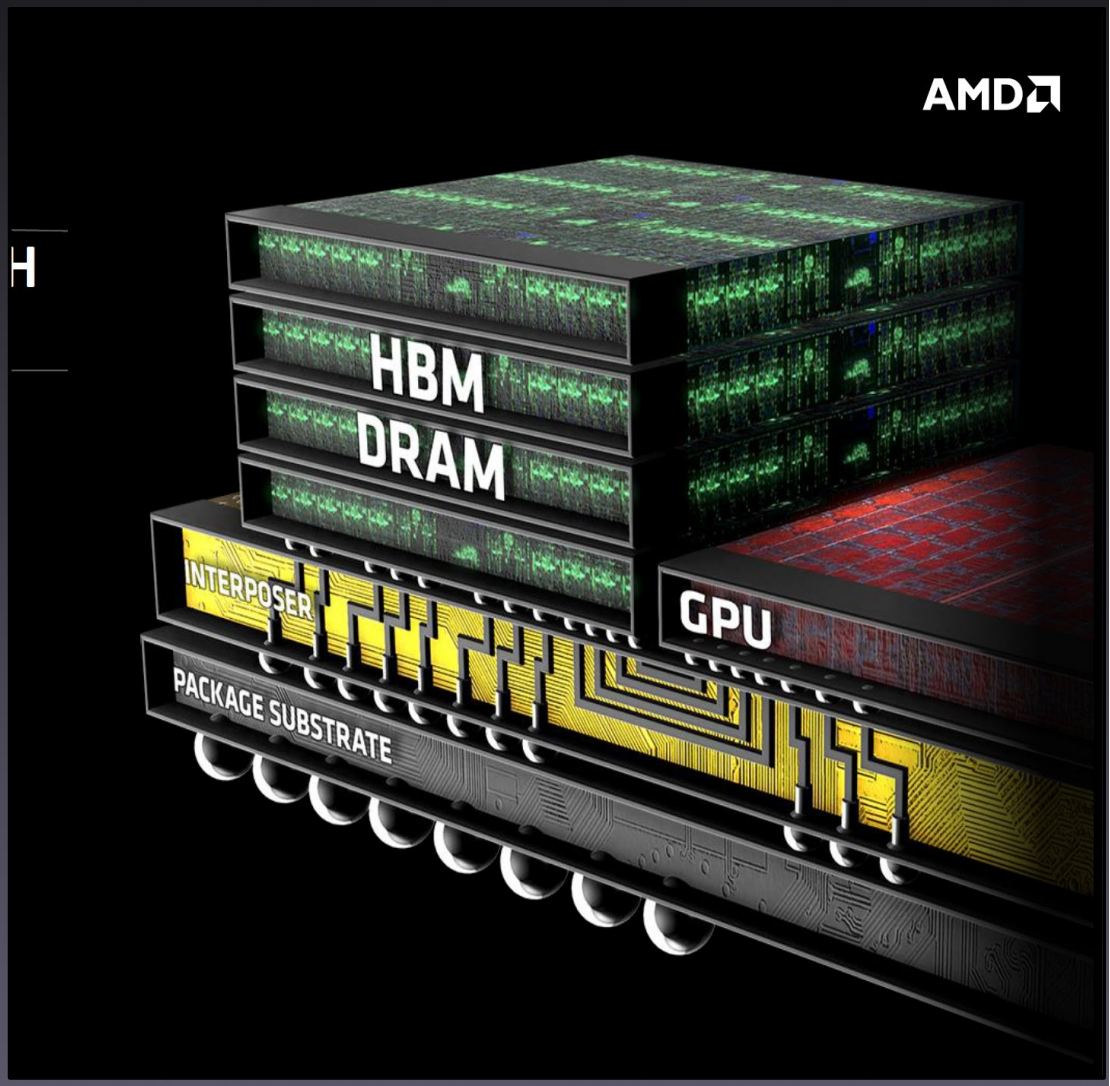
- Features
  - 192 × 192 array of 24x24 µm² pixels
  - 8 bit digital time stamp
  - Readout between ILC bunch trains of sparsified data
  - Analog signal output with CDS
  - Analog information available for improved resolution
  - Serial output bus
  - Polarity switch for collection of e- or h+





On the Side...

- New GPU's feature
  - High-Bandwidth DRAM
  - Interposers
- Enter Mainstream GPU market
  - AMD now
  - Nvidia in 2016
- It's all 3D Integration ..
  - No niche application anymore

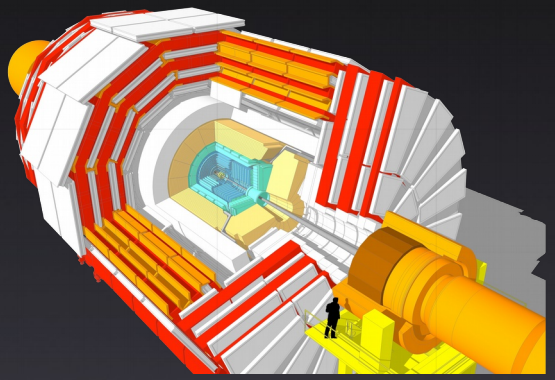


4D Tracking

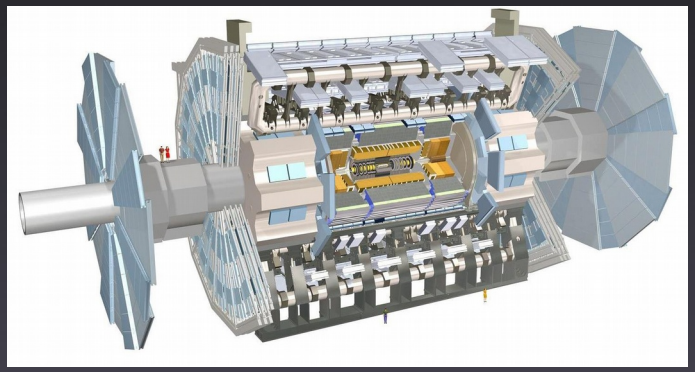
- The Hit timing as additional information
- Classic
  - Time-of-flight detectors
- Extend the idea to full tracking
  - Pattern recognition, tracking & vertexing including time information
- e.g. ILC
  - Suppress beam background tracks

- Realizations
  - Specialized silicon pad detectors
  - SiPM's
- E.g. Silicon Pad Detectors
  - Special Gain layer
  - Resolution ~ 100-200 ps
  - Prefers thin devices

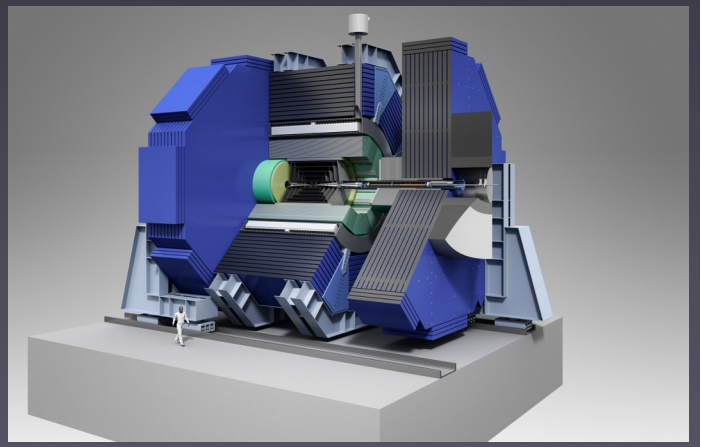
Doing it all-silicon tracking



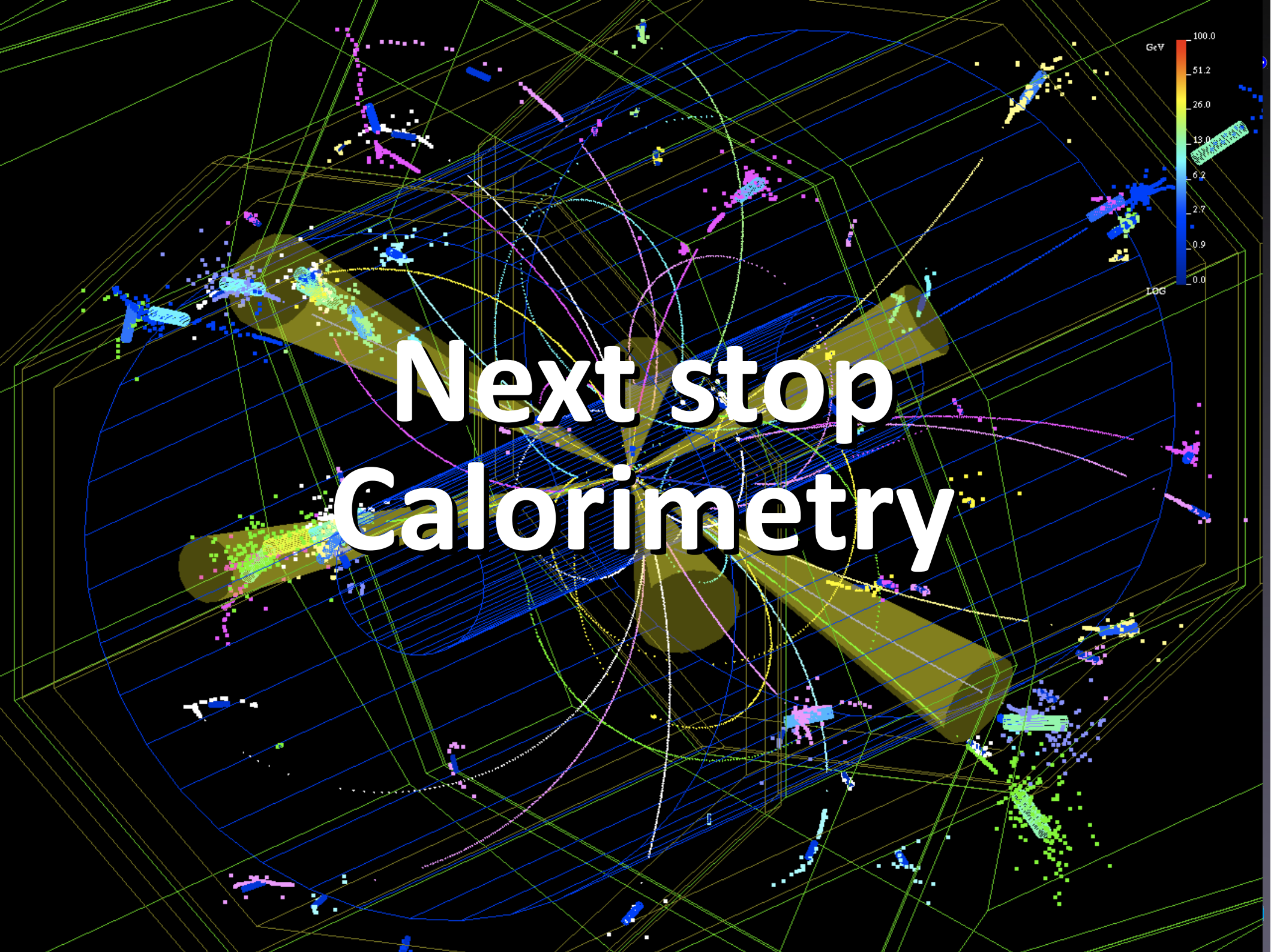
CMS Upgrade
HL-LHC



ATLAS Upgrade
HL-LHC



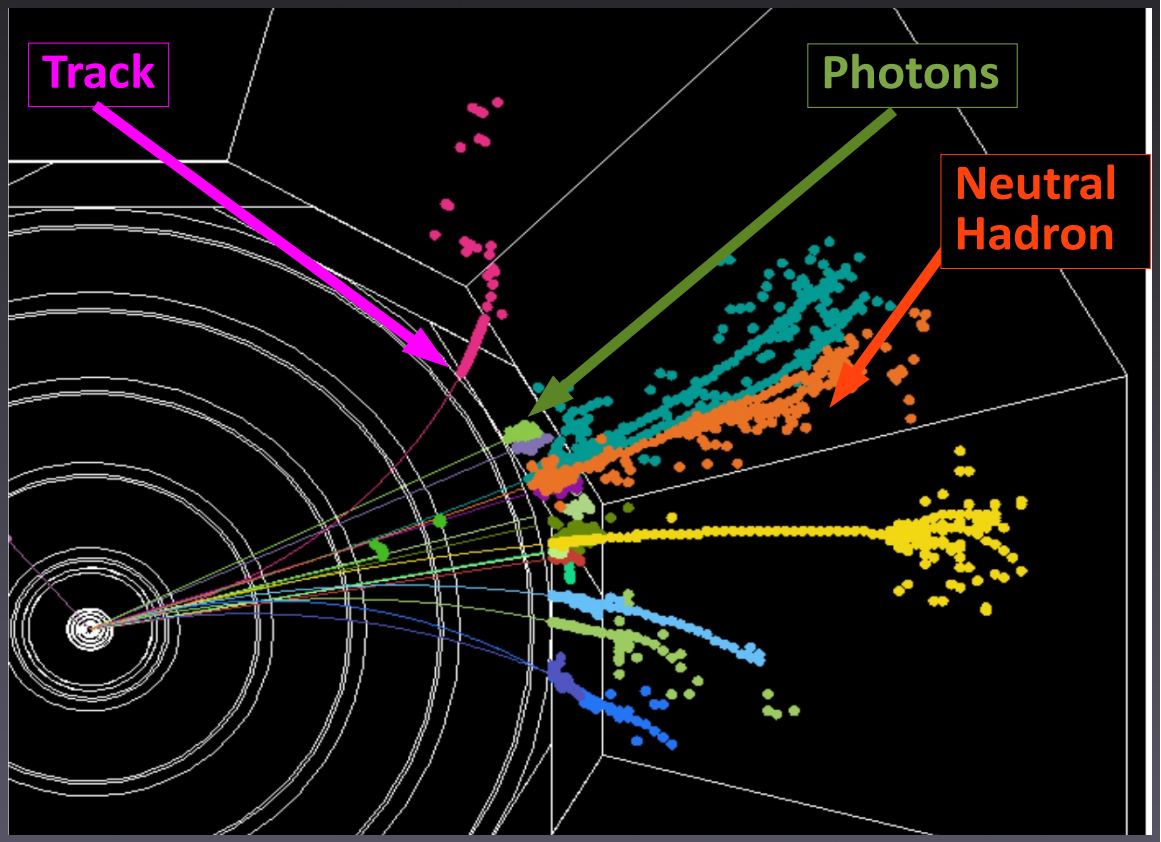
SiD
ILC



Next stop Calorimetry

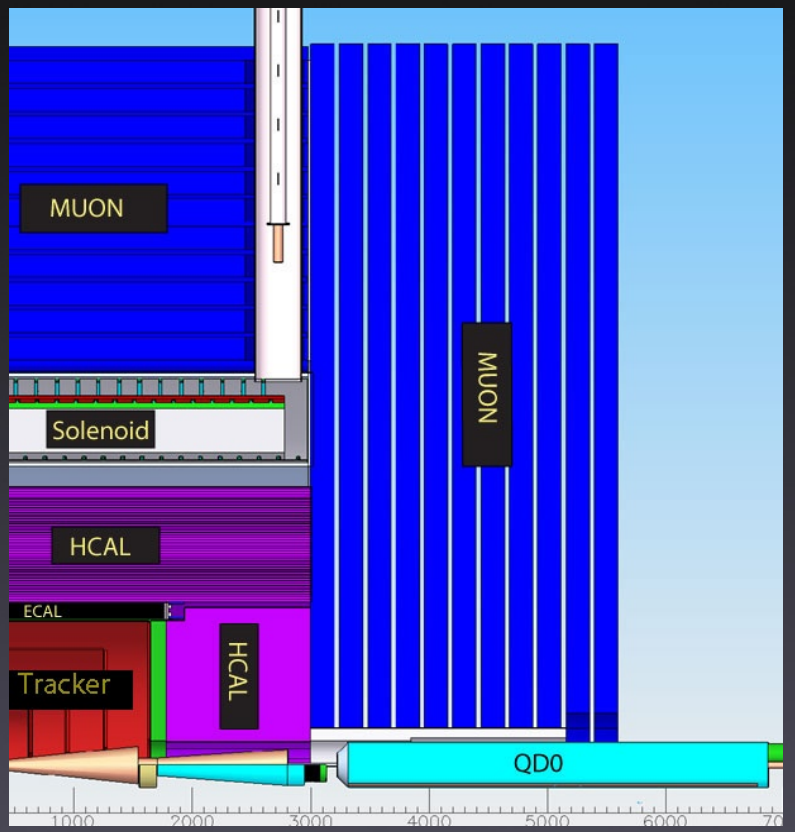
Silicon sensors for Calorimeters

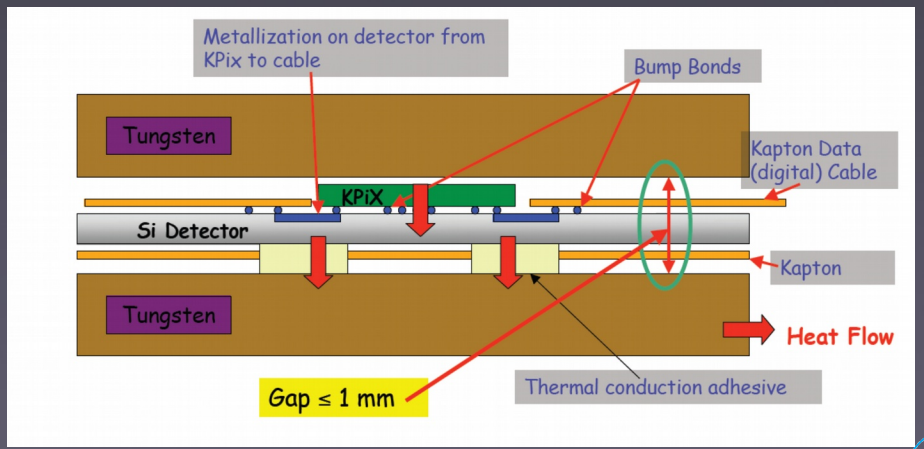
- Not exactly a new idea
  - e.g. OPAL Luminosity monitor: Silicon tungsten sandwich
  - Small devices
- SiW ECAL renaissance
  - Driven by ILC detector concepts: SiD and ILC
  - Ideal for Particle Flow paradigm
- Now picked up by CMS



The SiD ECAL

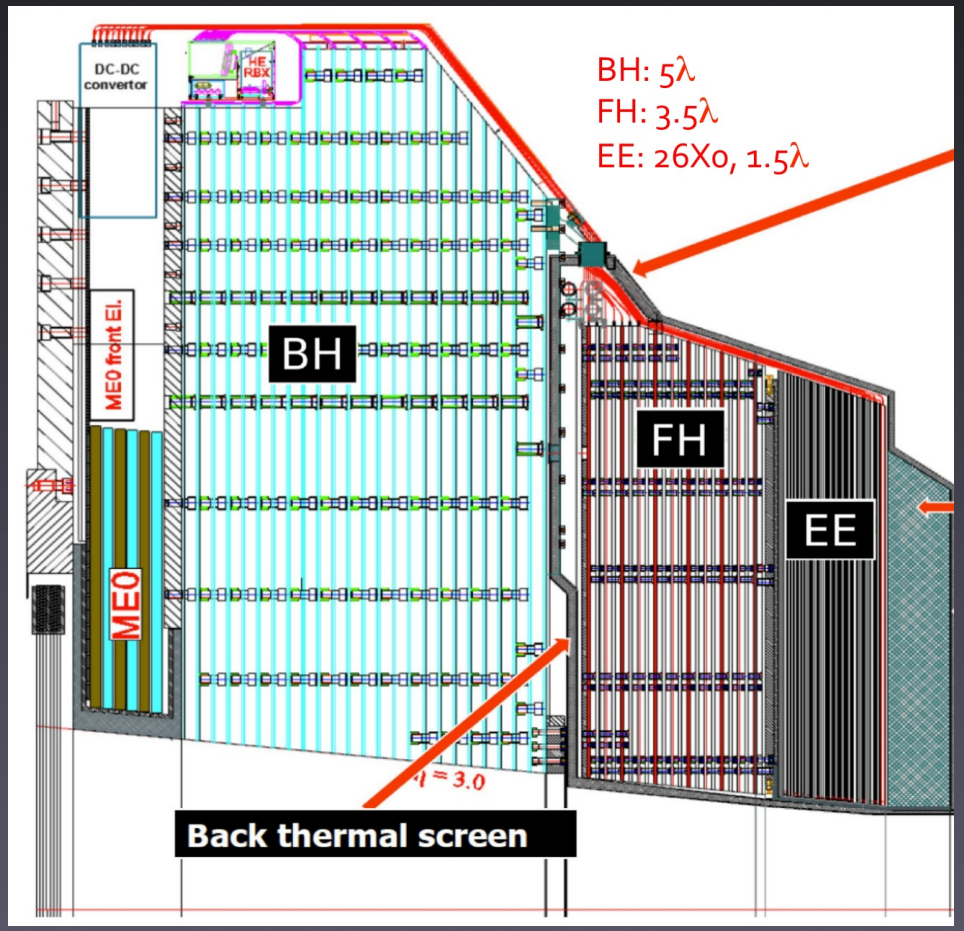
- Silicon-Tungsten ECAL
  - Both Barrel and Endcaps
  - 20+ 10 Layers
  - 2.5 mm/ 5 mm W with 1.25 mm readout gap
  - Readout Sensor bump-bonded to silicon
  - 1400 m^2 in total
- First final prototype set-up
  - Successful Test beam in 2014





CMS HGCAL for HL-LHC

- EE: Endcap ECAL
  - 28 layers of tungsten/copper absorber and silicon sensors
  - 26 X_0/ 1 Λ thick, 380 m^2 silicon 4.3 M channels
- FH: Front HCAL
  - 12 layers of brass absorber/silicon sensors
  - 3.5Λ thick, 209 m^2 silicon 1.8 M channels
- BH: Back HCAL
  - 12 layers of brass absorber and (radiation-hard) plastic scintillator
  - 5 Λ thick, 1K–10K channels



Large Systems some lessons learned

- Services to not scale well
  - Large systems require new approaches
  - Maybe not the “sexy” part, but it matters
- Going from hand-crafting to industrial production
  - Quantity & Yield do matter
  - Re-working is not an option
- Overall system approach
  - A detector is an integrated system not a mere assembly of individual subdetectors

Conclusions

- Silicon detectors have not reached the “end of the road”
  - In fact, they have only just started
- Next generation trackers will provide
  - Unprecedented performance with less material
  - Very attractive cost per channel
- Silicon will remain the dominant technology for tracking detectors
  - Currently no serious contender in sight
- Calorimetry is next
  - CMS HGCAL, SiD, ILD, CALICE